Biomedical Implant Packaging (December 2008 – May 2011)

Georgia Tech Project Final Report – May 2011

Summary

This report details progress and accomplishments in this two year collaborative research program between the University of Southern California, Georgia Tech, and TI. The overall goal was to develop technologies that can contribute to miniaturization of the electronic module components of medical implants. This can be accomplished by reducing component and system size by package miniaturization or embedded component technologies, or by designing circuits that do not require extra components to function. R&D has been conducted in circuit design, medical packaging, and high-density capacitors, towards this overall goal. This report summarizes the Year 1 accomplishments and describes Year 2 R&D in more detail for the Georgia Tech tasks only, namely, **Task 1.1a** Capacitor Integration, and **Task 1.2b** High Density Feedthroughs.

Task 1.1a Capacitor integration: (GT-PRC)

Objectives: The objective of this task is to demonstrate feasibility of high density capacitors on a silicon substrate with capacitance densities of 10 $\mu F/cm^2$ using low-cost solution technologies instead of MOCVD and ALD. The capacitor is rated at 10 V bias and should also meet the leakage and BDV targets of 1 $\mu A/\mu F$ and 20 V.

Approach: Chemical solution deposition, including sol-gel and other inorganic solution deposition technique, offers a low cost route to derive inorganic thin films in conformal structures. This is pursued as the front-up approach. The sol-gel coatings can be converted to a ceramic film using a rapid thermal annealing step. Trench coatings are proposed to be accomplished using two methods – radial trenches and vacuum infiltration. The first year focused on making solgel thin film planar devices with adequate capacitance density of 1 $\mu F/cm^2$ (at 10 V) so that they can be extended to 10 $\mu F/cm^2$ by using the trench approaches. The second year focus was on integrating such solgel derived capacitors in silicon TSV trenches.

Key results from year 1:

PZT film planar capacitors: First year efforts demonstrated sol-gel based capacitor on planar silicon. With lead zirconate titanate (PZT) as thin film dielectric, capacitance density of $3\mu F/cm^2$ was achieved with planar devices at 1 V bias. Under DC bias of 10 V, the capacitance density is 1 $\mu F/cm^2$. The leakage current with this approach is 1 $\mu A/\mu F$. The yield was 15% on 7 mm^2 devices (225-250 nF at 1 V) and 50% on 3 mm^2 devices (100-110 nF at 1V).

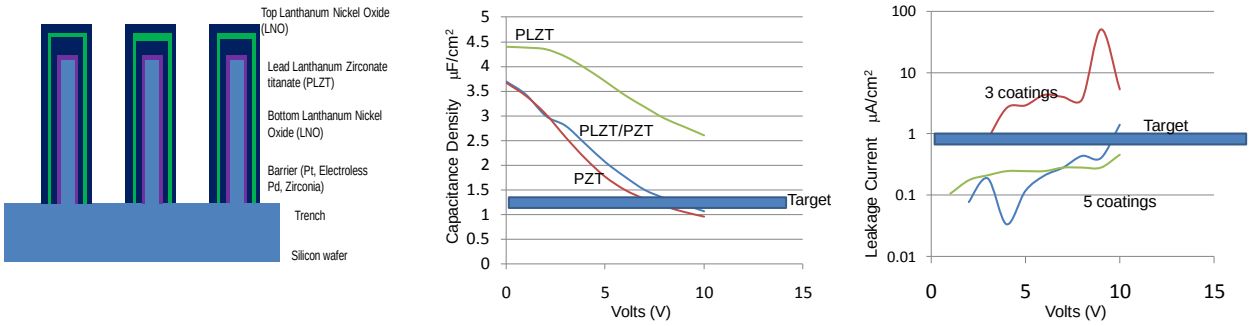


Figure 1: Key capacitance density and leakage current targets from year 1.

PLZT film planar capacitors: To increase the capacitance density at the operating voltage, antiferroelectric PLZT compositions were evaluated. These capacitors showed enhanced capacitance densities at higher voltages and much lower leakage currents (100-300 nA/μF) which demonstrated the benefits of lanthanum incorporation. More optimization in composition and thickness is expected to enhance the capacitance density by 2-3X at 10 V.

Solution-derived bottom electrodes: To achieve trench compatibility, the bottom electrode should be solution-deposited instead of sputtered metals that is widely employed for planar capacitors. Solgel LNO electrode process was developed to replace platinum sputtering process. The properties of PLZT/LNO were similar to those achieved on Pt electrodes. An all-solution process for depositing low-cost trench capacitors is thus shown to be feasible.

Year 2 Focus and Key Results:

Solution-derived bottom electrodes: As a major focus of year 2, the all-solution derived capacitor technology demonstrated with LNO as the bottom electrode and PZT as the dielectric material is then implemented on TSVs with sol-gel vacuum-infiltration to form a conformal coating with 5-10X enhancement in capacitance density. The capacitor technology, thus, has two major innovations: (1) an all-solution electrode and dielectric deposition as a low-cost alternative to sputtering, ALD or CVD, and (2) conformal-ceramic coatings over 3D structures with high-aspect-ratio profiles using the novel 3D-compatible sol-gel process compositions.

Experimental details:

Sol-gel technique was applied for the synthesis of LNO and PZT because of its advantages such as lower processing cost, flexibility in controlling stoichiometry and most importantly for its ability to form conformal coating over 3D topographies. LNO was synthesized starting with Lanthanum Nitrate Hexahydrate and Nickel Acetate Tetrahydrate with molar ratio 1:1 as precursors. The derived precursor solution was spin coated on a Si substrate and then baked on a hot plate at 400˚ C for 5 minutes. The steps were repeated three times to achieve adequate thickness, then heat treated in a tube furnace at 700˚ C for 30 minutes at a ramp of 5˚ C/min. For PZT, the starting materials were Lead Acetate Trihydrate, 70wt% Zirconium (IV) n-Propoxide in 1-propanol, and Titanium (IV) Isopropoxide. Precursor solution was made with Zr to Ti molar ratio of 13:12, and 10% lead excess, to get $Pb_{1.1}(Zr_{0.52}Ti_{0.48})O_3$. The precursors were sequentially dissolved in 2-methoxyethanol to form a 0.2 mol/L solution and refluxed at 120 ˚C for 2 hours. Derived precursor solution was spin coated onto the LNO film, and then heat treated at 700˚C for 1 minute using Rapid Thermal Processing (RTP). Flow chart for a representative sol-gel process is shown in Fig. 2.

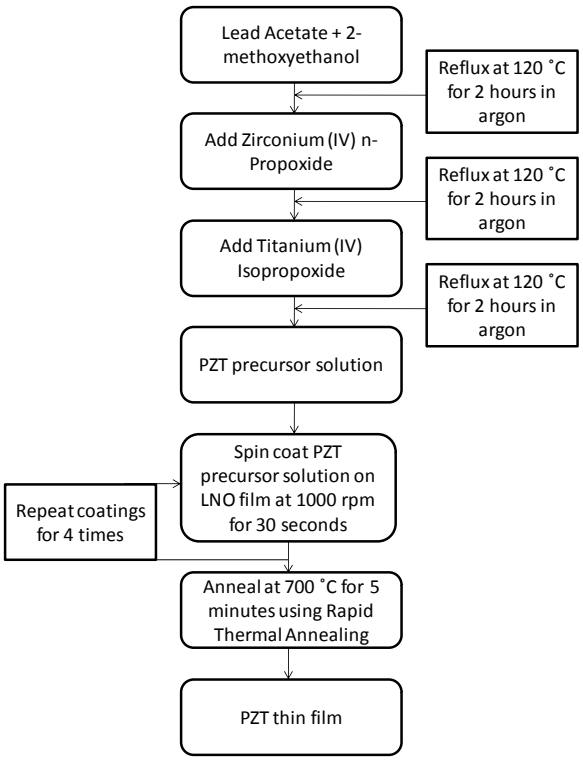


Figure 2: Flow chart for the PZT sol-gel process

Dielectric properties were tested with a 200 nm thick gold evaporated on the PZT thin film. Devices with a diameter of 0.5 mm were formed using a shadow-mask during the e-beam evaporation.

TSV wafers were obtained by bulk micromachining of silicon. Vias with diameters of 100 and 150 microns were formed using photolithography and Deep Reactive Ion Etching (DRIE). Photoresist (Megaposit SPR 220 – 7.0) was spin-coated on the silicon substrate, exposed (Karl Suss MA-6 Mask Aligner), developed and baked. The etching step was performed using an Inductively Coupled Plasma (ICP, Plasma-Therm Inc.) tool.

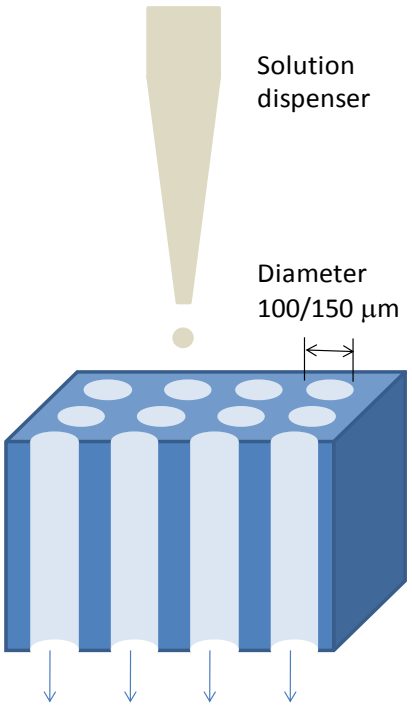


Figure 3: Schematic for sol-gel infiltration process

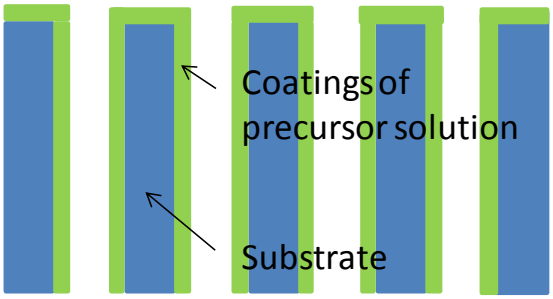


Figure 4: 3D structure after sol-gel vacuum-infiltration

For vacuum-infiltration process, the sol-gel precursor solution was dispensed on the TSV wafers while applying a pressure gradient over the wafer, as shown in Fig. 3. The sample was then heat treated on a hot-plate at 400˚ C for 5 minutes. Multiple coatings were applied to increase the thickness. The sample was then annealed in air at 700˚ C for 30 minutes. A 3D structure shown in Fig. 4 is thus formed, enabled by vacuum-infiltration of sol-gel derived solutions.

Results and Discussions

Planar capacitor results:

An all-solution capacitor process has to be realized first to benefit from the proposed vacuum-infiltrated trench capacitor technology. The first part of this discussion focuses on sol-gel derived PZT on LNO layers for thin film planar devices. The results for vacuum-infiltration into trenches are then shown.

The structure of the films was characterized with X-Ray Diffraction (XRD), Scanning Electron Microscopy (SEM) and X-ray Photoelectron Spectroscopy (XPS). XRD results, shown in Fig. 5, indicates a

randomly oriented film, instead of a strong (100) orientation mentioned in literature. The reason is attributed to the current deposition process for LNO. In this study, LNO was prepared by sol-gel method directly on a Si substrate to enable an all-solution derived capacitor. Literature reports (100) textured LNO film on Pt surface by RF magnetron sputtering, which then leads to a textured PZT film. A PZT film with a grain size of around 50-70 nm (Fig. 6a) and columnar structure as seen in the cross-section view (Fig. 6b), is thus formed. The film thickness is around 200 nm. The film is found to be dense and pore-free.

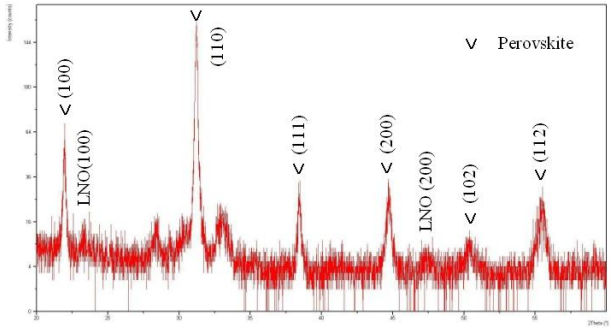
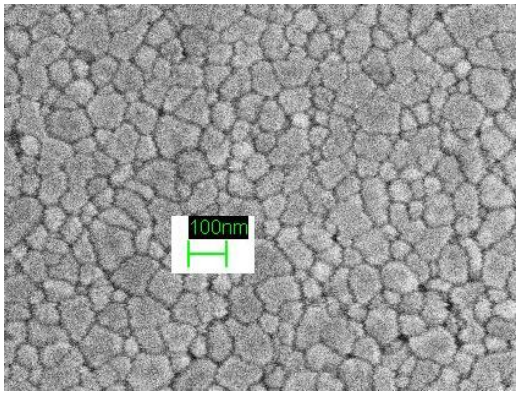
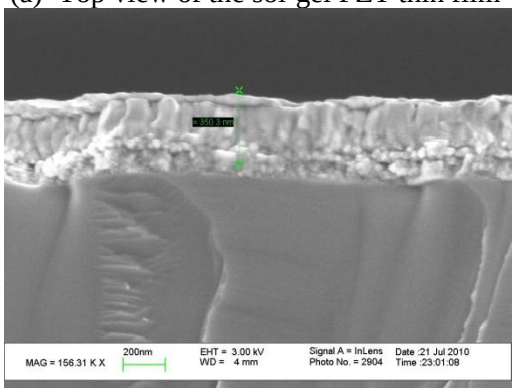


Figure 5: XRD result for PZT/LNO/SiO_2/Si planar device.



(a) Top view of the sol-gel PZT thin film



(b) Cross section of the sol-gel PZT/LNO thin film.

Figure 6 SEM pictures of planar PZT/LNO/SiO_2/Si devices.

	PZT/LNO	PZT/Pt
Capacitance Density ($\mu F/cm^2$) at 0V/100kHz	2.2 ~ 3.2	3.2 ~ 4.3
Leakage Current at 10V ($\mu A/cm^2$)	~7.8	~6.3

Table 1: Dielectric properties of planar devices.

With PZT as thin film dielectric, capacitance density of 3.2-4.3 $\mu F/cm^2$ was achieved with Pt electrode for planar devices. This corresponds to a permittivity of around 900, and is consistent with literature. With LNO layer as the electrode, capacitance density is found to be 2.2-3.2 $\mu F/cm^2$ for planar devices, as shown in Table 1. This is attributed to the roughness of the electrode, defects in sol-gel derived films and inter-diffusion between the LNO and PZT oxides. Surface roughness of LNO layer originates from the sol-gel process itself. With spin-coating and subsequent heat treatment step, the derived film is not as smooth as the one deposited by sputtering. With a relatively rough surface, the spin coating of PZT could be affected, resulting in thickness variations all over the surface which can be detrimental to the dielectric properties of the PZT film. Defects could result from hydrolysis of the sol, inhomogeneity in the solution or contamination picked up during any step of the process.

An XPS depth-profile analysis was conducted to confirm the inter-diffusion between the LNO and PZT layers. The analysis clearly shows a diffuse interface between LNO and PZT where the atomic percentages of Pb, Zr and Ti continuously decrease with etch-time (representing thickness) while the percentages of La and Ni increase, as shown in Fig. 7. The interdiffusion and interfacial reaction is the main cause for the difference in the PZT properties on LNO as compared to that on Pt electrodes.

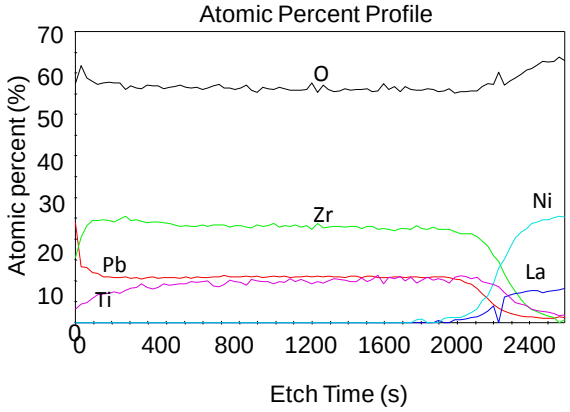
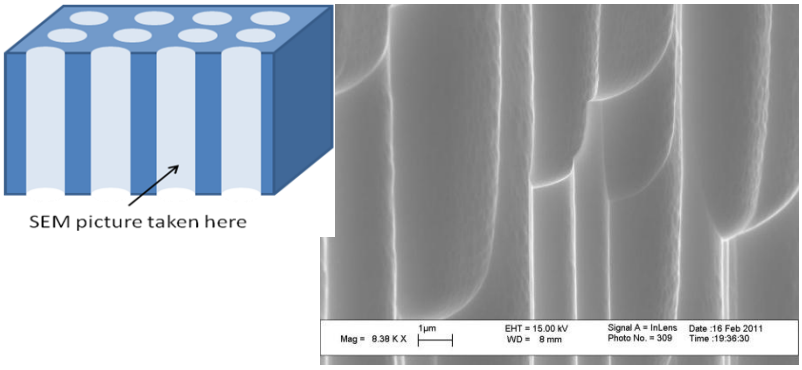


Figure 7: XPS compositional depth profile of the planar films

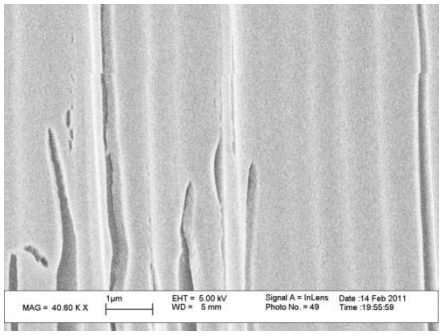
Vacuum-infiltrated TSV capacitor results:

Sol-gel vacuum-infiltration was then applied to form conformal ceramic electrodes with conducting oxides on the TSV structures. LNO was used to demonstrate the electrode structure. The location from

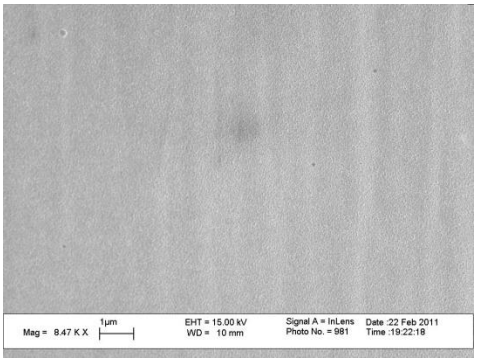
where the SEM image was obtained is shown in the schematic in Fig. 8(a). As indicated in Fig. 8(c), there is a conformal coating of LNO layer over the walls of the TSVs. Pressure gradient acts as a driving force to form the conformal coating of the precursor solution. However, too high a pressure can result in a non-uniform thickness of the solution coating, or shattering of the wafer. Furthermore, when concentration of the LNO precursor solution is too high or a relative high ramp rate is applied in the heat treatment step, cracks are seen in the film, as shown in Fig. 8(b). With further optimization in the solution concentration and heat treatment process, conformal coatings without pores or cracks, as shown in Fig. 8(c), were obtained.



(a) SEM of bare silicon TSV.



(b) TSV Coatings with cracks due to high concentration of precursor solution



(c) Conformal coating without cracks or pores with appropriate concentration and infiltration conditions.

Figure 8: SEM pictures LNO coatings over TSV by sol-gel vacuum-infiltration

In conjunction with the planar capacitors demonstrated in year 2, the feasibility of conformal solution coatings in trenches with aspect ratio of 5-10 can potentially lead to a capacitance density 10-30 $\mu F/cm^2$, which can meet the objectives of year 2, and emerging needs for thin power supply capacitors in a silicon interposer. These thin capacitor components can then be embedded in the package to enable true system integration and miniaturization.

Summary

The second year demonstrated vacuum infiltration as an innovative and low-cost solution-coating technology to form conformal electrodes and dielectrics in silicon trench structures to form trench-capacitors. In the first part of this work, an all-solution derived planar thin film capacitor with PZT/LNO/SiO_2/Si structure was demonstrated. Film crystallography, composition, morphology and interfacial reactions were studied using XRD, SEM and XPS.

This technique is then extended to Through-Silicon Trench (TST) or TSV structures using vacuum-infiltration. For sol-gel conformal coating on TSV structures, appropriate concentration for precursor solutions and the heat treatment steps are crucial to ensure crack- and pore-free vertical structures. The coating conformality in the trench is confirmed with SEM characterization.

Solution-infiltration is a high-throughput process that does not depend on slow and costly high-vacuum technologies. Conformal coating using sol-gel technique can be easily extended to other applications such as MEMS. Up to 10 times surface enhancement can be accomplished with this new technology.

Task 1.2b – High-density hermetic feedthroughs

Background: Implantable microelectronic systems have been used for almost half a century to treat medical conditions such as heart disease, chronic pain, movement disorders like Parkinson's, and deafness. These implants have been successful in spite of the challenges encountered when implanting electronic circuits in the body. Robust hermetic packaging is needed to keep moisture and ions away from the circuits. Package feedthroughs, once a common source of failure, have matured such that implantable electronics can expect decades of reliable operation. Currently, the microelectronics technology that has been employed is unsophisticated, relative to the state-of-the-art in consumer electronics. This is driven partially by business considerations (life-cycle of medical implants is longer versus cell phones, medical implant product volume is lower), but mostly by the fact that the electronic functionality needed for these implants is relatively low. The most sophisticated medical implants to date, cochlear implants for the deaf, require only 20-30 stimulus channels and do not have a sophisticated packaging scheme because of the large physical size and low number of inputs/outputs. Hermetic cases are made of titanium or ceramic and feedthroughs are large. However, more complex implants that are in development, such as retinal implants for blindness [1, 2] and cortical implants for blindness [3] and paralysis [4], will require technology that can support more complex electronic systems and a higher volume of input/output in a small space. Existing packaging technology (for biomedical implants) is not optimized for space, however higher density packaging techniques exist in cutting edge microelectronics research.

An example of a device that will require a high density packaging is a retinal prosthesis for the blind. These devices function as follows. A camera converts light into an electrical signal. This signal is processed and transmitted (typically wirelessly from an external camera system) to the implanted neural stimulator. Based on the input from the camera system, the stimulator applies a pattern of electrical stimulus pulses to the retina. The entire implant must be inside the bony orbit of the skull, with portions of the implant inside the eye to allow close contact with the retina. Clinical trials of prototype stimulators have shown that otherwise blind subjects can read large letters with relatively crude

implants. Improvements in mobility and object tracking have also been noted. A higher resolution device may be realizable and more effective. Simulations of prosthetic vision suggest that as the number of pixels increases, performance in visual tasks improves, possibly allowing face recognition and reading. [5, 6] However, such implants will need 1000 individual contact with the retina or 2-3 orders of magnitude above current implants in terms of the number of channels.

While many challenges remain to developing a retinal prosthesis as a useful therapy for blindness, enough feasibility has been shown in past studies to warrant continued development. However, the lack of a clear solution for packaging and feedthroughs will limit the effectiveness of more sophisticated retinal prostheses by increasing the size of device and restricting the number of electrodes. Devices that are currently being tested in human motor cortex, for a brain machine interface (BMI), will have similar packaging constraints. Prototype BMI systems tested in humans have a percutaneous connector and no active electronic parts implanted, in part because microelectronics cannot be appropriately packaged for implantation. Thus, there exists a need for high-density, high-volume hermetic packaging for biomedical implants.

Current package and feedthrough technologies, based on ceramic substrates with platinum wires, have a number of important properties [7], but are not capable of meeting the required channel density for future implants. Several polymers including polyimide, parylene and silicones have been investigated for implantable electrode arrays due to their flexibility for ease of surgical insertion. However, there are concerns over the long term stability of these materials, primarily due to their high moisture absorption, and insufficient interfacial adhesion to metals. Liquid crystal polymers (LCP) have attracted attention for implants due to their bio-compatibility, and extremely low moisture uptake (<0.04%) and excellent resistance to harsh chemicals. Recent work on large size (few hundred microns diameter) LCP feedthroughs for retinal implants reported promising hermeticity performance and long term stability in saline environments for few electrodes [8]. Most of the reported work on LCP for neural implants has focused on conventional semiconductor and PWB fabrication methods such as laser via ablation, sputtered metallization and thin film processes [9, 10, 11].

Objective: To demonstrate the feasibility of an integrated bio-electronic package with high density electrical feedthroughs, capable of 1024 stimulator channels in a 5mm x 5mm area using LCP substrates to enable implantable retinal prosthesis, and compatible with a bio-compatible stimulator chip, developed for epi-retinal charge delivery.

High Density Feedthrough Concept in LCP Substrate: A new and innovative method to form moisture-resistant and bio-compatible through via interconnections in LCP has been demonstrated to address the main concern of leakage in feedthroughs at fine pitch (100-250um pitch). This method, for the first time, applies fusion bonding concepts at low temperature (<300°C) to achieve very high array density (100-1000 in 5mm x 5mm) and low leak rates. Fusion bonding of polymer to metal results in high adhesion strength compared to deposited metal in via feedthroughs, and high interconnection densities such as 50um diameter vertical interconnects in 50um thick LCP substrates. Copper-core with noble metal barrier coatings was used for the electrical connections to reduce the cost of traditional Pt or Au wire feedthroughs.

Design of Feedthrough Array Test Vehicle: A test pattern layout was created for the via feedthrough substrate based on 512 and 1024 pad arrays to interconnect the stimulator chip. Various stimulator chip sizes from 3 mm to 4.5 mm (square) were emulated for designing the substrate pad arrays. The following design rules were included in the test vehicle.

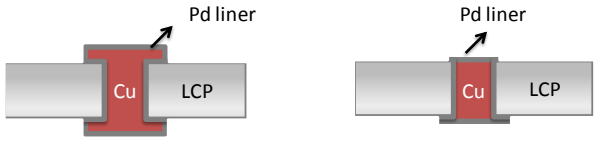
1. Via Feedthrough Size: 40µm, 50µm, 60µm, 75µm
2. Metal Pad Size: Via size+(30µm, 40µm, 45µm, 50µm)

3. Pad to pad spacing: 30µm, 35µm, 40µm, 45µm, 70µm

Figure 9 shows a fabricated LCP sample with pad arrays laid out in a 150mm x 150mm sample.

Figure 9. LCP Feedthrough Array Test Vehicle (150mm x 150mm)

Fabrication of high density feed-throughs in LCP: Two fabrication process flows were explored and demonstrated in flexible LCP substrates; a) conventional via based approach with high I/O density and b) vialess process by fusion bonding for high adhesion strength. The fabricated test coupons were subjected to Helium leak testing, to check the hermetic nature of the package. Figure 10 shows the schematic cross-sections of the vertical interconnections using the two different process options.

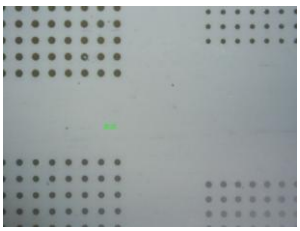


(a) Via process (b) Vialess process

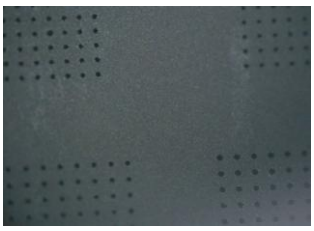
Figure 10: Schematic cross-section of vertical feed-through in LCP

Via-process: LCP substrates (Rflex 3850 from Rogers Corporation) with three different thickness (25um, 50um and 100um) was used for the 'via process'. Via arrays were drilled for different via diameters (40um to 250um) using 266nm UV laser ablation. The varied diameter designs were used to analyze the feasibility of the process. The pad size was designed to be atleast 30um greater than the through-via diameter for alignment accuracy during lithography and also to accommodate for the dimensional instability of the LCP core.

Copper and palladium were mainly used for the metallization of the through LCP vias. The biocompatibility of palladium makes it a good liner material, preventing the chemical reaction of copper with the biological fluids in the body. Electroless palladium deposition ensured a conformal plating on the LCP surface as well as the via side walls. The plating was carried out at a temperature of 55^{o}C and consisted of three steps; a) pre-dip – for surface cleaning, b) activation – catalyst for plating initiation and c) plating - electroless deposition. The electroless Pd showed good adhesion to the LCP surface, which was confirmed by performing a tape test. Figure 11 shows the optical images of the laser drilled LCP surface before and after Pd plating. The plating can also be carried out selectively (on the via pad and side walls) using a photo-resist liftoff process as shown in Figure 12.



(a) Top view optical image of laser drilled LCP



(b) Optical image after electroless Pd deposition

Figure 11: Laser ablated LCP surface before and after electroless Pd deposition

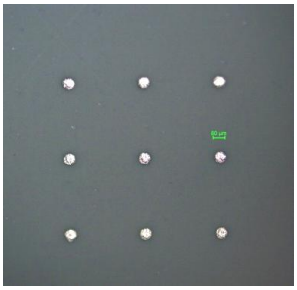


Figure 12: Selective palladium deposition on LCP using photoresist lift-off method showing 75µm diameter features

Plating of the 'through LCP vias' was carried out using electroless copper seed layer followed by copper electroplating which resulted in void free metallization. The blanket copper was thinned down to define the via feed- throughs. The palladium between the via pads were etched away to electrically isolate the individual vertical interconnects. Finally a palladium liner is deposited on top the copper pads to achieve a feedthrough structure where no copper is exposed to the LCP surface or to the external surfaces as shown in Figure 13.

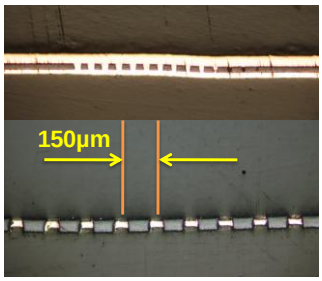


Fig 13: Cross-section of metalized LCP vias at 150µm pitch

Via-less process*:* A novel via-less process was explored and demonstrated for achieving vertical feedthroughs in LCP without using any laser via formation steps. The process flow schematic is shown in Figure 14.

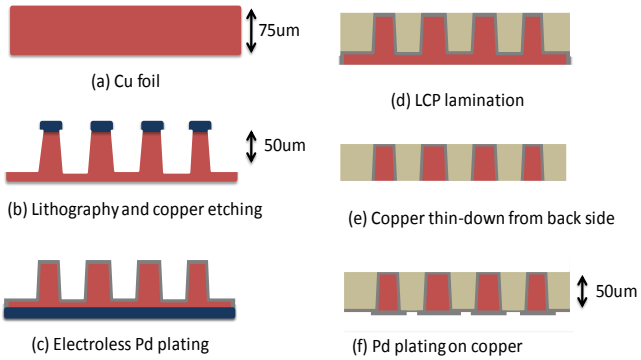


Figure 14: Process flow schematic for 'vialess' process

A copper foil with a thickness between 75um to 100um was used to etch down copper pillars (50um in height) by photolithography and wet chemical etching. To enhance the adhesion between copper and photo-resist, a non-etch adhesion promoter (NEAP) solution was used to treat the copper surface prior to photo-resist lamination in some samples. Spray etching at 115°F using copper chloride ($CuCl_2$) solution enabled almost vertical copper pillars with minimum taper. The side opposite to the patterned surface was laminated with photo-resist before electroless Pd plating to prevent back side Pd deposition. Pd plating was carried out for 30 minutes at 55^{o}C to achieve a plated metal thickness of 3um to 5um. The patterned copper foil was then laminated with 50um thick LCP using a hot press at 550°F and 100-300 psi pressure for 45-60 minutes.

The high lamination temperature (550F) makes the LCP flow within the patterned copper foil template resulting in a strong fusion bond between the metal and the polymer. Since the thickness of the LCP and the etched copper pillars are closely matched by design, the copper pillar is exposed on the top side through the LCP. Any thin LCP residue on top of the copper pillars was etched away using CF_4 + O_2 plasma ashing. The bottom side copper was etched away to expose the Pd surface and copper in the vias. A second lithography step was carried out on the bottom side of the LCP, to define pads and etch away the Pd between the pads for electrical isolation. Finally electroless Pd plating was carried out to completely cover the copper vias, resulting once again in a copper core feedthrough and pad structure fully encased in bio-compatible palladium. Figure 15 shows the micro-scope image of the fabricated copper pillars with uniform height distribution. A cross-section study was performed to study the fabricated test coupons. Figure 15 also shows the cross-section of 200µm pitch vias fabricated using the vialess process.

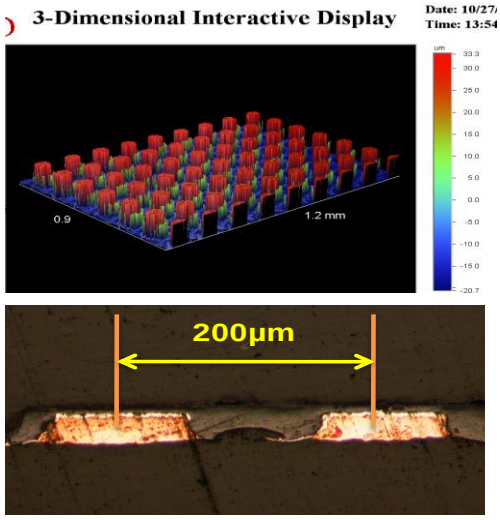


Fig 15: Image of copper pillar array, cross-section of LCP with Cu feedthrough

Hermeticity Testing of Bare and Plated LCP Substrates: Tests of the viability of liquid crystal polymer (LCP) substrates as a vehicle for bioimplants were performed. Several sets of samples were fabricated and then helium leak tested. In the first generation, 2 cm x 2 cm samples were produced with either bare LCP surfaces, or with a Pd/Cu patterned metallization layer as described above. In the second generation, the sample configurations were redesigned to (1) better interface with the He leak detection system, (2) assist with characterization of the individual leak points of patterned via-free and via-containing substrates, and (3) measure the relative differences between LCP substrates of differing thicknesses. Key to these new designs is a palladium/copper ring around a central 5 mm x 5 mm region that can contain either bare or patterned LCP samples, and that will eventually contain patterned via structures.

Five types of samples have been tested to date, with further testing ongoing following intensive optical inspection: (1) a first generation 25 µm thick bare LCP substrate (herein referred to as Sample 1); (2) a first generation 25 µm thick Pd/Cu patterned LCP substrate (Sample 2), with nine subregions of varying pad diameters (from 70 to 110 µm) and pitches (from 110 to 140 µm) on both sides of the substrate; (3) a first generation 25 µm thick Pd/Cu fully electroless plated LCP substrate (Sample 3); (4) a second generation 25 µm thick Pd/Cu ring structure with a bare LCP window (Sample 4); and (5) a second generation 25 µm thick Pd/Cu ring structure with a patterned LCP substrate, with 50 µm diameter pads on both sides of the substrate on a 150 µm pitch (Sample 5). Two optical photomicrographs showing the second generation patterned and unpatterned LCP samples are shown in Figure 16 below.

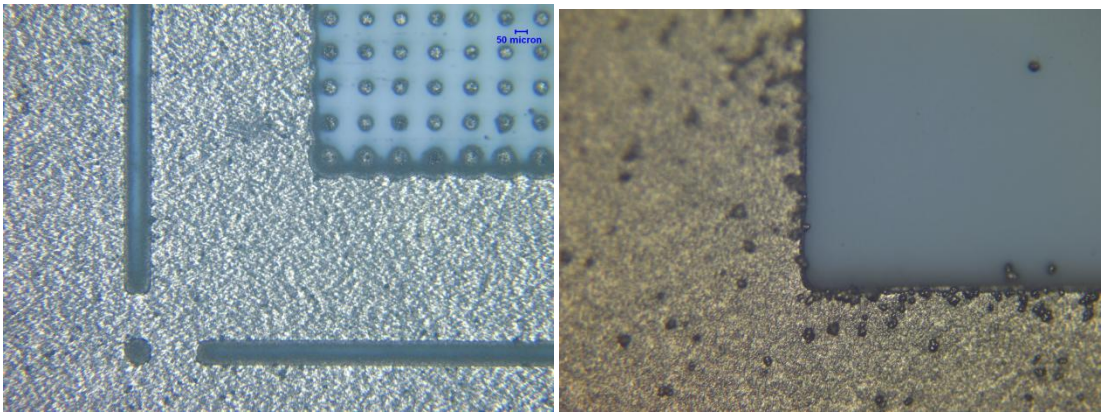


Figure 16. Optical photomicrographs of a patterned LCP second generation sample, showing the layout of multiple feedthrough pads (left), and of an unpatterned LCP second generation sample (right).

A photograph of the second generation LCP undergoing testing on the He leak detection system is shown in Figure 17 below. Of particular notice is the Pd/Cu guard ring that surrounds the bare LCP window.

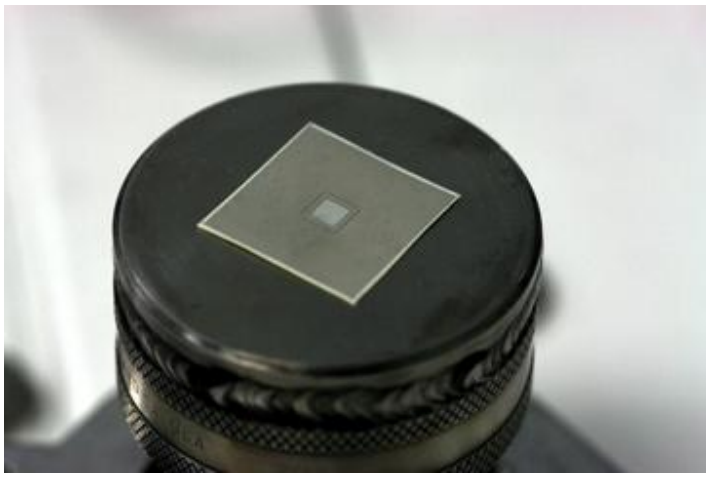


Figure 17. Second generation bare LCP sample mounted to the vacuum chuck atop the He leak detector measurement flange with Dow Corning® vacuum grease to form a vacuum seal.

A small 1.52 mm diameter hole through the vacuum chuck was covered with each sample and connected to an Adixen ASM 182 TD+ helium leak detector system. The samples were mounted to the vacuum chuck with Dow Corning vacuum grease to form a vacuum seal. The helium leak detector was then used to measure the helium flow rate through each of the three samples with a 20 psi helium gun located 1 cm above each sample providing a source of UHP helium gas.

The measured relative leak rates for each sample (in units of mbar-l/sec) are shown in Table 2 below.

Table 2. Leakage rates of both bare and patterned LCP samples

Sample	Description	Leakage Rate (mbar-l/sec)
Sample 1	First generation bare LCP	5×10^{-9}
Sample 2	First generation Pd/Cu patterned LCP	1.5×10^{-9}
Sample 3	First generation Pd/Cu overcoated LCP	3×10^{-10} No change relative to the background He leak level
Sample 4	Second generation Pd/Cu bare LCP	5×10^{-9}
Sample 5	Second generation Pd/Cu patterned LCP	2×10^{-9}

As expected, the bare LCP samples leaked the most, the patterned LCP samples less so, and the Pd/Cu overcoated samples (both sides coated with Pd/Cu) showed no detectable leaks at the sensitivity limit of the helium leak detector employed in these initial experiments.

The new seal provided by the Pd/Cu guard ring was proven highly effective by these initial measurements, as the background leak rate dropped to 1.4×10^{-10} mbar-l/sec, close to the instrumental sensitivity limit.

Hermeticity Testing of LCP Substrates with Feedthroughs

Prior to testing, a dual metal coated (both sides covered with metal) LCP sample was used to test all equipment and seals. Spraying He 1 cm from this sample resulted in no measurable helium penetration through the substrate. Once the integrity of the apparatus was confirmed, the new samples were prepared. As before, testing started with application of a vacuum oil seal and was followed by application of a vacuum grease seal to help eliminate any issues with either sealing system.

Measured He Leak Rates:

Sample 1: 2.1×10^{-8} atm-l/sec
Sample 2: 8.0×10^{-8} atm-l/sec
Sample 3: 1.2×10^{-8} atm-l/sec

Measurements on all three samples were the same for both oil and vacuum grease seals.

Summary: A novel “vialess” process using fusion bonding of liquid crystal polymer (LCP) substrates was demonstrated with promising low He leak rate levels. The LCP substrates can potentially improve the feedthrough channel density by 10 × to more than 1000 channels in a 5 mm × 5 mm area for microstimulator array analog ICs with 1000+ channel charge delivery capacity. This low-moisture, biocompatible, thin, and flexible package can enable 10 to 100 × higher pixel density retinal prostheses aimed at restoring face recognition and reading functions in people with certain types of blindness. Such a technology could also contribute to advancing the capabilities of high density neural prostheses.