MILLIMETER-WAVE QUADRATURE RECEIVERS FOR ATMOSPHERIC SENSING AND RADIOMETRY

A Dissertation
Presented to
The Academic Faculty

By

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

December 2021

MILLIMETER-WAVE QUADRATURE RECEIVERS FOR ATMOSPHERIC SENSING AND RADIOMETRY

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To my wonderful parents and sister,

and

my lovely wife.

ACKNOWLEDGMENTS

First and foremost, I would like to thank my advisor, Dr. John D. Cressler, for all of his guidance, teaching, and unwavering support throughout my PhD years. He is truly an outstanding mentor and role model, both professionally and personally. I will forever be grateful to him.

I would like to thank Dr. Paul Steffes and Dr. Nelson Lourenco for taking the time to serve on my reading committee. I would also like to thank Dr. Albin Gasiewski and Dr. Glenn Lightsey for serving on my defense committee, and especially Dr. Gasiewski who provided valuable feedback on our collaborative projects and my research.

The author gratefully acknowledges the support for this work offered by Orbital MicroSystems. I am also deeply grateful to IEEE MTT and SSCS societies for supporting me through the IEEE MTT Graduate fellowship, the IEEE MTT Satellite Challenge award, and the IEEE SSCS Predoctoral Achievement award.

I would like to thank former and current members of SiGe Devices and Circuits lab for all the discussions and supports, especially during tapeout times. I would like to thank, in no particular order, George, Chris, Adrian, Sunil, Cliff, Victor, Sanghoon, Saeed, Patrick, and Jeff. I am also grateful to the members of the ECE graduate office and GEDC staff for all their support over the years, including Daniela, Tasha, Jacqueline, Alison, Maria, Carolyn, Scott, and Daniel.

I would like to thank my parents, Roghaiyeh and Hossein, and my dear sister, Negin, who I missed so much, for their unconditional love and support. I am grateful for all my friends, who were like a family for me in Atlanta. Last but not least, I am thankful to my lovely wife, Sevda. Without her love, support, and encouragement, this would not have been possible.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of this research is to investigate the design challenges of millimeter wave (mm-wave) quadrature receivers for emerging applications and develop new ideas to address these challenges. Next-generation wireless networks, satellite communications, atmospheric sensing instruments, autonomous vehicle radars, and body scanners are targeting to operate at mm-wave frequencies, and high-performance electronics are needed to enable these technologies. In this research, we investigate novel circuit topologies to improve the performance of existing mm-wave quadrature receivers, particularly for radiometry and remote sensing applications. The following is a summary of contributions of this research:

1. A low-noise radiometry front-end was presented in which the Dicke switch was co-designed with the low-noise amplifier (LNA). The switch incorporates a transformer-based topology and serves as the input matching network of the LNA. This topology is configured to minimize the amplifier gain mismatch between the two switching states caused by process variations while providing a low noise figure (NF). The circuit is implemented in a 0.13μm SiGe BiCMOS technology, and it achieves more than 20 dB gain and minimum NF values of 4.5 and 0.58 dB at 300 and 20 K, respectively. It consumes a dc power of 15 mW. The front-end switch presents a peak isolation of 17 dB, and the input return loss is better than 15 dB across 45 - 70 GHz. This work was presented in *IEEE Radio Frequency Integrated Circuits*, August 2020 [1], and published in *IEEE Journal of Solid State Circuits*, May 2021 [2].

2. A broadband low-loss quadrature-hybrid-based network was presented that enhances the phase and the amplitude matching of quadrature signals. The performance of this network was investigated, and a detailed theoretical analysis is provided. Several stages of this network can be cascaded to generate broadband balanced quadrature signals. Each stage has a loss of 0.5 dB and enhances the image rejection ratio (IRR) by approximately 8 dB. Compared to conventional polyphase quadrature sig-

nal generation methods, this network enables lower insertion loss, wider bandwidth, and reduced sensitivity to process variations. To verify the theoretical analyses, two proof-of-concept image-reject mixers are implemented in a 0.13 μm SiGe BiCMOS technology. The first mixer achieves an average IRR of 37.5 dB across 40−76 GHz, whereas the second mixer achieves an average IRR of 33.5 dB across 40−102 GHz. This network is a promising solution for broadband quadrature signal generation at millimeter-wave frequencies as it eliminates the need for calibration and tuning. This work was published in *IEEE Transactions on Microwave Theory and Techniques*, Dec. 2018 [3], and it is protected by the U.S. patent US10979038B2 filed on August 21, 2019 [4].

3. A dual-band millimeter-wave quadrature signal generation network was presented comprising an RC-CR polyphase filter (PPF) and two quarter-wave coupled-line couplers. A common-centroid layout is suggested to improve the phase and amplitude matching of quadrature signals. The effects of interconnects and parasitic capacitances on PPFs are investigated, and design guidelines are provided to achieve low insertion loss and broad bandwidth. A proof-of-concept image-reject mixer is implemented in a 0.13 μm SiGe BiCMOS technology, which achieves a mean image-rejection ratio of 34 dB over a wide frequency range of 36 − 100 GHz. To the best of the authors' knowledge, this design achieves the widest bandwidth of any mm-wave mixer with a mean IRR above 30 dB, and accomplishes this without calibration or tuning. This work was published in *IEEE Transactions on Circuits and Systems II: Express Briefs*, Feb 2020 [5].

4. A Ka-band Gilbert frequency doubler (FD) was presented, in which the phase of the injected signal to switching transistors wass adjusted to maximize core conversion gain (CG) and power-added efficiency (PAE). It achieves a peak PAE of 26.2 % and a peak CG of 21 dB at 28 GHz, without any output buffer. The FD provides a

saturated output power of 11.9 dBm, a 3-dB bandwidth of 22−36 GHz, and a fundamental harmonic rejection of 32 dB. To the best of authors' knowledge, this FD achieves the highest CG and PAE among all reported Si-based FDs without output buffers. This work was published in *IEEE Microwave and Wireless Components Letters*, November 2018 [6].

5. The noise performance and reliability of several on-chip PN junctions were characterized, and two novel implementations of a V-band single-pole double-throw switch that facilitates the internal calibration of radiometers by integrating an ambient noise source and an avalanche noise source. High excess noise ratios of about 28 dB were achieved with a p-i-n diode the collector-base junction of a SiGe heterojunction bipolar transistor (HBT) at V-band frequency range. Moreover, a novel implementation of a V-band single-pole double-throw switch was presented that facilitates the internal calibration of radiometers by integrating an ambient noise source and an avalanche noise source. To the best of our knowledge, this is the first reliability study of on-chip noise sources in a SiGe BiCMOS technology and the first monolithic two-reference switch for calibrating millimeter-wave radiometers. This work was published in *IEEE Journal of Solid State Circuits*, May 2021 [2], and *IEEE Microwave and Wireless Components Letters,* April 2020 [7].

6. Several V-band receiver front-ends were designed and presented for space-borne atmospheric remote sensing. The receivers are implemented in a 0.13 μm SiGe BiCMOS technology and consists of a Dicke switch, an LNA, an image-reject mixer, a frequency multiplier, and an IF amplifier. The final implementation achieves a mean conversion gain of 20 dB, a minimum noise figure of 4.5 dB at 50 GHz, and a mean image rejection ratio of 40 dB. This chip consumes a total DC power of 45 mW and occupies an active area of 1.8 mm^2. This work was the first reported monolithic receiver front-end for atmospheric measurements across the V-band oxygen spec-

trum, and it achieves the lowest noise figure among similar Si-based Dicke radiometers. One of these implementations was presented in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, November 2018 [8].

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Millimeter-Wave Frequencies and Applications

The millimeter-wave (mm-wave) frequency spectrum is located between 30 to 300 GHz, and its unique properties make it attractive for a wide range of applications. It offers larger bandwidth and shorter wavelength than lower frequencies, which is needed to increase communication data-rates and realize smaller component and antenna sizes. This short wavelength is suitable for system integration of handheld devices and achieving a narrower beam-width for high-resolution radars and imagers. These signals propagate in the line of sight and are not reflected by the ionosphere layer. At typical power densities, mm-wave signals are blocked by building walls, and attenuation by rain is a serious problem even over short distances. Therefore, mm-wave signals generally have a short propagation range, which can be advantageous for low-interference and high-security applications. Car manufacturing companies are taking advantage of these properties to develop short-range radars, an essential piece of equipment for autonomous vehicles [9]. Furthermore, mm-wave body scanners are widely adopted to look for concealed weapons and objects at airport security ports. One of the other applications at mm-wave frequencies is remote sensing, which is the main focus of this work.

Remote sensing is the science of information acquisition about the Earth and its atmosphere by measuring the electromagnetic signals emitted due to the black-body radiation of its constituents. Some of the physical properties that can be obtained with mm-wave remote sensing are precipitation, snow rate, ocean salinity, vegetation mapping, and atmospheric temperature profile of the Earth. Figure 1.1 shows the attenuation level of mm-wave signals in the atmosphere with a few specific absorption lines at the resonance frequencies

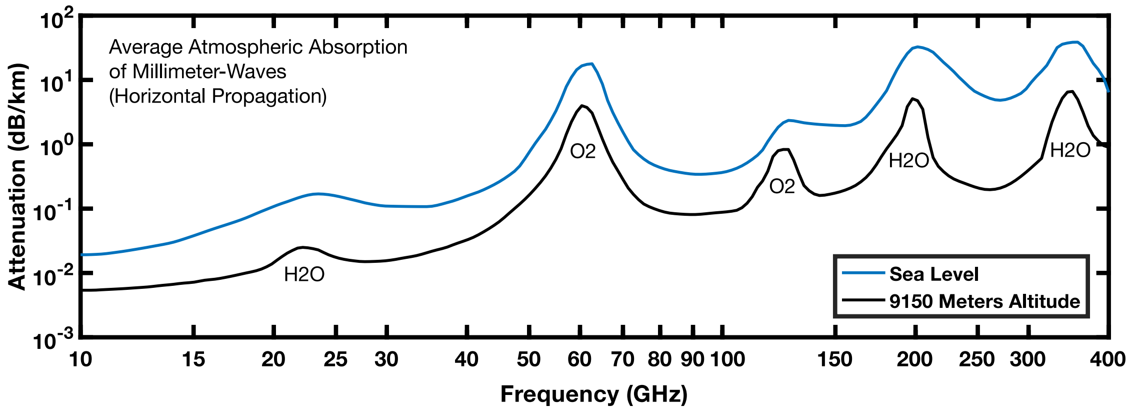


Figure 1.1: Atmospheric absorption across the mm-wave frequency range.

of oxygen and vapor water. In the 1-15 GHz range, the atmosphere is transparent, and radiometers operating in these frequencies are used for land and ocean observations, while resonance frequencies of oxygen and vapor water are around 60 GHz, 118 GHz, 183 GHz, and 325 GHz. At frequencies between these absorption lines, mm-waves have much less attenuation and much longer traveling range, and these are mostly used for wideband data communications, while the resonance frequencies are mostly used for atmospheric radiometry and obtaining vertical distribution profiles of the Earth's atmospheric temperature and humidity.

1.2 Importance of Atmospheric Remote Sensing

Atmospheric radiometry can help monitor and predict weather and environmental events, including tropical systems, tornadoes, dust storms, volcanic eruptions, wildland fires, atmospheric temperature, and humidity, as well as managing rescue missions [10]. Such capabilities lend support to authorities through providing critical weather information during events [11], and these are key enablers to meet public safety, economic and environmental mission requirements. In addition, weather and climate data are essential for agriculture, civil and urban planning, environmental and pollution monitoring, geological exploration, forestry, insurance, and terrestrial mapping. In agriculture, remote sensing satellites enable the identification of insects, diseases, and irrigation problems. Remote imagery assists local governments with urban planning, property appraisal, and emergency planning and response. Commercial weather industry analysts estimated that annual revenues in 2000 total about $ 430 million in the U.S. [12].

Aviation, probably more than any other transportation mode, is greatly affected by weather [13]. Every phase of flight can be impacted, and it has to deal with thunderstorms, snowstorms, wind, fog, and extreme temperature and pressure. Commercial aviation in the U.S., with its more than 16,000 daily flights, must regularly deal with these adverse weather types, and the cost is a significant budget item.

State and local emergency managers depend on vital up-to-the-minute information for disaster preparedness, response, and recovery, and the protection of the nation's critical infrastructure and natural resources [14]. In this regard, improved accurate forecasts can help better predict hurricane paths, allowing emergency managers to target their efforts and preventing unnecessary coastal evacuations that can cost up to $1 million a mile [15]. Because of the importance of space-based measurements from small satellites, the government started several programs and initiatives to support the research and development in this area.

To improve global climate models, NASA has been using satellite-based radiometers for decades to collect global-scale observations of the Earth. These measurements are vital to our understanding of the planet as a system both spatially and temporally and must be collected from satellites orbiting the Earth [16]. One of the high-level goals presented in the NASA 2014 Strategic Plan is to "Advance knowledge of the Earth as a system to meet the challenges of environmental change and to improve life on our planet"[17]. This high-level goal flows down into two sub-goals; scientific understanding of the climate system and technology development of Earth-based remote sensing instruments. More specifically, the NASA 2014 Science Plan called for researchers to "improve the ability to predict climate changes by better understanding the roles and interactions of the ocean, atmosphere, land, and ice in the climate system"[18] and the NASA 2015 Technology Roadmap called for re-

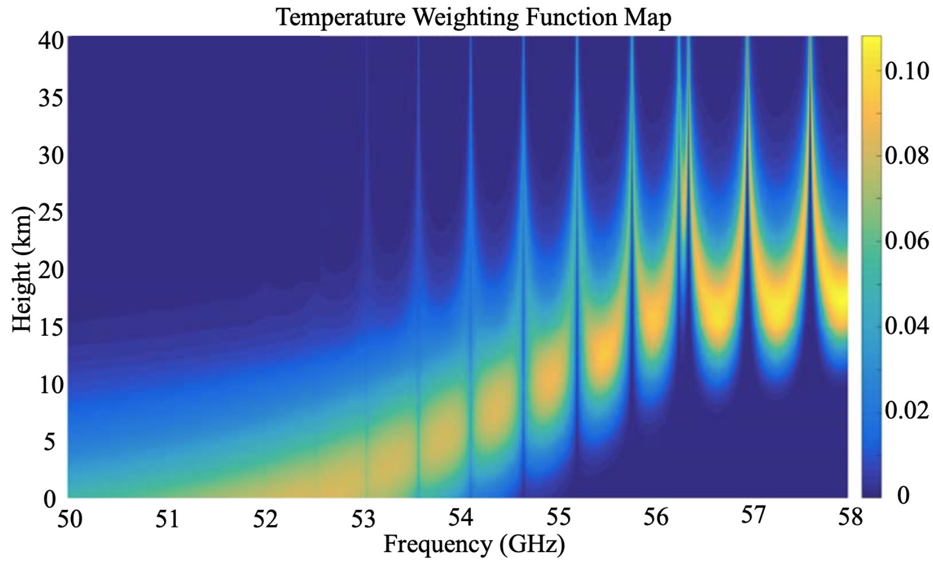


Figure 1.2: Clear-air temperature weighting function spectra (in km^{-1}) between 50-58 GHz (Courtesy of Dr. Albin J. Gasiewski).

searchers to ”improve remote sensing capabilities and performance” through ”investments in microwave, millimeter -... receiver component technology including low-noise receivers ... and field demonstration of active and passive instruments from mm to sub-mm wavelengths” [19].

1.3 Basics of Radiometry Systems

1.3.1 Oxygen Absorption Spectrum

At high altitudes, individual lines of the absorption spectrum at resonance frequencies of oxygen and water vapor are distinct, while near to sea level, collisional broadening of the lines smears the spectrum into a broad spectrum. Figure 1.2 shows the clear-air temperature weighting function spectra (in km^{-1}) for the lower wing of the 5-mm O_2 temperature sounding band from $50-58$ GHz. By processing the atmospheric radiations at those particular frequencies, the atmosphere’s temperature profile can be extracted. Depending on the application, the whole $50-58$ GHz frequency range can be down-converted and processed, or alternatively, a set of radiometer frequencies and bandwidths can be selected

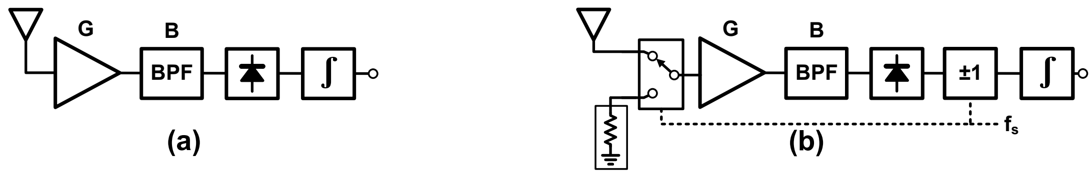


Figure 1.3: a) A total power radiometer and b) Dicke radiometer.

for constructing a temperature profilometer based on a few altitude bins [20]. The latter channelized approach lends itself naturally to a switched filter radiometer implementation, which is demonstrated in chapter 7.

1.3.2 Dicke Switching

The objective of a remote sensing receiver (radiometer) is to measure the radiated power of RF signals. It is common to express power in terms of the equivalent temperature of a blackbody that radiates the same power. Figure 1.3(a) shows a block diagram of a radiometer with a bandwidth of B and a gain of G. Assume this radiometer is pointed at an object with an equivalent temperature of T_A. The radiated signal is received with an antenna, filtered, and amplified. Ideally, the measured output power equals $P = kGBT_A$, where k is the Boltzmann's constant. However, in practice, the radiometry circuits generate an additional noise power, modeled with an input-referred equivalent temperature of T_N. Then, the measured output power of the radiometer is $P = kGB(T_A + T_N)$. If k, B, G, and T_N are constant over time, there is no stability problem. However, in practice, the gain and noise of the radiometer slowly change over time and invalidate the measurement. Therefore, the received power is integrated over time, and the minimum resolvable temperature of a radiometer is a function of the measurement integration period, τ, and is defined as the standard deviation of the output signal, $\Delta T = (T_A + T_N)/\sqrt{B\tau}$. R. Dicke in [21] suggested a solution to suppress gain fluctuations by inserting a single-pole double-throw (SPDT) switch at the receiver front-end, periodically switching between the antenna and a reference load at a rate higher than the gain fluctuations frequency. The block diagram of this architecture is shown in Figure 1.3(b), known as Dicke switching, and is commonly used

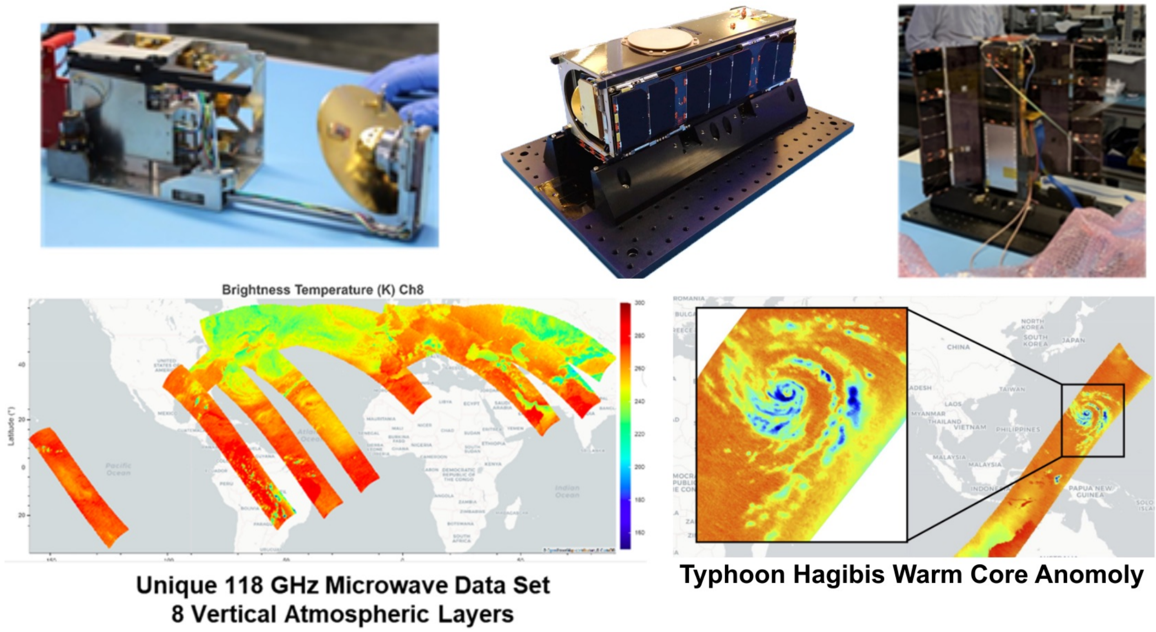


Figure 1.4: GEMS1 CubeSat developed by Orbital MicroSystems for microwave sounding at 118 GHz and a sample data on the Typhoon Hagibis warm core anamoly (Courtesy of Orbital MicroSystems [22]).

in today's remote sensing instruments. In practice, a down-conversion step is also added to the receiver chain so that the sampling rate of the baseband analog-to-digital-converters (ADCs) can cover the IF spectrum. The Dicke radiometer architecture is discussed in more detail in Chapter 2.

1.4 Classic Weather Satellites and CubeSats

Remote sensing observations should be made from space to collect global-scale data. Traditionally, spaceborne radiometers were hosted on large multi-instrument satellites. However, the challenge of data continuity induced a paradigm shift towards tiny satellites (e.g., CubeSats) in distributed constellations to achieve faster revisit rates. The small component and antenna size of the mm-wave radiometers reduces the instrument size, weight, power consumption, and cost (SWaP-C), and it enables economical manufacturing of mm-wave radiometers for Earth-observing CubeSat constellations. The benefits of such CubeSats are shown by the recent development of low SWaP-C radiometers. Figure 1.4 shows images of

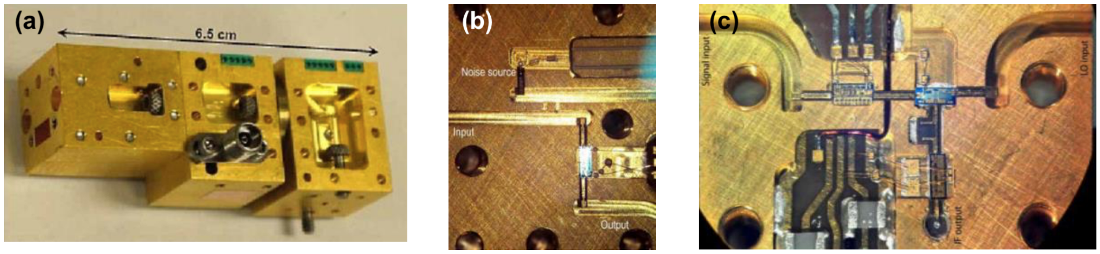


Figure 1.5: MicroMAS EDU receiver front-end electronics (left), MicroMAS first-stage receiver block (center), MicroMAS second stage receiver module with MMIC LNA, mixer, and IF amplifier (right). Image credit: MicroMAS team .

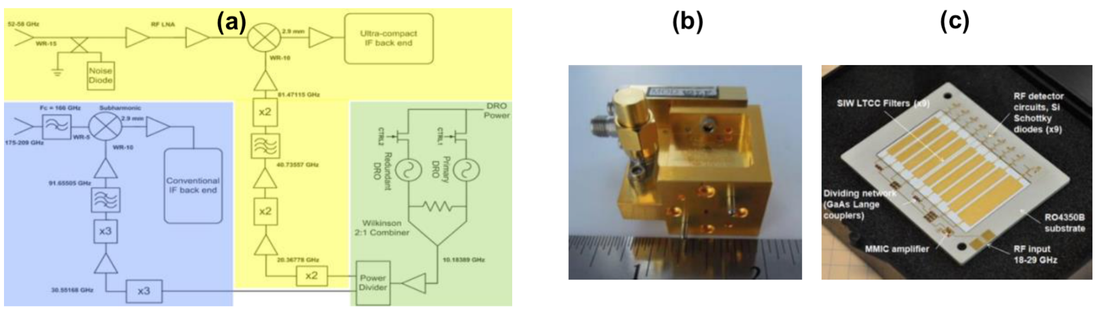


Figure 1.6: MiRaTA radiometer block diagram (left), Virginia Diode Inc mixer used for G-band down conversion (center), and multi-chip IF backend (right) including filter bank, Lange couplers, amplifiers, and RF detectors. Image credit: MiRaTA team.

the GEMS CubeSat-based radiometer developed for microwave sounding at 118 GHz and a sample of the collected data on the Typhoon Hagibis warm core anomaly [22].

In the past few years, several other CubeSat prototypes were designed and implemented ,including MicroMAS, MiRaTA, RACE, TEMPEST [23, 24, 25, 26, 27], which are briefly discussed in the following. The MicroMAS was a 3U CubeSat (shown in Figure 1.5) with a single-sideband total power radiometer measuring nine channels near 118 GHz [23]. This radiometer consists of multiple separately packaged modules, including a mixer module, a local oscillator module, and an RF preamplifier module. The average power consumption was 3W, which was primarily driven by the W-band LO generation block using a resistively tripled dielectric resonator along with a driver amplifier [23, 24].

Figure 1.6 shows the block diagram of the MiRaTA, which was another 3U CubeSat with a triband radiometer at 60, 183, and 206 GHz. This radiometer was implemented with separately packaged modules, including a V-band receiver, a G-band receiver which

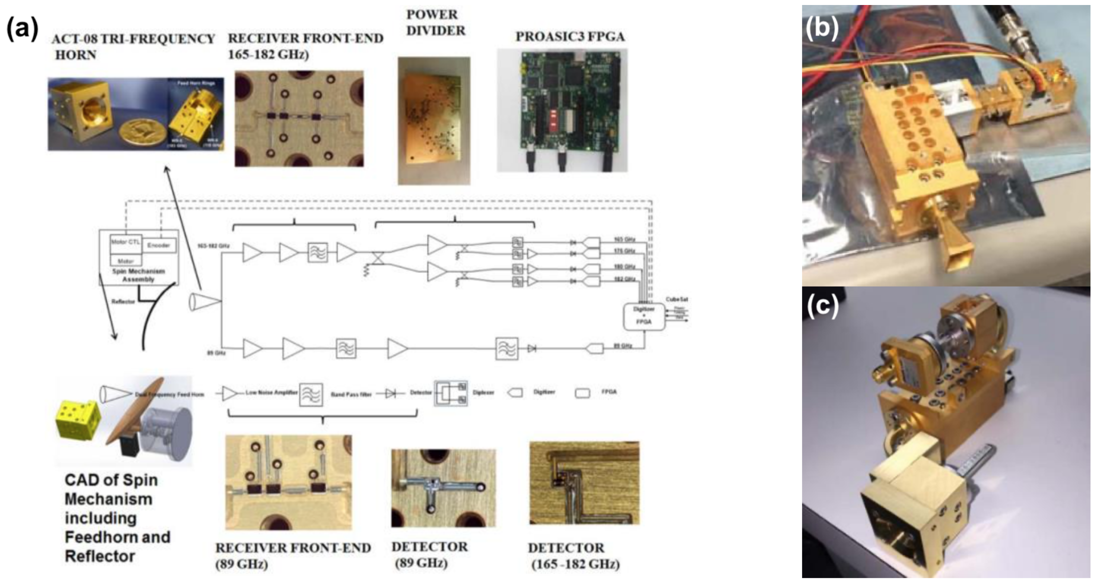


Figure 1.7: TEMPEST instrument block diagram and photos of components (left), radiometer frontends for G-band (right-top) and W-band (right-bottom). Image credit: TEMPEST-D team.

incorporates a subharmonic mixer, a dielectric resonator oscillator, and an IF spectrometer consisting of multi-chip amplifiers, power dividers, SIW LTCC filters, and RF detector circuits. The total power consumption of this instrument was about 6W, mostly consumed by the LO generation and IF backend [24, 25]. The RACE CubeSat was designed by NASA with a two-channel instrument at 183 GHz, which used a direct-detection architecture with a RF power detector to eliminate the need for mm-wave LO generation. The radiometer front-end was integrated into a compact waveguide module employing 35nm InP LNAs [26].

TEMPEST radiometer was another design by NASA (Figure 1.7), which employs a tri-frequency horn antenna and two receiver paths for 165-182 GHz and 89 GHz. All these receivers are implemented with discrete LNAs, detectors, filters, and power dividers, integrated on the package-level [27]. In addition to these multi-chip CubeSat-based radiometers, several single-chip solutions with less complex topologies are also reported for imaging purposes [28, 29]. These radiometers are mostly using a simple total-power radiometer, consisting of an LNA and a power detector. The most similar approach to our radiometer in this work is a W-band Dicke-free radiometer, designed by NASA and UC Davis [30]. This design employs a double sideband down-converter with zero-IF architecture, which has to sweep across all radiometry channels.

1.5 SiGe BiCMOS Technologies for Remote Sensing

SiGe heterojunction bipolar transistor (HBT) technologies have unique properties which are crucial for implementing monolithic CubesSat-based radiometers. The SiGe HBT is basically a Silicon BJT with a graded SiGe alloy in the base region that improves the transistor gain and noise performance. These devices offer excellent 1/f noise performance and low gain variation over long periods of time compared to III-V devices, inherent tolerance to total-dose radiation, and compatibility with standard CMOS fabrication processes, enabling system-on-chip integration.

1.6 Research Objectives and Dissertation Organization

The objective of this research is to investigate the design challenges of mm-wave quadrature receivers for emerging applications (i.e., CubeSat-based atmospheric remote sensing) and come up with novel designs to address these challenges. Figure 1.8 presents the block diagram of a Dicke radiometer depicting a visual outline of this dissertation. In Chapter II, a co-designed Dicke switch and low-noise amplifier (LNA) is presented in which the switch incorporates a transformer-based topology and serves as the input matching network of the LNA. This topology is configured to minimize the amplifier gain mismatch between the two switching states while providing a lower noise figure compared to conventional designs. The circuit is implemented in a 0.13-μm SiGe BiCMOS technology, and it achieves more than 20-dB gain and minimum noise figure (NF) values of 4.5 and 0.58 dB at 300 and 20 K, respectively. Chapter III and IV discuss the theory, design, and characterization of two broadband and low-loss quadrature LO generation networks for mm-wave down conversion. The effects of interconnects and parasitic capacitance on poly-phase filters are

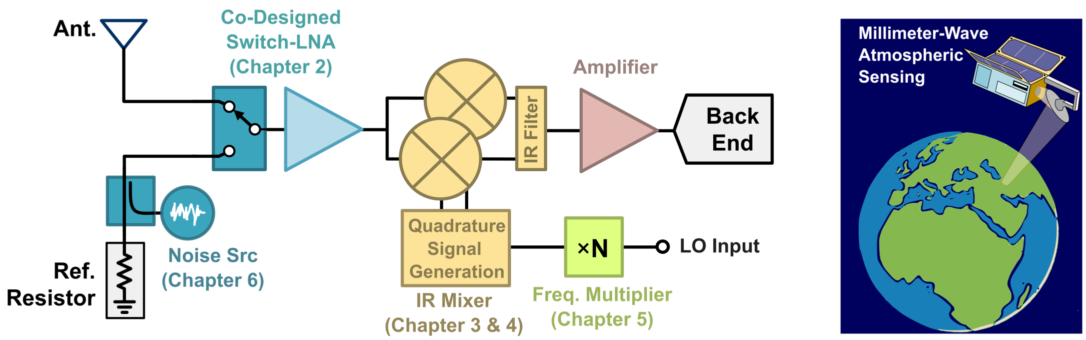


Figure 1.8: Block diagram of a radiometer receiver outlining the dissertation organization.

investigated, and design guidelines are provided to achieve low insertion loss and broad bandwidth. A proof-of-concept mixer was designed based on this network and achieved an average image rejection ratio of 37.5 dB across 40-76 GHz. Chapter V presents a Gilbert-based frequency multiplier, in which the phase of the injected signal to switching transistors is adjusted to maximize the core conversion gain and power-added efficiency. This frequency multiplier achieves the highest CG and PAE among all reported Si-based frequency multipliers without output buffers. Chapter VI compares the noise performance of several on-chip p-n junctions along with the first reliability study of on-chip noise sources in a SiGe BiCMOS technology. These solid-state noise sources may facilitate the internal calibration of radiometers by integrating an ambient noise source and an avalanche noise source. Chapter VII presents three integrated radiometers of this research, emphasizing that SiGe radiometers can be integrated on a single chip while providing competitive noise performance and high gain with a low SWaP-C. These designs can enable the economical manufacturing of mm-wave radiometers for Earth-observing CubeSat constellations. In fact, part of this research is funded by Orbital MicroSystems to develop next generation of commercial earth observation radiometry instruments. Chapter VIII summarizes the contributions of this work and discusses possible future works.

CHAPTER 2

TRANSFORMER-BASED SWITCH AND LOW NOISE AMPLIFIER

The classic Dicke radiometer is implemented with a single-pole double-throw (SPDT) switch, followed by an LNA. However, the loss of typical SPDT switch at V/W-band frequencies is around 1.5$\sim$3.0 dB, and this significantly limits the radiometer resolution. To reduce the switch loss, various topologies have been reported in the literature. For instance, a balanced LNA with an embedded Dicke switch has been presented in [31]. That front-end consisted of two branch-line couplers and two reflective-type phase shifters and achieved a receiver noise figure (NF) of 12 dB at 90 GHz [32]. In [33], a differential-correlating radiometer, with one side terminated to a 50 Ω impedance, was presented as a switch-less Dicke radiometer with a NF of 9.2 dB at 100 GHz. Bi *et al* presented a distributed amplifier with two input transmission lines in order to achieve a NF of 8.4 dB at W-band frequencies [34]. To further minimize the front-end switch loss, a dual-input LNA was suggested in [35]. This technique has been adopted in several other designs as well [36, 37, 38] and achieved low NF values of 5.2 and 6.4 dB at 78 and 75 GHz, respectively. However, these radiometers are vulnerable to process variations, and high-precision bias circuits are required to nullify transistor gain mismatch and maintain high sensitivity.

In this chapter, a transformer-based Dicke switch [39] is co-designed with an LNA, in which the transformer serves as the input matching network. This topology can reduce the passive loss and NF of the front-end and thereby improve radiometer sensitivity. The radiometer performance is investigated in terms of transistor gain variation and phase/amplitude mismatch in the balun, and it is demonstrated that the presented topology suppresses these errors. section 2.1 discusses the radiometer performance, including the sensitivity and transistor gain variation with temperature. section 2.3 explains the co-design of the input transformer and the LNA. Measurement and characterization results are presented in section 2.4.

2.1 Radiometer Performance

Radiometers are highly sensitive receivers aimed at detecting small levels of black-body radiation, which imposes challenging requirements on the NF and gain fluctuations of the mm-wave receivers. The sensitivity of a radiometer is given by

$$\Delta T = T_{\text{sys}}\sqrt{\frac{1}{B\tau} + \left(\frac{\Delta G}{G}\right)^2} \tag{2.1}$$

where B is the RF bandwidth, τ is the integration time, T_{sys} is the receiver noise temperature, and $\Delta G/G$ is the gain fluctuation [40]. To suppress the contribution of gain fluctuations, a single-pole double-throw (SPDT) switch, known as Dicke switch, can be inserted at the receiver front-end. The Dicke switch should alternatively switch between the antenna and a reference load at a rate higher than the frequency of the gain fluctuations [21]. This operation ensures gain stability of the radiometer at the expense of reducing the measurement time window, adding a few dB passive loss at the front-end and increasing the noise temperature of the receiver.

One way to improve the radiometer sensitivity is to maximize the integration time and bandwidth; however, this is not always feasible in applications such as satellite-based radiometry, which focus on particular narrow-band frequency channels and have a limited time on orbit for scanning. To achieve high sensitivities in radio astronomy, the receiver has to be cooled down to cryogenic temperatures to reduce the noise temperature. Several candidate circuit topologies were previously reported which focus on reducing the receiver noise temperature by eliminating the front-end switch loss and implementing its functionality by introducing two separate receiver paths for measurement and calibration [31, 33]. These circuits can potentially achieve a low noise temperature, but the transistor gain mismatch can degrade the precision of these radiometers due to process variations, particularly

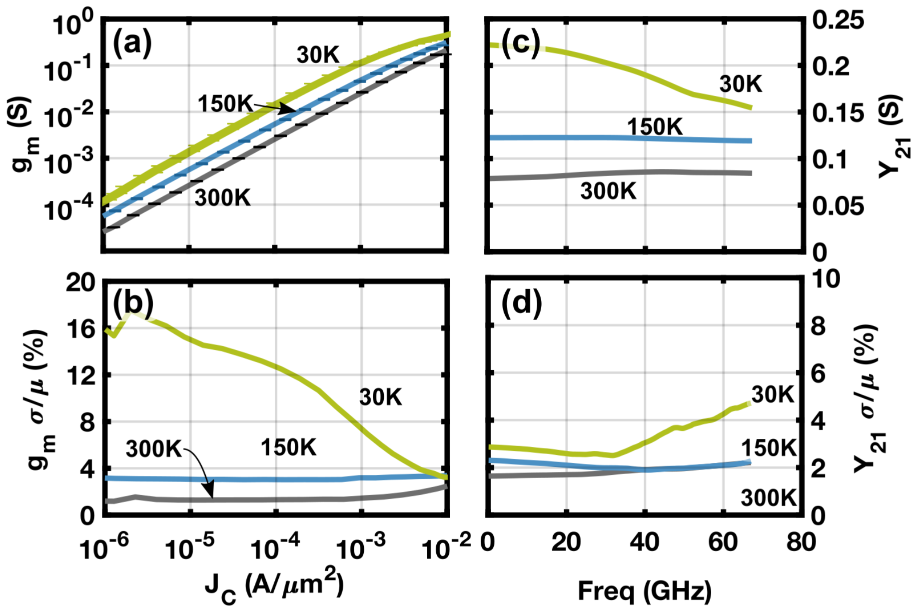


Figure 2.1: Measured g_m and Y_{21} of thirteen SiGe HBTs over temperature and their variations. The size of SiGe HBTs were $0.13 \times 9\,\mu$m, which is the same as the size of the transistors used in the amplifier design: a) transconductance (g_m) as a function of bias current density when $V_{\text{CB}} = 0$, b) standard deviation of g_m divided by the average g_m, c) measured Y_{21} as a function of frequency for $V_{\text{CB}} = 0$ and around the average current of 2.7 mA, and d) standard deviation of Y_{21} divided by the average Y_{21} (© 2021 IEEE).

at cryogenic temperatures.

2.1.1 Transistor Variability

SiGe HBTs have excellent RF performance under cryogenic conditions [41, 42], and they can operate at temperatures as low as 70 mK [43]. Previous studies have shown that receiver cooling improves the noise temperature, but it also results in increased gain fluctuation over time, as well as gain mismatch between identical devices [44, 45, 46]. We characterized the g_m and Y_{21} of thirteen SiGe HBTs located on the same die in an advanced 130 nm SiGe BiCMOS technology (GlobalFoundries SiGe 8XP). These devices were measured at 300, 150, and 30 K, and the results are presented in Figure 2.1. The g_m for current densities of less than 10^{-3} A/μm^2 increases by 4x between 300 K and 30 K, whereas the variability normalized to its mean value (standard deviation σ divided by average μ) increases by 6x − 8x for the same current densities. On the other hand, the ac performance is less sensitive

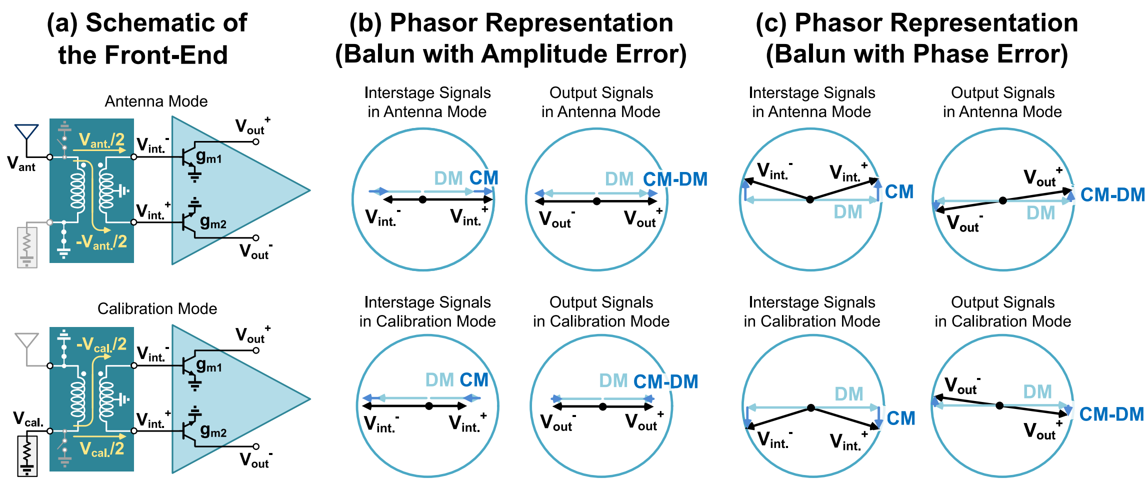


Figure 2.2: a) schematic of the front-end switch-LNA. Phase representation of CM and DM signals at the outputs of the balun and amplifier for a balun with b) amplitude error and c) phase error (© 2021 IEEE).

to temperature, and the normalized variability of Y_{21} is less than 2% and 5% at 300 and 30 K, respectively. This is particularly important for high-precision measurement circuits that employ identical transistors in their topology since these devices do not necessarily provide the same average gain in the presence of mismatch.

2.2 Transformer-Based Dicke Switch

In this work, we present a differential Dicke radiometer front-end with ultra-low-noise performance and minimized gain mismatch between the antenna and calibration paths. Figure 2.2(a) shows simplified schematics of this front-end in both states, where the Dicke switch is implemented with a transformer and two shunt switches. The transformer acts as a balun for the differential LNA, and the primary coil can be driven from both ends (i.e., from the antenna or the reference load). Co-design of the switch and the LNA eliminates the need for 50 Ω interstage impedance matching, relaxing the matching network design and minimizing the front-end passive loss and NF.

The gain mismatch between the antenna path and the calibration path of this topology is analyzed as follows. The outputs of an ideal balun are purely differential, as shown in

Figure 2.2(a). Even with transistor gain mismatch, the amplifier gain at both antenna and calibration states is equal to the average gain of two transistors. However, in practice, on-chip transformers present some phase and amplitude mismatch due to the asymmetric balun layout. This mismatch appears as a common-mode signal (CM) at the amplifier input. The CM signal can be completely suppressed in a gain-matched differential pair, whereas in a mismatched pair, this CM signal results in a differential error. At low frequencies, this error factor is equal to [47]

$$\text{Gain}_{\text{CM-DM}} \approx \frac{\Delta g_m R_L}{(g_{m1} + g_{m2})R_E + 1}, \tag{2.2}$$

and the CM rejection ratio (CMRR) of the differential pair can be calculated as

$$\text{CMRR} = \frac{\text{Gain}_{\text{DM}}}{\text{Gain}_{\text{CM-DM}}} \approx \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_E}{2\Delta g_m}, \tag{2.3}$$

where g_{m1} and g_{m2} are the transconductances of the first-stage transistors, Δg_m is the gain mismatch, R_L is the load impedance, and R_E is the tail resistance of the differential pair. With no tail impedance, the CMRR can be approximated by $g_m/\Delta g_m$. The high-frequency equivalent of this term would be $Y_{21}/\Delta Y_{21}$, and based on the results shown in Figure 2.1, it varies between $20 - 50$. Therefore, this topology can suppress the mismatch of the two states by one or two orders of magnitude. Note that any mismatch between passive components can also degrade the gain matching, and symmetric layout techniques should be used to minimize any asymmetries in transformers and capacitors.

Figure 2.2(b-c) show the phasor representation of CM and differential-mode (DM) signals at the output nodes of the balun and amplifier when the transformer has only amplitude or phase mismatch. In Figure 2.2(b), the amplitude error in the balun generates a CM signal between $V_{int.}^{-}$ and $V_{int.}^{+}$. This CM signal is attenuated in the amplifier, and due to device mismatch, it appears as a DM signal at the output of the amplifier. However, since this CM-DM signal has opposite polarities in the calibration and antenna states, it causes a small mis-

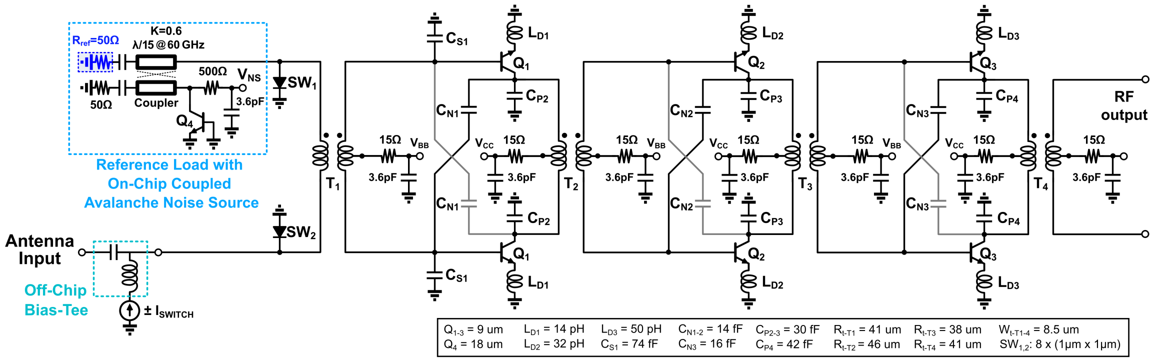


Figure 2.3: Schematic of the designed radiometer front-end. Switches SW_1 and SW_2 are implemented using PIN diodes (© 2021 IEEE).

match between the overall amplifier gain in both states. Whereas in Figure 2.2(c), the CM component is orthogonal to the DM counterpart at balun outputs, and it only changes the output phase and leaves the amplitude intact. The phase information of the received signal is typically not used in passive radiometry. In short, the amplitude mismatch of the balun is rejected by CMRR in the present topology, and the phase mismatch does not affect the sensitivity of the passive radiometer.

Two topologies have been presented in [31] and [33] to reduce the front-end passive loss by removing the front-end switch. In both designs, two separate amplifiers and a front-end hybrid coupler were employed for power splitting, introducing phase shift of 90°, and eventually implementing the switching functionality by signal conditioning. The topology presented in Figure 2.2(a) takes advantage of the differential nature of the design to minimize the effects of transistor gain mismatch and balun phase and amplitude errors, but this was not applicable in [31] and [33]. The gain matching between the measurement and calibration states in the present work can be further enhanced by adding an emitter degeneration to boost the CMRR of the differential pair.

2.3 Circuit Design

Figure 2.3 presents the schematic of the designed radiometer front-end which consists of a transformer-based Dicke switch, a three-stage differential LNA, and an on-chip coupled noise source for calibration purposes. In this work, we co-designed the LNA and the input transformer-based switch to circumvent the need for interstage 50-Ω impedance matching. This approach relaxes matching requirements, shrinks the passive loss, and hence improves the overall NF. The noise source will be discussed in chapter 6.

Co-design of the LNA and transformer requires determining the optimum dimensions (i.e., trace width and radius) of the input transformer (T_1) and the proper emitter length of the transistors in the input stage of the LNA. The simulation setup shown in Figure 2.4 is used to achieve this goal, where W_t and R_t are the trace width and radius of the transformer, respectively. A hexagonal transformer with a ratio of one-to-one was realized in two thick top metal layers of the technology to minimize passive loss. In Figure 2.4, L_D1 is the degeneration inductor, and it is used to bring the input impedances of the transistors close to the conjugate of their optimal noise impedance (S^*_opt) and therefore realize simultaneous noise and impedance matching, C_N1 is neutralization capacitor needed to nullify the impact of the collector-base capacitor (C_CB) and improve the gain and stability, C_S1 is the matching capacitor connected to the secondary side of the transformer, and Z_Lopt is the optimal load impedance. It is worthwhile to note that although C_N1 slightly degrades the noise figure and f_T of the transistor [48], it elevates the gain of the first stage and therefore mitigates the noise contribution of the subsequent stages. The optimum value of C_N1 is chosen to minimize the NF of a three-stage LNA, assuming that each stage has a similar gain and noise performance.

The transistors were operated in low-injection (i.e., lower than peak f_T bias point) for minimum noise contribution. The switch was modeled by a 2-Ω resistor in its ON state [49], whereas its OFF capacitance was about 25 fF. The pad capacitance was estimated to be 20 fF based on the electromagnetic simulation results. A 15-Ω resistor was connected to the center point of T_1 to suppress undesired oscillations.

After initial simulations and design of the LNA with an ideal transformer model [50], an AEL script in Keysight ADS was used to optimize transformer dimensions and other circuit

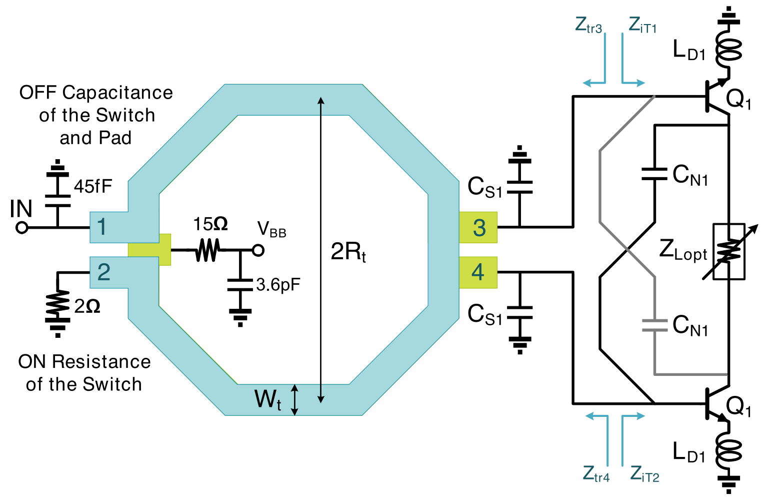


Figure 2.4: Simulation setup to co-design the transformer and the input stage of the LNA. An AEL script in Keysight ADS was run to co-optimize the transformer layout and circuit schematic (© 2021 IEEE).

parameters, simultaneously. At each optimization iteration, the software set transformer dimensions in layout, ran EM simulations for it, and then optimized the circuit based on the EM-simulated transformer. This cycle was repeated for different transistor sizes, where the following goals were defined for the optimization process.

1. The input reflection coefficient should be less than -13 dB.
2. The amplitude mismatch between ports 3 and 4 of T_1 should be less than ± 0.5 dB.
3. The phase mismatch between ports 3 and 4 of T_1 should be less than $\pm 5°$.
4. The overall NF should be minimized, while achieving a high gain (e.g., 7 dB).

Figure 2.5 depicts the optimum values of the circuit parameters obtained for 60 GHz, where

1. The power gain and NF improve when emitter length increases, as shown in Figure 2.5(a).
2. If emitter length is higher than 6 μm, the optimal collector-emitter voltage (V_{CE})

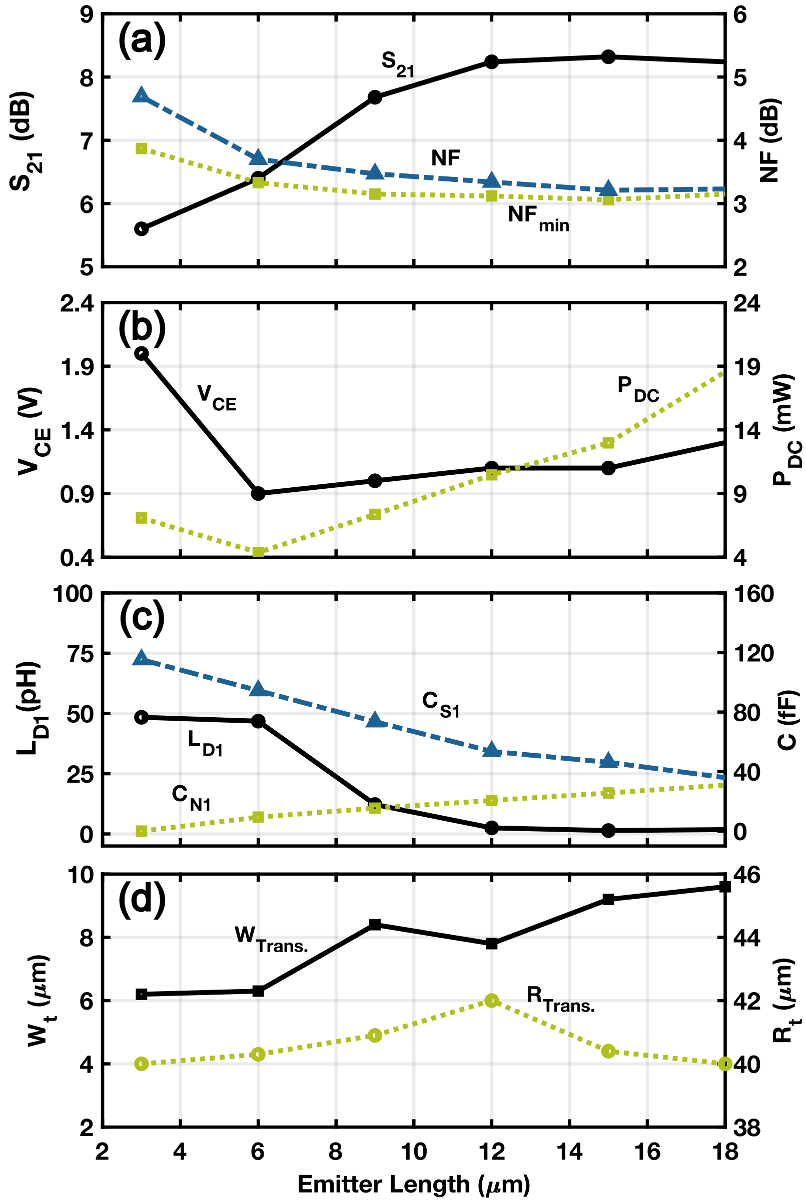


Figure 2.5: Optimal design values versus the emitter length of the transistor at 60 GHz. (a) gain (S_{21}), minimum noise figure ($\mathrm{NF_{min}}$), and noise figure (NF), (b) dc power consumption (P_{DC}) and collector-emitter voltage (V_{CE}), (c) trace width (W_{t}) and radius (R_{t}) of the transformer, and (d) C_{N1}, L_{D1} and C_{S1} (© 2021 IEEE).

slightly increases as emitter length becomes larger. This increases dc power consumption of the circuit, as shown in Figure 2.5(b).

3. The optimum values of L_{D1} and C_{S1} reduce with increasing emitter length. On the other hand, the value of the neutralization capacitor (C_{N1}) should be increased when

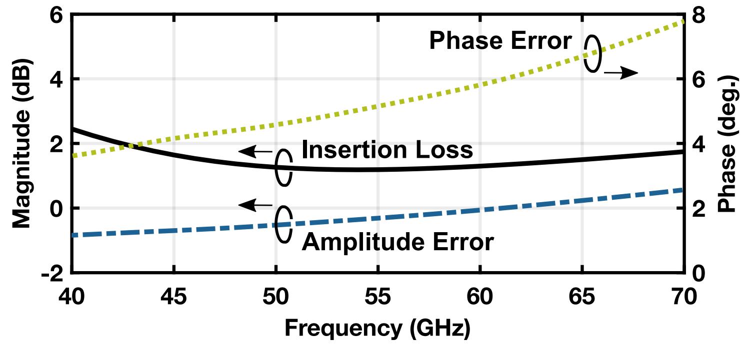


Figure 2.6: Transformer insertion loss, amplitude error, and phase error versus the frequency (© 2021 IEEE).

the transistor size becomes larger.

4. The optimum trace width of the input transformer gradually increases as we enlarge the input transistors.

Considering the above points, there exists a trade-off between the optimum NF, gain, and the dc power consumption of the circuit. Therefore, from Figure 2.5(a) and (b), emitter length of 9 μm were chosen in the present work as a compromise between the NF and P_{DC}.

As shown in Figure 2.5(d), the optimum trace width and transfomer radius for emitter length of 9 μm are 8.5 and 41 μm, respectively. The loss of this transformer is presented in Figure 2.6, where the achieved loss is less than 1.2 dB at mid-band. The transformer loss, with the impedance terminations shown in Figure 2.4, is defined as the ratio of the power delivered to port 1 of the transformer to sum of the output powers achieved from ports 3 and 4, i.e., $L = 10\log[P_{\mathrm{T1}}/(P_{\mathrm{T3}} + P_{\mathrm{T4}})]$. The simulated amplitude and phase errors are also shown in Figure 2.6. The amplitude error is less than 0.5 dB in the desired bandwidth, while the maximum phase error is 8°.

The input transformer and first-stage of the LNA are followed by two gain stages to increase the overall power gain. The emitter length for the second and third stage transistors is 9 μm, and they are biased to operate at a base current of 5 μA. Transformers with unity turn ratio and additional shunt capacitors (C_{P2} to C_{P4} in Figure 2.3) were used as interstage and output matching networks. DC bias voltages of the transistors are provided through

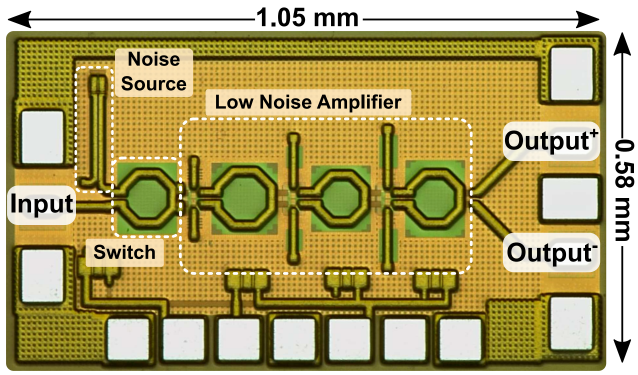


Figure 2.7: Chip micrograph of the front-end with a die area of 0.6 mm^2 (© 2021 IEEE).

the center-tap of the transformers. Due to moderate gain of the first stage (i.e., $\approx$ 9 dB excluding the loss of the transformer), degeneration inductors (L_{D2} and L_{D3}) were used in the second and third stages to compromise between the achived gain and noise figure. Furthermore, to compensate the gain drop due to the degeneration inductors, we employed neutralization capacitors, C_{N2} and C_{N3}, in the second and third stages as well, to increase the overall gain of the circuit.

PIN diodes with eight 1×1 μm^2 fingers were employed to realize the input shunt switches (SW_1 and SW_2). These diodes can be turned ON and OFF by sourcing or sinking a dc current to the primary coil of the input transformer. The ON resistance (R_{ON}) and OFF capacitance (C_{OFF}) of the diode load the input transformer, and it should be considered in the co-design of the transformer and LNA, as shown in Figure 2.4. For the chosen diode geometry, simulation results indicate that $R_{\text{ON}} = 2\ \Omega$ and $C_{\text{OFF}} = 25$ fF. Please note that PIN diode switches can be replaced with CMOS transistors or reverse-saturated SiGe HBTs [49], which provide easier control of switching voltages/currents through the gate or the base terminals. In this work, the minimum NF of the SiGe HBTs without neutralization capacitor is about 1.9 dB, and it increases to 2.1 dB after adding C_{N1}. The loss of the input matching network is 1.2 dB at the center frequency. It is noteworthy that 0.3 dB of this loss comes from the ON-state resistance of the shunt switch.

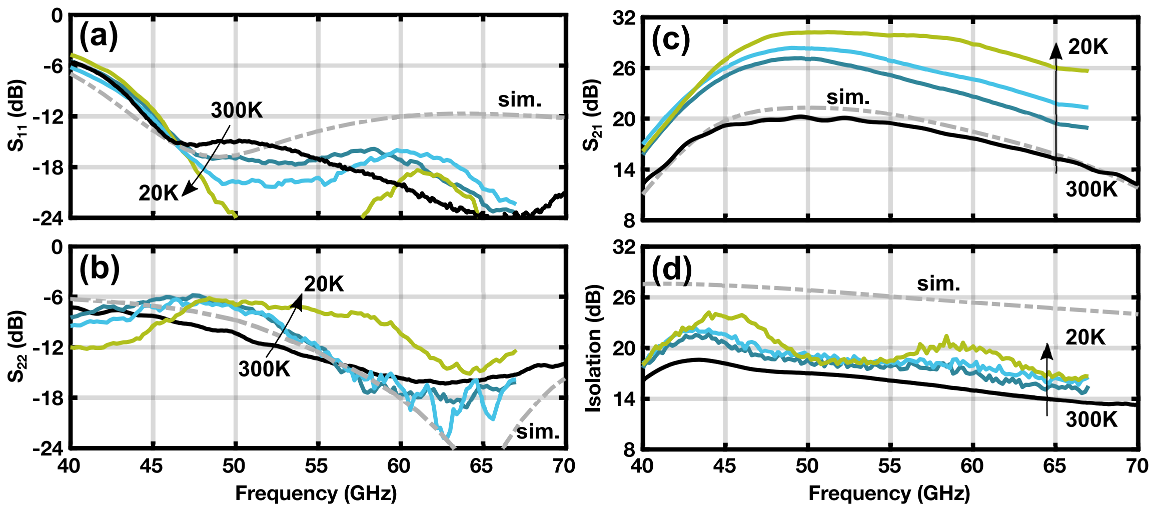


Figure 2.8: Simulated S-parameters of the receiver front-end at 300 K and measured S-parameters at different temperatures (© 2021 IEEE).

2.4 Measurement Results

The co-designed switch and LNA were fabricated in a commercial 130 nm SiGe BiCMOS platform and it occupies a die area of $0.58 \times 1.05\,\text{mm}^2$, as shown in Figure 2.7. The LNA consumes a dc power of 15 mW from a 1 V supply. It was measured via on-chip probing on a commercial cryogenic probe station, and the S-parameters were measured using an Agilent E8361C network analyzer while the device temperature was set to 300, 150, 78, and 20 K. The S-parameter calibration reference plane was the tip of probes, and the simulation data and measurement results are shown in Figure 2.8. The input port is matched with better than -15 dB reflection over $45-70$ GHz, and the output port is matched with a better than -10 dB reflection at room temperature. The circuit achieves a peak gain of 20.1 dB at 300 K, and the gain increases to 30.3 dB at 20 K. The switch state is selected by sinking or sourcing a dc current via a bias-tee connected to the input pad. This current is swept from -16 to 16 mA, and a mean isolation of 17 dB was measured at mid-band. The isolation increases to 20 dB at low temperatures.

The NF measurement setup is shown in Figure 2.9, where a Quinstar WR-15 noise source and an Agilent E4440A spectrum analyzer were used. The calibration reference

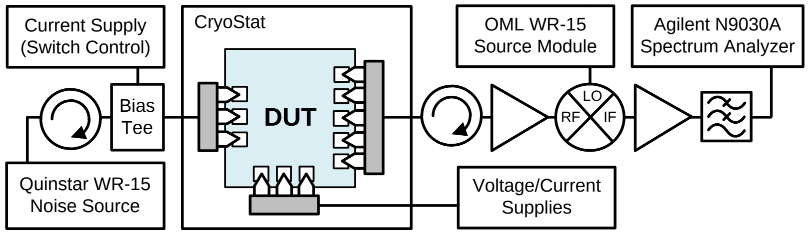


Figure 2.9: Noise figure measurement setup (© 2021 IEEE).

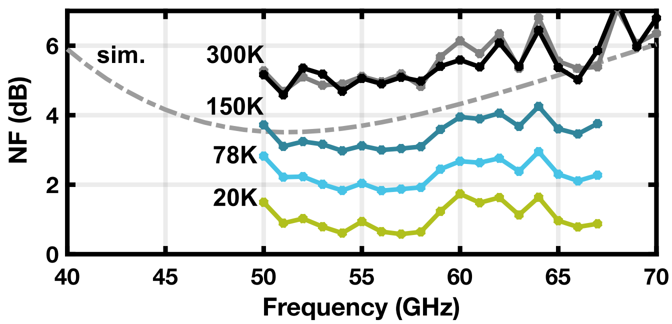


Figure 2.10: Simulated noise figure of the front-end at 300 K along with the measured noise figure of the receiver front-end at 300, 150, 78, and 20 K (© 2021 IEEE).

plane for NF measurements was the input of the CryoStat, and the loss of cables and probes were de-embedded. The uncertainty of NF measurements was about 0.14 dB. The simulated and the measured NF are compared in Figure 2.10, where a measured minimum value of 4.5 dB at room temperature was achieved. This measured value is higher than the simulated result, which is due to the fact that PIN diodes were not properly modeled in the PDK for reverse bias conditions [51]. The measured NF decreases significantly as temperature decreases, achieving a minimum NF value of 0.58 dB at 54 GHz and an average NF of 0.7 dB across 50 – 58 GHz at 20 K. The performance of this mm-wave front-end is compared with the performance of state-of-the-art mm-wave receivers and Dicke radiometer front-ends in Table 2.1. Our design achieves the lowest NF among similar Si-based Dicke radiometer front-ends at V-band frequencies. Table 2.4 compares the performance of this receiver front-end with the state-of-the-art cryogenic LNAs. The noise temperature of the current design is less than the noise temperature of the V-band LNA presented in [52].

Table 2.1: Performance Comparison of the State-of-the-Art mm-Wave Receivers and Dicke Radiometer Front-ends (© 2021 IEEE)

Ref.	Technology	Freq. (GHz)	Gain (dB)	NF[a] (dB)	IL (dB)	Iso. (dB)	P_{DC} (mW)	Area[b] (mm^2)	Topology
[8]	130 nm SiGe	56–69	66	6.1	1.8	18.9	180	3.1	SPDT + LNA + IR Mixer + Freq. Mult. + IF amp.
[32, 31]	180 nm SiGe	71–97	30	12	–	≥10	200	12.5	SPDT + LNA + (Detector + Baseband)
[34]	130 nm SiGe	80 – 105	42	8.4	0.93	18+	28.5	3.42	SPDT-DA + LNA
[37]	65 nm CMOS	65 – 90	26.8	6.4	–	40+	52.3	0.47	Dual-Input Pseudo Switch LNA
[38]	130 nm SiGe	23–26	15.9	6.1	–	–	21.9	0.36	Dual-Input Pseudo Switch LNA
[53]	130 nm SiGe	55–64	7.2	10.2	–	–	90	1.2	Switch + LNA + Mixer
[54]	65 nm CMOS	82–93	27	11.2	4.2	25	38.4	0.31	SPDT + LNA + (Detector)
[55]	120 nm SiGe	85–99	24.7	10.3	2.3	21	34.8	0.4	SPDT + LNA + (Detector)
This Work	130 nm SiGe	42–62	20.1	4.5	1.2[c]	17	15	0.6	Co-Designed Switch-LNA + Noise Source

[a]Minimum noise figure (this value does not account for the power detector noise). [b]Active area. [c]Simulated insertion loss.

Table 2.2: Performance Comparison of the State-of-the-Art Cryogenic LNAs in SiGe BiCMOS Technologies (© 2021 IEEE)

Ref.	Tech.	Temp. (K)[a]	Freq. (GHz)	T_{N}^{b} (K)	Gain (dB)	P_{DC} (mW)
[56]	120 nm	15	0.1-5	4.3[c]	>29.6	20
[57]	130 nm	19	0.5-4	<8	>25	8.3
[58]	120 nm	15	19-23.5	<45	>20	0.9
[52]	130 nm	20	52-65	191[c]	15.6	6.3
This Work	130 nm	20	50-58	50.7[c]	30.3	15

[a]Temperature. [b]Noise temperature. [c]Average value.

2.5 Summary

An integrated V-band SiGe radiometer front-end is presented for use in millimeter-wave remote sensing, imaging, and radio astronomy. The front-end consists of a transformer-based switch, a differential low noise amplifier, and an on-chip avalanche noise source. The transformer-based switch was co-designed with the low noise amplifier where the transformer serves as the input matching network of the amplifier, reducing the front-end loss and minimizing the overall noise figure while suppressing the gain mismatch between the input stage devices. The front-end circuit achieves peak gain values of 20.1 and 30 dB at 300 and 30 K, respectively. The minimum measured noise figures are 4.5 dB at 300 K and 0.58 dB at 30 K, achieving the best results among the reported mm-wave Dicke radiometers implemented on silicon. This work was published in *IEEE Journal of Solid State Circuits*, May 2021 [2].

CHAPTER 3

QUADRATURE DOWN CONVERSION

One of the main challenges of mm-wave quadrature down converters is generating highly-balanced quadrature LO signals. I/Q signal generation circuits can be divided into four categories: 1) quadrature voltage oscillators (QVCOs), 2) frequency divide-by-two circuits, 3) polyphase filters (PPFs) and quadrature all-pass filters (QAFs), and 4) quadrature hybrids, Lange-couplers, and branch-lines. QVCOs suffer from a higher phase noise and a lower tuning range compared to their non-quadrature counterparts [59]. Frequency divide-by-two circuits can generate I/Q signals, but they require an oscillator to operate at twice the desired frequency, where typically the low-Q tanks degrade the performance of the oscillator [60]. PPFs (e.g., conventional RC-CR networks) are narrowband, lossy, and sensitive to process variations. To improve the robustness of PPFs against process variations and to extend the operating bandwidth, several stagger-tuned stages can be cascaded, but at the expense of increased insertion loss [61]. QAFs split the phase orthogonally in RLC networks over a wide bandwidth, but they are sensitive to parasitic load capacitance [62]. Quadrature hybrids (QH) and Lange-couplers are physically large at RF and microwave frequencies due to the required $\lambda/4$ transmission lines in their structure. While footprints of QHs and Lange-couplers are relatively small at mm-wave frequencies, their amplitude matching is still highly dependent on the coupling factor [63].

To improve the phase/amplitude matching of I/Q signals, several calibration techniques have been reported. DSP algorithms have been used to compensate I/Q mismatch, but the realization of these techniques requires control circuits, additional die area, and substantial computational power [64, 65, 66]. A power-locked loop system has been presented in [67] which monitors the power level of the I and Q signals and automatically reduces the difference between them. Two voltage detectors, an attenuator, and an operational amplifier are required to implement such a power-locked loop. Mismatch tuning of the circuits reported in [68] and [69] should be performed manually, using varactors and CMOS transistors, to obtain accurate I/Q signals. In addition, a transformer-based network has been demonstrated in [70] to generate I/Q signals from 2.7 to 24 GHz.

In this work, a passive low-loss quadrature signal generation network is presented which inherently enhances the phase/amplitude matching of the I/Q signals and extends the bandwidth of the network presented in [70] to mm-wave frequencies. In the present work, two QHs are employed to generate narrowband I/Q signals. Then, the I/Q signals are applied to a quadrature hybrid ring (QHR) that combines these I/Q signals and compensates their quadrature errors. This provides I/Q signals over a broad bandwidth. Several QHR stages can be cascaded to provide more balanced I/Q signals. Compared to the calibration techniques found in the literature, this method is more efficient due to superior linearity, frequency scalability, design simplicity, and zero static-power consumption. To validate this quadrature signal generator, two IR mixers are implemented in a 0.13 μm SiGe BiCMOS technology.

This chapter is organized as follows. Coupled-line couplers are discussed in section 3.1. The performance of QHR stages is theoretically analyzed in section 3.2. Circuit design and measurement results are presented in section 3.3 and section 3.4, respectively, where the accuracy of I/Q signals is benchmarked based on image rejection ratio (IRR). Finally, section 3.5 concludes this work.

3.1 Quadrature Signal Generation Based on Coupled-Line Couplers

A coupled-line coupler (CLC) is a four-port network typically used for power dividing and combining. It can be designed to divide the input power evenly between two outputs, with a 90° phase shift. The operation of a 90° CLC with a coupling factor of C is described by the following scattering-parameter (S-parameter) matrix [71]

$$S = \begin{bmatrix} 0 & -j\beta & \alpha & 0 \\ -j\beta & 0 & 0 & \alpha \\ \alpha & 0 & 0 & -j\beta \\ 0 & \alpha & -j\beta & 0 \end{bmatrix}, \tag{3.1}$$

in which $\beta = \sqrt{1 - C^2}$ and $\alpha = C$. Figure 3.1 presents the schematic and the signal flow graph (SFG) of a coupler, terminated in Γ_S at the input port, in Γ_L at the coupled and the through ports, and in Γ_0 at the isolation port. Based on the SFG of Figure 3.1(b), the input reflection coefficient of a CLC is given by

$$\Gamma_{in} = (\alpha^2 - \beta^2)\Gamma_L. \tag{3.2}$$

As a result, if the coupler is designed to provide matched amplitudes at center frequency ($\alpha = \beta$), the input port would be matched ($\Gamma_{in} = 0$) regardless of the Γ_L value. It can be shown that the loading reflection coefficient (Γ_L) does not introduce any phase/amplitude mismatches as long as the output ports are terminated in identical impedances. In an ideal coupler, no power is coupled to the isolation port. In case of any mismatch, if any signal couples to the isolation port, no power will be reflected, since ideally this port is terminated in $\Gamma_0 = 0$. So, port 4 is not included in future analyses.

To generate differential quadrature signals, a differential input signal is required, and if these inputs have any amplitude and phase errors, they directly appear at the output, as shown in Figure 3.2. This drastically degrades the accuracy of the differential quadrature signals. To address this problem, we introduce a passive low-loss broadband network (i.e., QHR) that enhances the phase/amplitude matching of quadrature signals. QHR stages are studied in the next section.

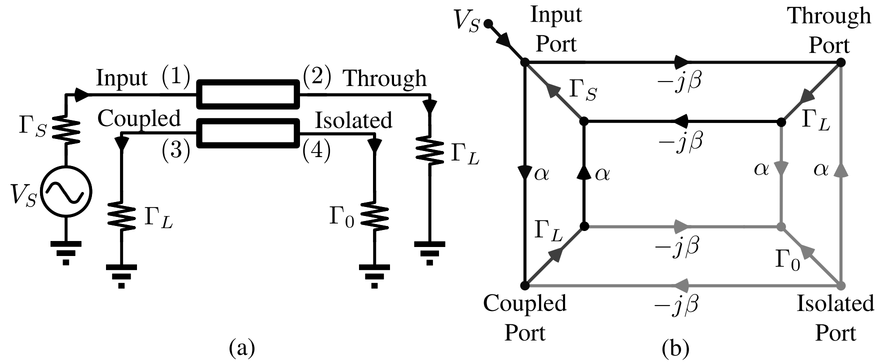


Figure 3.1: (a) A coupled-line coupler and terminations. (b) A simplified SFG of the coupler when $S_{ii} = 0$ for $i = 1, 2, 3,$ and 4 (© 2018 IEEE).

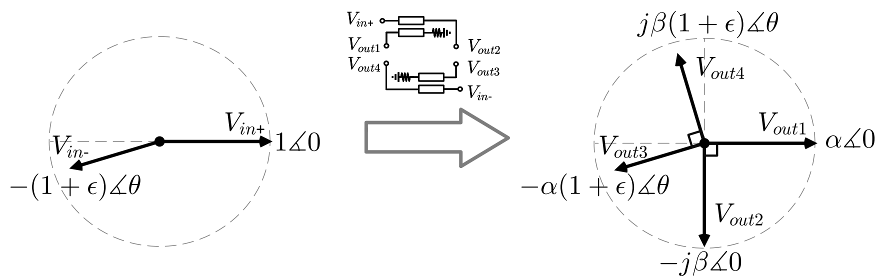


Figure 3.2: The response of a CLC to an unbalanced differential signal. θ and ϵ are the phase and the amplitude mismatches, respectively (© 2018 IEEE).

3.2 Quadrature Hybrid Ring

To enhance the phase/amplitude matching of quadrature signals, we employ a passive network which is placed after the quadrature signal generation block (i.e., QH). This network consists of four quadrature hybrids arranged in a ring and is called a quadrature hybrid ring (QHR). Figure 3.3 shows the schematic of a QHR, which has four inputs and four outputs. In this network, the I/Q inputs are combined with proper phase and ratio to produce more balanced signals. In the following, the quality of quadrature signals is evaluated based on IRR given below[72]

$$IRR = \frac{(1+\epsilon)^2 - 2(1+\epsilon)\cos\theta + 1}{(1+\epsilon)^2 + 2(1+\epsilon)\cos\theta + 1} \tag{3.3}$$

where θ and ϵ are the phase and the amplitude mismatches, respectively.

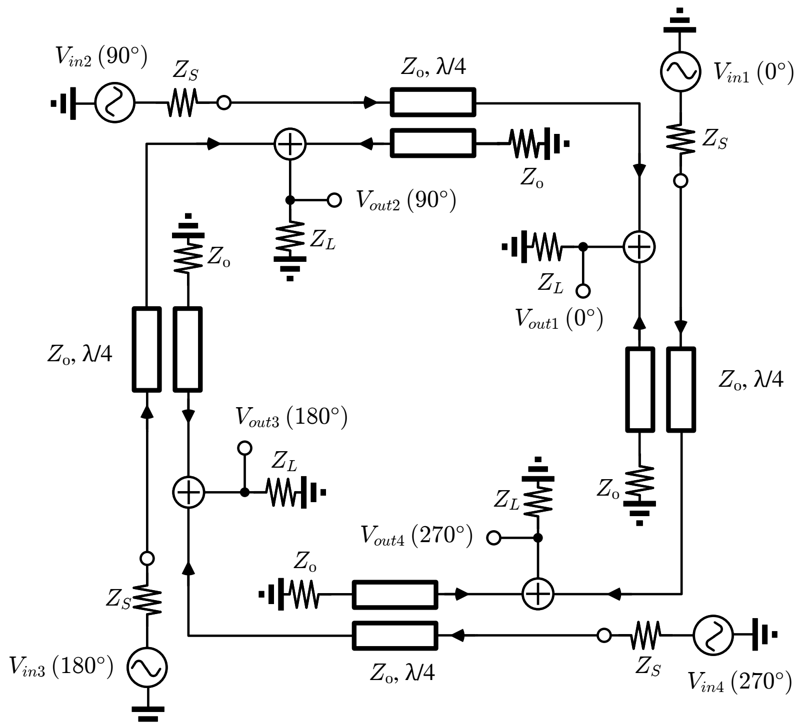


Figure 3.3: The schematic of a quadrature hybrid ring (© 2018 IEEE).

Assume two quadrature hybrids with a coupling factor of C_1, followed by a QHR with a coupling factor of C_2, are utilized to generate enhanced I/Q signals. Figure 3.4 depicts mathematically-calculated IRRs for various combinations of C_1 and C_2 values. As C_1 and C_2 increase up to $1/\sqrt{2}$, the amplitude error becomes smaller and the IRR is improved. The cases with $C_2 = 0$ are similar to when no enhancement stage (i.e., QHR) is employed. Comparing the cases with $C_2 = 0$ to those with $C_2 = C_1$, the value of the IRR is squared (doubled in dB) for $C_2 = C_1$. As a result, a QHR stage significantly enhances the matching of I/Q signals. Unlike RC-CR polyphase networks, CLC and QHR networks do not use resistors in the signal path. This enables low-loss cascading of QHR stages for balanced I/Q signal generation in both RF and LO paths.

3.2.1 Signal Flow Graph of a QHR

To investigate the performance of a QHR, the transfer function of this network is calculated using Mason's gain rule (MGR) [73]. To this end, the SFG of the QHR is generated

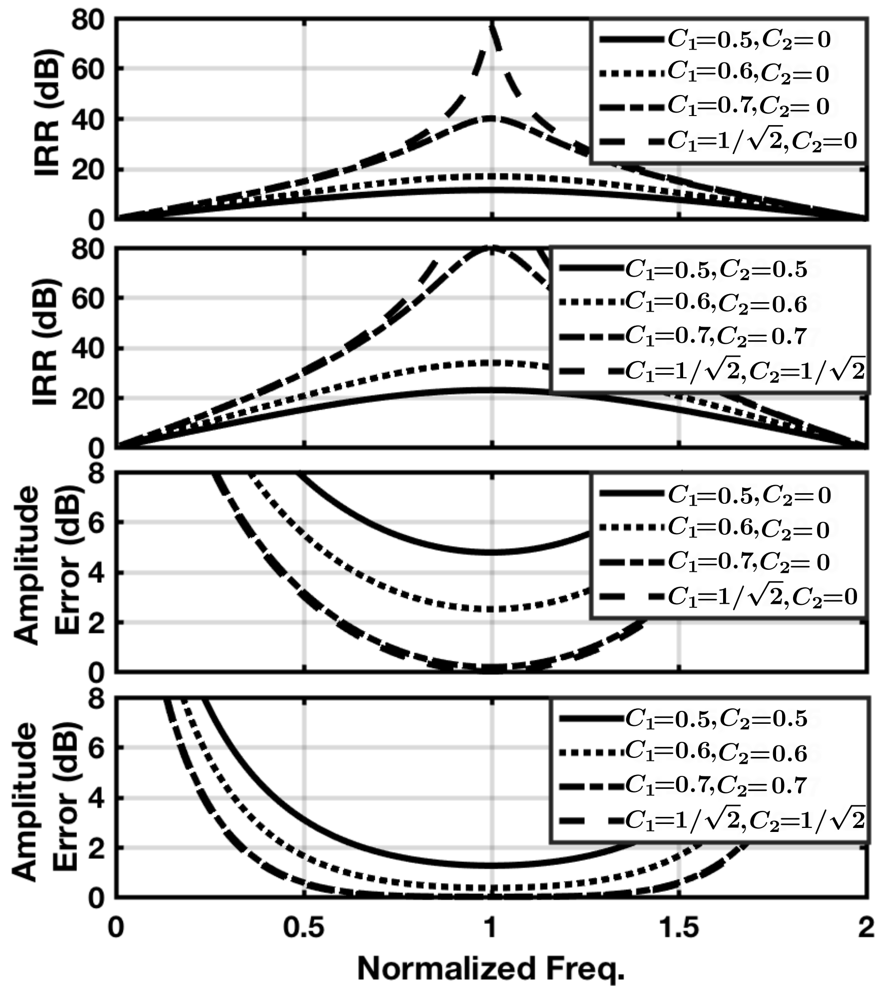


Figure 3.4: The amplitude error and the IRR of a two-stage I/Q signal generator when two quadrature hybrids with coupling factors of C_1 in the first stage are cascaded by a QHR with a coupling factor of C_2 in the second stage (© 2018 IEEE).

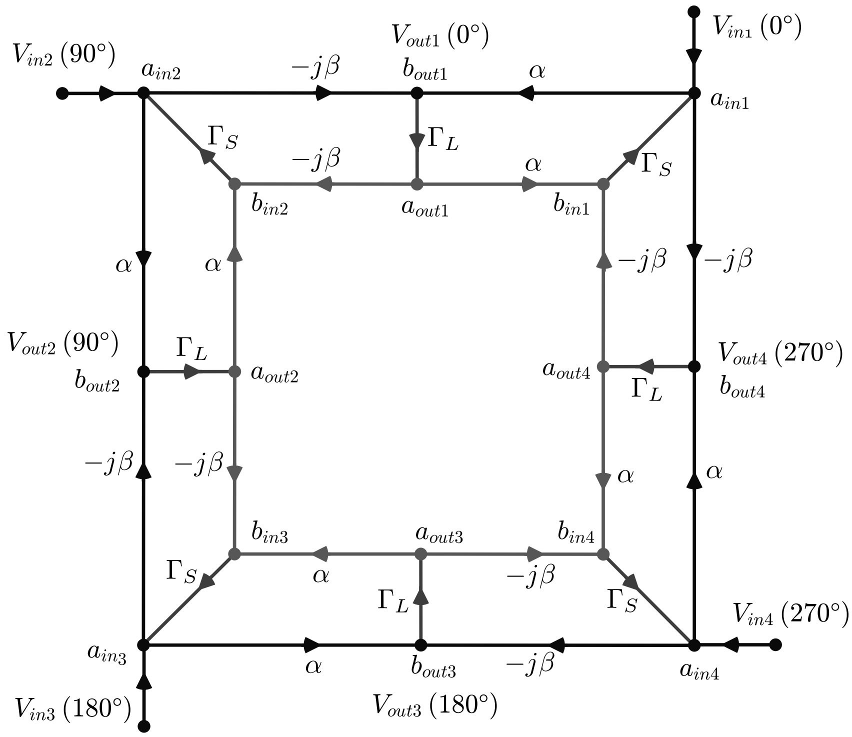


Figure 3.5: The signal flow graph of the quadrature hybrid ring (© 2018 IEEE).

as shown in Figure 3.5. In this SFG, Γ_S models the reflection coefficient of the source impedance (Z_S), and Γ_L models the reflection coefficient of the equivalent load impedance of each coupler. Using the SFG, MGR is used to derive the transfer functions from node V_{in1} to output nodes, as follows

$$\begin{aligned}\frac{V_{out1}}{V_{in1}} = \frac{1}{\Delta_p}\Big[\alpha - \Gamma_S\Gamma_L(3\alpha^3 - 2\alpha\beta^2) + \\ \Gamma_S^2\Gamma_L^2(\alpha\beta^4 + 3\alpha^5 - 2\alpha^3\beta^2) - \Gamma_S^3\Gamma_L^3(\alpha^7 - \alpha^3\beta^4)\Big],\end{aligned} \tag{3.4}$$

$$\begin{aligned}\frac{V_{out2}}{V_{in1}} = \frac{1}{\Delta_p}\Big[-j\Gamma_S\Gamma_L(\beta\alpha^2) + \\ \Gamma_S^2\Gamma_L^2(2j\beta\alpha^4 - j\beta\alpha^6) + \Gamma_S^3\Gamma_L^3(j\beta^5\alpha^2)\Big],\end{aligned} \tag{3.5}$$

$$\begin{aligned}\frac{V_{out3}}{V_{in1}} = \frac{1}{\Delta_p}\Big[-\Gamma_S\Gamma_L(\alpha\beta^2) + \\ \Gamma_S^2\Gamma_L^2(-2\alpha\beta^4 - \alpha\beta^6) + \Gamma_S^3\Gamma_L^3(\alpha^5\beta^2)\Big],\end{aligned} \tag{3.6}$$

and

$$\frac{V_{out4}}{V_{in1}} = \frac{-1}{\Delta_p}\Big[j\beta + \Gamma_S\Gamma_L(3j\beta^3 - 2j\beta\alpha^2) + \Gamma_S^2\Gamma_L^2\times$$
$$(j\beta\alpha^4 + 3j\beta^5 - 2j\beta^3\alpha^2) + \Gamma_S^3\Gamma_L^3(j\beta^7 - j\beta^3\alpha^4)\Big], \tag{3.7}$$

where the graph determinant, Δ_p, is defined as

$$\begin{aligned}\Delta_p = 1 &- \Gamma_S\Gamma_L(4\alpha^2 - 4\beta^2) \\ &+ \Gamma_S^2\Gamma_L^2(6\alpha^4 + 6\beta^4 - 8\alpha^2\beta^2) \\ &- \Gamma_S^3\Gamma_L^3(4\alpha^6 - 4\beta^6 - 4\alpha^4\beta^2 + 4\alpha^2\beta^4) \\ &+ \Gamma_S^4\Gamma_L^4(\alpha^8 + \beta^8).\end{aligned} \tag{3.8}$$

Since a QHR is a symmetric network, transfer function from all inputs to all outputs can be derived from (Equation 3.4)-(Equation 3.8). The superposition principle is applied to calculate the net response of the system. To study the sensitivity of a QHR to Γ_S and Γ_L, one of them is swept over Smith chart while the other is set to 0 and 0.1. Figure 3.6(a) indicates that the transfer functions are constant when one of the Γ_S and Γ_L is set to zero, and Figure 3.6(b) shows that the transfer functions do not change significantly ($< 2\%$) when $|\Gamma_S|$ or $|\Gamma_S|$ is less than 0.1.

To analyze the basic operation of a QHR, (Equation 3.4)–(Equation 3.7) are simplified as following by assuming $|\Gamma_S|$ or $|\Gamma_L| = 0$:

$$\begin{aligned}V_{out1} &= \alpha V_{in1} - j\beta V_{in2} \\ V_{out2} &= \alpha V_{in2} - j\beta V_{in3} \\ V_{out3} &= \alpha V_{in3} - j\beta V_{in4} \\ V_{out4} &= \alpha V_{in4} - j\beta V_{in1}.\end{aligned} \tag{3.9}$$

Thus, (Equation 3.9) implies that the output signal at port n is a combination of the input signals at ports n and $n+1$. In a properly designed QHR ($\alpha = \beta$ at the desired frequency),

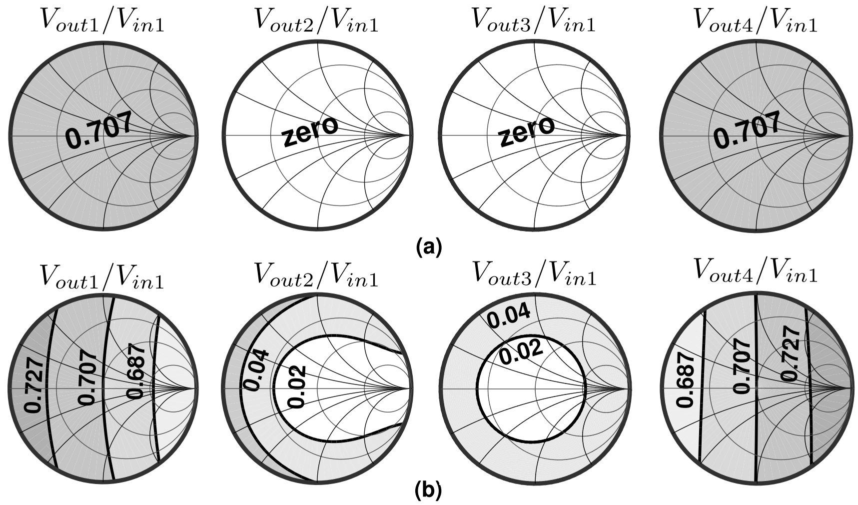


Figure 3.6: The transfer functions from one of the input ports to output ports for (a) $\Gamma_S = 0$ and (b) $\Gamma_S = 0.1$ when Γ_L is swept over Smith chart. Γ_S and Γ_L are interchangeable in the transfer function (© 2018 IEEE).

the input signals are combined to minimize quadrature errors. This topic is explained in the next subsection.

3.2.2 Response to an Arbitrary Signal Set

The response of a QHR to an arbitrary input set is investigated to demonstrate how the phase and amplitude errors are suppressed. According to the theory of symmetric components, any unbalanced system of N vectors can be represented as the sum of N symmetric vector systems [74]. As an example, Figure 3.7 presents four arbitrary sine-wave inputs (V_{in1}, V_{in2}, V_{in3}, and V_{in4}) decomposed into four symmetric sequences: quadrature counterclockwise, quadrature clockwise, collinear differential, and collinear in-phase [61]. Thus, we assume that

$$
\begin{aligned}
V_{in1} &= ja - jb - c + d \\
V_{in2} &= -a - b + c + d \\
V_{in3} &= -ja + jb - c + d \\
V_{in4} &= a + b + c + d
\end{aligned}
\tag{3.10}
$$

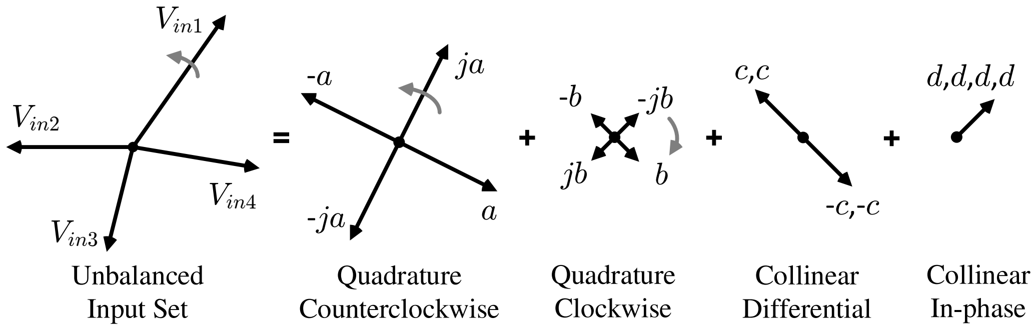


Figure 3.7: A set of four arbitrary inputs decomposed into basis functions (© 2018 IEEE).

where a, b, c, and d represent the basis vectors of symmetric sequences. The values of these vectors are determined by inverting the matrix of coefficients:

$$
\begin{aligned}
a &= \frac{1}{4}(-jV_{in1} - V_{in2} + jV_{in3} + V_{in4}) \\
b &= \frac{1}{4}(jV_{in1} - V_{in2} - jV_{in3} + V_{in4}) \\
c &= \frac{1}{4}(-V_{in1} + V_{in2} - V_{in3} + V_{in4}) \\
d &= \frac{1}{4}(V_{in1} + V_{in2} + V_{in3} + V_{in4}).
\end{aligned}
\tag{3.11}
$$

The analysis of a QHR network is simplified by decomposing the arbitrary set of inputs into symmetric sequences. In fact, QHR outputs can be calculated separately for each symmetric sequence. In the following, the components of the symmetric sequences are extracted from (Equation 3.10) and substituted into (Equation 3.9) to calculate the outputs.

Quadrature Counterclockwise (CCW)

In this case, the output n is a constructive addition of the input signals at ports n and $n+1$. As derived in the following, quadrature CCW inputs pass through a QHR without any loss.

$$\begin{aligned} V_{out1}|_{\text{CCW}} &= 0.5(+ja) - j0.5(-a) = ja \\ V_{out2}|_{\text{CCW}} &= 0.5(-a) - j0.5(-ja) = -a \\ V_{out3}|_{\text{CCW}} &= 0.5(-ja) - j0.5(+a) = -ja \\ V_{out4}|_{\text{CCW}} &= 0.5(+a) - j0.5(+ja) = a. \end{aligned} \tag{3.12}$$

The quadrature CCW component of the output signals is

$$a_{out} = \frac{1}{4}(-jV_{out1} - V_{out2} + jV_{out3} + V_{out4})|_{\text{CCW}} = a. \tag{3.13}$$

Quadrature Clockwise (CW)

In this case, the output n is a destructive addition of the input signals at ports n and $n+1$. It is shown in the following that quadrature CW inputs cancel each other completely.

$$\begin{aligned} V_{out1}|_{\text{CW}} &= 0.5(-jb) - j0.5(-b) = 0 \\ V_{out2}|_{\text{CW}} &= 0.5(-b) - j0.5(+jb) = 0 \\ V_{out3}|_{\text{CW}} &= 0.5(+jb) - j0.5(+b) = 0 \\ V_{out4}|_{\text{CW}} &= 0.5(+b) - j0.5(-jb) = 0. \end{aligned} \tag{3.14}$$

Thus, the quadrature CW component of the output signals is

$$b_{out} = \frac{1}{4}(jV_{out1} - V_{out2} - jV_{out3} + V_{out4})|_{\text{CW}} = 0. \tag{3.15}$$

Collinear Differential

If the primary differential inputs contain phase/amplitude errors (e.g., generated by a balun mismatch), the collinear differential component will have a non-zero value. This component is attenuated in a QHR, as shown in the following.

$$\begin{aligned}
V_{out1}|_{\text{Col. Diff.}} &= 0.5(c) - j0.5(-c) = 0.5(+c + jc) \\
V_{out2}|_{\text{Col. Diff.}} &= 0.5(-c) - j0.5(c) = 0.5(-c - jc) \\
V_{out3}|_{\text{Col. Diff.}} &= 0.5(c) - j0.5(-c) = 0.5(+c + jc) \\
V_{out4}|_{\text{Col. Diff.}} &= 0.5(-c) - j0.5(c) = 0.5(-c - jc).
\end{aligned} \tag{3.16}$$

The collinear differential component of the output signals is given by

$$c_{out} = \frac{1}{4}(-V_{out1} + V_{out2} - V_{out3} + V_{out4})|_{\text{Diff. Col.}} = \frac{c\angle 225^\circ}{\sqrt{2}} \tag{3.17}$$

where a QHR network attenuates the amplitude of this component by $1/\sqrt{2}$, enhancing the phase/amplitude matching.

Collinear In-Phase

This case is similar to the previous one (i.e., collinear differential). Therefore, the collinear in-phase component is attenuated in a QHR, as shown below.

$$\begin{aligned}
V_{out1}|_{\text{Col. In-Ph.}} &= 0.5(d) - j0.5(d) = 0.5(d - jd) \\
V_{out2}|_{\text{Col. In-Ph.}} &= 0.5(d) - j0.5(d) = 0.5(d - jd) \\
V_{out3}|_{\text{Col. In-Ph.}} &= 0.5(d) - j0.5(d) = 0.5(d - jd) \\
V_{out4}|_{\text{Col. In-Ph.}} &= 0.5(d) - j0.5(d) = 0.5(d - jd)
\end{aligned} \tag{3.18}$$

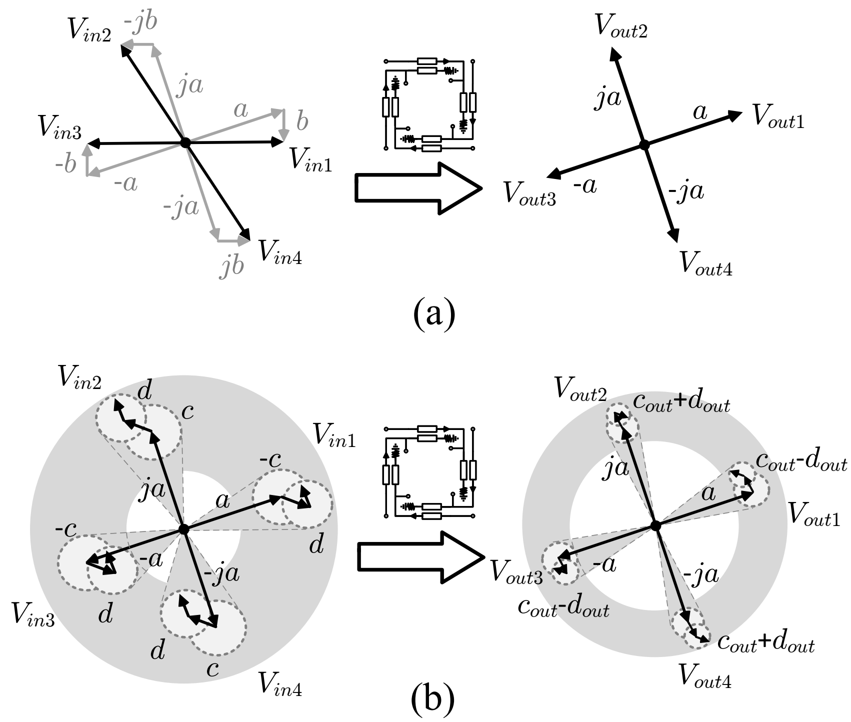


Figure 3.8: (a) A set of four signals with $c = d = 0$ are applied to a QHR, which passes the quadrature CCW component but rejects the quadrature CW component. (b) A set of four signals with $c \neq 0$ and $d \neq 0$ are applied to a QHR, which attenuates collinear components by $1/\sqrt{2}$ (© 2018 IEEE).

The collinear in-phase component of the output signals is

$$d_{out} = \frac{1}{4}(V_{out1} + V_{out2} + V_{out3} + V_{out4})|_{\text{Col.}} = \frac{d\angle 315^\circ}{\sqrt{2}}. \tag{3.19}$$

A QHR network attenuates the amplitude of this component by $1/\sqrt{2}$, improving the phase and amplitude matching.

In summary, a QHR passes the main quadrature component (basis vector a), rejects the reverse quadrature component (basis vector b), and attenuates the amplitude of collinear errors (basis vectors c and d). Figure 3.8 presents two sets of unbalanced inputs with associated QHR outputs wherein the complete rejection of CW sequence as well as the attenuation of collinear sequences are illustrated. Although a QHR cannot reject collinear components completely, the quality and bandwidth of I/Q signals are improved significantly by cascading low-loss QHR stages. Figure 3.9(a) depicts the calculated IRR of a

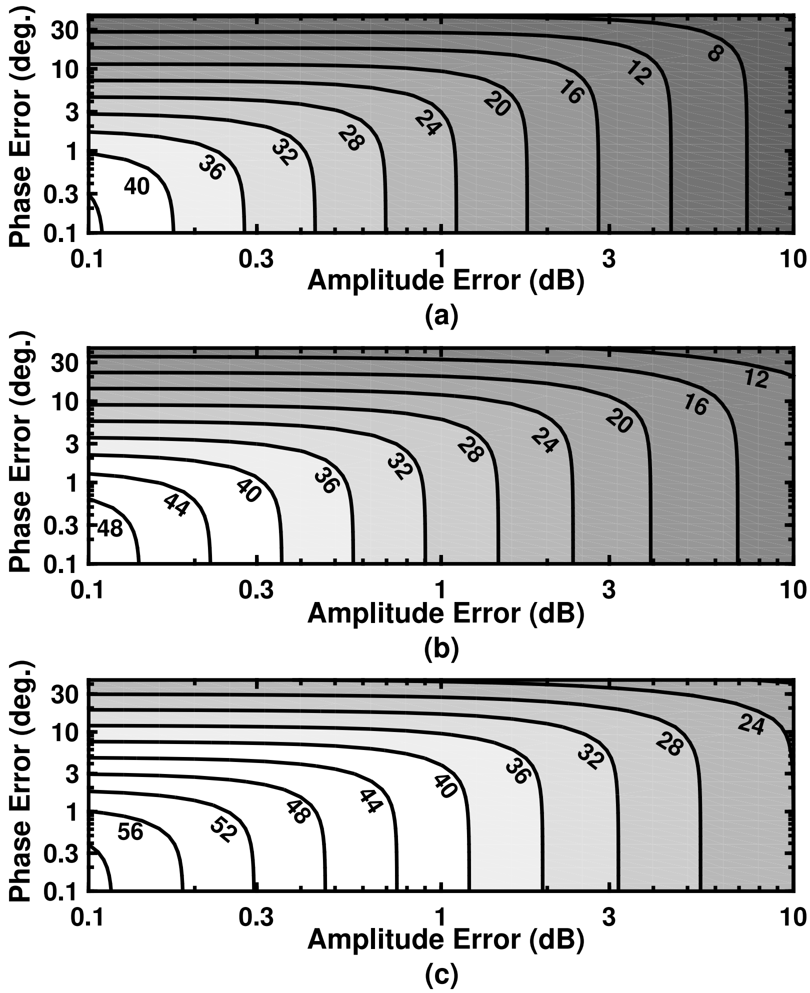


Figure 3.9: The IRR of (a) a CLC, (b) a CLC followed by a QHR stage, and (c) a CLC followed by two QHR stages vs. the phase/amplitude mismatch of input signals. The coupling factor of couplers are $1/\sqrt{2}$ (© 2018 IEEE).

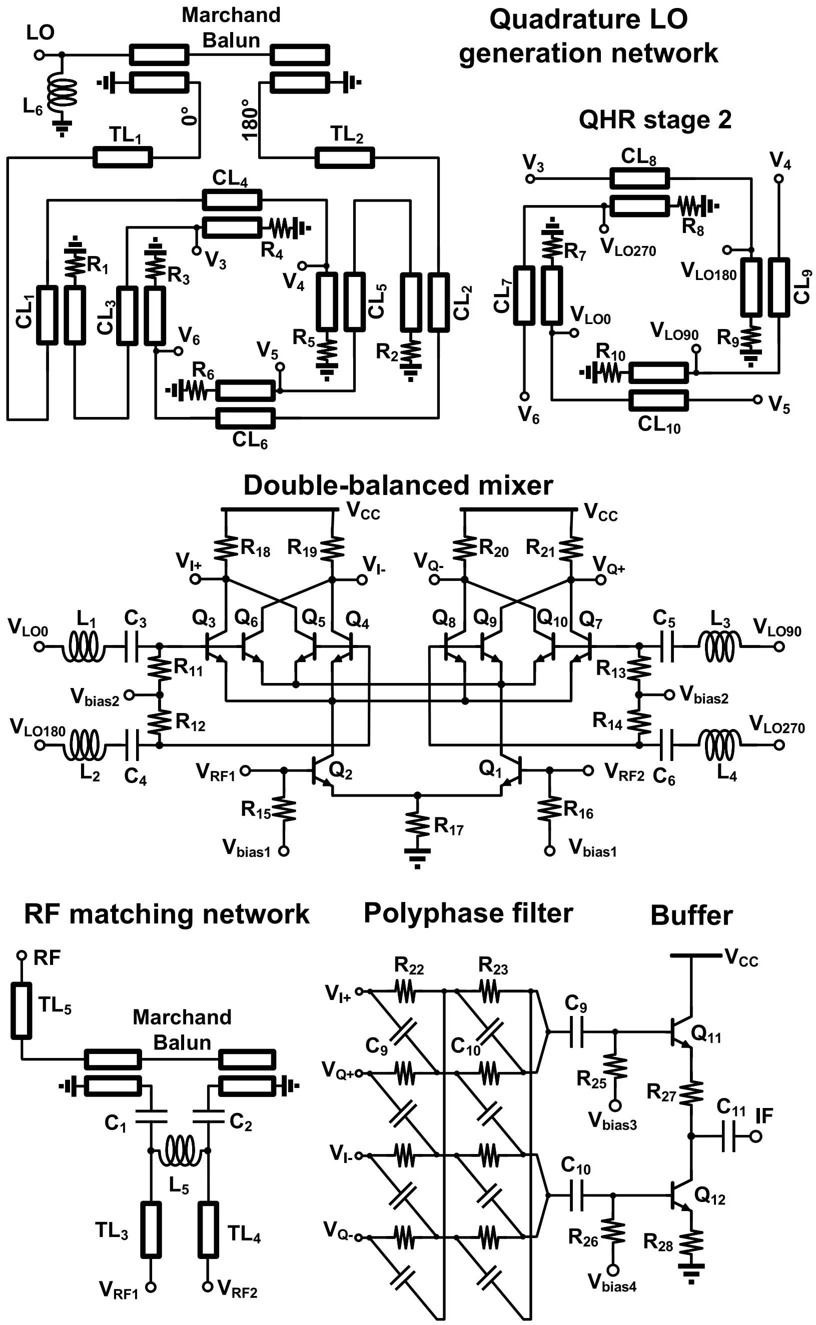
CLC versus the phase and amplitude errors of input differential signals. Similar plots are also presented when one [Figure 3.9(b)] and two [Figure 3.9(c)] QHR stages are cascaded with the CLC. Calculated results suggest great improvements in the quality of the quadrature signals. According to Figure 3.9, each QHR stage with a coupling factor (CF) of $1/\sqrt{2}$ improves the IRR by about 8 dB. Several QHR stages can be cascaded to produce more balanced I/Q signals; however, at the cost of mismatch between them ($\Gamma_S \neq 0$).

3.3 Circuit Design and Implementation

Two prototype image-reject mixers are designed to down-convert mm-wave RF signals to a 1-GHz IF frequency. In these mixers, QHR stages are employed in the local oscillator (LO) generation network. The accuracy of the LO signals is evaluated based on the IRR of mixers. Both mixers are fabricated in GlobalFoundries 8XP platform, which is a 0.13 μm SiGe BiCMOS process that provides high-speed SiGe HBTs with a peak f_T/f_{max} of 250/330 GHz, high-density MIM capacitors, low-parasitic TaN resistors, five copper layers (M1-M5), and two thick aluminum layers (M6 and M7). The present back-end-of-line (BEOL) layers are similar to the layers referenced in [75], where the thickness of M6 and M7 are reported to be 1.25 and 4 μm, respectively.

3.3.1 Image-Reject Mixer-1

Figure 3.10 shows the schematic of the IR mixer-1, which comprises a double-balanced Gilbert cell, a quadrature LO generation network, an IF polyphase filter, and a buffer stage. The circuit is designed to convert V-band RF signals to a 1 GHz IF frequency. Two Marchand baluns are employed at the RF and LO ports to generate differential signals from single-ended inputs. The differential LO signals are split into quadrature signals with two quadrature hybrids, passed through QHR stages to enhance the phase/amplitude matching, and connected to switching transistors. Series inductors ($L_1 - L_4$) are used at the input terminals of switching transistors to resonate out the input capacitance of Q_3–Q_{10}. A passive network is employed to match the transistors of g_m stage ($Q_1 - Q_2$) to the RF Marchand balun. After down-conversion, the IF signal is passed through a two-stage RC-CR polyphase network to reject the image signal. A buffer stage combines the differential IF signals to generate a single-ended signal at the output. The backbone of the quadrature LO generation network is a quadrature hybrid. This hybrid provides the minimum amplitude error and the maximum IRR at the center frequency when its coupling factor is $1/\sqrt{2}$.



$R_{1\text{-}10}$: 48 Ω	$R_{25\text{-}26}$: 1.7 kΩ	$C_{9\text{-}10}$: 1 pF	$TL_{1\text{-}2}$: 57 Ω, 52°
$R_{11\text{-}14}$: 1.5 kΩ	R_{27}: 25 Ω	C_{11}: 10 pF	$TL_{3\text{-}4}$: 35 Ω, 80°
$R_{15\text{-}16}$: 300 Ω	R_{28}: 18 Ω	$L_{1\text{-}4}$: 0.1 nH	TL_5: 60 Ω, 38°
R_{17}: 14 Ω	$C_{1\text{-}2}$: 0.5 pF	L_5: 0.18 nH	$CL_{1\text{-}10}$: 48 Ω, 90°,0.71
$R_{18\text{-}21}$: 0.4 kΩ	$C_{3\text{-}6}$: 1.8 pF	L_6: 0.17 nH	$Q_{01\text{-}02}$: 6 μm/0.12 μm
R_{22}: 0.68 kΩ	$C_{7\text{-}8}$: 0.2 pF		$Q_{03\text{-}10}$: 3 μm/0.12 μm
R_{23}: 0.78 kΩ			$Q_{11\text{-}12}$: 3 μm/0.12 μm

Figure 3.10: The schematic and component values of double-balanced quadrature down-converter (© 2018 IEEE).

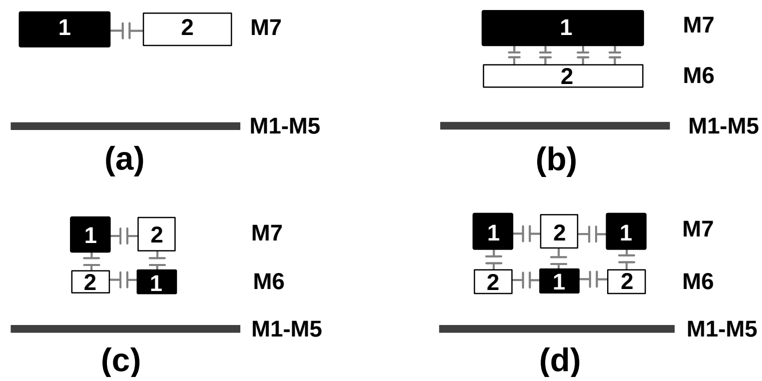


Figure 3.11: (a) Edge-coupled, (b) broadside-coupled, and (c-d) Lange couplers (© 2018 IEEE).

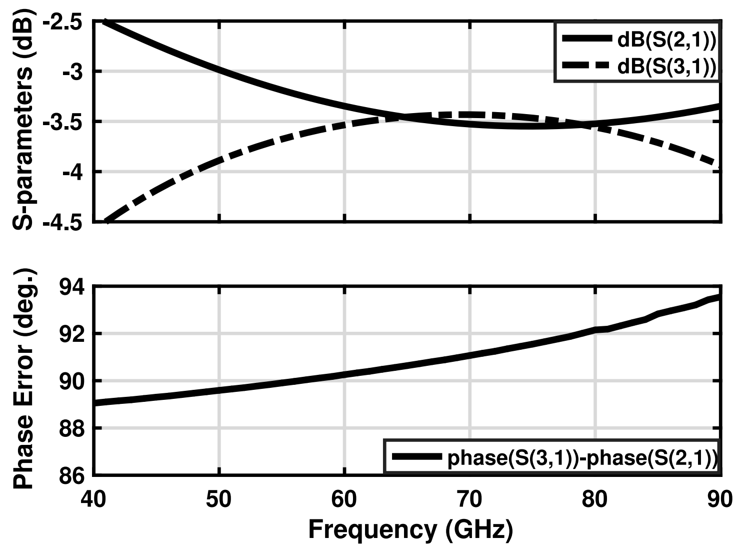


Figure 3.12: The S-parameters of the EM-simulated quadrature hybrid (© 2018 IEEE).

To realize such a hybrid with a characteristic impedance (Z_0) of 50 Ω in the 8XP SiGe platform, several structures, including edge-coupled, broadside-coupled, and Lange coupler, are investigated. Figure 3.11 shows the cross-section of these structures implemented on the top two metal layers (M6-M7). The spacing between coupler conductors is minimized to achieve the highest coupling factor. Electromagnetic (EM) simulations in Sonnet indicate that an edge-coupled coupler features a Z_0 of 50 Ω with a low CF of 0.46, while the broadside-coupled coupler achieves a higher CF of 0.66, with unequal characteristic impedances of 41 Ω and 50 Ω for the coupled lines. On the other hand, the Lange-coupler shown in Figure 3.11(c) achieves a CF of 0.71 with a Z_0 of 48 Ω when the ground plane is

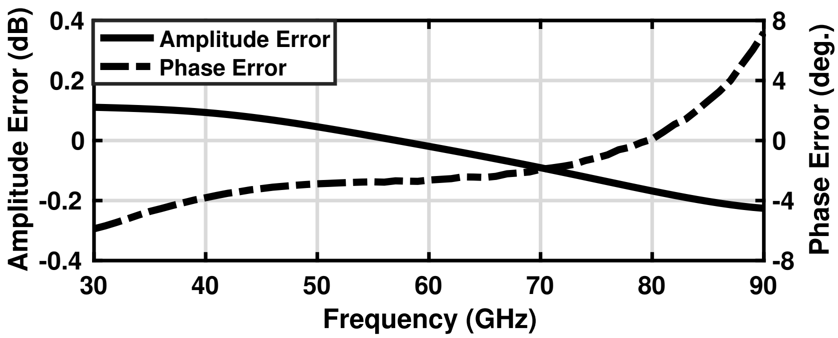


Figure 3.13: The EM simulated phase/amplitude errors of the LO Marchand balun (© 2018 IEEE).

realized with M1. This Lange-coupler is EM simulated, and the resulting S-parameters are shown in Figure 3.12. The length of the Lange-coupler is 550 μm, and it features perfect amplitude matching at 64 and 79 GHz. The power loss of the Lange-coupler is 0.5 dB, and the phase difference between the coupled and the through ports at the center frequency is 91°. This 1° phase error is due to the extra capacitance of the connections at the ends of the coupler. A V-band Marchand balun is also designed to provide differential LO signals. Simulation results of this balun are shown in Figure 3.13 where the amplitude and phase errors are less than ± 0.2 dB and 3° across the band, respectively.

To ensure balanced generation of I/Q signals, a symmetrical layout should be realized for high-frequency signals (e.g., RF and LO paths). The floor plan of mixer-1 is shown in Figure 3.14(a) where the quadrature signal generation network is placed on one side of the core. A compact layout is designed for the IF polyphase filter. Although this compact layout simplifies the IF connections, it causes a length mismatch of 240 μm in the polyphase filter [Figure 3.14(b)], resulting in an effective mismatch of 0.6° at IF frequency. The polyphase filter is EM simulated and ideal quadrature signals are applied to the switching transistors to investigate the effects of the length mismatch. Figure 3.15 presents the simulated IRR of the IF filter versus IF frequency, where maximum IRR is achieved at 1 GHz. It should be noted that the maximum IRR is limited by the length mismatch in the IF polyphase filter. To ensure that the LO network does not reduce the IRR, two QHR stages

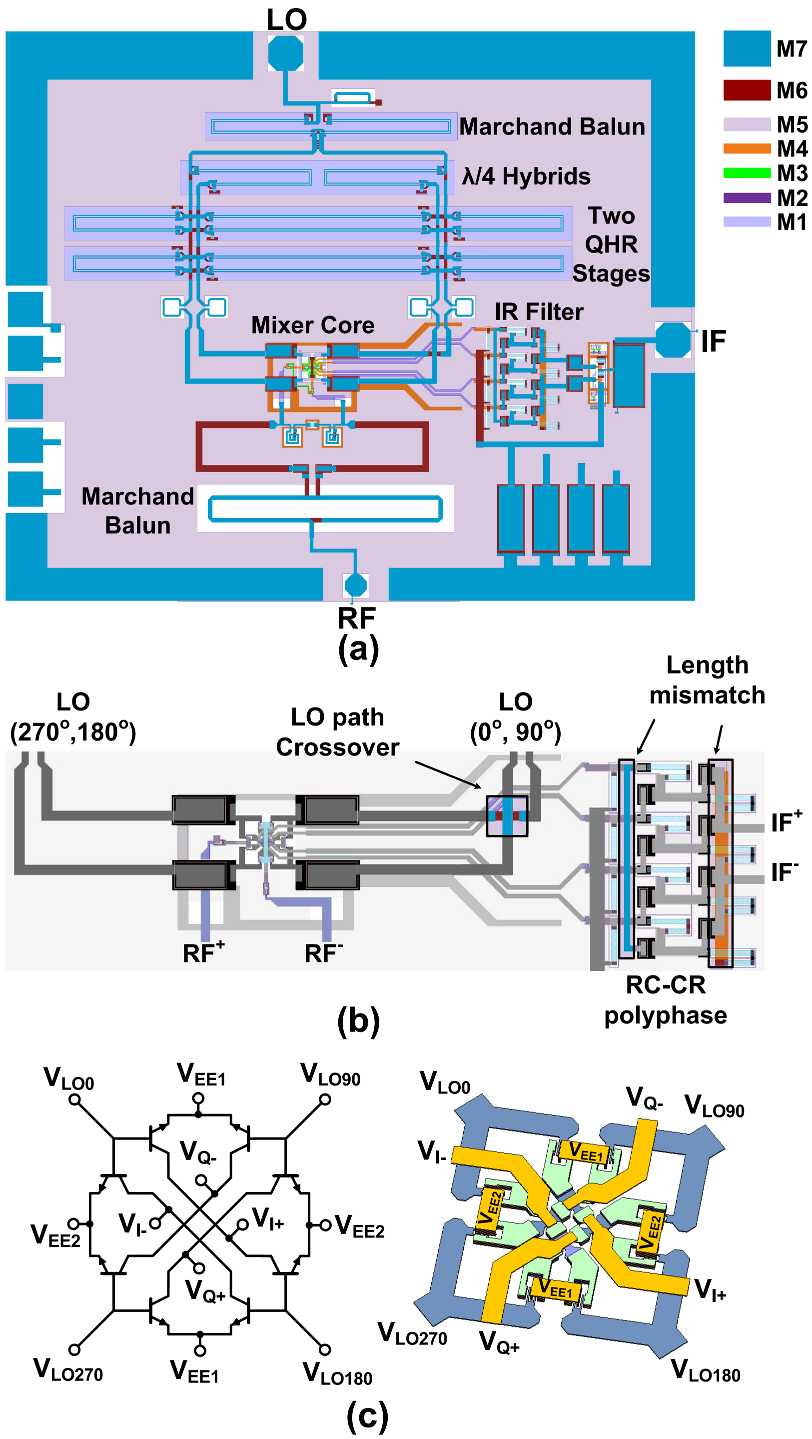


Figure 3.14: (a) The floor plan of the image-reject mixer-1, (b) the IF polyphase filter and its connections, and (c) the schematic and the symmetric layout of the switching transistors (© 2018 IEEE).

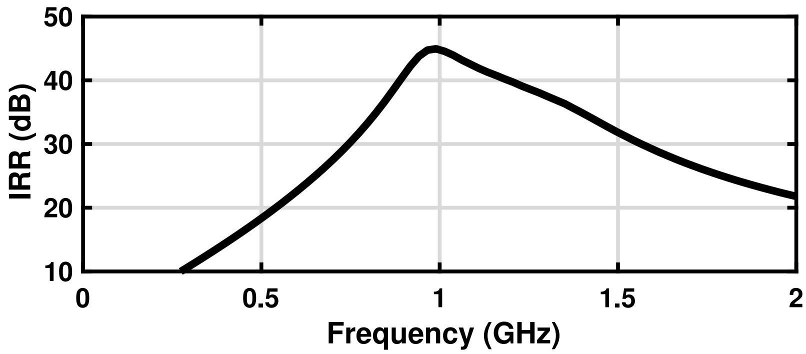


Figure 3.15: The IRR of the IF filter versus frequency when ideal quadrature LO signals are applied (© 2018 IEEE).

are employed, and a common centroid layout is drawn for the mixer core. Figure 3.14(c) illustrates the schematic and the symmetric layout of switching transistors ($Q_3 - Q_{10}$). These transistors are connected to the IF polyphase filter via inverted transmission lines (i.e., M1 below M5 ground plane). The overlap capacitance at the core of the mixer, between LO and IF connections, is about 1 fF, and it yields a high impedance at the frequency of operation.

3.3.2 Image-Reject Mixer-2

The IR mixer-1 has an LO path crossover in the layout [Figure 3.14(b)], which requires careful simulations using multiple design iterations. Therefore, another floor plan is suggested to avoid high-frequency signal crossovers [Figure 3.16]. In the new floor plan, the quadrature hybrids of the QHR stage form a square where the mixer core is placed at the center, and RF and IF pads are placed on the left and right sides of the chip, respectively. The LO-generation network has a symmetric common-centroid layout, and can potentially offer a high IRR. To avoid LO and RF/IF interferences, a higher metal layer (i.e., M5) can be chosen as the ground plane of the Lange-couplers so that RF/IF signals can be routed under it.

The Lange-coupler of Figure 3.11(c) is simulated with different ground planes, and the resulting CF and Z_0 are shown in Figure 3.17. The coupling factor and the characteristic impedance will be reduced if a higher metal layer is selected as the ground plane. In the

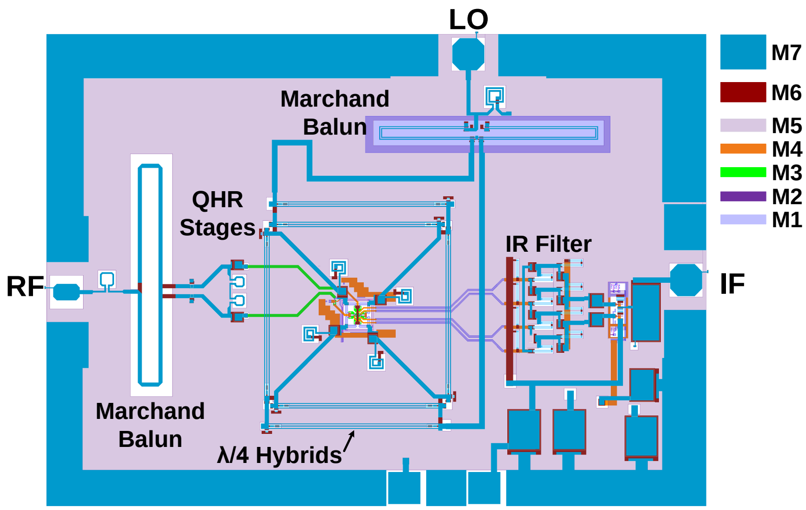


Figure 3.16: The floor plan of the IR mixer-2 (© 2018 IEEE).

present work, M5 is chosen as the ground plane, and the Lange-coupler geometry is reconfigured to Figure 3.11(d) to increase the coupling factor ($CF = 0.67$). The M5 ground plane gives us enough space to route RF and IF signals via inverted transmission lines. Nevertheless, this is realized at the expense of further reduction in value of Z_0 (i.e., Z_0 =34 Ω). It should be noted that the characteristic impedance of this Lange-coupler cannot be as high as 50 Ω, since the value of the effective capacitance to ground is higher. The length of Lange-couplers used in mixer-2 are 400 μm as they are tuned to a higher frequency compared to mixer-1. Since mixer-2 employs only one QHR stage with a lower coupling factor compared to that of mixer-1, the peak IRR of mixer-2 is expected to be lower. In addition, the simulated input third-order intercept-point (IIP3) and the single-sideband noise figure of mixers are -3 dBm and 12.5 dB at the center frequency, respectively.

3.3.3 IRR Sensitivity to Variations and Mismatches

The IRR sensitivity of the demonstrated mixers to process corner, voltage, temperature (PVT), and metal thickness variations are evaluated, and Monte-Carlo (MC) simulations are performed to investigate the effects of device mismatch. Please note that although the quadrature LO generation network and the IF polyphase filter both contribute to the IRR,

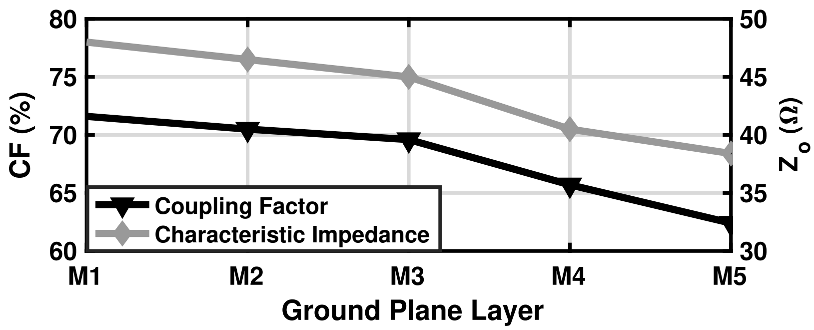


Figure 3.17: The EM simulated coupling factor and characteristics impedance of the Lange-coupler vs ground plane layer (© 2018 IEEE).

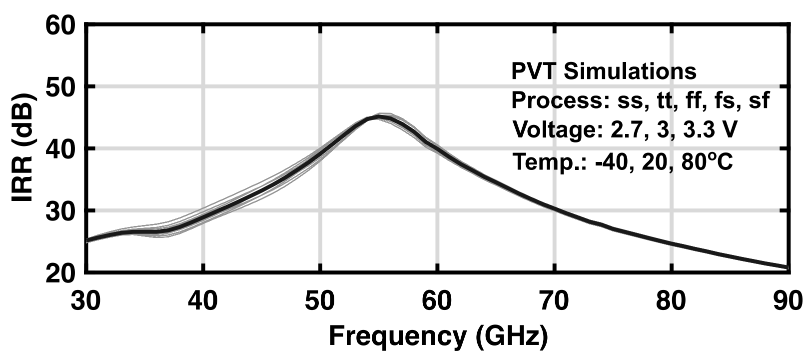


Figure 3.18: The IRR sensitivity to PVT variations in mixer-1 (© 2018 IEEE).

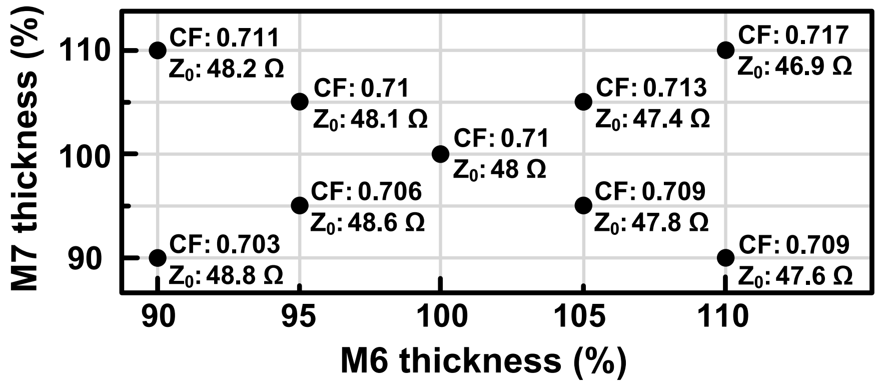


Figure 3.19: The EM simulated CF and Z_o of the Lange-coupler versus metal thickness variations. $\pm 10\,\%$ variations in the thickness of coupler conductors yield to only $1\,\%$ and $2\,\%$ variation in CF and Z_0, respectively (© 2018 IEEE).

the main goal is to investigate the sensitivity of the mm-wave quadrature LO generation network. Therefore, the component values of IF polyphase filter are held constant in these simulations.

Figure 3.18 presents the simulated IRR of mixer-1 across different process corners, with $10\,\%$ variations in supply voltages, and over a temperature range of -40 to $80\,°$C. It can be seen that IRR is robust to PVT variations. Metal thickness variations are also investigated by EM simulating the Lange-couplers with $\pm\,10\,\%$ thickness variations, while the line width and the spacing between coupler conductors are fixed. These thickness variations yield only $1\,\%$ and $2\,\%$ variations in CF and Z_0, respectively [Figure 3.19]. According to Figure 3.4 and Figure 3.6, these variations have no impact on IRR values less than 60 dB. Device mismatch is analyzed via Monte-Carlo simulations, and the results are shown in Figure 3.20: Figure 3.20(a) presents the IRR of mixer-1 across frequency, and Figure 3.20(b) demonstrates the histogram of the IRR at 55 GHz. The IRR at 55 GHz has a mean value of 42.44 dB and a standard deviation of 6.23 dB.

3.4 Measurement Results

The chip photographs of IR mixer-1 and IR mixer-2 are shown in Figure 3.21 where die sizes are 1.57×1.22 and 1.65×1.18 mm^2, respectively. The fabricated chips are tested via

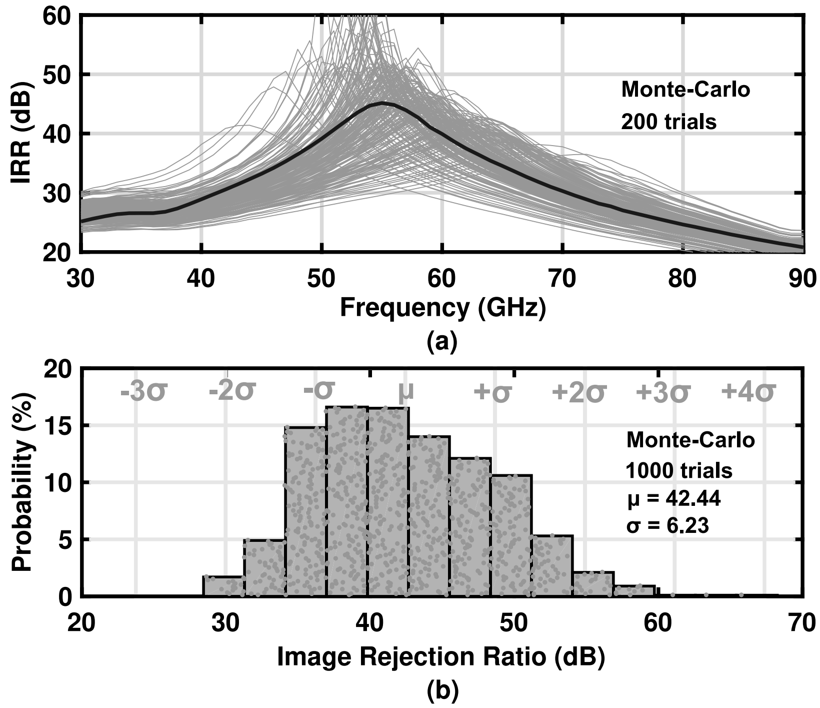


Figure 3.20: (a) The IRR of mixer-1 over 200 trials of a Monte-Carlo simulation (b) IRR of the mixer-1 resulted from a Monte-Carlo simulation over 1000 trials at 55 GHz (© 2018 IEEE).

on-chip probing of the RF and DC pads. Both chips consume 10.6 mA from a supply voltage of 3 V. Figure 3.22 presents input reflection coefficients of RF and LO ports from 20 to 70 GHz. The S-parameters are measured using an Agilent E8361C network analyzer. The RF port of mixer-1 is well-matched to 50 Ω from 42 to 70 GHz, and the RF port of mixer-2 is matched to 50 Ω over 41-70 GHz bandwidth. The reflection coefficients of LO ports (Γ_{LO}) in mixer-1 and mixer-2 are better than -7.5 and -7.3 dB, respectively. The measured Γ_{LO} is degraded by few dB compared to simulation results, mostly because of imperfect pad modeling.

Figure 3.23 presents the test setup used to measure conversion gain (CG) and IRR over the frequency band of 30–110 GHz. The RF and LO signals are provided by an Agilent signal generator (E8257D), a V-band source module (S15MS), and W-band source modules (S10MS) for different frequency bands. The measurements are performed with an LO power of 0 dBm. The power level of the source modules is controlled by a voltage-

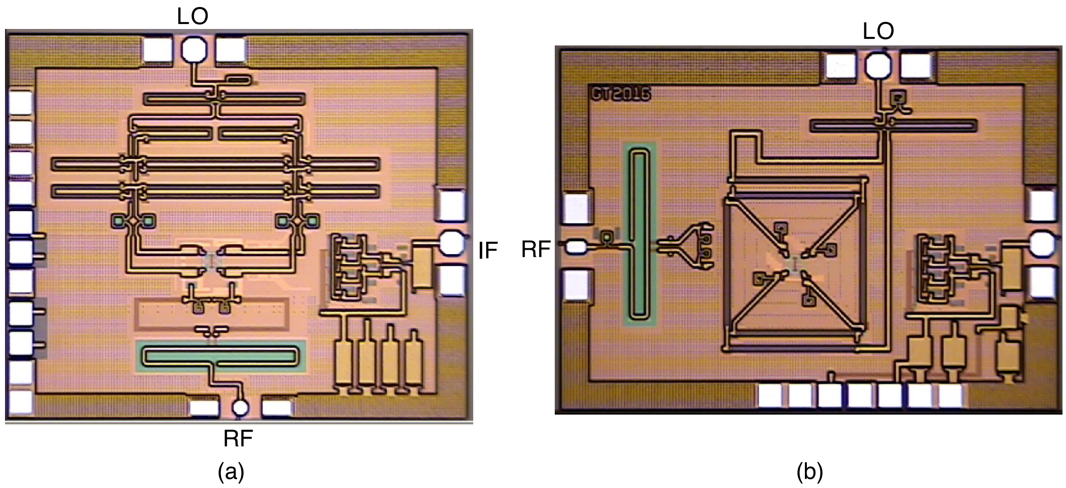


Figure 3.21: (a) The die photograph of image-reject mixer-1 with a chip area of $1.57 \times 1.22\,\mathrm{mm}^2$ as well as (b) the die photograph of image-reject mixer-2 with a chip area of $1.65 \times 1.18\,\mathrm{mm}^2$ (© 2018 IEEE).

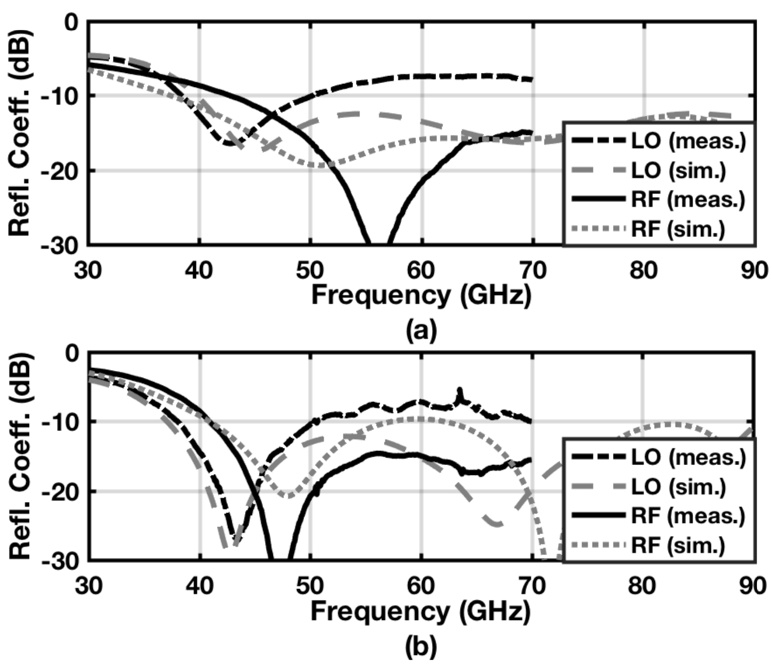


Figure 3.22: The input reflection coefficients of RF and LO ports for (a) IR mixer-1 and (b) IR mixer-2 (© 2018 IEEE).

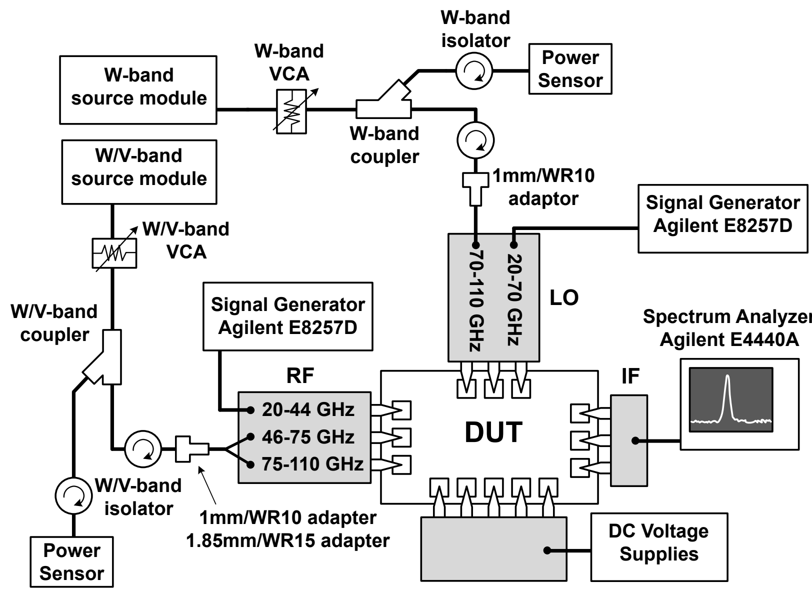


Figure 3.23: The test setup used to measure the conversion gain and IRR (© 2018 IEEE).

controlled attenuator and monitored with power sensors (V8486A and W8486A). A MATLAB script is used to control the equipment via a GPIB controller to sweep the frequency and power levels and to measure the IF signal with an Agilent spectrum analyzer (E4440A). The power loss of cables, probes, and waveguide sections are measured separately and de-embedded from the measurement results.

The image-rejection is measured at an IF frequency (f_{IF}) of 1 GHz. At each RF frequency (f_{RF}), the LO frequency is set to $f_{IF} \pm f_{RF}$ and the power of IF signal is measured in order to calculate CG and IRR. The measured and simulated CG and IRR of mixers are presented in Figure 3.24, where mixer-1 and mixer-2 have average CGs of 0 and 3 dB from 40 to 76 GHz, respectively. Although the gain of mixers drop after 70 GHz, we continued the measurement up to 110 GHz to characterize the broadband performance of the quadrature signal generation network. Based on the measurement results, mixer-1 shows an average IRR of 37.5 dB across 40 to 76 GHz with a peak IRR of 42.1 dB at 56 GHz. Mixer-2 features an average IRR of 33.5 dB across 40-102 GHz with a peak IRR of 36.7 dB at 96 GHz. These results are consistent with simulations as the maximum IRR of mixer-1 is 42.1 dB. Mixer-2 employs only one QHR stage with a lower CF, and results in a lower

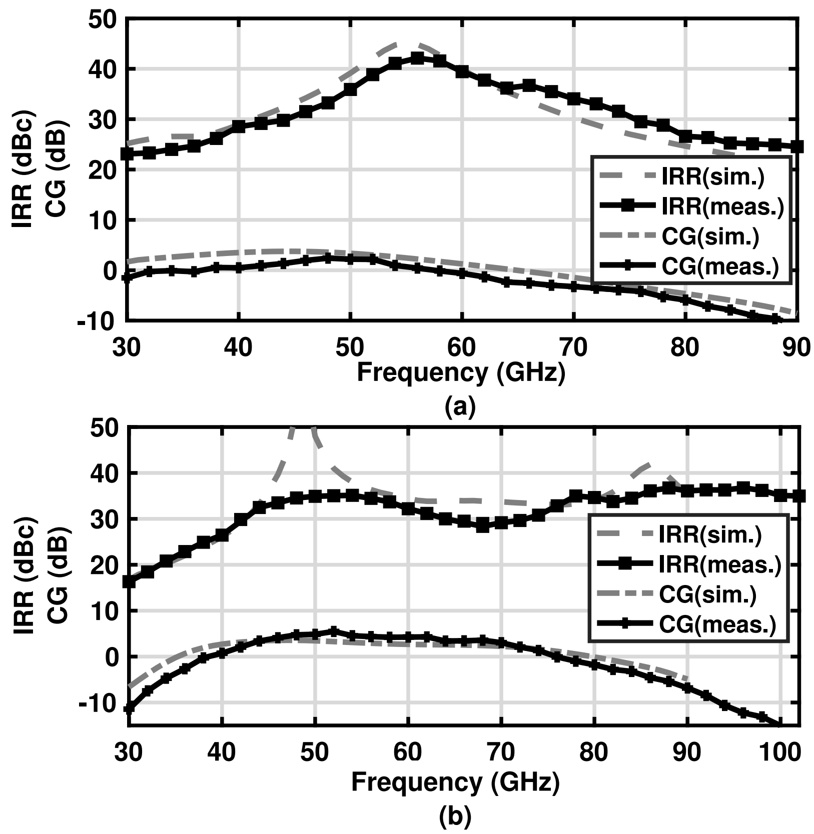


Figure 3.24: The conversion gain (CG) and the image rejection ratios of (a) IR mixer-1 and (b) IR mixer-2 when $P_{LO} = 0\,\mathrm{dBm}$ (© 2018 IEEE).

peak IRR compared to mixer-1. The length of Lange-couplers in mixer-2 is shorter than those of mixer-1; therefore, the IRR of mixer-2 at higher frequencies is better than the IRR of mixer-1. The input-referred P_{1dB} of the mixers are more than -14.5 dBm, and the LO-to-RF isolation of both mixers are better than 40 dB over the desired bandwidth.

The performance of both mixers presented in this work are compared with state-of-the-art mixers and I/Q (de)modulators at mm-wave frequencies in Table 3.1. Mixers discussed in [76, 67, 77, 69] were calibrated/tuned after fabrication to achieve IRRs higher than 30 dB, whereas [72] presents a load insensitive design and benefits from low IF frequency of 1.25 MHz to make IF signals less sensitive to length mismatches. The present mixers achieve high IRRs over a broad frequency range, without calibration, and the maximum IRR in this work (i.e., 42 dB) is limited by the length mismatch at the 1 GHz IF polyphase filter. Although the IRR of 42 dB is sufficient for most of the applications, it can be further improved by choosing a lower IF frequency and employing a symmetric layout for IF filter. In addition, QHR networks can occupy a large area due to the required $\lambda/4$ couplers, and defected ground and slow-wave structures can be employed to minimize their footprint [78].

Table 3.1: Performance Comparison of the State-of-the-Art Image-Reject Mixers and I/Q (De)modulators (© 2018 IEEE)

Reference	Process (f_T/f_{max})	RF Freq. (GHz)	IF Freq. (GHz)	IRR (dB) Freq (GHz)	Cal.[a]	CG_{max} (dB)	LO - RF iso. (dB)	P_{DC} (mW)	P_{LO} (dBm)	Size (mm^2)
[76] JSSC 2013	0.18 μm BiCMOS (240/270 GHz)	70–100	0.01	>30 (84–93.5) > 40 (89–92)	Yes	-	-	-	-	1.4[b]
[67] TMTT 2013	0.15 μm GaAs (85/120 GHz)	51–68	0.1	> 40 (51–65)	Yes	-12	> 40[c]	420	-1.5	4.48
[77] JSSC 2015	40nm CMOS (-)	62–85	0.1	> 30 (62–85) > 35 (69–80)	Yes	1[d]	-	-	5	0.57[b]
[69] EuMC 2016	90 nm CMOS (-)	76–88	0.1	> 40	Yes	-1.5	-	26.6	4	0.67
[72] TMTT 2013	65 nm CMOS (-)	64–84	0.00125	> 40	No	1	> 50[c]	40.8	2	0.86
[79] TMTT 2016	0.25 μm InP (350/650 GHz)	110–170	1	> 25	No	5[d]	>14	40.6	4	0.2[b]
[80] MWCL 2016	32 nm SOI CMOS (-)	158–182	1–10	> 20	No	8/-23[e]	-	74/0[e]	4	0.75
[81] Electronics Letters 2016	0.1 μm GaAs (-)	75–96	0.025	> 20	No	-6.9	> 43	-	14	1.73
This Work	0.13 μm BiCMOS (250/330 GHz)	42–76	1	> 30 (44–76) > 40 (53–59)	No	2.4	> 40	31.8	0	1.91
This Work	0.13 μm BiCMOS (250/330 GHz)	41–74	1	> 29 (42–102)	No	5.5	> 40	31.8	0	1.94

[a] Calibration and tuning. [b] Graphically estimated. [c] 2LO-to-RF isolation. [d] The transmitter gain excluding the amplifier gain. [e] The simulated gain of the mixer (with $P_{DC} = 0$ mW) is -23 dB, and the measured gain of the integrated mixer-IF amplifier (with $P_{DC} = 74$ mW) is 8 dB.

3.5 Summary

A broadband, passive, low-loss, I/Q signal generation network is presented for use in mm-wave applications. Two quadrature hybrids are employed in the first stage to generate I/Q signals. Then, the I/Q signals are applied to a QHR network to suppress phase/amplitude errors. Compared to calibration-based techniques, the presented method is more efficient because of zero power consumption, frequency scalability, and design simplicity. Two image-reject mixers are designed employing this approach, and they achieve average IRRs of 33.5 and 37.5 dB over 40–102 and 40–76 GHz frequency bands. These IRRs are obtained without any calibration, tuning, or trimming. The fabricated circuits achieve the widest bandwidths among the reported mm-wave mixers and I/Q (de)modulators with $\geq$ 30 dB average IRR. The presented method is a promising solution for broadband I/Q signal generation at mm-wave frequencies. This work was published in *IEEE Transactions on Microwave Theory and Techniques*, Dec. 2018 [3], and it is protected by the U.S. patent US10979038B2 filed on August 21, 2019 [4].

CHAPTER 4

DUAL-BAND QUADRATURE SIGNAL GENERATION

In chapter 3, we discussed that quadrature signal generation plays a key role in today's receivers. These signals are conventionally generated with RC-CR polyphase filters (PPFs), and PPFs should be cascaded [61] to improve the phase and amplitude matching as shown in Figure 4.1(a). However, this approach is less attractive at mm-wave frequencies due to the increased insertion loss. Similarly, $\lambda/4$ coupled-line couplers (CLCs) can be cascaded [3, 4] to generate low-loss and wideband quadrature signals as shown in Figure 4.1(b). But their footprint is relatively large at the lower end of mm-wave frequencies. In multi-band radiometry applications, we may need to cover different resonance frequencies of oxygen and vapor water. Thus, quadrature signals should be provided at different frequencies across the lower- and the higher-end of mm-wave frequency range. In this chapter, we present a dual-band mm-wave quadrature signal generation network employing both $\lambda/4$ CLCs (for higher frequencies) and PPFs (for lower frequencies). A symmetric floorplan is suggested to improve phase and amplitude matching and absorb the effects of parasitics and interconnects without degrading IRR. section 4.1 covers design challenges and provides guidelines to achieve low-loss and broadband performance. section 4.2 presents the measured data of the fabricated chip, where the phase and amplitude matching of quadrature signals are benchmarked with IRR, and a summary is provided at the end.

4.1 Circuit Design

A simplified schematic of the dual-band quadrature signal generation network is shown in Figure 4.2(a). This network consists of two λ/4 CLCs and a PPF, with center frequencies of f_{CLC} and f_{PPF}, respectively. To simplify the analysis, let us assume $f_{PPF} \ll f_{CLC}$. At low frequencies, CLCs are ideally short-circuited and the schematic is simplified to a

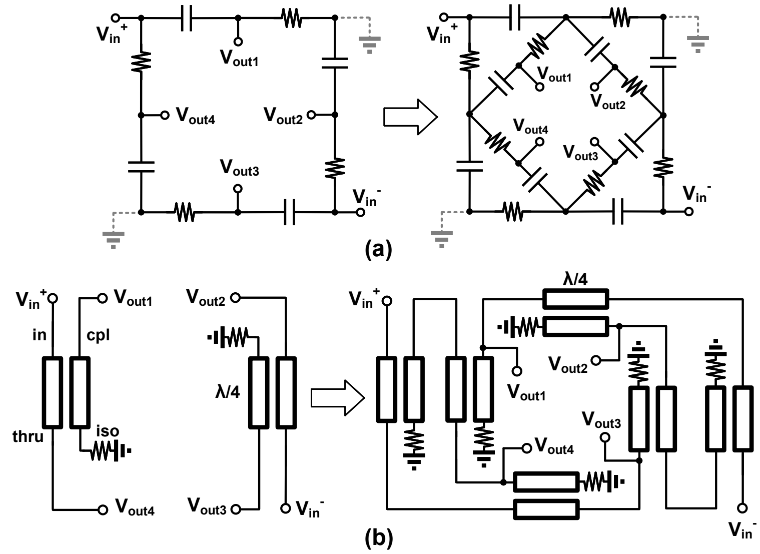


Figure 4.1: Cascading a) RC-CR PPFs and b) $\lambda/4$ CLCs to achieve higher IRR over a wider bandwidth (© 2020 IEEE).

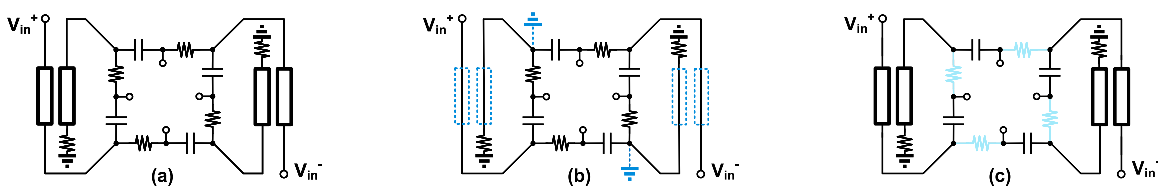


Figure 4.2: a) Simplified schematic of the dual-band quadrature LO generation network comprising an RC-CR PPF and two $\lambda/4$ CLCs. The PPF and the CLCs can independently set the center frequencies of the intended lower and upper frequency bands, respectively. b) At low frequencies, the transmission lines of the CLC are ideally short-circuited and c) at high frequencies, the capacitance of the PPF are ideally short-circuited (© 2020 IEEE).

single-stage PPF (refer to Figure 4.2(b)), and at high frequencies, the capacitance of the PPF is short-circuited and the schematic is simplified to a single-stage CLC (refer to Figure 4.2(c)). Therefore, the PPF and the CLC can independently set the center frequencies of the intended lower and the upper frequency bands. Best practice design considerations for achieving low-loss and broadband performance are discussed, including layout floorplan, effects of interconnects, parasitic capacitance in the PPF, coupling factor, and impedance matching of the CLCs.

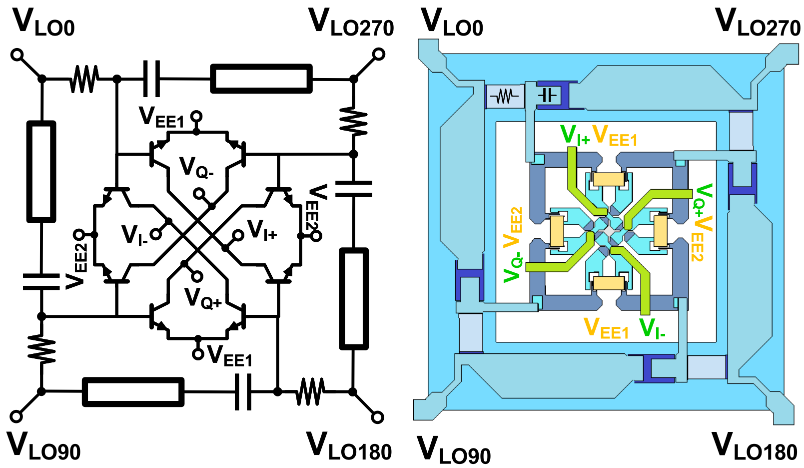


Figure 4.3: Symmetric schematic and layout of the PPF and switching transistors, where interconnects are modeled as transmission lines (© 2020 IEEE).

4.1.1 Common-Centroid PPF Layout

One of the key requirements for achieving good phase and amplitude matching is a symmetric layout. A semi-symmetric PPF floorplan was introduced in [82] to decrease the phase and amplitude mismatch, where different capacitor values were adopted in a PPF stage to compensate for different interconnect lengths. In the present work, we propose a fully-symmetric floorplan with identical interconnects to minimize mismatches. Figure 4.3 shows the common-centroid schematic and layout of the PPF and the switching transistors of the mixer, where the interconnects and the parasitic capacitances are modeled as transmission lines (TLs) with a characteristic impedance of Z_o and an electrical length of βl. This symmetric implementation reduces the sensitivity of the phase and amplitude matching to loading capacitance.

4.1.2 Effects of Interconnects on PPF Loss and IRR

The inductance and parasitic capacitance of interconnects introduce an undesirable phase-shift in the PPF. Figure 4.4(a) presents an ideal RC-CR PPF, in which the outputs always have a 90° phase-shift at all frequencies since the input signal is divided between a pure real and a pure imaginary impedances. To maintain this 90° phase-shift in a PPF imple-

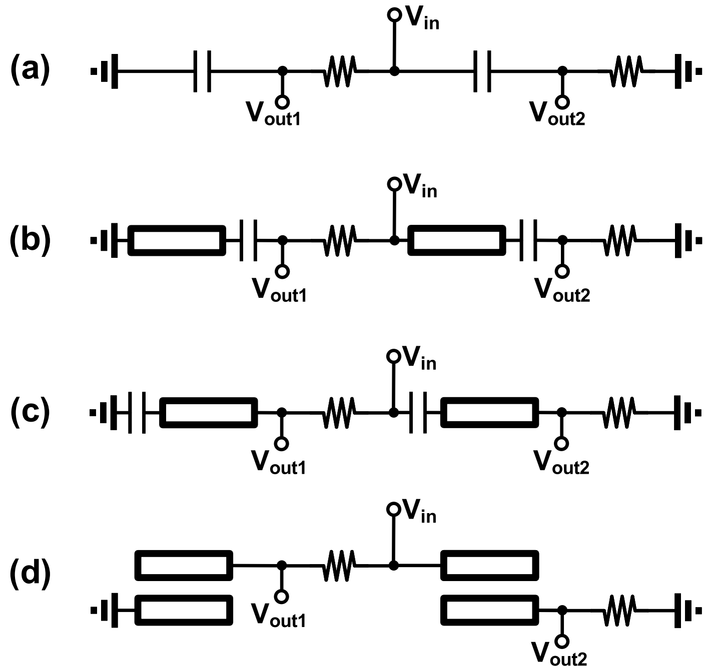


Figure 4.4: a) Ideal PPF, b) PPF in Configuration I, c) PPF in Configuration II, and d) PPF with a short-section of CLC as a capacitor (© 2020 IEEE).

mentation with interconnects, the output signal should be taken from a node on the PPF branch which divides it into a pure real and a pure imaginary impedances. Two cases of this kind are shown in Figure 4.4(b-c), where the real impedance is a resistor and the imaginary impedance is a capacitor in series with a TL. In the present work, the cases shown in Figure 4.4(b) and Figure 4.4(c) are referred to as "Configurations I and II," respectively. The imaginary impedance of Configuration I is a capacitor in series with a short stub, and that of Configuration II is a TL terminated in a shunt capacitor, whose impedance values are calculated as

$$Z_{in} = -j\big(X - Z_o \tan\beta l\big), \tag{4.1a}$$

$$Z_{in} = -j\Big(\frac{X - Z_o \tan\beta l}{1 + \frac{X}{Z_o}\tan\beta l}\Big) \tag{4.1b}$$

respectively, where $-jX$ is the impedance of the PPF capacitance. Based on (Equation 4.1), the filter capacitance resonates with long and high-Z_o interconnects, and to avoid this, lower Z_o, βl, and higher X values are preferred. βl is usually limited to the minimum physical distance in the layout. However, a wider interconnect and a smaller MIM filter capacitance can be employed to minimize the undesired effects of the interconnects and push the resonance to higher frequencies. Nevertheless, if the filter capacitance is too small, the center frequency of the filter can be sensitive to process variations. In that case, low-density capacitors (e.g., MOM capacitors) can be used to reduce the sensitivity, or short-sections of CLCs [see Figure 4.4(d)] can be employed as distributed capacitors between two conductors. Figure 4.5 depicts the reactance of both configurations at 60 GHz, demonstrating the resonance of larger capacitors with interconnects. Moreover, it shows that the CLCs can provide the same imaginary impedance with a proper coupling factor (CF). In the following analysis, the gain of the PPFs are derived and the effects of interconnects on the accuracy of quadrature signals are investigated.

Configuration I

Using ABCD matrixes, the output voltages of a PPF in Configuration I are derived as

$$\frac{V_{out1}}{V_{in}} = \frac{R}{\cos\beta l(R - jX) + jZ_0 \sin\beta l} \tag{4.2a}$$

$$\frac{V_{out2}}{V_{in}} = \frac{-j(Xcos\beta l - Z_0 sin\beta l)}{\cos\beta l(R - jX) + jZ_0 \sin\beta l} \tag{4.2b}$$

which shows that outputs are always in quadrature, and they have equal amplitudes when

$$R = Xcos\beta l - Z_0 sin\beta l. \tag{4.3}$$

Substituting (Equation 4.3) in (Equation 4.2), the gain at center frequency is calculated as

$$\left|\frac{V_{out1}}{V_{in}}\right| = \left|\frac{V_{out2}}{V_{in}}\right| = \left|\frac{1}{\cos\beta l - j}\right|. \tag{4.4}$$

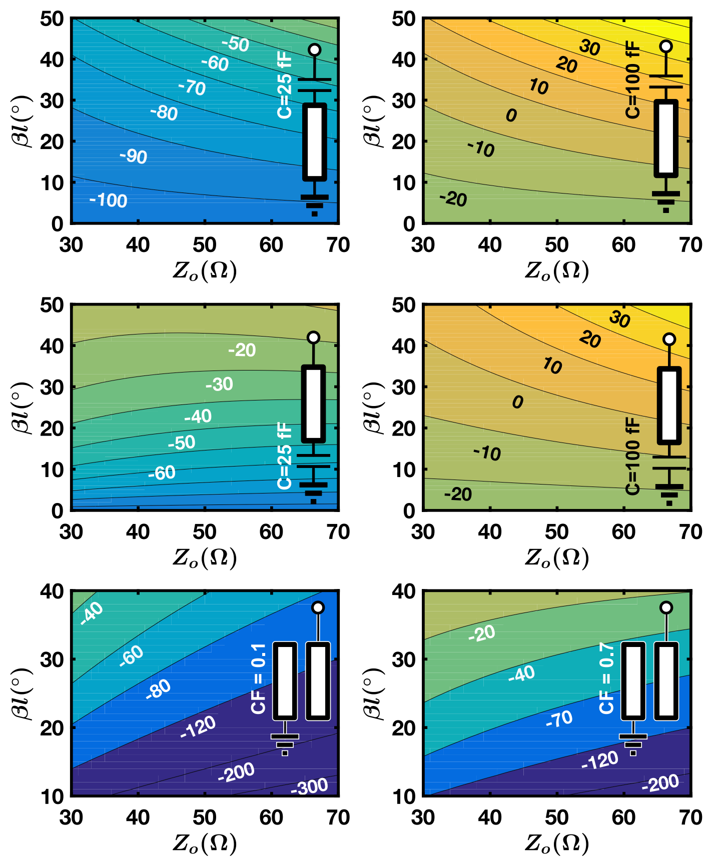


Figure 4.5: Reactance of Configurations I and II and a shorted CLC at 60 GHz as a function of Z_o and βl (© 2020 IEEE).

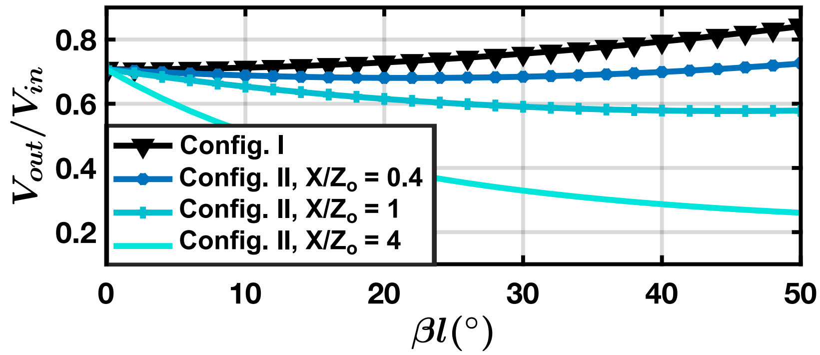


Figure 4.6: Gain of PPF configurations as a function of Z_o and βl (© 2020 IEEE).

Configuration II

Similarly, the output voltages of a PPF in Configuration II are derived as

$$\frac{V_{out1}}{V_{in}} = \frac{R}{\cos\beta l(R - jX) + \sin\beta l(jZ_0 + \frac{XR}{Z_0})} \tag{4.5a}$$

$$\frac{V_{out2}}{V_{in}} = \frac{-j(X\cos\beta l - Z_0 sin\beta l)}{\cos\beta l(R - jX) + \sin\beta l(jZ_0 + \frac{XR}{Z_0})}, \tag{4.5b}$$

where outputs are always in quadrature, and (Equation 4.3) should be satisfied at center frequency. The gain at this frequency is derived by substituting (Equation 4.3) in (Equation 4.5) as

$$\left|\frac{V_{out1}}{V_{in}}\right| = \left|\frac{V_{out2}}{V_{in}}\right| = \left|\frac{1}{(\cos\beta l - j) + \frac{X}{Z_0}\sin\beta l}\right|. \tag{4.6}$$

In general, the loss of PPFs consists of intrinsic and loading losses [61]. First, let us discuss the intrinsic loss, where the outputs of PPF are not loaded. For an unloaded PPF with $\beta l = 0$, the gain of the PPF is about 0.707, but when interconnects are taken into account, using (Equation 4.4) and (Equation 4.6), Configurations I and II can behave quite differently. Figure 4.6 shows the gain of the PPF in Configuration I, where gain increases as βl increases. On the other hand, the gain of Configuration II for small X/Z_o is similar to Configuration I, but for large X/Z_o, it decreases as βl increases.

The effects of interconnects and parasitic capacitances on the accuracy of quadrature

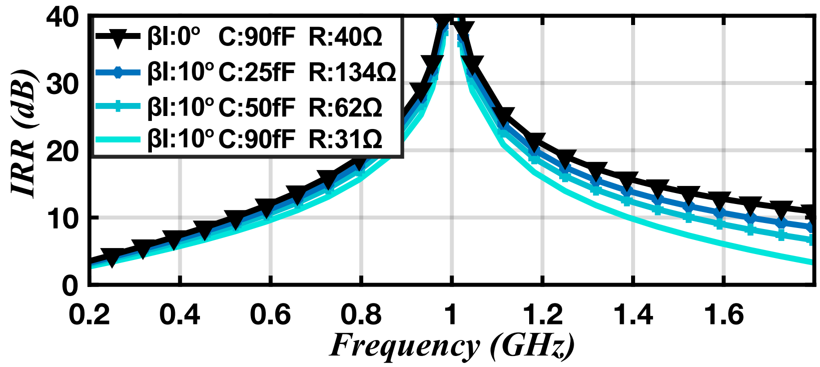


Figure 4.7: IRR of the PPF versus normalized frequency. The IRR of Configurations I and II are the same (© 2020 IEEE).

signals is also important and it should be investigated. The phase and amplitude matching of quadrature signals can be benchmarked with IRR given as [72]

$$IRR = \frac{(1+\epsilon)^2 - 2(1+\epsilon)\cos\theta + 1}{(1+\epsilon)^2 + 2(1+\epsilon)\cos\theta + 1}, \tag{4.7}$$

where ϵ and θ are the amplitude mismatch ($|V_{out2}/V_{out1}| - 1$) and the phase mismatch ($\measuredangle V_{out2}/V_{out1} - 90°$), respectively. As discussed earlier, interconnects and parasitic capacitances do not degrade the phase matching of quadrature signals if the PPF is implemented in Configuration I or II. However, the amplitude ratio for both configurations is altered by interconnects and parasitic capacitances as

$$\frac{V_{out1}}{V_{out2}} = \frac{jR}{X\cos\beta l - Z_0 \sin\beta l}. \tag{4.8}$$

Since the ratio of V_{out1}/V_{out2} is equal in configurations I and II, the IRR of PPFs in these configurations will be the same if they have the same center frequency. Figure 4.7 shows this value for a few different cases, where interconnects can reduce the bandwidth of the quadrature signals. Nonetheless, we will present a technique that using a CLC stage before the PPF we can significantly improve the amplitude matching and make interconnect effects negligible.

4.1.3 Coupled-Line Coupler Design

A CLC is a four-port network, typically used for power dividing and combining. The outputs of a CLC are in quadrature and it can provide perfect amplitude matching at two frequencies when over-coupled (CF > 0.707). Moreover, it can be shown that load impedance reflections of the CLC do not degrade phase and amplitude matchings as long as the output ports are terminated in identical impedances.

Figure 4.2 presented a simplified schematic of the dual-band quadrature signal generation network consisting of two CLCs followed by a PPF stage. As previously discussed, both CLC and PPF stages provide perfect phase matching at all frequencies. Therefore, the bandwidth of the quadrature signals is only a function of amplitude matching. In the present work, the PPF is designed to provide perfect amplitude matching at 44 GHz (R = 129 Ω and C = 25 fF), and the CLC is designed for a CF of 0.71 and a length of $\lambda/4$ at 90 GHz. Figure 4.8(a) demonstrates the amplitude ratio of the outputs in this quadrature signal generator, where three perfect amplitude matching points are achieved when CF > 0.707. Depending on the target frequency ranges, the length and the CF of the CLC can be tuned to provide highly balanced quadrature signal across a broad frequency range. For example, Figure 4.8(b) depicts two ideal designs with 40 dB IRR across $40-100$ GHz and 30 dB IRR across $35-152$ GHz. To provide a better impedance matching between the PPF and the CLC stages, a series inductor, L_1, is inserted to resonate with the input capacitance of the PPF at the center frequency of CLCs.

4.1.4 Series Inductive Peaking

At mm-wave frequencies, the input impedance of the mixer switching transistors can be highly capacitive, which loads the PPF output, introducing more loss and limiting the frequency bandwidth. LO buffer stages are commonly employed to decrease this loading effect. In the present design, the size of each switching transistor is $6\times$ 0.13 μm^2 and conventional inductive peaking technique is preferred, since it can improve the bandwidth and

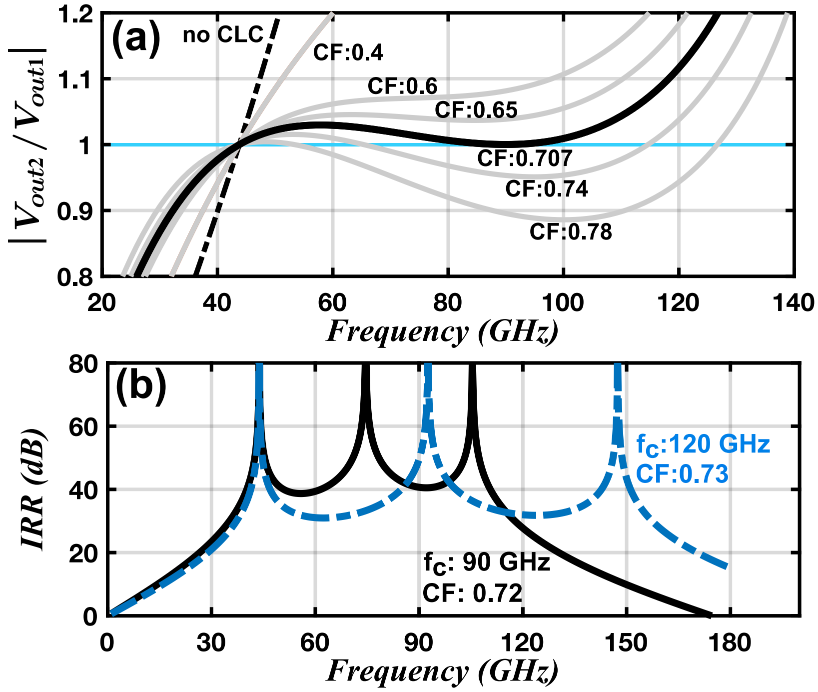


Figure 4.8: a) Amplitude ratio of the PPF outputs for various coupling factors, b) IRR of the quadrature signals for two different cases (© 2020 IEEE).

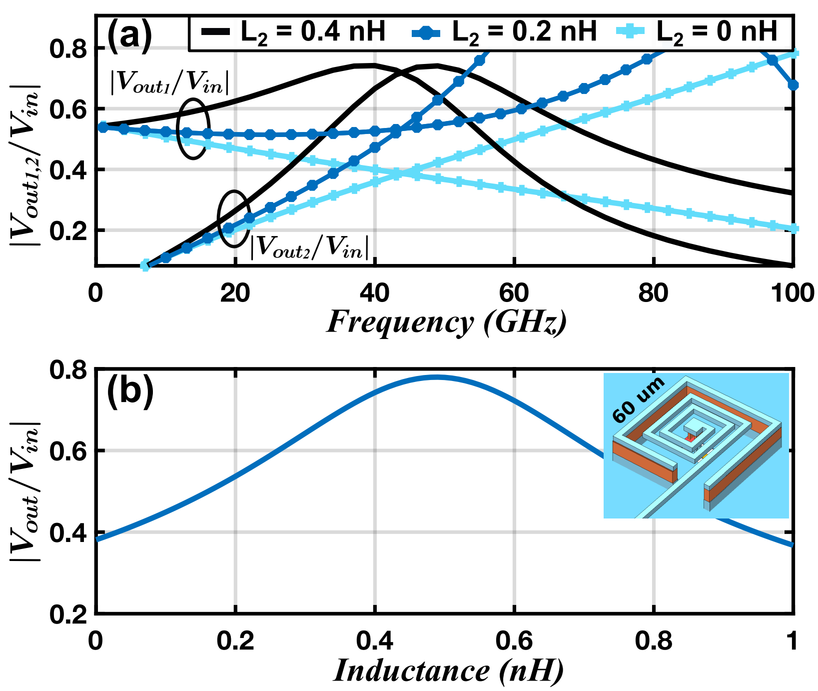


Figure 4.9: a) PPF gain as a function of frequency for various series peaking inductances. b) PPF gain at center frequency as a function of the series peaking inductance (© 2020 IEEE).

compensate the loading loss with zero power consumption, simply by adding an inductor, L_2, in series with the load. Figure 4.9(a) presents the gain of the PPF when loaded with switching transistors for $L_2 = 0$, 0.2, and 0.4 nH, and Figure 4.9(b) demonstrates the gain at the center frequency as a function of L_2. The optimum inductance is 0.5 nH, but we chose a smaller inductance of 0.2 nH to keep βl smaller than 10°, which still improves the gain from 0.38 to 0.53. Figure 4.9(b) shows the inductor layout with a ground cage around it, occupying $60 \times 60\,\mu\text{m}^2$.

In this work, the performance of both configurations are similar since βl is small, and we chose configuration II for easier impedance matching between CLC and PPF at high frequencies. Figure 4.10 shows the final schematic and die photo of the suggested quadrature signal generation network.

4.2 Measurement Results

As a proof-of-concept, an image-reject mixer is fabricated in a $0.13\,\mu$m SiGe BiCMOS technology which employs the presented quadrature signal generation network. The schematic and layout of this Gilbert-based mixer is the same as the one dicussed in the previous chapter. To measure the mixer, the RF and local oscillator (LO) signals were provided by an Agilent E8257D signal generator, a V-band S15MS source module, and W-band S10MS modules to cover $20 - 100$ GHz frequency range. The measurements were performed at an IF frequency (f_{IF}) of 1 GHz and with an LO power of 1 dBm, while the power level of source modules was controlled with attenuators and monitored with V8486A and W8486A power sensors. At each RF frequency (f_{RF}), the LO frequency is set to $f_{RF} \pm f_{IF}$ and the IF signal was measured with an Agilent E4440A spectrum analyzer to calculate IRR.

Figure 4.11 demonstrates the Monte-Carlo results of mixer IRR for $\pm 3\,\sigma$ statistical variations of all process parameters, accounting for load impedance mismatches (switching transistors). These results are compared with the measured IRR, which is higher than 29 dB for $36 - 98$ GHz. The performance of the quadrature signal generation network is

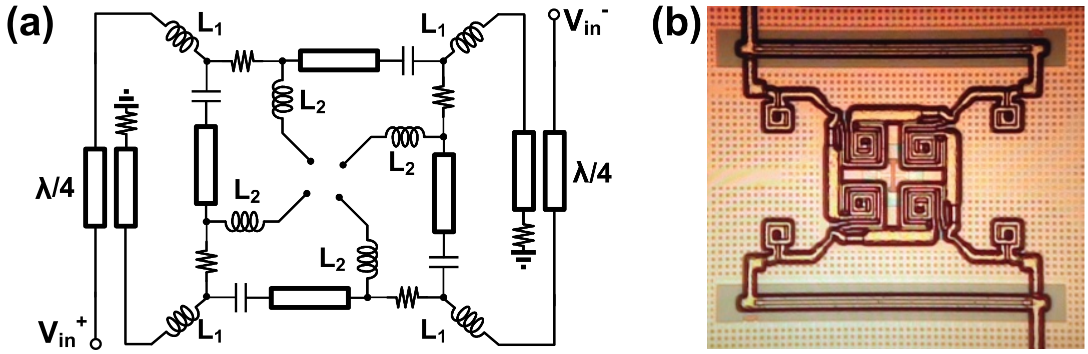


Figure 4.10: a) Schematic and b) layout of the dual-band quadrature signal generation network. This network occupies a chip area of 0.5×0.43 mm^2 (© 2020 IEEE).

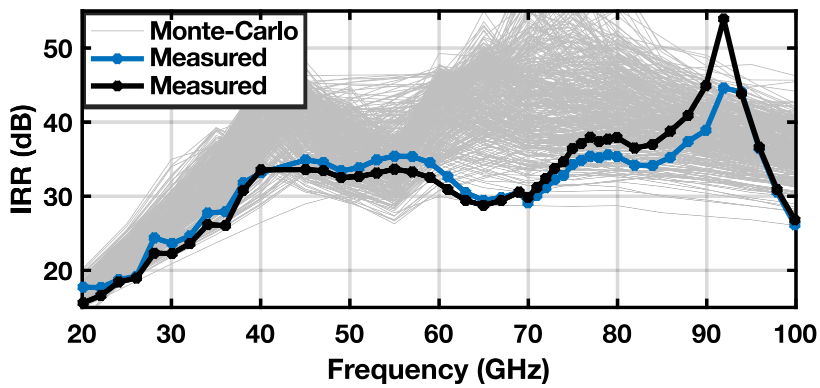


Figure 4.11: Monte-Carlo results of process variations and device mismatches with 400 iterations and measured IRR (© 2020 IEEE).

compared with state-of-the-art mixers and I/Q modulators in Table 4.1. Mixers presented in [76, 77, 69, 83] are tuned and calibrated after fabrication to reduce the phase and amplitude mismatches, while [72, 83] benefit from low IF frequencies of 1.25 and 0.5 MHz, respectively, to make IF signals less sensitive to length mismatches. The design in [3] cascades $\lambda/4$ CLCs to achieve low-loss and broad bandwidth, but it can not be easily scaled to frequencies lower than 30 GHz while maintaining a small footprint, whereas, in the present work, the PPF and the CLCs can independently set the center frequencies of the lower and upper frequency bands, respectively, to cover a broad frequency range with a smaller footprint.

Table 4.1: Performance Comparison of the State-of-the-Art Image-Reject Mixers and I/Q (De)modulators (© 2020 IEEE)

Ref.	RF Freq. (GHz)	IF Freq. (GHz)	IRR (dB)	Cal.[a]	Size[b] (mm^2)
[76]	84–94	0.01	> 30	Yes	1.4[c]
[77]	62–85	0.1	> 30	Yes	0.57[c]
[69]	76–88	0.1	> 40	Yes	0.67
[83]	28–44	0.0005	> 40	Yes	3.91
[72]	64–84	0.00125	> 40	No	0.86
[79]	110–170	1	> 25	No	0.2[c]
[80]	158–182	1–10	> 20	No	0.75
[3]	42–102	1	> 29	No	1.94
This Work	36–98	1	> 29	No	1.65

[a] Calibration and tuning. [b] mixer size [c] Graphically estimated.

4.3 Summary

A dual-band quadrature signal generation network is presented for use in mm-wave systems. This network consists of two coupled-line couplers followed by a RC-CR polyphase filter. A common-centroid floorplan is suggested for LO generation networks and switching transistors to improve the phase and amplitude matching and to reduce sensitivity to loading capacitance. Design tradeoffs and best practices are discussed for achieving low loss and wideband performance, and a proof-of-concept SiGe image-reject mixer is demonstrated employing this quadrature LO generation network. This mixer achieves a mean image-rejection ratio of 34 dB across $36 - 100$ GHz. This network presents a promising solution for emerging mm-wave dual-band and broadband quadrature signal generation needs. This work was published in *IEEE Transactions on Circuits and Systems II: Express Briefs*, Feb 2020 [5].

CHAPTER 5

HIGH EFFICIENCY FREQUENCY MULTIPLIER

In mm-wave systems, typically a low phase noise oscillator is followed by a high power and high efficiency frequency multiplier to provide a stable mm-wave signal. Among reported circuits, frequency doublers (FDs) are commonly designed based on push-push and Gilbert-cell topologies, where amplifier stages at the output [84] and harmonic reflectors at the input [85] are employed to increase power-added efficiency (PAE) and conversion gain (CG). In [86], the core efficiency of a push-push frequency quadrupler was increased by controlling the phase of the injected signal at different nodes of the circuit. Phase controlling has also been implemented in Gilbert-cells to obtain balanced outputs [87, 88]. In the present work, we maximize the CG and the core efficiency of a Gilbert FD by adjusting the phase of the injected signal into switching transistors. We demonstrate that the output signal of a Gilbert FD can be doubled with proper phasing. A Ka-band SiGe FD is designed based on this analysis, and it achieves a record performance of 26.2 % PAE and 21 dB CG, without any output buffer.

5.1 Gilbert Frequency Doublers

A mixer schematic with ideal switches is shown in Figure 5.1, where V_{SW} has θ_{chop} phase shift with respect to V_{RF}. The chopped output waveforms for $\theta_{chop} = 0°$, 90°, and 180° are presented in Figure 5.1 with associated Fourier coefficients. When θ_{chop}= 90°, the outputs are balanced and their DC component (a_0) is zero. Notably, the 2^{nd} harmonic component of this case is twice as strong compared to θ_{chop}= 0° and 180°. Therefore, θ_{chop}= 90° is desired to achieve higher output power and efficiency. This can be implemented with a Gilbert FD where RF and LO signals are in quadrature.

Figure 5.2 shows two Gilbert FD topologies, a conventional one and a bootstrapped

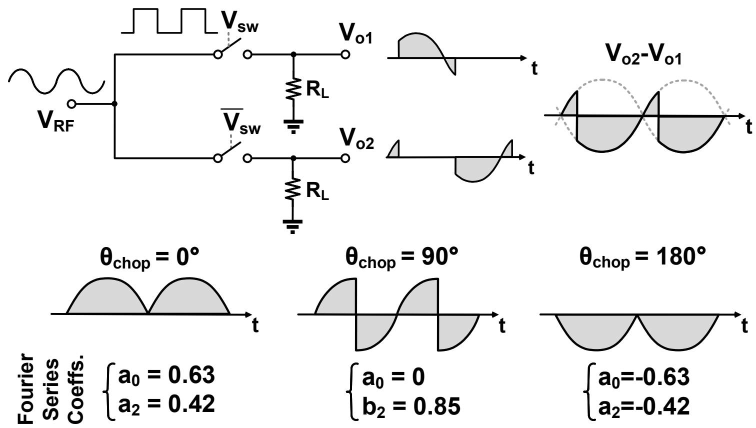


Figure 5.1: Mixer schematic and waveforms of the chopped RF signal as a function of θ_{chop}, along with associated Fourier coefficients. a_n and b_n are the $cos(n\omega_o t)$ and the $sin(n\omega_o t)$ coefficients, respectively (© 2018 IEEE).

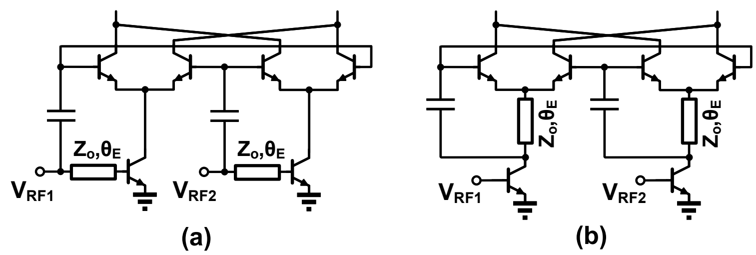


Figure 5.2: (a) Conventional and (b) bootstrapped Gilbert FD employing transmission lines to realize $\theta_{chop} = 90°$ (© 2018 IEEE).

one, where transmission lines (TLs) are employed to realize $\theta_{chop} = 90°$ [87, 88]. In the bootstrapped design [see Figure 5.2(b)], the voltage across this TL is directly applied to the base-emitter junction of switching transistors, giving two advantages over the conventional design [87]: 1) the required power for switching is lower, and as a result, 2) the second-harmonic component at the emitter of switching transistors has a smaller amplitude, which reduces output imbalance.

In Figure 5.1, the output waveforms of θ_{chop}= 0° and 180° are the same as the waveforms of a class-B push-push FD. Based on this analysis, a bootstrapped Gilbert FD can achieve a higher CG compared to a push-push FD when switching transistors provide sharp signal switching and consume a low RF power. In other words, the switching transistor parasitic capacitance should be small, imposing a tradeoff between device size (output power) and frequency. Otherwise, a push-push FD can achieve a better performance.

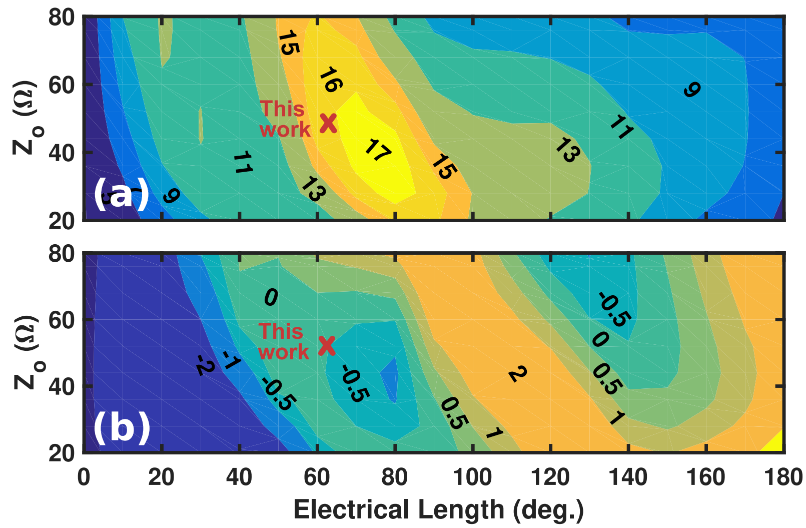


Figure 5.3: Contours of a) the differential collector current at the second harmonic ($I_{diff.}|_{2fo}$), and b) the associated current imbalance as a function of Z_o and θ_E for a 14 GHz input signal. The unit of currents is mA (© 2018 IEEE).

5.2 Circuit Design

A Ka-band FD is implemented with a bootstrapped-Gilbert topology in a 0.13 μm SiGe BiCMOS process. The input transistors are sized $2 \times 6.8\,\mu$m $\times\, 0.13\,\mu$m, and biased in class AB to achieve high gain and high PAE, while switching transistors are sized $6\,\mu$m $\times\, 0.13\,\mu$m, and biased with a DC base voltage of 1.3 V. In Figure 5.1, the CG of the FD with ideal switches is only a function of θ_{chop}, whereas in the bootstrapped-Gilbert, the switches are not ideal, and the CG is a function of the electrical length (θ_E) and the characteristic impedance (Z_o) of the TLs as well as the switch delay. Figure 5.3 shows the contours of the differential collector current at the second harmonic ($I_{diff.}|_{2fo}$), and the associated current imbalance as a function of Z_o and θ_E. The output $I_{diff.}|_{2fo}$ is a strong function of θ_E, and the peak value is achieved around a θ_E of $70° - 80°$, which is slightly less than 90° because of the switch delay. The $I_{diff.}|_{2fo}$ is also a weak function of Z_o, because transistors turn on/off faster with a larger sine amplitude, and a higher Z_o value provides a larger voltage swing across the base-emitter junction of switches, reducing the optimum θ_E. For example, the performance of a FD with θ_E= 90° and Z_o= 30 Ω is similar to the performance of the

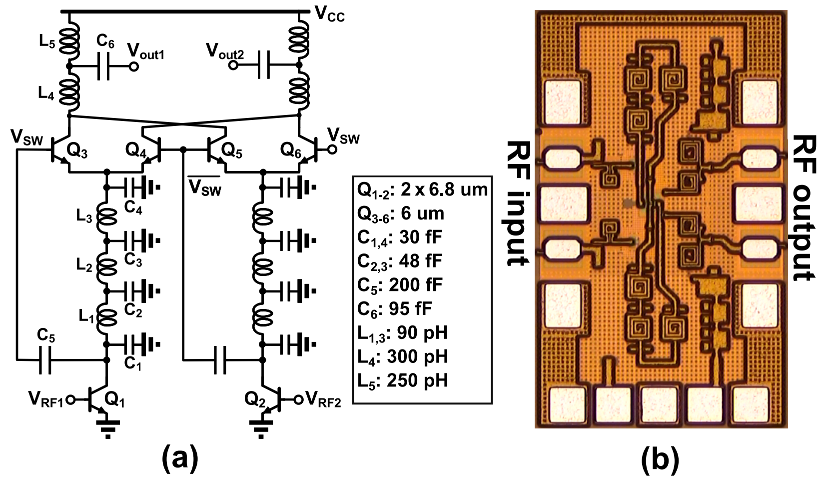


Figure 5.4: (a) Schematic of the FD and component values. (b) Die photograph of the FD with a chip area of 0.53 $\times$ 0.9 mm^2 with pads and 0.3 $\times$ 0.75 mm^2 without pads (© 2018 IEEE).

one with θ_E= 60° and Z_o= 70 Ω. In the present design, Z_o = 50 Ω and θ_E = 63° is chosen to minimize the current mismatch and to provide a high current swing simultaneously.

Figure 5.4 shows the schematic and the layout of the FD with component values. The delay-lines are implemented with artificial TLs to make the footprint smaller, and an output matching network, consisting of two inductors and a DC-blocking capacitor, is designed. This output matching network is simulated with the Sonnet electromagnetic solver and shows a 1 dB insertion loss at 28 GHz.

5.3 RF Reliability and Revised Load Line

The SiGe HBT breakdown voltage is a function of the base termination, and in this process, it varies between a BV$_{CEO}$ of 1.8 V and a BV$_{CBO}$ of 5.8 V. The reliability of SiGe amplifiers under DC and RF operations are studied in [89] where significantly increased impact ionization damage was observed under DC operation compared to RF condition. This study suggests that the DC reliability constraints are too conservative and they overestimate the RF damage. Therefore, a revised load line was introduced to relate the RF load line to the DC safe operating area (SOA), wherein the transistor capacitive current I_{cap} is subtracted

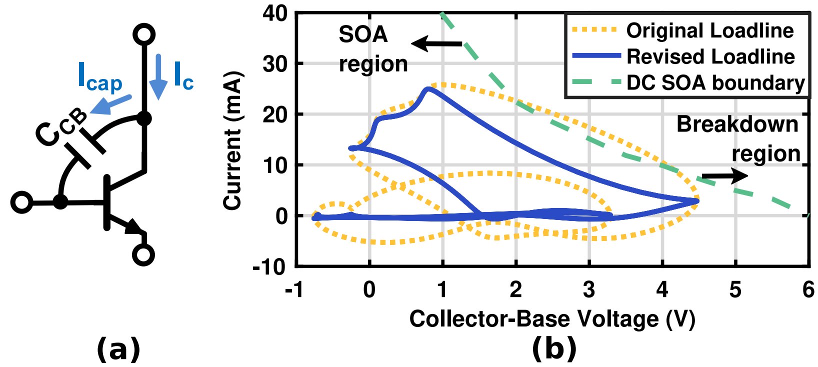


Figure 5.5: a) Definition of I_c and I_{cap}. b) Original and revised load lines with SOA region indicated (© 2018 IEEE).

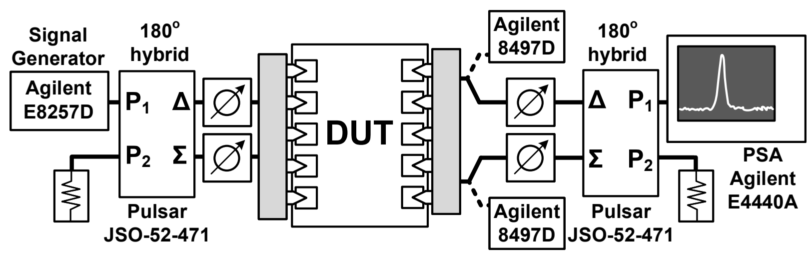


Figure 5.6: Measurement setup (© 2018 IEEE).

from the collector current I_c to isolate DC reliability conditions from time-varying currents [see Figure 5.5(a)].

In the bootstrapped-Gilbert FD, the input transistors are shielded from high voltage swing and the reliability of switching transistors are investigated in Figure 5.5(b), where the original and revised load lines along with the DC SOA region of switching transistors are shown. The revised load line is inside the SOA, indicating the reliable operation of the FD, and this load line is derived with a first-order approximation of the base-collector capacitance.

5.4 Measurement Results

The measurement setup is shown in Figure 5.6, where two 180° hybrids are used as input and output baluns and phase shifters are used to improve the phase matching. The loss of the input/output fixtures are measured separately and de-embedded from the measurement

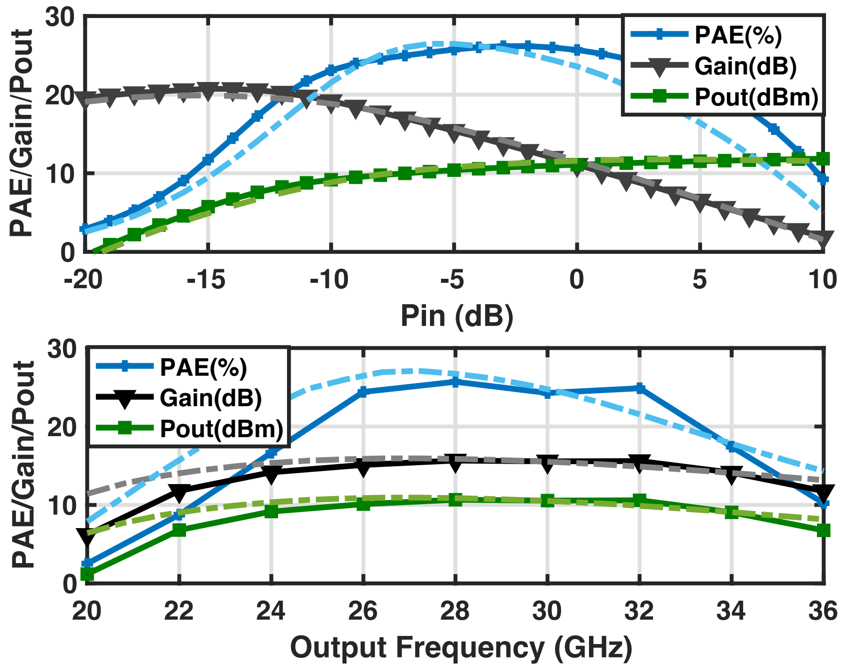


Figure 5.7: Simulated and measured PAE, gain, and Pout of the FD (a) at 28 GHz, and (b) with $P_{in} = -5$ dBm (© 2018 IEEE).

results. The output powers are measured with two Agilent 8487D power sensors, and the fundamental rejection ratio is measured with an Agilent E4446A spectrum analyzer. The chip consumes a 17 mA DC current from a 2.5 V supply voltage for a -5 dBm input power. Figure 5.7(a) shows the measured and the simulated P_{out}, CG, and PAE of the FD as a function of the input power at 14 GHz, and Figure 5.7(b) shows the same parameters across frequency for $P_{in} = -5$ dBm. The doubler achieves a 3-dB bandwidth of 22-36 GHz, a peak CG of 21 dB, a peak PAE of 26.2 %, and a saturated output power of 11.9 dBm. The performance of this FD is compared with the state-of-the-art Ka-band FDs in Table 5.1. The present work achieves the highest PAE and CG among all reported Ka-band Si-based FDs without output buffers.

Table 5.1: Performance Comparison of the State-of-the-Art Ka-band Frequency Doublers (© 2018 IEEE)

Ref.	Technology	Topology	Freq.[a] (GHz)	$P_{sat.}$ (dBm)	Peak η / PAE[b] (%)	Peak CG (dB)	FR[c] (dB)	P_{dc} (mW)	Size (mm^2)	Pow. Den. (mW/mm^2)
[67]	0.18 μm CMOS	Push-Push Stage	15-36	-5.2	2.7 / -	-10.2	33	11	0.32	0.94
[90]	0.18 μm SiGe	Push-Push Stage + Amp.	26-40	5	4.8 / -	-4	14	66	0.56	5.64
[91]	0.8 μm SiGe	Push-Push Cascode	34-37	10.5	9.8 / 6.4	4.5	35	114	0.54	20.78
[92]	0.5 μm GaAs	Dual-Gate Stage	36-41	7	14.3 / -	-0.9	15	25	1	5
[93]	0.13 μm SiGe	Push-Push Cascode + Amp.	27-41	8	18 / 16.9	19.8	26	32	0.34	18.56
[94]	65 nm CMOS	Balanced Push-Push	22-25	5	9.9 / 6.5	5	44	31	0.47	6.72
[85]	0.13 μm SiGe	Cascode Push-Push	25-40	13	22.9 / 22	14	35	87	0.5	40
This work	0.13 μm SiGe	Bootstrapped Gilbert-Cell	22-36	11.9	27.4 / 26.2	21	32	43.1[d]	0.48	33

[a] 3-dB Bandwidth [b] $\eta = P_{out}/P_{dc}$ and PAE = $(P_{out} - P_{in})/P_{dc}$ [c] Fundamental Rejection [d] P_{in} = -5 dBm.

5.5 Summary

In this chapter, we demonstrate that the output power of Gilbert frequency doublers are maximized when switching transistors chop the RF signal with a 90° phase shift. A Ka-band SiGe bootstrapped Gilbert frequency doubler was designed, employing transmission lines to realize the phase shift. This phase shift is a function of the electrical length and the characteristic impedance of transmission lines, as well as the switch delay. The doubler achieves a peak PAE of 26.2 % and a peak conversion gain of 21 dB at 28 GHz. These are the highest PAE and the highest CG achieved without output buffers among reported Si-based frequency doublers. This work was published in *IEEE Microwave and Wireless Components Letters*, November 2018 [6].

CHAPTER 6
ON-CHIP NOISE SOURCES FOR RADIOMETER CALIBRATION

Radiometers must be regularly calibrated to ensure accurate measurements. To calibrate a radiometer, two or more noise references with precisely known noise temperatures are injected into the instrument, which enables the calculation of the transfer function. This calibration procedure corrects for changing instrument performance due to ambient temperature fluctuations, aging of components in the receiver, and random long-term $1/f$ gain fluctuations. Ideal radiometer calibration sources exhibit both uniform performance across frequency and temperature, as well as long-term stability.

For example, radiometers are often pointed at physical targets with known noise temperatures, such as temperature-controlled microwave absorber, or deep space [40, 7]. In modern radiometers, electronic calibration sources are often integrated into the receiver in front of the LNA to enable frequent in-situ calibration. Two sources are required to enable linear calibration—one is generally a matched load at ambient temperature, and the other is an active source that generates noise above ambient temperature. Active sources are generally implemented using weakly-coupled diodes reverse-biased to avalanche breakdown. For low-cost applications, the avalanche noise sources can be monolithically designed from numerous device types available in modern silicon processes, including CMOS bulk junctions [95], Schottky diodes [96], and diode-configured SiGe HBTs [7]. These noise sources can be potentially used to implement the advanced noise injecting radiometer topologies monolithically, which clearly offers integration advantages. The avalanche noise of these devices is technology dependent and is not captured by the compact models offered by the foundry.

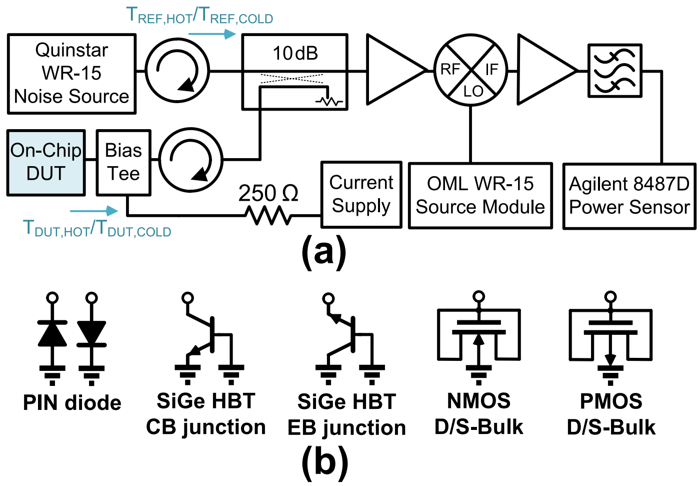


Figure 6.1: a) block diagram of the ENR measurement setup [7], and b) schematic diagram of the noise source devices. The anode-ground and cathode-grounded PIN diodes have identical performance (© 2021 IEEE).

6.1 ENR of On-Chip Noise Sources

To determine the most suitable avalanche noise source for an integrated radiometer front-end, an investigation was performed on the devices of a 130 nm SiGe BiCMOS platform. Five PN-junctions were evaluated: nFET and pFET source/drain-to-bulk junctions, diode-configured SiGe HBT emitter-base (EB) and collector-base (CB) junctions, and a PIN diode. The excess noise ratio (ENR) was measured using the setup shown in Figure 6.1(a), following the approach outlined in [7]. The devices under test (DUT) in this setup are shown in Figure 6.1(b), which are the standalone PN-junctions of the above-mentioned devices. The output of a calibrated noise source (both HOT and COLD) is combined with the weakly-coupled output noise from the DUT (both ON and OFF), and then the combined noise is down-converted to baseband and measured with a power sensor. The ENR at the output of the DUT was calculated using the following equations [7]:

$$T_{\mathrm{ON}} = \frac{T_{\mathrm{hot}} - Y_{\mathrm{ON}} \times T_{\mathrm{cold}}}{Y_{\mathrm{ON}} - 1} \tag{6.1}$$

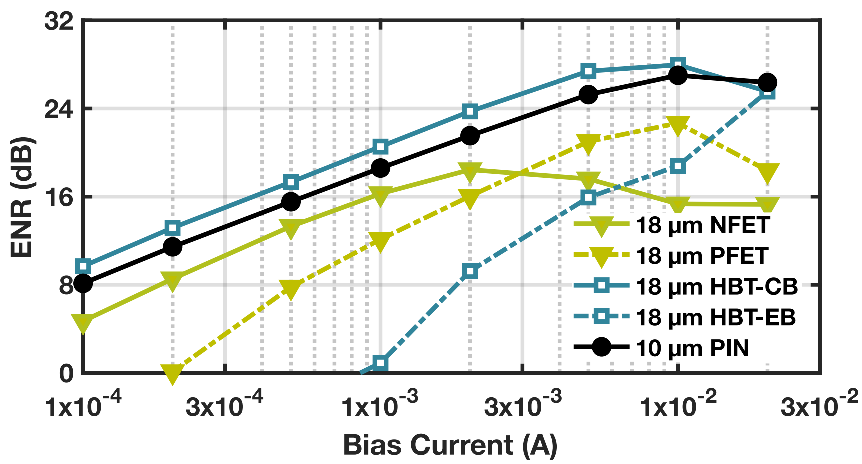


Figure 6.2: ENR of different junctions in a commercial SiGe BiCMOS platform (© 2021 IEEE).

$$T_{\text{OFF}} = \frac{T_{\text{hot}} - Y_{\text{OFF}} \times T_{\text{cold}}}{Y_{\text{OFF}} - 1} \tag{6.2}$$

$$T_{\text{g}} = (T_{\text{ON}} - T_{\text{OFF}}) \times \frac{1 - C}{C} \times L_{\text{fixt}} \tag{6.3}$$

$$\text{ENR (dB)} = 10 \times \log(\frac{T_{\text{g}} - T_{\text{amb}}}{T_{\text{amb}}}) \tag{6.4}$$

where T_{ON} and T_{OFF} are the noise temperatures at the coupler output when the DUT is ON and OFF, T_{g} is the noise temperature generated by the DUT, C is the coupling factor, L_{fixt} is the insertion loss between the coupled port of the coupler and the DUT, and T_{amb} is the ambient temperature. This ratioed measurement does not require a noise receiver calibration and is insensitive to performance variations in the noise receiver.

The measured ENRs of the candidate devices at 50 GHz are shown in Figure 6.2 for various bias currents. All candidate devices exhibit a steadily increasing ENR with bias, and all devices except for the SiGe HBT emitter-base (EB) junction exhibit saturation at some point within the measurement range. The PIN diode and the SiGe HBT collector-base (CB) junction exhibit the highest measured ENR (27 and 28 dB, respectively) with a

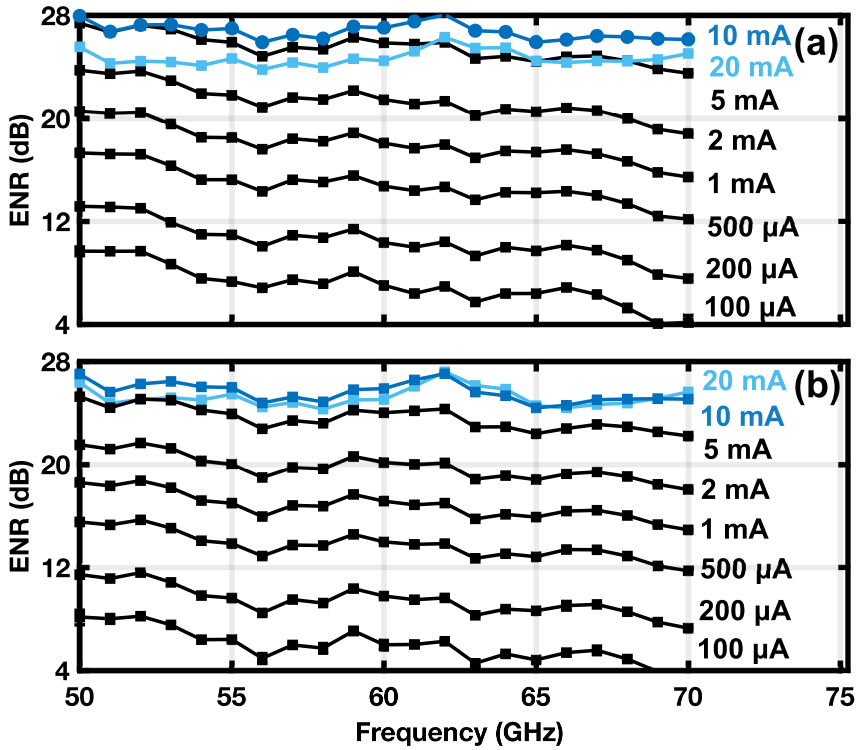


Figure 6.3: ENR of a) the PIN diode and b) the collector-base junction of a SiGe HBT (© 2021 IEEE).

monotonic slope versus bias at low currents and a stable ENR when biased near 10 mA. The high ENR of these devices is attractive—a fixed HOT calibration noise temperature can be injected into the radiometer receiver using weaker coupling than for a lower-ENR device, which reduces the impact of the ON-state versus OFF-state impedance mismatch on the receiver and therefore improves calibration accuracy. The PIN diode and the SiGe HBT CB junction were therefore selected for further consideration. The measured ENRs of these devices across 50 – 70 GHz at multiple bias currents are shown in Figure 6.3. At low bias currents, both devices exhibit an ENR reduction of 5 dB across the band; However, near saturation, the total across-band ENR variation is 3 dB for the SiGe HBT CB junction and 2 dB for the PIN diode. The breakdown voltages of the SiGe HBT CB junction and PIN diode are 6 and 6.7 V, respectively. Figure 6.4 shows the impedance variations of the PIN diode and the SiGe HBT CB junction across different bias currents and over frequency.

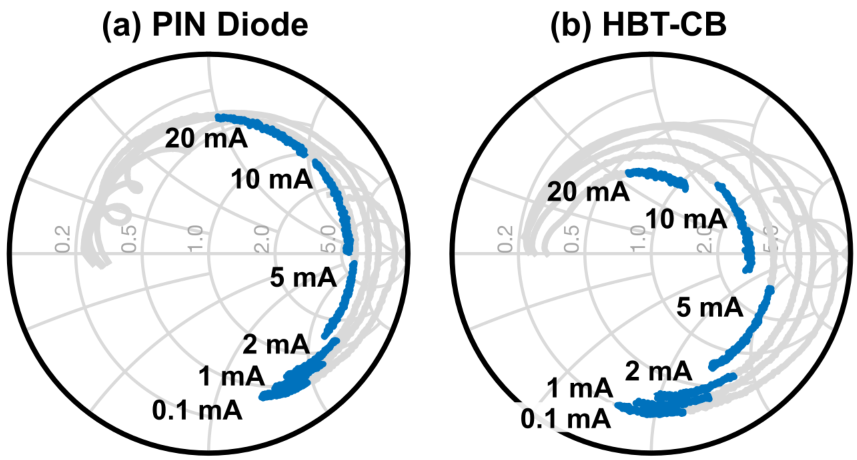


Figure 6.4: Impedance of a) the PIN diode and b) the CB junction of the SiGe HBT for different bias currents from 0.1 to 20 mA. Gray and blue curves show the impedance across 10 MHz – 50 GHz and 50 – 70 GHz, respectively (© 2021 IEEE).

6.2 Reliability of On-Chip Noise Sources

Since satellite-based radiometers are often employed for long-term missions, the reliability of noise sources should to be examined. In particular, noise sources should maintain the same noise characteristics between calibrations and repeated use. These noise sources are operated in the avalanche region, which generates high-energy electrons and holes in the PN junction, commonly referred to as hot carriers. Such hot carriers can damage the interface of isolation oxide, which are ubiquitously used in semiconductor processing. The damage shows up as generation-recombination (G/R) centers that are associated with increased leakage current in PN junctions. If the same voltage is used in the avalanche process, after some period of time, the number of G/R centers will saturate, and any further avalanche process will not create additional G/R centers. In short, the noise source performance should reach a steady-state condition after electrical stressing.

To characterize how the leakage current and ENR change over time, the noise source was reverse biased with 20 mA bias current to accelerate the aging mechanisms, and the ENR was recorded over a duration of 25,000 seconds. The recording was interrupted at fixed time steps to record the leakage current at low forward bias. Figure 6.5 shows the

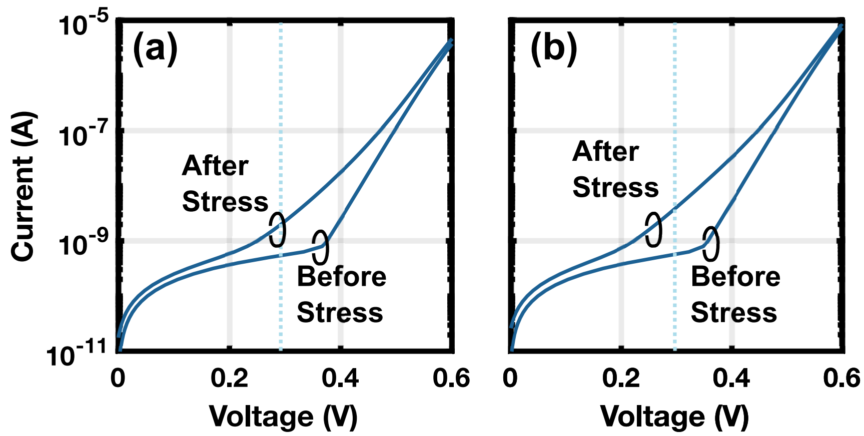


Figure 6.5: Forward I-V curves before and after 25,000 seconds of operation in the avalanche region for a) the PIN diode and b) the CB junction of the SiGe HBT (© 2021 IEEE).

forward I-V curves of the PIN diode and CB junction of the SiGe HBT, both before and after 25,000 seconds of operation in the avalanche region. To observe the rate of changes in the device, Figure 6.6(a) shows the ratio of the leakage current at 0.3 V to the initial leakage current at the same bias. The leakage current of the PIN diode increases by a factor of 6 and reaches a saturation in the first few hundred seconds, whereas the CB junction of the SiGe HBT requires a longer period of time to reach this state. In addition, Figure 6.6(b) shows the standard deviation of eight ENR measurements at each time step. There is no significant change considering that the lab environment (temperature and humidity) is not tightly controlled.

These results clearly indicate the potential for using PIN diode and CB junction of SiGe HBTs as monolithic noise sources. Both noise sources provide high ENR values that are mostly constant across 25,000 seconds of operation when the device is biased with a forced current. To the best of authors knowledge, this is the first investigation of the consistency and degradation of on-chip noise sources over time and their reliability implications.

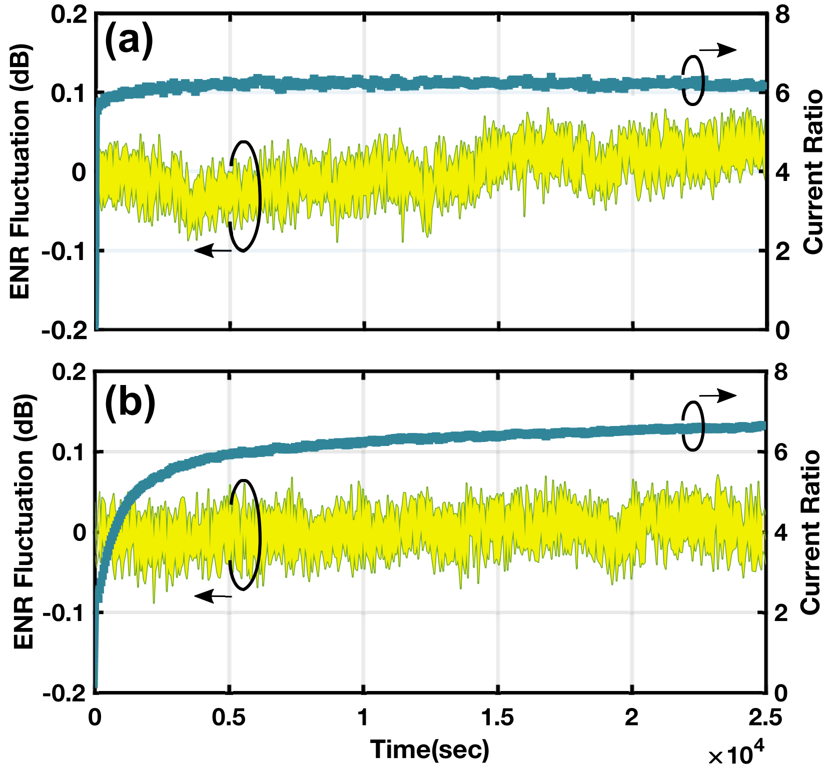


Figure 6.6: ENR fluctuations and current ratio at forward bias voltage of 0.3 V for a) the PIN diode and b) the CB junction of a SiGe HBT (© 2021 IEEE).

6.3 Calibration Switch Design

In this section, a novel implementation of a V-band single-pole double-throw switch is presented that facilitates the internal calibration of radiometers by integrating an ambient noise source and an avalanche noise source. As the time of designing this switch the PIN diode was not offered by the foundry, so the noise source was implemented using the CB junction of a SiGe HBT. Two HBTs with an emitter length of 18 μm were used in parallel to achieve a high noise output with a compact size. The base and emitter nodes were connected to ground, and the collector was used as the output node, so a positive voltage applies a reverse bias.

The circuit design is based on the quarter-wave shunt SPDT switch presented in [49]. A schematic is shown in Figure 6.7. Reverse-saturated SiGe HBTs Q1 and Q2 are used as the shunt switching elements; each was implemented using $0.13\,\mu\text{m} \times 12\,\mu\text{m} \times 3\,\mu\text{m}$

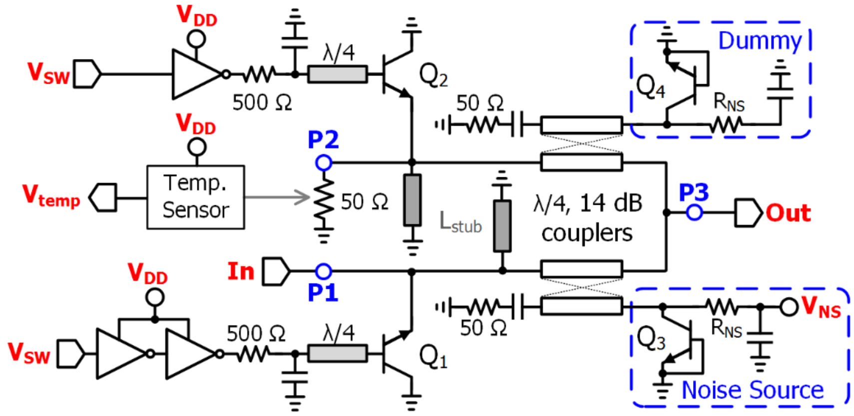


Figure 6.7: Schematic of the SiGe HBT calibration switch (© 2020 IEEE).

devices to balance the ON-state resistance (R_{ON}), the OFF-state resistance (R_{OFF}), and the capacitance (C_{OFF}). A shunt stub (L_{stub}) resonates the C_{OFF} for each switch cell. Each device is biased through a λ/4 microstrip line, and high-current CMOS inverters allow for the use of a single control bit, V_{SW}. When V_{SW} is low, Q2 creates a low R_{ON} at port P2, which presents a high impedance to the common port P3 through a λ/4 transmission line; meanwhile, Q1 presents a high R_{OFF} and creates a low-loss path between P1 and P3. The 50-Ω load connected to P2 serves as the ambient noise source. To ensure the calibration accuracy, a simple CMOS temperature sensor was placed directly under the load resistor.

The λ/4 transmission lines typically used between P1/P2 and P3 in this topology were replaced with a directional coupler, and the avalanche noise source described in Section II was connected as Q3. This coupler allows for noise injection with only a small increase in the size and insertion loss of the switch, while the weak coupling mitigates the unmatched impedance of Q3. Biasing is applied to Q3 through a 580-Ω R_{NS} to increase the nominal bias voltage to 15 V for the 5-mA bias current. An always-off Q4 is included on the reference path to ensure similar impedances are presented to each coupler. A small asymmetry is introduced when Q3 is ON, but the impact is negligible due to the weak coupling and the high impedance presented to P3.

The directional couplers were implemented using edge-coupled microstrip traces. The avalanche noise was modeled in Keysight's Advanced Design System (ADS) using the

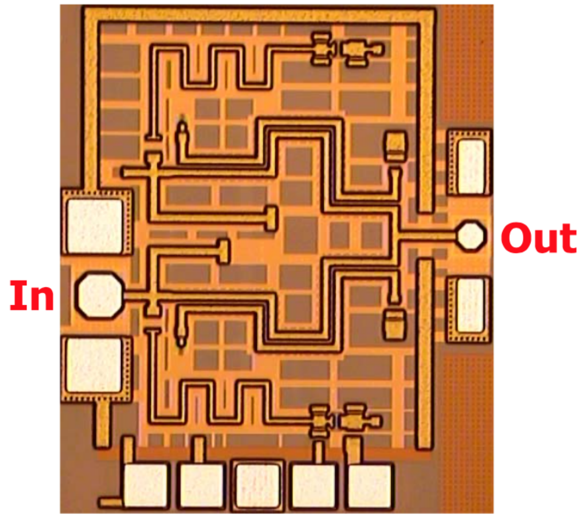


Figure 6.8: Die photograph of the fabricated calibration switch. The size of the chip is 0.77 mm × 0.90 mm, including pads (© 2020 IEEE).

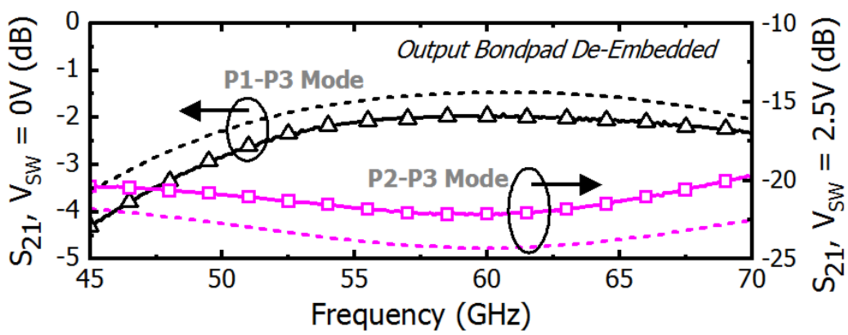


Figure 6.9: Measured (solid) and simulated (dashed) insertion loss and isolation of the switch (© 2020 IEEE).

measured impedance of the noise source along with an ideal 50-Ω resistor with a physical temperature of T_g. Frequency dependence of the noise was not modeled. An increase of 500–800 K in the effective input-referred noise temperature (T_e) was desired for calibration, and ADS simulations indicated that the optimal coupling factor to achieve an increase in this range was 14.0 dB. This coupling factor was achieved using a 10-μm separation between the signal traces. A photograph of the fabricated switch is shown in Figure 6.8. A large input bond pad was used to facilitate packaging, and a shorter L_{stub} was used with Q1 to resonate the extra signal pad capacitance. Small pads were used at the output for probing. The switch consumes 2.9 mA from the 2.5-V VDD.

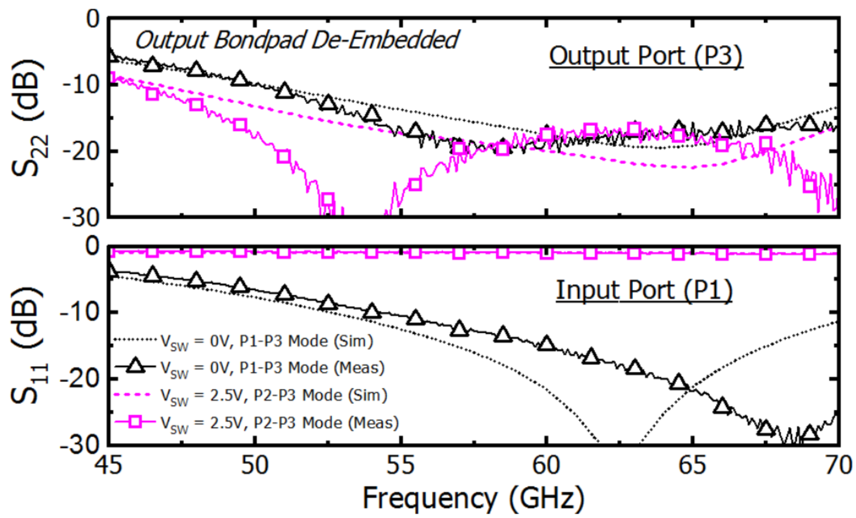


Figure 6.10: Measured (solid) and simulated (dashed) return loss of the switch (© 2020 IEEE).

6.4 Calibration Switch Measurement

The S-parameters of the switch were measured on-wafer to 70 GHz using an Agilent E8361C network analyzer. As shown in Figure 6.9, the measured insertion loss and isolation are 2.0 and 22 dB, respectively. Both parameters somewhat deviated from simulation, which is not unexpected, since the SiGe HBT compact models are not optimized for reverse-saturation biasing. Although the 2.0 dB insertion loss is higher than simulated, to the best of the authors' knowledge, this value is only 0.5 dB higher than that of the lowest loss reported 60 GHz Si-based SPDT switch [97] while adding additional functionality. Figure 6.10 shows that the return loss is better than 10 dB from 54 to 70 GHz. There was no noticeable difference in the return loss with the noise source ON versus OFF.

The Y-factor method, using a waveguide noise source connected to the input and an Agilent N9030A signal analyzer, was used to measure the Te of the switch with the avalanche source both ON ($T_{e,ON}$) and OFF ($T_{e,OFF}$). Figure 6.11 shows that the measured $T_{e,ON}$ and $T_{e,OFF}$ generally agree with simulation, although $T_{e,OFF}$ is higher than simulated due to the increased insertion loss compared to simulation. Although some fluctuations can be observed in $T_{e,ON}$ and $T_{e,OFF}$ due to imperfect calibration of the measurement setup, the

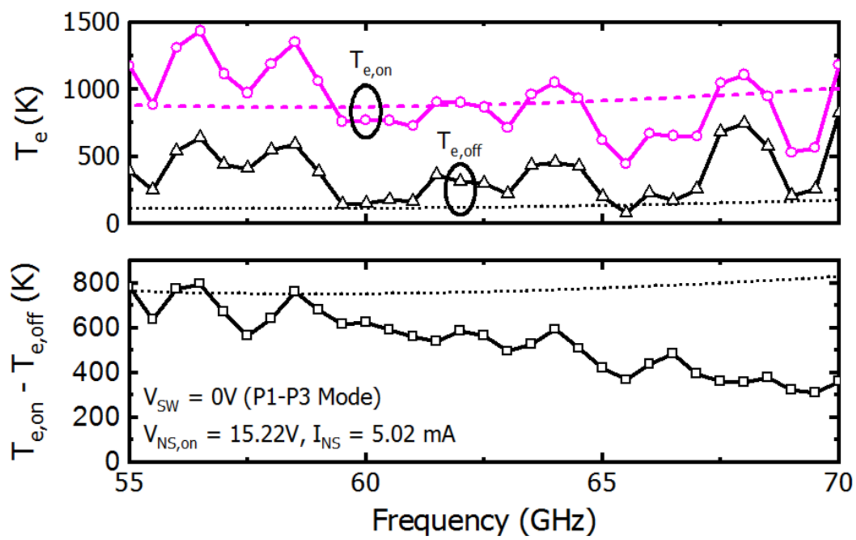


Figure 6.11: Measured (solid) and simulated (dashed) T_e of the switch versus frequency. The upper plot shows Te with the noise source OFF versus ON, and the lower plot shows the noise temperature increase due to the noise source (© 2020 IEEE).

difference $T_{e,ON}$ - $T_{e,OFF}$ steadily rolls off between 800 and 310 K across the band in a similar manner to the measured ENR in Figure 6.3. The added noise at 60 GHz is 620 K.

6.5 Summary

The noise performance and reliability of several on-chip p-n junctions were characterized to be integrated with a radiometer front-end and enable on-chip calibration. The p-i-n diode and the SiGe HBT CB junction exhibit the highest measured ENR (27 and 28 dB, respectively) with a monotonic slope versus bias at low currents and a stable ENR when biased near 10 mA. ENR values were consistent across 25000 seconds of operation when the device is biased with a forced current.

A novel SPDT switch with integrated ambient and avalanche noise sources for calibrating radiometers were presented. The avalanche noise source in the SPDT switch achieved an ENR of 18.7 dB at 60 GHz at the selected bias current. The switch achieves an insertion loss of 2.0 dB and has an excess T_e of 620 K when the noise source is turned on. This switch enables rapid and frequent internal calibration of V-band radiometers without compromising integration or sensitivity. To the best of our knowledge, this is the first reliability study of on-chip noise sources in a SiGe BiCMOS technology and the first use of a diode-configured SiGe HBT as an avalanche noise source. This work was published in *IEEE Journal of Solid State Circuits*, May 2021 [2], and *IEEE Microwave and Wireless Components Letters,* April 2020 [7].

CHAPTER 7
INTEGRATED RADIOMETERS

During the course of this research, building blocks of a V-band receiver for radiometry applications were designed, and novel circuit topologies were suggested to improve the overall radiometer performance. In this chapter, we go over the integrated implementations of this frontend and their measured performance.

Figure 7.1(a) shows an appropriate set of radiometer frequencies and bandwidths for constructing a temperature profilometer with five altitude bins [98], and Figure 7.1(b) shows the weighting functions for temperature measurements arising from this choice of center frequencies and bandwidths. This channelized approach lends itself naturally to a switched filter radiometer implementation. The block diagram of such a radiometer with single-sideband down conversion is shown in Figure 7.1(c), and it consists of a single-pole double-throw (SPDT) switch, a low-noise amplifier (LNA), an image-reject (IR) mixer, an IF amplifier, and a frequency multiplier. This receiver is designed to measure radiometry channels in the $56-69$ GHz range and down-convert them to a fixed-IF frequency (1 GHz). The down-converted signal goes through an off-chip filter bank to limit the bandwidth of target channels.

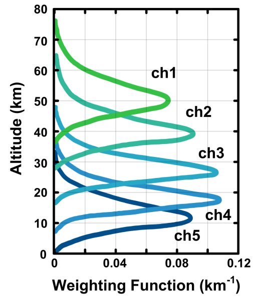
7.1 First implementation

The first implementation of this frontend includes an SPDT switch, an LNA, and an IR mixer, fabricated in GlobalFoundries BiCMOS 8XP technology, which offers 0.13 μm CMOS devices along with SiGe HBTs with peak f_T/f_{MAX} of 250/330 GHz. Regarding the SPDT switch, a shunt switch topology will yield lower insertion loss and higher isolation than a series switch at these frequencies. Therefore, the Dicke switch was designed using a quarter-wave shunt topology. Figure 7.2 presents the schematic of the Dicke switch,

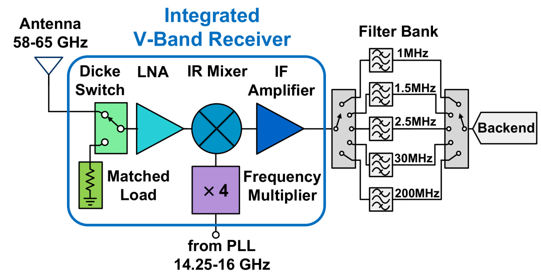
FREQUENCY CHANNELS FOR ALTITUDE WINDOWS

Channel No.	F_C (GHz)	BW (MHz)
1	60.4365	1
2	60.4409	2.5
3	58.388	30
4	60.82	200
5	64.47	200

(a)



(b)



(c)

Figure 7.1: a) an appropriate set of radiometer frequencies and bandwidths for constructing a temperature profilometer with five altitude bin, b) weighting functions for temperature measurements, and c) the block diagram of the SiGe receiver.

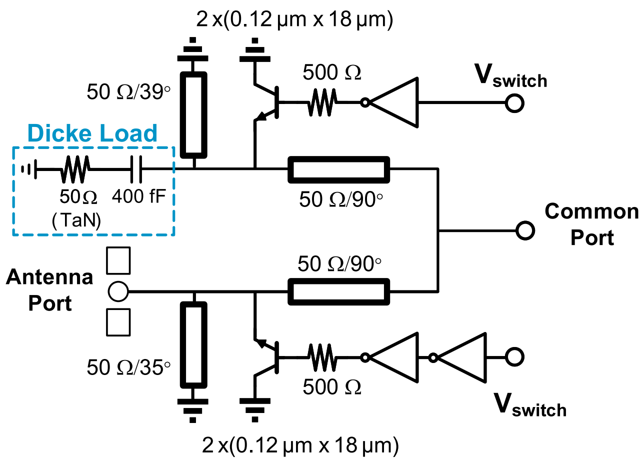


Figure 7.2: Schematic of the SPDT switch with reverse-saturated HBTs.

where shunt switches are realized with SiGe HBT devices in a reverse-saturated configuration. This configuration offers a higher off-state resistance because of the improved isolation from emitter to the conductive silicon substrate [49]. The parasitic capacitance of the switch HBTs is resonated out with shunt stubs. The matched load of the Dicke switch is realized with a 50 Ω TaN resistor. The switching signal is provided through digital inverters and is controlled with a single digital bit. Moreover, the maximum achievable isolation of the SPDT switch is limited by the total resistance from the switch transistor to the top metal layer. Therefore, isolation is independent of the technology node [99]: $S_{21} = 2R/(Z_0 + 2R) = -22\,\text{dB}$ for $R = 2\,\Omega$.

A three-stage low-noise amplifier was designed to achieve about 25 dB of gain across

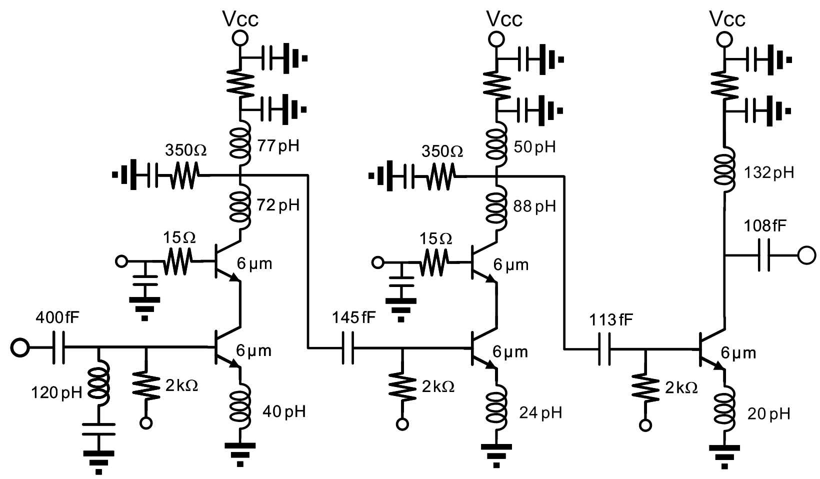


Figure 7.3: Schematic of the SiGe low-noise amplifier.

$56-69$ GHz, and its schematic is shown in Figure 7.3. The LNA is implemented using two high-gain cascode stages followed by a common-emitter output stage in order to achieve a wideband output match. The transistor sizes and degeneration inductors are designed to achieve a low noise figure (NF) with a simple input matching network that consists of a shunt inductor and a series DC blocking capacitor. The cascode transistors are biased at 0.7 mA/μm, rather than the peak-f_T bias point, to achieve a minimum noise figure of 3.8 dB and a gain of 9.5 dB at 60 GHz. Choosing the peak-f_T bias point in SiGe HBTs will not result in NF_{min}, since an increase in the bias current of the transistor will significantly increase shot noise. To avoid instability, a 15 Ω series resistor, and a shunt RC are placed in the base of the upper transistors and the output node of the cascode stage, respectively. The matching networks were realized using inductors and capacitors rather than transmission lines to facilitate a compact layout.

An image-reject mixer was designed to enable single-sideband down-conversion in the receiver. The schematic of the mixer is similar to the ones presented in chapters 3 and 4, configured in a double-balanced topology to reduce LO-to-IF feedthrough. Transformer baluns were utilized at the RF and LO ports to convert the single-ended LNA output and LO input to differential signals. A two-stage RC PPF with a perfectly symmetric layout was employed to generate matched quadrature LO signals and to achieve a high image

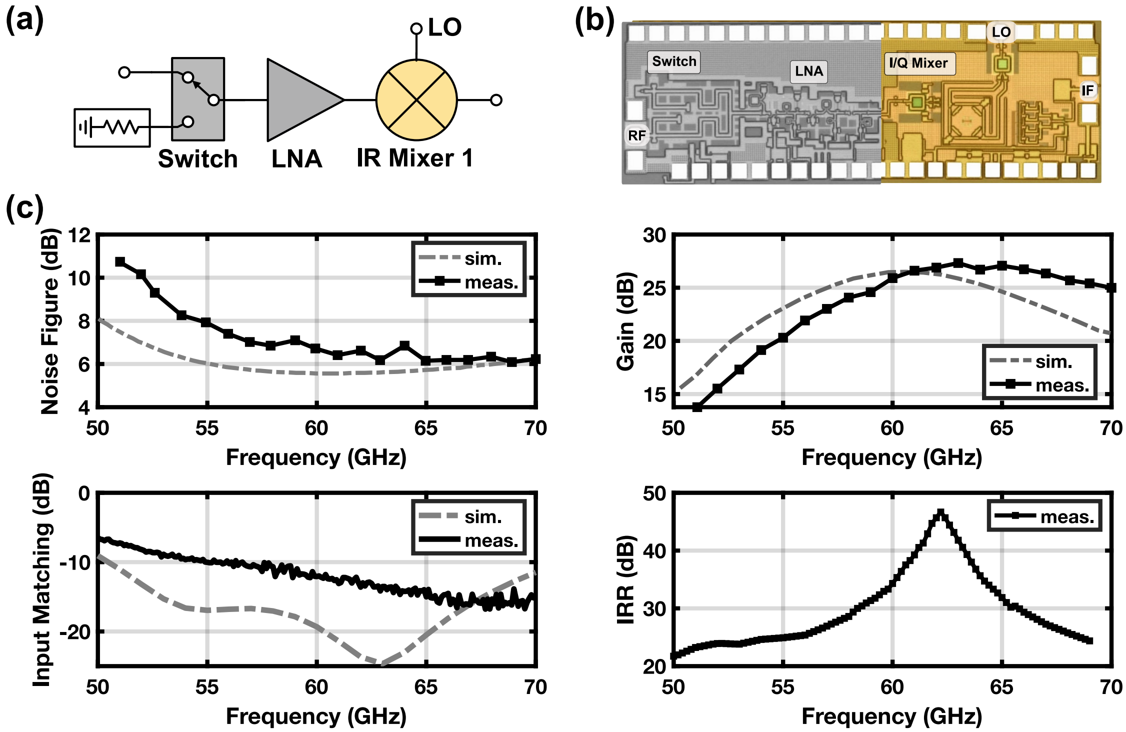


Figure 7.4: First integrated radiometer a) block diagram, b) die micrograph, and c) measurement data.

rejection ratio. A buffer stage follows the mixer to combine the differential IF signals. Figure 7.4 shows the radiometer block diagram, die photo, and measured performance. The chip occupies an active area of 2 mm^2 and consumes a total DC power of 63 mW from 1.5 V and 3 V supplies.

The fabricated chip was measured via on-chip probing, while DC bias pads were wire-bonded to a printed circuit board. The S-parameters were measured using an Agilent E8361C network analyzer, and the input port is matched with better than -12 dB reflection coefficient. For conversion gain measurements, the RF was provided from an Agilent E8257D signal generator, and a 12 dBm LO signal was generated by an OML S15MS source. The IF signal was captured using an Agilent E4440A spectrum analyzer, where the frontend conversion gain was higher than 25 dB for the desired band, and the mean NF was 6.5 dB. The mixer achieved an IRR of higher than 30 dB for 58 - 65 GHz, and the SPDT switch isolation was 19 dB.

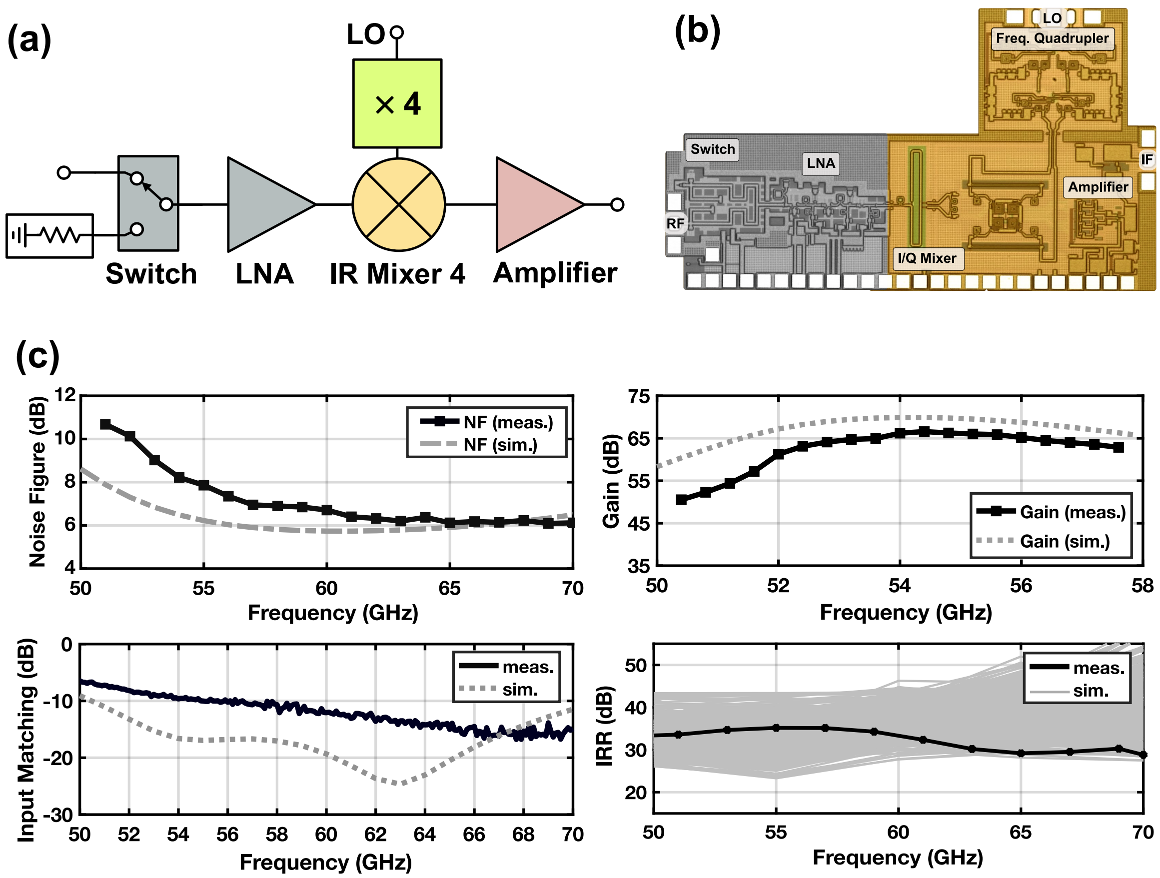


Figure 7.5: Second integrated radiometer a) block diagram, b) layout, and c) measurement data.

7.2 Second Implementation

The first receiver implementation satisfies most of the system requirements for CubeSat-based radiometry. But some techniques can be used to facilitate the integration of the overall system. For example, providing a high power (12 dBm) LO signal at the V-band frequency range can be challenging, and this was mainly due to the lossy RC PPF with a narrow image-rejection band. Chapter 4 provides insights into the effects of interconnects in mm-wave PPFs and how to enhance their performance. In order to reduce the loss of the quadrature LO generation network, the mixer was implemented with the topology presented in chapter 4, and it was integrated with two cascaded frequency doublers. The first frequency doubler is the same as the one shown in chapter 5, and the second one is a scaled version of that. After the mixer, a two-stage resistive-feedback amplifier was employed to provide 40 dB gain. The chip occupies an active area of 3.1 mm^2 and consumes a total DC power of 180 mW. Figure 7.5 presents the front-end layout and simulated vs measured RF performance. The NF and input matching are mostly the same the first implementation. But the required LO power was as low as -18 dBm at 14.25 - 16 GHz. The fabricated front-end achieves a conversion gain of 65 dB and an IRR of 30 dB across the desired frequency range. The performance of the receiver front-end is compared with state-of-the-art mm-wave Dicke Radiometers and receiver front-ends in Table 7.1. The receiver front-end achieves the lowest noise figure among similar Si-based Dicke radiometers. This design was presented in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, November 2018 [8].

Since the main application of this front-end circuit is for space-borne radiometry, the receiver/ radiometer performance was tested before and after being exposed to a dose associated with the LEO orbit. No significant change was observed in the RF performance metrics, such as noise figure, gain, and IRR.

Table 7.1: Performance Comparison of the state-of-the-Art mm-Wave Receiver Front-Ends and Dicke Radiometers (© 2018 IEEE)

Reference	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	SPDT IL (dB)	SPDT Iso. (dB)	Front-End Integration	Power (mW)	Area[a] (mm^2)
2010 TMTT [55]	0.12 μm SiGe BiCMOS	85−99	24.7	10.3	2.3	21	SPDT + LNA + Detector	34.8	0.4
2010 JSSC [54]	65 nm CMOS	82−93	27	11.2	4.2	25	SPDT + LNA + Detector	38.4	0.31
2011 JSSC [31]	0.18 μm SiGe BiCMOS	71−97	30	12	-	$\geq$5	SPDT + LNA + Detector + Baseband	200	12.5
2016 TMTT [34]	0.13 μm SiGe BiCMOS	93−105	43	8.4	0.93	18	SPDT-DA + LNA + Detector	28.5	3.42
2016 TMTT [100]	90 nm CMOS	60	20	9	N/A	N/A	LNA + IR Mixer + Rectifier + Auto Wake-up	49	0.82
2016 TMTT [101]	0.13 μm SiGe BiCMOS	71−76	70	<7	N/A	N/A	LNA + Mixer + Freq. Multiplier + VGA + Mixer + Synthesizer	650	6.1
2016 TMTT [102]	90 nm SiGe BiCMOS	71−86	26.4	7.6	N/A	N/A	LNA + Mixer + LO amplifier + IF amplifier + PA	138	1.35
This Work	0.13 μm SiGe BiCMOS	56−69	66	4.3[b]/6.1	1.8	18.9	SPDT + LNA + IR Mixer + Freq. Quadrupler + IF amplifier	180	3.1

[a] active area. [b] without the SPDT switch.

7.3 Third Implementation

With the development of 5G technologies at the mm-wave frequency range, mitigating RF interference around radiometry frequency bands could be very challenging because the black body radiations of the atmosphere have much lower power than the communications signals. After the allocation of 5G mm-wave bands, we decided to re-design some of the radiometer blocks and use alternative radiometry channels which would be more robust against 5G RF interference. As a result, the radiometer frontend has to cover 50 - 58 GHz (shown in Figure 1.2), and this opportunity was used to improve some of the key specifications of the final implementation. The first and second integrations of the radiometer used a $\lambda/4$ SPDT switch, followed by an LNA, and achieved a NF of 6.3 dB, whereas in the third implementation, the radiometer was designed based on the transformer-based switch and differential LNA of chapter 2 to achieve a NF of 5 dB. Employing the latter design can reduce the noise temperature of the frontend from 890 K to 590 K. Furthermore, the IR mixer of Figure 3.21(a) and Figure 3.24(a) was modified and used in this implementation to obtain a higher IRR and a lower insertion compared to the previous variants.

The Gilbert FD was designed in the early stages of our research to provide 12 dBm output power for the IR mixer with high loss in the LO generation network. However, after developing low-loss quadrature signal generation networks, only 0 dBm LO power was needed to saturate the LO port and desensitize the conversion gain to LO power fluctuations. As a result, we designed a low-power frequency quadrupler (FQ) to reduce the overall DC power consumption of the receiver. The previous variants require differential LO inputs where the IRR was strongly affected by the input phase and amplitude errors. Therefore, we decided to use an on-chip balun with fixed and optimized phase and amplitude errors rather than power-level-dependent errors.

This FQ was implemented with two cascaded push-push FDs. The harmonic component of collector current in a push-push FD is a function of conduction angle, the input

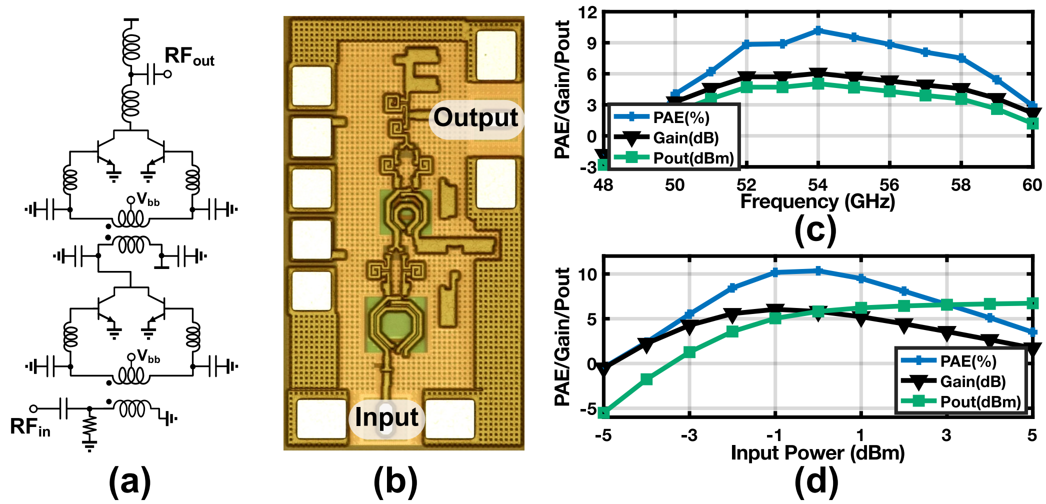


Figure 7.6: Class-C push-push frequency quadrupler: a) schematic, b) die micrograph, c-d) measurement results.

driving power, and the base bias point. If the collector current of a push-push FD is modeled as a train of rectified cosine pulses, the Fourier series of the collector current can be represented as [103]

$$I(t) = I_0 + I_1 \cos(\omega_o t) + I_2 \cos(2\omega_o t) + I_3 \cos(3\omega_o t) + ... \tag{7.1}$$

where I_n is the nth harmonic component and

$$I_0 = duty\,cycle \times \frac{4}{\pi}, \tag{7.2}$$

$$I_{2k} = \frac{8}{\pi} \times duty\,cycle \left| \frac{\cos(n\pi \times duty\,cycle)}{1 - (2n \times duty\,cycle)^2} \right|, \tag{7.3}$$

and

$$I_{2k+1} = 0. \tag{7.4}$$

Based on these equations, the second harmonic component is maximized with a duty cycle of 32% for each transistor, which leads to a 2nd-harmonic Fourier coefficient of 0.74. We designed a frequency quadrupler, as shown in Figure 7.6, in which the transistors are biased

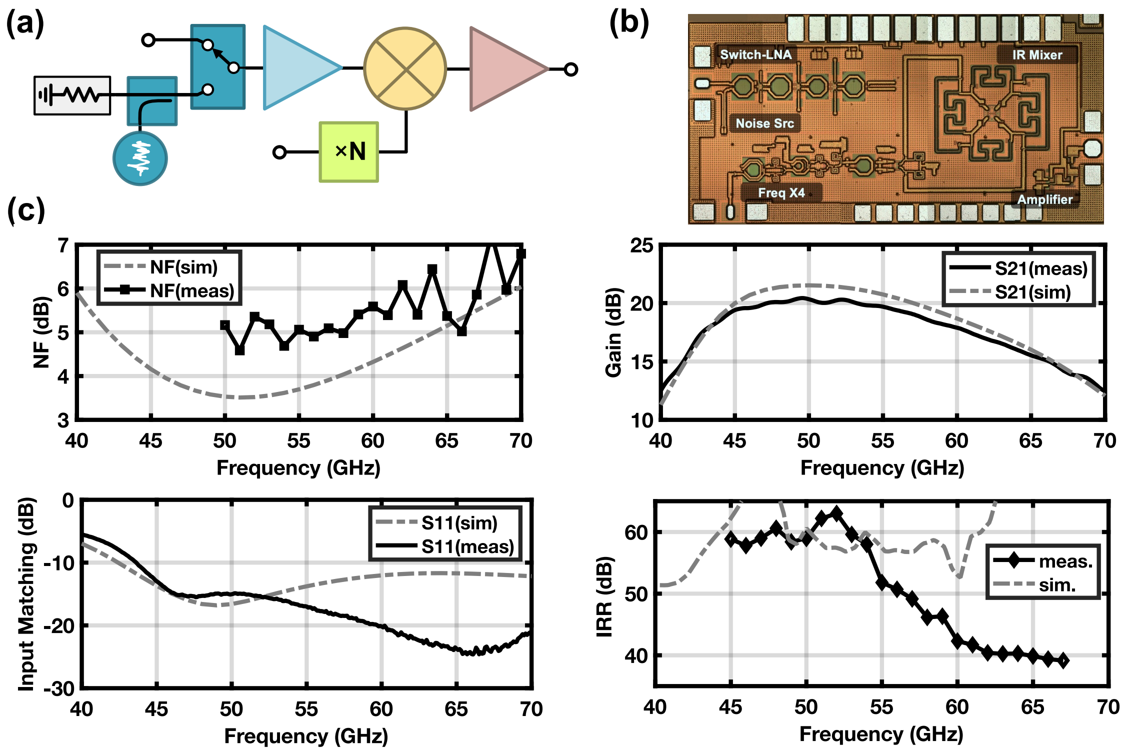


Figure 7.7: Third integrated radiometer a) block diagram, b) die micrograph, and c) measurement data.

in class-C (32% duty cycle) to maximize the 2nd-harmonic component in each of the push-push doubler stages. The FQ achieves a peak saturated output power of 6 dBm and a peak PAE of 10.4%, the highest reported value among state-of-the-art frequency quadruplers.

Figure 7.7 shows the block diagram, die micrograph, and simulated/measured performance of the third radiometer. This design occupies a chip area of 1.8 mm^2 and consumes 45 mW of DC power. The input ports are matched with better than -12 dB reflection coefficient, and the mean NF is 5 dB across 50 - 58 GHz. The frequency quadrupler is followed by a differential pair amplifier as an LO buffer to reduce the impedance mismatch reflections. Similar to the IR mixer presented in chapter 3, both designs had a common-centroid layout for the LO signal generation network. However, the IF PPF in this design is also drawn symmetrically under the ground place, whereas the previous design had some asymmetry (see Figure 3.14(b)). As a result, the frontend achieves an IRR of above 50 dBc, 20 dB better than the previous one. Overall, the final integration has a superior performance compared to the previous implementations.

CHAPTER 8

CONCLUSION

8.1 Summary of Contributions

The research presented in this dissertation was focused on investigating the design challenges of quadrature receivers for remote sensing and developing novel and high performance circuits. Below is the summary of contributions:

1. A low-noise radiometry front-end was demonstrated in which the Dicke switch was co-designed with the low-noise amplifier (LNA). The switch incorporates a transformer-based topology and serves as the input matching network of the LNA. This topology is configured to minimize the amplifier gain mismatch between the two switching states caused by process variations while providing a low noise figure (NF). The circuit is implemented in a 0.13μm SiGe BiCMOS technology, and it achieves more than 20 dB gain and minimum NF values of 4.5 and 0.58 dB at 300 and 20 K, respectively. It consumes a dc power of 15 mW. The front-end switch presents a peak isolation of 17 dB, and the input return loss is better than 15 dB across 45 - 70 GHz. This work was presented in *IEEE Radio Frequency Integrated Circuits*, August 2020 [1], and published in *IEEE Journal of Solid State Circuits*, May 2021 [2].

2. A broadband low-loss quadrature-hybrid-based network was presented that enhances the phase and the amplitude matching of quadrature signals. The performance of this network was investigated, and a detailed theoretical analysis is provided. Several stages of this network can be cascaded to generate broadband balanced quadrature signals. Each stage has a loss of 0.5 dB and enhances the image rejection ratio (IRR) by approximately 8 dB. Compared to conventional polyphase quadrature signal generation methods, this network enables lower insertion loss, wider bandwidth,

and reduced sensitivity to process variations. To verify the theoretical analyses, two proof-of-concept image-reject mixers are implemented in a 0.13 μm SiGe BiCMOS technology. The first mixer achieves an average IRR of 37.5 dB across $40-76$ GHz, whereas the second mixer achieves an average IRR of 33.5 dB across $40-102$ GHz. This network is a promising solution for broadband quadrature signal generation at millimeter-wave frequencies as it eliminates the need for calibration and tuning. This work was published in *IEEE Transactions on Microwave Theory and Techniques*, Dec. 2018 [3], and it is protected by the U.S. patent US10979038B2 filed on August 21, 2019 [4].

3. A dual-band millimeter-wave quadrature signal generation network was presented comprising an RC-CR polyphase filter (PPF) and two quarter-wave coupled-line couplers. A common-centroid layout is suggested to improve the phase and amplitude matching of quadrature signals. The effects of interconnects and parasitic capacitances on PPFs are investigated, and design guidelines are provided to achieve low insertion loss and broad bandwidth. A proof-of-concept image-reject mixer is implemented in a 0.13 μm SiGe BiCMOS technology, which achieves a mean image-rejection ratio of 34 dB over a wide frequency range of $36 - 100$ GHz. To the best of the authors' knowledge, this design achieves the widest bandwidth of any mm-wave mixer with a mean IRR above 30 dB, and accomplishes this without calibration or tuning. This work was published in *IEEE Transactions on Circuits and Systems II: Express Briefs*, Feb 2020 [5].

4. A Ka-band Gilbert frequency doubler (FD) was presented, in which the phase of the injected signal to switching transistors wass adjusted to maximize core conversion gain (CG) and power-added efficiency (PAE). It achieves a peak PAE of 26.2 % and a peak CG of 21 dB at 28 GHz, without any output buffer. The FD provides a saturated output power of 11.9 dBm, a 3-dB bandwidth of $22-36$ GHz, and a fun-

damental harmonic rejection of 32 dB. To the best of authors' knowledge, this FD achieves the highest CG and PAE among all reported Si-based FDs without output buffers. This work was published in *IEEE Microwave and Wireless Components Letters*, November 2018 [6].

5. The noise performance and reliability of several on-chip PN junctions were characterized, and two novel implementations of a V-band single-pole double-throw switch that facilitates the internal calibration of radiometers by integrating an ambient noise source and an avalanche noise source. High excess noise ratios of about 28 dB were achieved with a p-i-n diode the collector-base junction of a SiGe heterojunction bipolar transistor (HBT) at V-band frequency range. Moreover, a novel implementation of a V-band single-pole double-throw switch was presented that facilitates the internal calibration of radiometers by integrating an ambient noise source and an avalanche noise source. To the best of our knowledge, this is the first reliability study of on-chip noise sources in a SiGe BiCMOS technology and the first monolithic two-reference switch for calibrating millimeter-wave radiometers. This work was published in *IEEE Journal of Solid State Circuits*, May 2021 [2], and *IEEE Microwave and Wireless Components Letters,* April 2020 [7].

6. Several V-band receiver front-ends were designed and presented for space-borne atmospheric remote sensing. The receivers are implemented in a 0.13 μm SiGe BiCMOS technology and consists of a Dicke switch, an LNA, an image-reject mixer, a frequency multiplier, and an IF amplifier. The final implementation achieves a mean conversion gain of 20 dB, a minimum noise figure of 4.5 dB at 50 GHz, and a mean image rejection ratio of 40 dB. This chip consumes a total DC power of 45 mW and occupies an active area of 1.8 mm^2. This work was the first reported monolithic receiver front-end for atmospheric measurements across the V-band oxygen spectrum, and it achieves the lowest noise figure among similar Si-based Dicke radiome-

ters. One of these implementations was presented in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, November 2018 [8].

8.2 Future Work

During the course of this work, we identified several topics that could be further explored or implemented to improve the performance of existing integrated radiometer frontends.

1. A large constellations of CubeSat-based radiometers with high spectral resolution is needed to track the temperature changes of the atmosphere. For this aim, [104] has presented the advantage of differential-correlating radiometry, consisting of a front-end hybrid, two radiometers, and a digital correlator. The demonstrated prototype in [104] was implemented based on off-the-shelf RF components and did not have a small form factor, whereas the presented integrated circuits in this work can be leveraged to design a low SWaP-C differential correlating radiometer.

2. Chapter 7 investigates the noise and reliability performance of the PN junctions biased in avalanche mode. Furthermore, these noise sources should be integrated in a radiometer to enable on-chip calibration functionality. These noise sources can be leveraged to implement advanced radiometry topologies, such as noise-injecting radiometer, on a single chip.

3. One of the main challenges of radiometers is the gain fluctuations of the receiver over time, as discussed in detail in chapter 2. The transistors inside microwave amplifiers are usually matched to the input and output ports only at the operating frequency. Usually, the impedance of the biasing network at low frequencies does not affect the high-frequency performance as long as it does not cause oscillation. Since these gain fluctuations have a low-frequency nature, an analog circuit can be designed to

minimize these gain fluctuations. Different biasing schemes can be explored, and of course, some large off-chip capacitors will be needed.

4. With the increasing demand for higher data rates, communication systems at frequencies beyond 100 GHz are being developed. In order to enable advanced modulation schemes on such systems, quadrature signal generation network are needed. Chapter 3 presented such a system at V-band frequencies, but it can be easily scaled for higher frequencies, and we expect to achieve a higher performance with lower phase and amplitude errors in quadrature signals.

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