

**HYBRID MATERIAL AND DEVICE PLATFORMS FOR THE
NEXT-GENERATION INTEGRATED NANOPHOTONICS**

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The Academic Faculty

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**HYBRID MATERIAL AND DEVICE PLATFORMS FOR THE
NEXT-GENERATION INTEGRATED NANOPHOTONICS**

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To my parents, my sisters, and in memory of my grandfather, Ali.

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TABLE OF CONTENTS

ACKNOWLEDGMENTS	iv
LIST OF TABLES	ix
LIST OF FIGURES	x
SUMMARY	xvi
CHAPTER 1: PROLOGUE	1
1.1 Integrated Silicon Photonics	1
1.2 Applications of Silicon Photonics	4
1.3 Beyond Single-Layer Silicon	7
CHAPTER 2: THEORETICAL BASES AND FUNDAMENTAL RELATIONS	11
2.1 Dynamics of Electromagnetic Waves and Fields	11
2.2 Optical Waveguides: Modal Analysis and Characteristic Relations	16
2.3 Integrated Microresonators and Microcavities	22
2.3.1 Properties of Integrated Microcavities	24
2.3.2 Coupled Mode Theory in Waveguide Coupled Microcavity Structures	30
CHAPTER 3: DOUBLE LAYER SILICON MATERIAL PLATFORM FOR RECONFIGURABLE AND PROGRAMMABLE INTEGRATED PHOTONICS	37

3.1	Tunable and Reconfigurable Integrated Silicon Photonics	37
3.2	Double Layer Crystalline Silicon Material Platform	40
3.3	Platform Development	42
3.3.1	Optimization of Thermal Oxidation	43
3.3.2	Hydrophilic Bonding and Backside Etching	45
3.4	Proof-of-Concept Devices in The DLSi Platform	47
3.4.1	Fabrication and Characterization of High- Q Microresonators	48
3.4.2	Tunable Compact Microresonator for Reconfigurable Photonics . .	52
 CHAPTER 4: VERTICAL INTEGRATION OF SILICON INTO SILICON NITRIDE PLATFORM		 56
4.1	Cointegration of Silicon and Silicon Nitride	56
4.2	Crystalline Silicon on Silicon Nitride Material Platform	59
4.2.1	SON Platform Development	60
4.3	Design of an Adiabatic and Broadband Interlayer Coupler	64
4.4	Demonstration of Broadband, Compact and High- Q Functionalities in Si- on-SiN Material Platform	68
4.4.1	Passive Device Fabrication	68
4.4.2	Demonstration of Ultra-Low-Loss Interlayer Coupler	69
4.4.3	Demonstration of 3D Optical Path and High- Q Functionality	72
 CHAPTER 5: ACTIVE ELECTRO-OPTICAL DEVICES IN SILICON-ON- SILICON-NITRIDE PLATFORM		 75
5.1	Design and Optimization of Ion Implantation Plan for Active Functionality in the SON Platform	75

5.2	Rapid Thermal Annealing: Feasibility Study and Demonstration in the SON Platform	83
5.3	High Speed, High- Q Resonant Coupling Modulation in the SON Platform .	87
5.3.1	Device Architecture and Fabrication	89
5.3.2	Thermal, DC and High-Speed Characterization	93
5.3.3	Discussion	98
CHAPTER 6: EPILOGUE		101
6.1	Future Works	101
6.2	Achievements and Contributions to the Field	103
REFERENCES		107

LIST OF TABLES

1	Performance metrics of various active device architectures utilizing high-speed plasma dispersion effect for electro-optic modulation.	77
2	Summary of design parameters and computed ion dose and energies for realization of vertical PN junction on heterogeneous material platforms. . .	81
3	Output power amplitude of 8 pairs of interlayer hybrid coupler integrated in SON platform for different RTA temperature treatments.	85

LIST OF FIGURES

1	(a) Cisco VNI forecasts per month of IP traffic by 2020 [17]. (b) SiP growth forecast [18].	4
2	3D schematics of an integrated (a) fully-etched waveguide, and (b) partially etched waveguide on Si substrate.	16
3	(a) Adaptive mesh generated by COMSOL software to compute a single-mode integrated photonic waveguide. The guiding structure is composed of silicon nitride (WG region), SiO ₂ (Substrate region), and air (Cladding region). (b) and (c) depict the average power (Poynting vector) profiles of localized states supported by the geometry. The computed effective refractive indices are 1.5768 and 1.5205 for (b) and (c), respectively. Note the discontinuity in profiles at interfaces: where power is primarily carried by E_x (H_x) field component, the profile discontinuity is located at interfaces along y (x) dimension.	18
4	Cross-sectional profiles of electric and magnetic field components for the TE mode of the single-mode waveguide. The unit for \mathbf{E} and \mathbf{H} components is arbitrary, yet meaningful comparatively. The image confirms that E_x - H_y pair dominate the mode profile.	20
5	Cross-sectional profiles of electric and magnetic field components for the TM mode of the single-mode waveguide. The unit for \mathbf{E} and \mathbf{H} components is arbitrary, yet meaningful comparatively. It is clear from the image that E_y - H_x pair dominate the mode profile.	20
6	Diagrams of TE (blue) and TM (magenta) (a) effective mode index dispersion and group index dispersion in the single-mode silicon nitride waveguide. (b) Group velocity dispersion of the corresponding waveguide. According to the definition of GVD parameter, the negative D_λ corresponds to normal dispersion.	22

7	Computed whispering gallery modes of a typical Si microring resonator. White circles indicate inner and outer edges of the microcavity. Top row shows the average power flow in the ϕ direction, and the bottom row shows the dominant E_z component of each mode. Out of several modes of the structure, the 1 st , 4 th , and 7 th radial TM modes are depicted.	23
8	(a) 3D schematic of an integrated microring resonator with an access waveguide. (b) The cross-sectional representation of the microring resonator in the ϕ -z plane.	25
9	Profiles of TE ₁ , TE ₂ , TE ₃ , and TM ₁ modes for the silicon nitride microring, from the top to bottom respectively. The left column shows the average power (Poynting vector) distribution and the right column depicts the dominant electric field component (E_r or E_z) of each mode.	26
10	(a) Schematic of a typical directional coupler. (b) Top view of a typical waveguide-coupled microring resonator. The extended coupling length between access waveguide and microresonator can enable coupling to different radial mode orders.	31
11	Computed spectral response of a typical resonator. The intrinsic (Q) is 2×10^3 . (a) Power transmission response of an under-coupled, over-coupled and critically coupled structure. (b) Corresponding transmission phase response in each regime near a resonance wavelength.	35
12	(a) 3D schematic of an integrated single-mode waveguide in the proposed DLSi platform. (b) and (c) Poynting vector distribution profiles of the TM and TE modes, respectively. The insets depict the dominant electric field component (E_y and E_x , respectively), for each mode. In simulations, the thickness of Si layers, the interface oxide, and the width of the waveguide are 110 nm, 60 nm, and 500 nm, respectively.	41
13	3D schematic of the process flow to develop DLSi platform. (a) A pair of SOI dies with the same size are diced out of an SOI wafer (b) A thin layer of oxide film (30 nm) is grown on Si through thermal oxidation. (c) Assisted by pressure at an elevated temperature, dies are fused in one. (d) Schematic of the bonded platform after removing the substrate Si and the BOX layers from the backside of the top SOI die (Die I).	42

- 14 Ellipsometry and AFM measurements of a(n) (average) 31.5 nm SiO₂ layer thermally grown over two Si wafers in two separate runs: Run 1 ((a) and (c)), and Run 2 ((b) and (d)). The roughness is visibly higher in the Run 2, which has higher non-uniformity over the thickness. For AFM, the phase response of the probe is used to reveal topographic features, since the phase shift is proportional to the amount of inelastic energy transferred from the tip to the sample surface. Such local energy dissipation can be related to surface chemistry changes, visco-elastic changes, and topography changes. 45

- 15 (a) Optical micrograph image of a DLSi sample. Channels are etched in the bottom SOI layer prior to bonding to reduce void formation, which will be discussed in detail in the next Chapter. As can be seen in the microscope image, the bonding yield is close to 100% visible void formed. (b) Cross-sectional SEM of the processed DLSi platform. By precise control of the fabrication processes, the thickness of the developed heterostructure has met the target values within 1.5 nm margin. 47

- 16 (a) Bird's-eye SEM view of a DLSi waveguide structure at the facet of the chip (the tilt angle is 60 degrees). (b) Cross-sectional SEM of an etched and FOx-coated DLSi waveguide. The thickness of SiO₂ interface layer is reduced to 30 nm in the platform development. (c) Cross-sectional SEM of an etched DLSi waveguide with 60 nm oxide layer. 49

- 17 (a) SEM image of a waveguide-coupled single-mode ring microresonator (R = 10 μ m) fabricated in the DLSi platform. (b) The spectral response of a 10 μ m radius multimode microring (ring width = 3 μ m) for the TE polarization. The waveguide width is 500 nm, and the waveguide cavity gap is 120 nm. (c) The transmission spectrum for the resonance marked in (b) with the black dashed ellipse. The red curve shows a Lorentzian function fitted to the experimental data, which confirms $Q_i = 2.35 \times 10^5$ 51

- 18 Reconfigurable resonance in a DLSi microdisk resonator (R = 3 μ m) by free carrier accumulation. Voltage is changed from 0 to 20 V in 5 V increments. 54

- 19 Summary of the SON platform fabrication process. (a) Piece 1, an SOI piece. (b) Dry thermal oxidation reduces the Si thickness. (c) Wet etching of SiO₂ followed by the second dry oxidation. (d) Piece 2, a bare Si piece, goes through oxidation to grow 5 μ m of SiO₂. (e) An LPCVD SiN layer is deposited, followed by the deposition of a 30-nm SiO₂ layer using ALD. (f) Vent channels are introduced using optical lithography, dry etching of SiN, and wet etching of bottom SiO₂ layer. (g) Two pieces are bonded using a low-temperature hydrophilic bonding method. (h) Backside removal of the Si substrate followed by wet etching of the BOx layer. 61

20	AFM images from the surface of a 30-nm SiO ₂ layer on SiN, deposited by (a) HSQ annealing, average surface roughness (R_a) is 2.39 Å; (b) ALD, R_a = 3.83 Å; (c) PECVD, R_a = 7.45 Å.	62
21	(a) Top view of a void-free bonded SON piece under optical microscope. Lines represent vent channels. (b) The cross-sectional SEM of a typical vent channel after bonding process. (c) A bonded sample at the edge where the vent channels are terminated. Bubbles can be clearly seen in the area without vent channels, while the channeled area is void-free.	63
22	(a) The schematic of the proposed coherent vertical tapering method. (b) The crosssectional image of the electric field profile along the length of a 30-um coherent vertical coupler; the inset is the top-view image of the coupler and the dashed line indicates the cross-section surface.	66
23	3D FDTD simulation of the transmission efficiency for the adiabatic inter-layer coupler with coherent tapering technique.	67
24	Schematic of the device fabrication process on the SON platform. (a) The first pattern is transferred to HSQ using an EBL machine. (b) The Si device layer is etched to transfer the pattern. (c) The second pattern is transferred to ZEP using the EBL machine. (d) The interface SiO ₂ layer and SiN layer are etched to define the aligned second pattern on SiN. (e) False-colored crosssectional SEM of a waveguide defined in Si layer of the SON platform.	69
25	(a) Colorized SEM of the adiabatic coherent vertical coupler; (b) Colorized SEM of the compact vertical coupler. (c) The experimentally measured (solid line, magenta) and theoretically calculated (dashed line, blue) spectra of the coupling efficiency of the adiabatic vertical coupler, and (d) the experimentally measured (solid line, magenta) and theoretically calculated (dashed line, blue) spectra of the coupling efficiency of the compact vertical coupler. The shaded areas in (c) and (d) mark the regions outside the bandwidth of the access input/output gratings.	71
26	(a) A schematic of the hybrid optical path with SEMs of constituent elements in the path. (b) The transmission spectrum of a 60 um radius multimode ring resonator fabricated on the SON chip. (c) The transmission spectrum of the same SiN resonator fabricated on the inspection SiN chip. As depicted in the inset figures, the highest intrinsic quality factor in each platform is measured to be $Q_{int} = 3 * 10^6$. In both measurements, the spectrum is limited by the input/output grating bandwidth (Si gratings in (b) and SiN gratings in (c)).	74

27	(a) Ion implantation plan for PN junction realization in a Si waveguide with pedestal. Each number refers to an ion implantation step introducing a donor or acceptor material. (b) Computed power flow profile cross-section of the Si-rib waveguide in the heterogenous Si/SiO ₂ /SiN (SON) material platform.	79
28	(a) Computed ion range profile: (a) for phosphorous dopant at 40 keV, (b) for arsenic dopant at 320 keV. The 20 nm ALD SiO ₂ is included in the simulation, which is originally added for anti-channeling at zero-degree implantation.	80
29	(a) SEM image of an opening on PMMA resist exposed at 700 uC/cm ² , (b) same pattern with 800 uC/cm ² exposure dose. The width of opening is 4.1 um in the design.	82
30	Optical micrograph images of a compact R = 3 um disk and a large R = 90 um ring, before and after RTA treatment. Morphing of different implanted areas into a single color is visible.	87
31	(a) 3D schematic of the resonant device with a hypothetical time-varying coupling coefficient. $k(t)$ represents the field coupling coefficient from the resonator to waveguide. (b) Output power transmission as the function of k for three different Q values of a typical integrated resonator. Notice the sharp transition of transmission at low k values as Q increases.	88
32	(a) Heterogeneously integrated modulator structure. (b) Computed dynamics of the transmission response with the phase change in the Si waveguide. In the simulations, Q is increased to $5 * 10^5$ to demonstrate high efficiency of the modulation as Q increases.	91
33	SEM micrographs of a 20 nm ALD SiO ₂ on top of Si etched with the Cl ₂ -based recipe. The surface is visibly rough after etching with above 10 nm variation of the etching profile over the sampled area.	92
34	The dark-field micrograph image of the fabricated modulator. Si can be differentiated from SiN due to their different reflected color spectra.	93
35	Thermal response of the hybrid coupling modulator. At an appropriate bias point (1610.75 nm for the specified azimuthal order), more than 10 dB extinction is recorded.	94
36	(a) DC electro-optical characterization of the integrated heterogenous modulator. The blue shift of the resonance confirms the free carrier dynamics of the change in effective phase of Si waveguide. (b) Measured DC i-v curve of the PN junction diode integrated inside the Si waveguide.	95

37	The schematic of the high-speed measurement setup. Blue elements denote optical path and the orange denotes the electrical path and power.	97
38	(a) Measured eye diagram of PRBS (2^7-1 pattern) at 10 Gb/s. It is important to mention the rise-time and fall-time suggesting the possibility of higher bit rates for the device. (b) The measured EOE S_{21} of the modulator after direct detection. The curve is normalized to S_{21} value at 1 GHz.	98
39	The schematic of an integrated Tb/s interconnect based on Kerr frequency comb generation in a SiN microcavity and high-speed resonant modulation utilizing plasma dispersion effect of Si. Each resonator acts as an add-drop filter and modulator simultaneously. The blue layer is SiN, and the red layer denotes Si.	102

SUMMARY

Silicon (Si) has received great attention in the past century to build advanced electronic devices and systems, which continues to this date. Owing to its mature integration technology in the microelectronics industry, Si has been extensively used in the past two decades to demonstrate various photonic applications, especially in the optical signal processing, sensing, and light-matter interaction areas. However, Si hits a limit in several key features to address the ever-increasing demands of photonic integrated circuits. The objective of this Ph.D. research is to investigate and develop new heterogeneous material and device platforms beyond single-layer silicon (Si) to enable novel functionalities not otherwise feasible in Si-based integrated nanophotonic devices and systems. In particular, CMOS-compatible integration of ultra-low-loss silicon nitride (SiN) into Si platform has been pursued to reduce linear optical loss, enable high-quality microresonators, improve optical power handling, support various nonlinear phenomena, and thus enable the next-generation of integrated electro-optical nanophotonic devices on a single hybrid-Si chip.

The intellectual merit of the demonstrated discipline is in the platform build-up, device design and corresponding fabrication techniques. As will be discussed in detail, the SiN platform offers superior performance metrics in a large set of integrated photonic applications, and its proper integration into Si platform is of theoretical interest and practical merit. The broader impact of this work would include, but is not limited to, offering a universal method for dense integration of different materials, such as III-V compounds, into Si to enable coherent light generation and efficient detection. Since the envisioned optical fabrication method is a CMOS-compatible fusion bonding technology, it can be readily transferred to other materials, devices, and systems to be integrated with Si on a single chip.

With the successful demonstration of passive device functionalities in the heterogeneous platform, including a record low-loss and broadband interlayer coupler, an ultrafast

and low power electro-optic modulator is designed and demonstrated to showcase the performance of an active photonic device. Considering the increased quality factor of the cavity, coupling modulation is employed to remove the cavity lifetime limit of modulation, whose successful demonstration is confirmed through the high-speed RF photonic characterization of the fabricated device. The further integration of advanced electronic circuitry into the multi-material platforms can revolutionize the Si photonics to support compact, high efficiency, and low-power integrated devices and systems.

CHAPTER I

PROLOGUE

1.1 Integrated Silicon Photonics

Silicon photonics (SiP), the study of photonic systems which use silicon (Si) as the main optical medium, offers an unprecedented level of control over the flow of light and its properties at the chip scale [1-3]. From a chronological point of view, the free-space and fiber optics set the stage for the emergence of integrated photonics. Fundamental theories governing the light and its interaction with the matter were developed in the free-space optics over the course of several centuries. Later, the fiber optics offered a practical solution for the efficient localization and transmission of light using ultra-pure silicon dioxide (SiO_2) as the core material, which enabled long-haul—i.e., hundreds of kilometers, data transmission and led to the emergence of fiber optic networks, among other important applications. The availability of optical fibers also played a key role in the perception and demonstration of several fundamental nonlinear optical phenomena, including stimulated Raman and Brillouin scattering [4,5], optical parametric amplification (OPA) [6], and Kerr soliton formation [7]. Upon successful demonstration of systems based on enabling features of fiber optics, such as fiber optic networks, the demand for faster, more compact, and more efficient devices and systems has been ever increasing, which in turn requires reliable and inexpensive technologies for the implementation of photonic components. Even to this date however, many optical components are usually built independently using different technologies, such as free-space, fiber-based, and thin-film technology. The

implementation of photonic systems with such methodology usually leads to bulky structures that are expensive and impractical for commercialization.

In order to reduce the size and cost of elements and enable novel aspects in photonic devices and systems, there has been a considerable increase in the research and development efforts to miniaturize fundamental optical functionalities. Integration of various optical devices based on the planar lightwave circuit platform is a promising approach for this purpose. Planar technologies can offer dense integration through shrinking the critical dimensions of the device to the coherent light wavelength level, which allows large scale photonic integration on an envisioned platform. Also, the well-developed and increasingly mature microelectronic device integration processes, such as complementary metal-oxide semiconductor (CMOS) fabrication technology, can be readily used as an all-purpose toolbox to provide the foundation for the fabrication and integration of photonic devices and their applications. In principle, such an approach can follow a trend similar to the electronic Moore's law [8] to shrink in size, allow more elements per unit area, and progress in efficiency, which can substantially reduce the cost through integration.

Considering the infrastructure provided by microelectronics through processes such as CMOS, it is of utmost importance for any platform of choice to be compatible with available fabrication processes and manufacturing facilities. Among various material options, Si is arguably the most natural choice. Due to its continued success in realizing numerous microelectronic devices and systems, Si has a clear technological advantage over any other material of its class. Well-developed growth and purification methods have been offering intrinsic Si material with a relatively low cost. The material purity reduces its

optical loss, which is a critical parameter for the photonic device performance directly affecting many metrics such as insertion loss, field enhancement, sensitivity, and dynamic range. Therefore, creating low-cost photonics for mass-market applications is feasible by utilizing the electronic integrated circuit (IC) industry, which has been the underlying motivation of Si to be used as the prevailing material platform. Another motivation is the development of reliable processes to provide high-quality silicon-on-insulator (SOI) wafers, an ideal platform for creating photonic integrated circuits (PICs) [9]. The fact that SiO_2 can be thermally grown on Si with minimal stress and high purity is another key feature of Si, which has been extensively used in Si photonic platform, device and system integration including the SOI development process.

The strong optical confinement offered by the high index contrast between Si ($n = 3.45$) and SiO_2 ($n = 1.45$), allows to scale photonic devices to the sub-micron level. Such lateral and vertical dimension requirements can be met by advanced IC fabrication processes, and thus is compatible with electronic implementation. However, fabrication imperfections due to lithography resolution are more pronounced with the increased index contrast, resulting in the first few generations of Si photonic devices to be large (hundreds of wavelength). With the progress in electron-beam-lithography (EBL) techniques in the past decade, more efforts are devoted to the miniaturization of efficient photonic components in Si. In addition, the high index contrast between Si and SiO_2 makes it possible to localize the intensity in the Si waveguide and observe nonlinear optical interactions at higher optical intensities—e.g., nonlinear Raman [10,11] and Kerr effects [12] in chip-scale devices, which offers methods to realize and integrate new nonlinear

photonic applications in the SOI platform, such as optical parametric amplification [13] and wavelength conversion [14,15].

1.2 Applications of Silicon Photonics

Among various visions implemented in SiP, long and short-haul data transceivers have emerged as primary applications. The need for the high speed and low power data communication arises from the rapid growth of information created, stored or shared over different data platforms. The new information produced and transferred across all platforms in 2002 was estimated to be 5 exabytes (5×10^{18} bytes) [16], while Cisco reported the total data traffic exceeding 1000 exabytes in 2015 through internet alone, with the projected compound annual growth rate (CAGR) of 22% through 2020, as shown in Figure 1(a) [17]. Transporting such levels of data around with existing standalone electronic technologies has reached power consumption, speed, and density limits in conventional interconnects. Photonics has continued to replace electronics throughout networks, including in the data center, in the rack and on the board to transfer data packets.

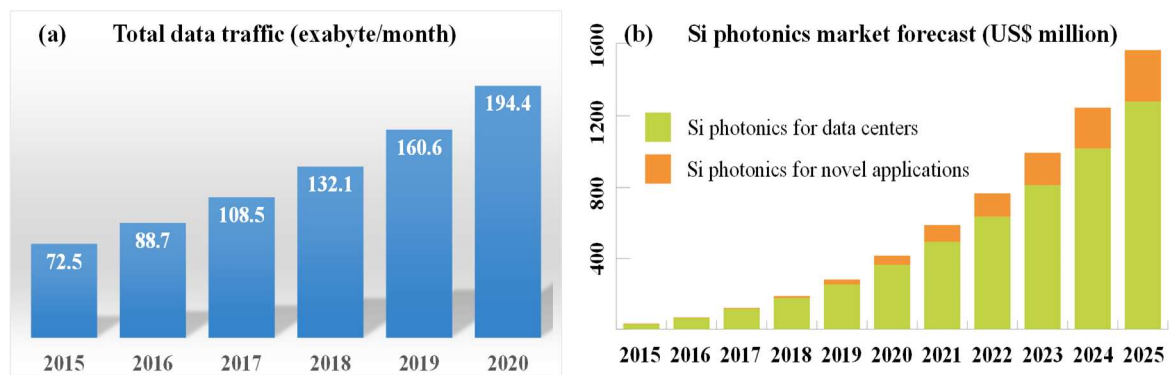


Figure 1: (a) Cisco VNI forecasts per month of IP traffic by 2020 [17]. (b) SiP growth forecast [18]

Besides the data center, two other applications are particularly attractive as they can push the integration of optical functionalities and miniaturization further to achieve successful products. Those applications are the light imaging, detection, and ranging (LIDAR) systems [19] and biomedical/chemical sensors. Lidars are the natural extension of radio detection and ranging (RADAR) systems utilizing the optical portion of electromagnetic waves. The main advantage of migration from radio to optical waves is the $\sim 10^5$ reduction of wavelength and corresponding increase in resolution, which enables extremely accurate ranging for lidars. Such an increase in resolution makes it a useful element of ranging in autonomous vehicles [20] and robotics [21]. Conventional lidar systems rely on moving parts to scan the full 2π field-of-view (FOV) in the horizontal dimension based on an assembly of individual optical and mechanical parts. The mechanical moving parts are costly and bulky elements not suitable for outdoor environments, reducing their effective lifetime in an automobile. Furthermore, the physical rotation of the device limits the scan rate to several Hz, substantially limiting the overall scanning speed. SiP offers a viable solution toward miniaturization by realization of chip-scale lidar without moving elements. The idea here is to use nanophotonic phased arrays (NPA) [22-24] to steer the beam to a relatively wide angle—e.g., 51° [25], and utilize multiple interlinked sensors (8 in this case) to cover the full 360° FOV. A prototype frequency-modulated continuous-wave integrated lidar system based on NPA is recently demonstrated on the Si platform at the telecom wavelength [26]. The envisioned fabrication of such integrated systems using a standard 300-mm-wafer CMOS process flow [27] can reduce the size and cost of an individual lidar chip below \$100 and make it practical for

the mass production and broad usage in the emerging ranging and detection markets which require accurate three-dimensional map of the environment with high frame rates.

Another emerging market for Si photonic integration is in the biomedical applications of optics. Integrated biomedical and gas sensors are not new, however the interest in gas and bio-sensing has gotten a new lease on life due to the prospect of large volume medical test and diagnostic applications. In principle, a photonic biosensor utilizes the interaction of light with matter to detect and quantify a specific type of element, compound, or cell in a host mixture of materials. Integration of biomedical or gas sensors into smartphones or wearables is currently on the roadmap of many bio-engineering companies. However, the size, cost and sensitivity are still challenging. To push biosensor miniaturization further, the industry is actively considering SiP as an integration platform for such devices. For example, on-chip interferometric configurations offer an approach to realize sensitive devices: integrated Mach-Zehnder interferometers (MZI) based on the splitting of light (typically coherent) into two arms; one of which exposed to the analyte, while the other covered with a protective layer [28]. MZI sensors with ~ 2 mm long waveguides on the SOI platform have achieved a limit of detection as low as 0.3 pg/mm^2 [29]. In addition to interference, resonance can offer sensitive devices suitable for biomaterial detection. Among methods to realize resonance, microring/microdisk and photonic crystal based resonators have been extensively utilized to demonstrate integrated biosensors with low limits of detection [30-36].

Figure 1(b) shows the market trends and the forecast of the SiP market share. According to one technology report [18], the average CAGR of 32% is expected in the next decade, which outperforms the growth of data transfer on information technology (IT)

platforms. While data centers keep being the main drive of Si photonic products, the emergence of new markets in integrated photonic sensors is predicted through 2025.

1.3 Beyond Single-Layer Silicon

With the brief introduction on the SiP as a discipline for photonic integration and its applications, the importance of the material platform selection as an enabling infrastructure in the design and realization of integrated photonic devices and systems is clear. However, the choice of a single-layer Si on SiO₂ as the material platform, as in the SOI, poses a number of critical challenges to PIC design and implementation. In principle, material limitations of Si do not allow or support the integration of several important optical functionalities. In other cases, while Si can offer a solution, alternative materials can provide superior performance to Si and enable higher efficiency devices and systems.

First and foremost, Si is an indirect bandgap material [37], therefore the high-efficiency photonic generation (lasing), amplification (gain), and detection are not available for the crystalline material in its un-doped form. On the other hand, materials with direct electronic bandgap such as III-V compounds—e.g., Indium Phosphide (InP) and Indium Gallium Arsenide (In_{0.53}Ga_{0.47}As, or InGaAs), efficiently support such applications [38-40]. However, III-V thin films are usually expensive due to the high cost of material growth. Also, the epitaxial growth of such compounds is usually performed at elevated temperatures above 550°C, which is CMOS incompatible and makes it further costly to cointegrate with Si. Even neglecting the thermal incompatibility, the crystalline mismatch between Si and III-V materials is a major challenge that leads to a high level of defects in the grown material on Si substrate. A recent report attempts to mitigate the defect issue by

introducing V-grooves in the Si substrate to trap defects near the V localizations [41, 42], however the growth on top of a functional SOI platform has yet to be demonstrated.

The window of transparency of crystalline Si (c-Si) is another important limitation which is imposed by its electronic band structure. Si is transparent at 1550 nm and the corresponding telecom bandwidth, making it a suitable platform for electro-optical applications in the near-IR optical communication. However, the optical transparency vanishes for wavelengths below $\sim 1.1 \mu\text{m}$ [43]. This puts the visible spectrum, and its diverse applications from visible optical communication to biosensors, out of reach of the Si platform. Another limitation arises in the mid-IR at wavelengths at $4 \mu\text{m}$ and above, where SiO_2 layer of the standard SOI platform begins to absorb optical carrier significantly. Even though Si is transparent through mid-IR wavelengths up to $8 \mu\text{m}$, the linear and nonlinear absorption mechanisms triggered by three-photon absorption (3PA) reduce the transparency of the material between $2.3 \mu\text{m}$ to $3.3 \mu\text{m}$ [44], overall limiting the continuous transparency window to $1.1 \mu\text{m}$ to $2.3 \mu\text{m}$.

On the other hand, several optical loss mechanisms exist in Si. The intrinsic linear optical loss is the free-carrier absorption (FCA), which is due to the semi-conductive nature of Si generating a considerable number of electron-hole pairs ($n_i = 1.5 \times 10^{10}$) at the room temperature. At the telecom wavelengths, there is a nonlinear contribution to the overall optical loss through two-photon absorption (TPA) mechanism ($\beta_{\text{TPA}} = 7 \times 10^{-12} \text{ m/W @ } \lambda = 1550 \text{ nm}$) [45]. Because of the quadratic dependence of the nonlinear loss to the optical intensity, TPA severely limits the Si material's capacity of handling high-power signals in the linear regime and supporting ultra-low-loss photonic devices. In addition to TPA, Si exhibits the third-order optical nonlinearity at much lower optical intensities compared to

SiO₂, due to its large Kerr coefficient ($n_{2, \text{Si}} = 5 \times 10^{-18} \text{ m}^2/\text{W}$ @ $\lambda = 1550 \text{ nm}$; $n_{2, \text{SiO}_2} = 2.7 \times 10^{-20} \text{ m}^2/\text{W}$ @ $\lambda = 1550 \text{ nm}$) [46, 47]. Such nonlinear performance is especially detrimental to linear resonant optical devices, where the higher field enhancement is highly favored to improve device performance such as power efficiency and device sensitivity. While the high Kerr coefficient itself may seem to favor nonlinear demonstrations in Si, the poor nonlinear figure of merit (due to the high TPA) reduces its application and efficiency for nonlinear devices and systems [48]. Another limitation of Si for nonlinear applications stems from its centrosymmetric unit cell (diamond lattice crystal structure), which imposes its intrinsic second order nonlinearity to be zero.

From a geometrical point of view, the standard Si platform faces an important barrier for dense integration. The planar lightwave circuitry extends in two dimensions in the crystalline Si platform, and the third dimension is not being effectively used. In the SOI platform, the only available photonic layer is a 2D sheet of Si, and the vertical dimension is usually used for electronic pads and the passivation/isolation layer. With the increasing demand for dense integration and the corresponding reduction in cost for increased elements per unit area, the vertical integration of photonic elements is inevitable.

Considering the enabling and limiting properties of Si, both as a material and in its single-layer form, this work has aimed to define a path toward an all-inclusive 3D photonic ecosystem that can support various needs of integrated photonic design and fabrication which cannot be met in a single-layer Si on SiO₂ platform. As discussed briefly, the limitations of Si do not allow PICs to support and target a wide variety of applications, while its enabling features are well developed and suitable for many integrated photonic applications. Thus, the ultimate solution is envisaged through multi-layer platforms of

various materials on a chip, which can support different elements in different host materials to enable new features for photonic integration. Throughout this work, I call such platforms “hybrid” or “heterogeneous” material platforms to point out their multi-material nature, and focus on key methods to develop, solve integration challenges, and demonstrate proof-of-concept devices to verify the performance of such platforms.

In the following chapters, the theoretical background of integrated photonic devices is briefly reviewed, and various methods are envisioned to realize compact, low power and high speed photonic devices and systems on a hybrid chip. In contrast to electronics, where the essential device is a transistor and the dominant material is Si, the toolbox of fundamental devices required for PICs is diverse. Therefore, novel material platforms beyond single-layer Si are employed to host the next-generation of devices and systems, which is the core subject of this PhD work. Also, I discuss the current degrees of integration achieved in the Si platform, and cover our demonstrations on novel hybrid photonic platforms, devices and systems to further improve the performance. The final chapter briefly discusses contributions to the field and offers a viewpoint for future directions.

CHAPTER II

THEORETICAL BASES AND FUNDAMENTAL RELATIONS

The current chapter is dedicated to the core physical and mathematical description for the evolution of electromagnetic waves, with a vision to understand the dynamics of integrated photonic devices and systems. Subsequently, a framework to accurately model and compute integrated photonic elements such as waveguides, couplers, traveling wave resonators etc. is developed and their key dynamics are properly formulated.

2.1 Dynamics of Electromagnetic Waves and Fields

Classical electromagnetics, the theory describing the macroscopic evolution of electromagnetic waves in an arbitrary media, is a limit of quantum electrodynamics exceedingly accurate for small momentum (compared to the momentum of the material system) and large number of photons. The majority of current integrated photonic devices work at levels of photon flux and momentum that fits into this description. Therefore, the interaction of light and matter in such conditions is properly described by the classical interpretation of Maxwell equations [49]

$$\nabla \times \mathbf{E} + \frac{\partial \mathbf{B}}{\partial t} = 0, \quad (1)$$

$$\nabla \times \mathbf{H} - \frac{\partial \mathbf{D}}{\partial t} = \mathbf{J}, \quad (2)$$

$$\nabla \cdot \mathbf{D} = \rho_v, \quad (3)$$

$$\nabla \cdot \mathbf{B} = 0. \quad (4)$$

The curl relations, Equations 1 and 2, are well known as Faraday and Ampere's laws. Equation 3 is also known as Gauss law, and Equation 4 manifests the absence of free magnetic poles. The theory employs 4 separate vectorial fields to fully describe the electromagnetic evolution, electric field (\mathbf{E})¹, magnetic field (\mathbf{H}), electric flux density (\mathbf{D}), and magnetic flux density (\mathbf{B}), each are functions of time and space—e.g., $\mathbf{E} = \mathbf{E}(\mathbf{r}, t)$. The electric and magnetic flux densities \mathbf{D} , \mathbf{B} are related to the field intensities \mathbf{E} , \mathbf{H} via the constitutive relations, whose precise form will be discussed next, and depend on the material in which the fields exist. In vacuum, they take simple forms as

$$\mathbf{D} = \epsilon_0 \mathbf{E}, \quad (5)$$

$$\mathbf{B} = \mu_0 \mathbf{H}, \quad (6)$$

where the ϵ_0 and μ_0 are the permittivity and permeability of vacuum, respectively. There are two source variables present in Maxwell equations: the free electric charge density (ρ_v), and free electric current density (\mathbf{J}), which can be functions of time and space. It is also worth noting that several other important relations in electromagnetics, such as Lorentz equation of force and the continuity equation for charge and current density, can be derived from Maxwell equations (Equations 1 through 4). Therefore, the description of macroscopic electromagnetic fields in the vacuum is complete if the sources, ρ_v and \mathbf{J} , are known everywhere. In case of homogeneous equations where sources are null (vacuum with no free charge), the fields can be solved in a closed form using a scalar and a vector potential to describe electric and magnetic field, respectively. However, in case of many sources, or otherwise macroscopic aggregates of matter, the determination of the fields is

¹ In this chapter, the bold notation of variables is reserved to denote vectors of the space coordinates $\mathbf{r} = (x, y, z)$, or other equivalent orthonormal bases describing space coordinates.

almost impossible. Excluding settings with a small number of definite sources, any other configuration of sources need some level of averaging to be properly determined.

The question of what nature of averaging is appropriate is to be dealt with carefully. In a microscopic world created by electrons and nuclei, and for dimensions above 10^{-14} m, the nuclei and electrons can be treated as points. A macroscopic amount of matter (such as one mole) has $\sim 10^{25}$ electrons and corresponding number of nuclei, all in motion due to zero-point energy vibrations, thermal agitations, and orbital motions. The electromagnetic fields produced by these charges vary extremely fast in space and time. The spatial variations happen over distances in the order of an atom—i.e., ~ 1 Å, and the temporal fluctuations occur with rates of 10^{14} to 10^{17} Hz. Current monitoring systems average over time and distance intervals much larger than these, diminishing the fluctuations.

To determine the domain of validity for the macroscopic description of electromagnetic phenomena, we resort to experiments with different wavelengths of coherent light. While photons at ~ 5 eV energy level (visible light) do not expose the atomic nature of a material, they clearly do at 100 keV (X-ray). Therefore, it is acceptable to consider length of ~ 2 nm as the critical lower limit of the macroscopic domain (l_c). A volume of l_c^3 approximately has 10^4 nuclei inside. Thus, in any region of macroscopic size ($> l_c$) there are so many atoms that the fluctuations are washed out by spatial averaging. However, the time averaging is prohibited, as time scale associated with l_c ($l_c/c \approx 10^{-17}$ s) is well within the range of atomic motions and the corresponding time response needs to be preserved. However, the microscopic temporal fluctuations of the medium are appropriately removed through spatial averaging, as in the absence of specific microscopic temporal interlocking mechanisms, the time variations of microscopic fields are not

correlated over distances of l_c order, and are stochastically nonexistent upon spatial averaging.

The spatial averaging opens a path to significantly simplify the Maxwell notation of waves propagating in a matter through microscopic averaging of constitutive equations. Without getting into details, the macroscopic \mathbf{D} and \mathbf{H} can no longer be represented by a multiple coefficient in a matter generally, and rather have components with forms as

$$D_i = \epsilon_0 E_i + P_i - \sum_j \frac{\partial Q_{ij}}{\partial x} + \dots, \quad (7)$$

$$H_i = \mu_0^{-1} B_i - M_i + \dots, \quad (8)$$

The quantities \mathbf{P} , \mathbf{M} , Q_{ij} etc. represent macroscopically averaged electric dipole, magnetic dipole, and higher moment densities of the medium. This way, the effect of bound electric charges and magnetic multipoles is included in the equation, and ρ_v and \mathbf{J} represent free charges and current densities. Most materials however have very weak higher moment terms, and \mathbf{P} and \mathbf{M} , describes their response to high degree of accuracy. In majority of substances, and in weak field regime, the induced electromagnetic polarization is proportional to the applied field, and therefore the material is linear. The components of \mathbf{D} and \mathbf{H} can then be written as

$$D_i = \sum_j \epsilon_{ij} E_j, \quad (9)$$

$$B_i = \sum_j \mu_{ij} H_j. \quad (10)$$

The linear description neglects the spatial and temporal dependence of the response of a medium to the applied field. A more general description includes the non-spontaneous and nonlocal response through convolution of spatiotemporal permittivity with the applied fields as

$$D_i(\mathbf{r}, t) = \sum_j \int dv' \int \epsilon_{ij}(\mathbf{r}', t') E_j(\mathbf{r} - \mathbf{r}', t - t') dt'. \quad (11)$$

The Fourier transform of the non-spontaneous nonlocal constitutive relation has a rather simpler form

$$D_i(\omega, \mathbf{k}) = \sum_j \epsilon_{ij}(\omega, \mathbf{k}) E_j(\omega, \mathbf{k}). \quad (12)$$

The permeability follows similar relations substituting ϵ with μ , \mathbf{D} with \mathbf{B} , and \mathbf{E} with \mathbf{H} . For the wavelengths above UV, it is acceptable to neglect nonlocality in the matter. That reduces the permittivity to a function of frequency, and in isotropic² non-magnetic case which covers majority of materials in this work, the constitutive equations are reduced to a constant permeability and a dispersive permittivity in time harmonic domain. The Faraday and Ampere's laws are rewritten in a homogeneous³ medium, with no source, and for waves with harmonic time dependence, $\exp(j\omega t)$, as

$$\nabla \times \mathbf{E} = -j\omega\mu_0\mathbf{H}, \quad (13)$$

$$\nabla \times \mathbf{H} = j\omega\epsilon_0\epsilon_r(\omega)\mathbf{E}, \quad (14)$$

where $\epsilon_r(\omega) = n^2(\omega) = \epsilon(\omega)/\epsilon_0$. Combining the two results in Helmholtz equation

$$\nabla^2 \mathbf{F} = \left(\frac{\omega \times n(\omega)}{c} \right)^2 \mathbf{F}, \quad (15)$$

where \mathbf{F} can be substituted with \mathbf{E} or \mathbf{H} , and $c = (\mu_0\epsilon_0)^{-\frac{1}{2}}$ is the speed of light in vacuum.

The analytical solution to the Helmholtz equation in a homogeneous medium has the form of

$$\mathbf{F} = \mathbf{F}_0 \exp(-j\mathbf{k} \cdot \mathbf{r}), \quad (16)$$

in which $|\mathbf{k}| = \omega \times n(\omega)/c = 2\pi n(\omega)/\lambda$. Such set of solutions are called plane waves, as their phase fronts are planes perpendicular to the \mathbf{k} vector. While analytical solutions can

² The assumption reduces the general tensor of a characteristic coefficient to a single-value diagonal one.

³ Homogeneity assumes translational symmetry for characteristic coefficients.

be derived for such a case, as well as few other specific configurations, the solution is not analytically achievable for the general configurations [50].

2.2 *Optical Waveguides: Modal Analysis and Characteristic Relations*

A fundamental structure of integrated photonics, as well as fiber optics, is conceived as a two-port element which can localize and carry light through with minimal distortion and loss, delivering the coherent photons at the other end. Optical fibers of different spatial configuration, modal spectra, and wavelength range are examples of such devices mainstream in visible and near-IR fiber optic systems. For integrated photonic applications, the waveguide is usually formed through etching of a thin film material with high refractive index, surrounded by lower index material(s). The index contrast can provide localization of light and the lower refractive index material is used as a support layer for the mechanical stability and durability of the nanowire. In the SOI platform, Si acts as the high index material and the support layer is consisted of the bottom oxide layer, also called buried oxide layer (BOX). Figure 2 shows the schematic for two classes of waveguides extensively used in SiP: the fully etched configuration, or ridge waveguide in Figure 2(a), and the partially etched form, or rib waveguide in Figure 2(b).

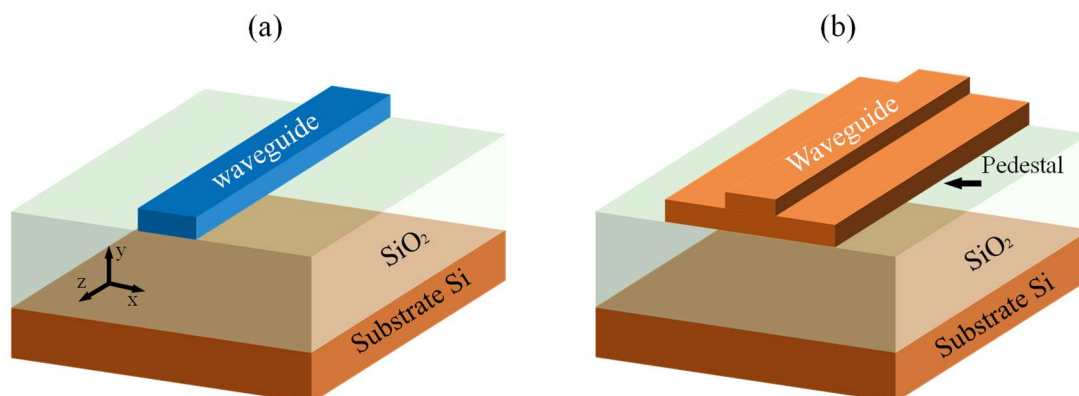


Figure 2: 3D schematics of an integrated (a) fully-etched waveguide, and (b) partially etched waveguide on Si substrate.

In a systematic approach, the design parameters of an integrated waveguide are defined as its height, width and the height of the pedestal. It is also possible to define a design role to other parameters of a waveguide such as the cladding material, its height, the over-etching depth (in case of a ridge waveguide), and the angle of sidewalls. However, the latter parameters tend to significantly increase the complexity of the device implementation. It is therefore more robust to import such parameters from the fabrication processes to be treated as fixed constants rather than design parameters. Since the envisioned waveguide has a translational symmetry along the propagation axis (z-axis in Figure 2), electromagnetic field can be considered to have a solution similar to the Equation 16 along the axis of symmetry ($\mathbf{F} \propto \exp(\pm jk_z z)$), and the fields can be expressed as

$$\mathbf{E}(\mathbf{r}, t) = \mathbf{E}(x, y) \exp[j(\omega t \pm k_z z)], \quad (17)$$

$$\mathbf{H}(\mathbf{r}, t) = \mathbf{H}(x, y) \exp[j(\omega t \pm k_z z)], \quad (18)$$

where $\beta \equiv k_z$ is the propagation constant of the mode in the z direction. The propagation constant carries an important set of information about the wave and its dynamics, including the effective index ($n_{eff} = \beta c / \omega$), and the phase velocity ($v_p = \omega / \beta$). Replacing the above field expressions into the Equations 13 and 14, the equation is reduced to

$$\nabla_t^2 \mathbf{E}(x, y) = \left[\beta^2 - \left(\frac{\omega \times n(\omega)}{c} \right)^2 \right] \mathbf{E}(x, y). \quad (19)$$

As mentioned in the previous section, it is not generally possible to obtain a closed-form expression for such an equation, and we are to resort to numerical methods based on the finite-element (FE) method and the finite-difference (FD) algorithms to model and compute the frequency-domain and time-domain evolution of coherent light, according to the nature of a design. For the modal analysis of an integrated waveguide, such as in Figure 2, FE method can properly solve the characteristic equation—i.e. Equation 19, and provide

the basic information associated with each supported mode. For this purpose, the COMSOL software package offers two modules to solve for characteristic equations in arbitrary geometries: *Wave Optics Module* and *RF module*. In the first stage of computation, a mesh is defined over the simulation area, as depicted in Figure 3(a). This fine pattern is numerically solved for the Equation 19 over its uniform area, and the field values are matched at the borders to the neighboring mesh sections using boundary conditions driven from Maxwell equations. In the example shown in Figure 3, a typical silicon nitride waveguide ($\epsilon_r = 3.99$ at 1550 nm) with the height of 450 nm and width of 750 nm is numerically computed. The substrate of waveguide is SiO_2 , and air surrounds the waveguide elsewhere. Figures 3(b) and 3(c) show the cross sectional-view of the waveguide with the computed time-averaged power flow for the first two fundamental modes of the waveguide in the z direction (i.e., the direction of light propagation).

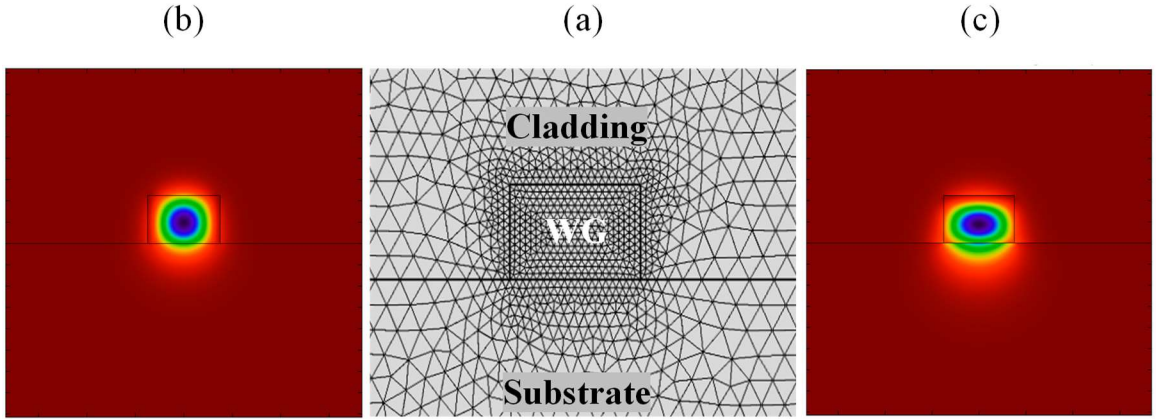


Figure 3: (a) Adaptive mesh generated by COMSOL software to compute a single-mode integrated photonic waveguide. The guiding structure is composed of silicon nitride (WG region), SiO_2 (Substrate region), and air (Cladding region). (b) and (c) depict the average power (Poynting vector) profiles of localized states supported by the geometry. The computed effective refractive indices are 1.5768 and 1.5205 for (b) and (c), respectively. Note the discontinuity in profiles at interfaces: where power is primarily carried by E_x (H_x) field component, the profile discontinuity is located at interfaces along y (x) dimension.

The mode families of a waveguide can be classified into two categories according to the polarization of each mode, which is done through their corresponding electrical and magnetic field components. In the current example, as shown in Figure 4, comparison between the corresponding electrical and magnetic field components of each mode indicates that the first mode carries most of the optical power in the E_x - H_y conjugate components. Figure 5 shows the second mode components, in which the majority of the optical energy is in the H_x - E_y pair. According to a universally used convention, the first mode (with $n_{eff} = 1.5768$) is referred to as the transverse electric (TE), or more accurately the TE-like, and the second mode (with $n_{eff} = 1.5205$) is called the transverse magnetic (TM), or the TM-like mode. In contrast to one-dimensional (1D) waveguides (slabs), here the waveguide does not support a mode of complete TE or TM nature, in which the TE mode only has E_x , and no E_y component. However, the contrast is such that one polarization dominates the dynamics. As can be inferred from Maxwell equations, as well as the results of the numerical computation depicted in Figures 4 and 5, the TE and TM modes form an orthogonal basis to span all possible guided solutions of electromagnetic power inside the waveguide. It guarantees optical power is preserved in each mode throughout the travel, and none is coupled to another, if the practical non-idealities such as roughnesses and discontinuities are negligible. The geometry of silicon nitride waveguide only supports a pair of TE/TM conjugate modes. All higher order modes in both vertical and lateral dimensions are not confined, thus included in the radiation continuum of the basis. This is called the cutoff condition for higher order modes. In principle, the optical power can be launched into one of the two modes of such a waveguide by appropriate polarization matching, and therefore it is called single-mode. Single modality of a waveguide is often

preferred in the design for the superior control of power and lower crosstalk between unwanted higher modes, while the fabrication of such waveguides is more sensitive to imperfections due to relatively higher power interacting with nonidealities at interfaces.

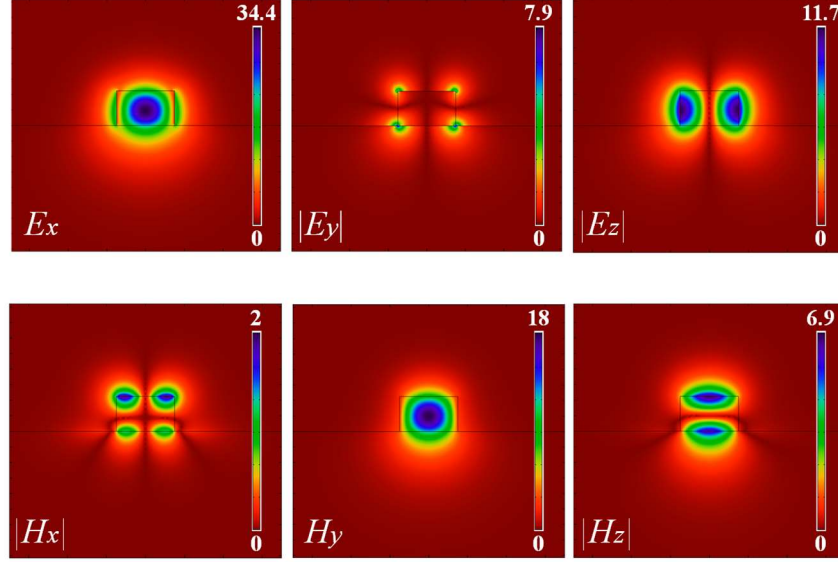


Figure 4: Cross-sectional profiles of electric and magnetic field components for the TE mode of the single-mode waveguide. The unit for \mathbf{E} and \mathbf{H} components is arbitrary, yet meaningful comparatively. The image confirms that E_x - H_y pair dominate the mode profile.

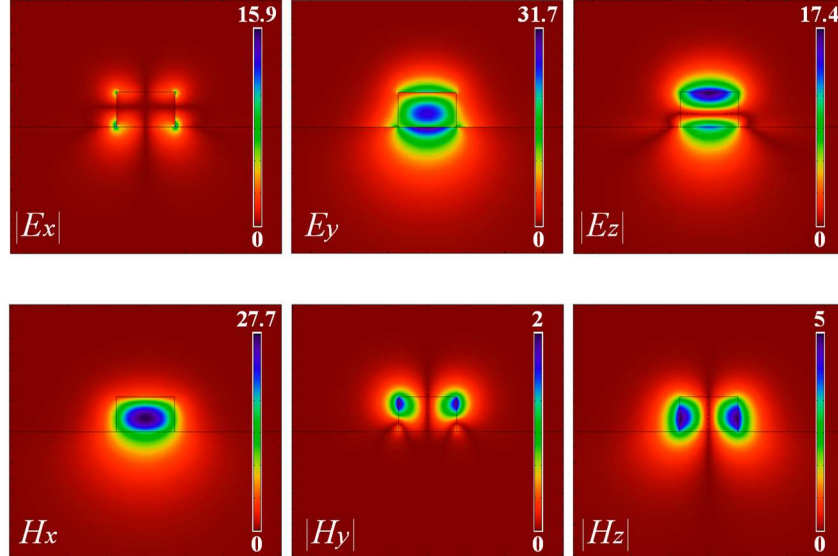


Figure 5: Cross-sectional profiles of electric and magnetic field components for the TM mode of the single-mode waveguide. The unit for \mathbf{E} and \mathbf{H} components is arbitrary, yet meaningful comparatively. It is clear from the image that E_y - H_x pair dominate the mode profile.

The spatial localization of light in a waveguide alters the dynamics of energy transfer compared to the free space propagation. As discussed previously, the phase velocity for a particular mode is derived as

$$v_{pi} = \omega / \beta_i, \quad (20)$$

in which β_i represents the i -th mode's propagation constant. Therefore, group velocity of that mode is

$$v_{gi} = \partial \omega / \partial \beta_i. \quad (21)$$

The group index of a mode is therefore given by

$$n_{gi} = \frac{c}{v_{gi}} = c \times \left(\frac{\partial \omega}{\partial \beta_i} \right)^{-1}. \quad (22)$$

Unlike the vacuum, for an arbitrary waveguide geometry, the relationship between the propagation constant (or equivalently, effective index) and the frequency of the confined electromagnetic wave is not trivial, and usually found through numerical analysis. Most waveguide configurations exhibit a change in the effective index across frequency, which is called dispersion. As the result of dispersion in the phase velocity, the group velocity is also changed across the optical spectrum. To quantify the change in the group velocity, the group velocity dispersion (GVD) is defined as

$$GVD \equiv \frac{\partial (v_{gi})^{-1}}{\partial \omega} = \frac{\partial \beta_i^2}{\partial^2 \omega}. \quad (23)$$

Conventionally, the GVD parameter is widely used in optical fibers. In the context of optical fiber communications, the dispersion is usually defined as the derivative with respect to wavelength rather than frequency, which can be calculated from the above-mentioned GVD parameter as

$$D_\lambda = -\frac{2\pi c}{\lambda^2} GVD = -\frac{2\pi c}{\lambda^2} \frac{\partial \beta_i^2}{\partial^2 \omega}. \quad (24)$$

For the wave propagating in the single-mode silicon nitride waveguide of Figure 3, the dispersion relations for the supported TE and TM modes are plotted in Figure 6. The dispersion parameters of such a waveguide are primarily controlled by its corresponding geometrical specifications. In general, engineering the cross-sectional dimensions of a waveguide can significantly change its dispersion. In addition to modal dispersion, most materials exhibit similar changes in the refractive index with frequency, which is called material dispersion. The competition between the two different dispersion mechanisms, and the overall dispersion has significant applications in nonlinear optical processes, and is further discussed in the corresponding chapter.

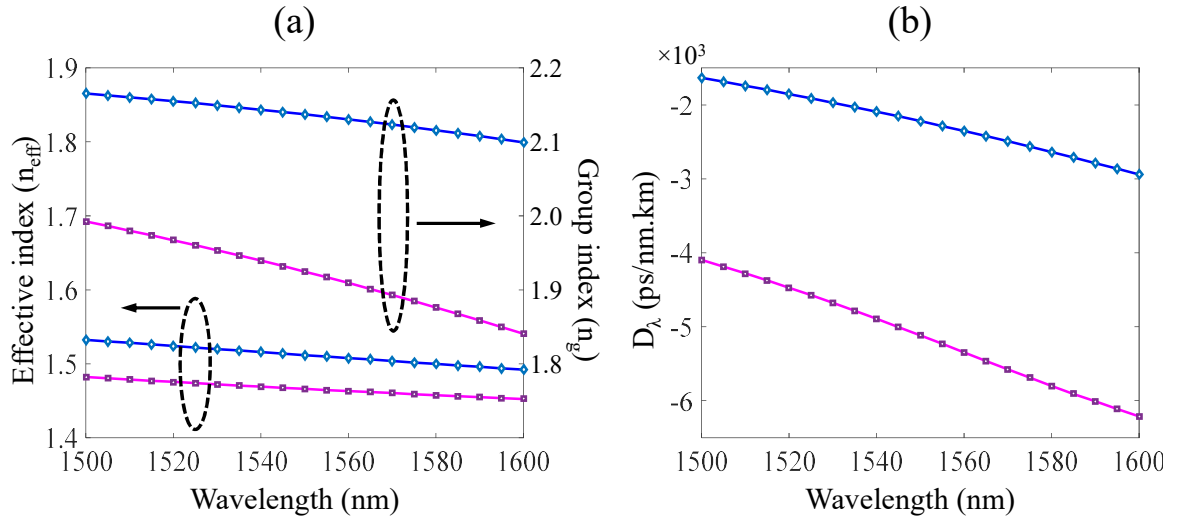


Figure 6: Diagrams of TE (blue) and TM (magenta) (a) effective mode index dispersion and group index dispersion in the single-mode silicon nitride waveguide. (b) Group velocity dispersion of the corresponding waveguide. According to the definition of GVD parameter, the negative D_λ corresponds to normal dispersion.

2.3 Integrated Microresonators and Microcavities

Photonic microcavities, also called optical microresonators, are one of the key building blocks in integrated photonic systems due to their capability of localizing and storing optical waves in spatial and temporal domain simultaneously. Trapping the optical energy

for extended periods of time, the intensity of optical field is enhanced in such structures with respect to waveguides [51]. The corresponding field enhancement significantly improves light-matter interactions, which is widely used to build compact devices for low-power modulation, ultra-low detection limit sensing, and low-power device tuning. The enhanced light-matter interaction also enables more efficient nonlinear processes, and offers an integrated method to study fundamental opto-mechanical phenomena [52] and cavity quantum electrodynamics [53].

Microcavities utilize a traveling or standing wave to support the field localization and enhancement. In a traveling wave resonator, optical field travels around the resonator in one direction. In standing-wave resonators, the degenerate z -reversal fields travel against one another forming a standing wave. An optical mode traveling along the circumference of a cavity is also called a whispering gallery mode, few modes of which are depicted in Figure 7 for a Si microresonator.

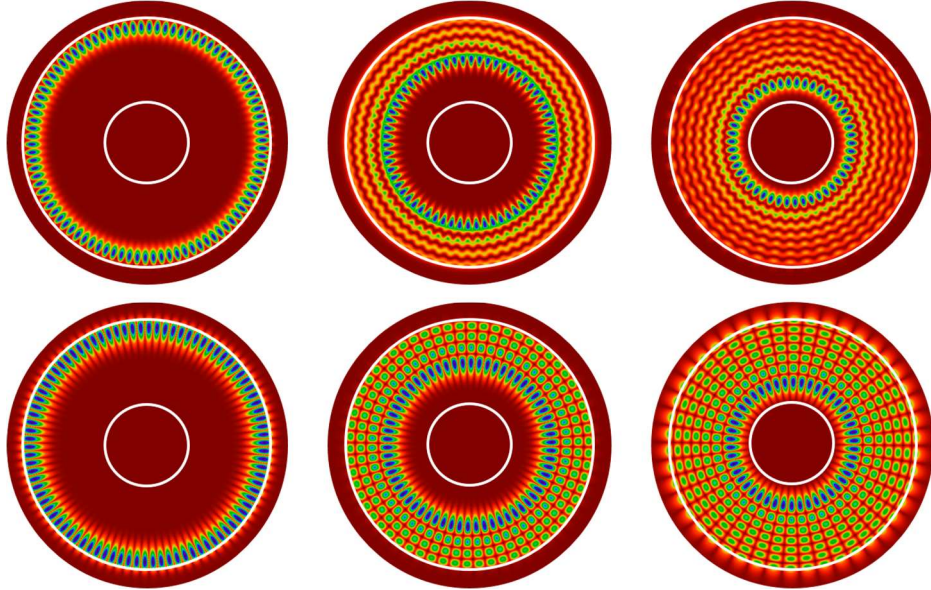


Figure 7: Computed whispering gallery modes of a typical Si microring resonator. White circles indicate inner and outer edges of the microcavity. Top row shows the average power flow in the φ direction, and the bottom row shows the dominant E_z component of each mode. Out of several modes of the structure, the 1st, 4th, and 7th radial TM modes are depicted.

In general, a microcavity can be realized through several different structural forms and variations, including (micro) rings, disks, toroids, spheres, and photonic-crystal-based nanobeam resonators. All except the last are examples of traveling wave microcavities, which are usually simpler in design and realization. Without losing the general picture, this work focuses on properties of planar whispering gallery mode microrings and microdisks, results of which can be readily extended to other forms of cavities with appropriate modifications.

2.3.1 Properties of Integrated Microcavities

Figure 8(a) shows a typical microring structure. A waveguide, also known as access or bus waveguide, is positioned near the cavity so that the optical wave can be evanescently coupled to the cavity. The coherent light launched into the access waveguide partially couples into the resonator, and back out of it to the access waveguide. The interference of traveling wave inside the resonator with itself after a roundtrip can be either constructive or destructive. Constructive interference can only occur when the roundtrip phase picked up by the traveling wave is equal to an integer number of 2π phase shifts, otherwise the arrival phase washes out any signal after multiple roundtrips (destructive interference). Therefore, constructive interference imposes a set of discrete wavelengths (frequencies) which are called resonance wavelengths, and are found by

$$m\lambda_R = n_{eff}L, \quad (25)$$

in which L is the effective roundtrip length traveled by the electromagnetic wave, and m is an integer determining the azimuthal order of the mode.

Similar to waveguide structures, structural symmetries are useful to be included for fast and efficient solution of microresonator modes. The typical stand-alone

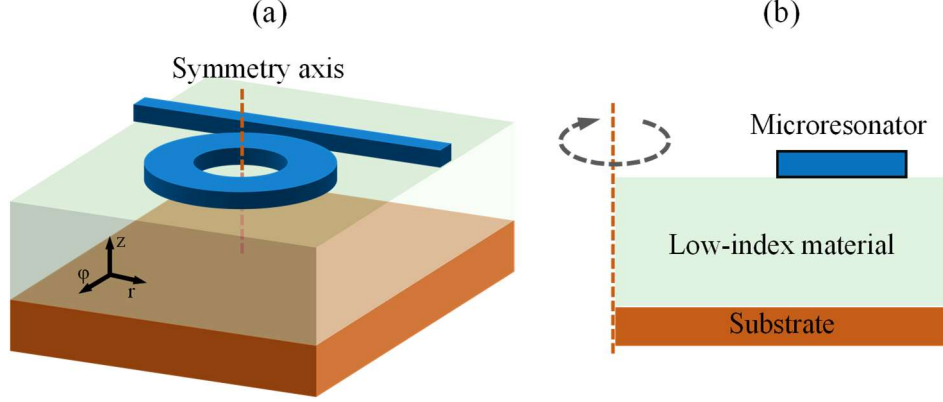


Figure 8: (a) 3D schematic of an integrated microring resonator with an access waveguide. (b) The cross-sectional representation of the microring resonator in the ϕ - z plane.

microresonator of Figure 8(a) has a cylindrical symmetry, and therefore it is suitable to be described in cylindrical coordinates. The symmetry along the z -axis enables the fields to be expanded as

$$\mathbf{E}(\mathbf{r}, t) = \mathbf{E}(r, z) \exp[j(\omega t + m\phi)], \quad (26)$$

$$\mathbf{H}(\mathbf{r}, t) = \mathbf{H}(r, z) \exp[j(\omega t + m\phi)]. \quad (27)$$

Therefore, the solution of Maxwell's equations can be reduced to solving $\mathbf{E}(r, z)$ and $\mathbf{H}(r, z)$. Setting the azimuthal order, and considering the axial symmetry of $\mathbf{E}(r, z)$ and $\mathbf{H}(r, z)$ around the z -axis, the solution of microring mode is appropriately performed by solving over the cross-sectional area of the Figure 8(b) for the eigenfrequency which supports the mode of interest. As a numerical example, Figure 9 shows several computed eigenmodes of a silicon nitride microring resonator. The height of the silicon nitride film is 450 nm. The outer and inner radii of the microring are 40 μm and 35 μm , respectively.

As inferred from Equation 25, one feature of microcavities is the recurrence of the resonance at infinite countable wavelengths. The frequency difference of the two nearest resonances of a mode family (i.e., the consecutive azimuthal orders of a mode) is defined

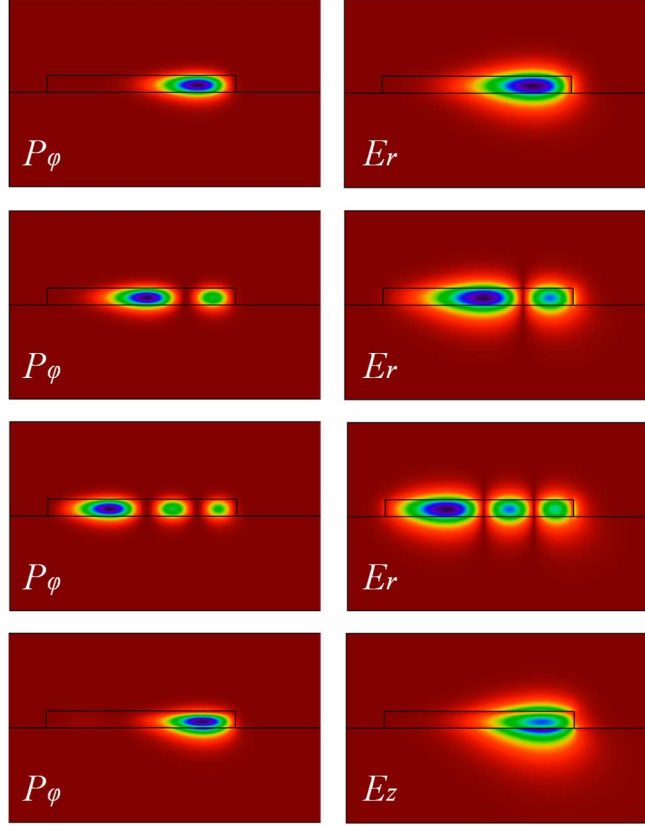


Figure 9: Profiles of TE₁, TE₂, TE₃, and TM₁ modes for the silicon nitride microring, from the top to bottom respectively. The left column shows the average power (Poynting vector) distribution and the right column depicts the dominant electric field component (E_r or E_z) of each mode.

as the Free Spectral Range (FSR). In the most general form, FSR can be derived from the Equation 25 by direct differentiation as

$$\text{FSR}_f = \frac{v_g}{L}. \quad (28)$$

From a practical point of view, FSR can be effectively used to interpret and identify different mode families in a microcavity. As it is numerically computed for the case of silicon nitride microring resonator in Figure 9, a typical microring or microdisk can support several radial modes. As will be repeatedly seen in the next chapters, the spectrally resolved response of a typical resonator has several different azimuthal and radial mode classes in the spectral region of interest, such as in the 1550 nm telecom band or in visible spectrum,

making the overall spectral response rather crowded. One effective method to classify each mode family and properly assign corresponding properties to each resonance is to numerically solve for the FSR of each family, and then use the data to identify each radial resonance out of a rather crowded spectral resonance set. Even in the case of a single-mode microring, there is at least a two-fold ambiguity due to TE and TM modes of the cavity. However, since the group indices of each mode is different (as shown in Figure 6(a) for a single-mode silicon nitride waveguide), the corresponding FSR's of each mode class is different, and therefore each resonance family can be properly identified.

Perhaps the most important characteristic of a microresonator is the quality factor, or Q , which is defined as

$$Q \equiv \omega_0 \frac{W}{P_d}. \quad (29)$$

in which W is the energy stored in the cavity, P_d is the total energy dissipation rate, and ω_0 is the frequency of oscillation. Using the relation of power loss to cavity energy ($P_d = -\frac{dW}{dt}$), it is straightforward to solve for W in the Equation 29 and arrive at

$$W(t) = W_i \exp(-\omega_0 t / Q), \quad (30)$$

from which the cavity photon lifetime is defined as $\tau_0 = Q / \omega_0$. It is also useful to define losses per length to quantify waveguide loss through its equivalent microresonator quality factor. In a waveguide, the propagation losses can be defined as:

$$\frac{dP}{dl} = -\alpha P. \quad (31)$$

Solving the Equation 31 for length, the power is found as

$$P(l) = P_i \exp(-\alpha l). \quad (32)$$

For a resonator made from the waveguide with α propagation loss, the total resonator energy relation with dissipated power can be derived as

$$P_d = -\frac{dW}{dt} = -\frac{dW}{dl} \times \frac{dl}{dt} = \alpha W \times v_g. \quad (33)$$

Plugging Equation 22 into Equation 33, the Equation 29 can be rewritten as

$$Q = \frac{2\pi n_g}{\alpha \lambda}. \quad (34)$$

The above equation provides a systematic method to calculate the loss per length of a waveguide by measuring the quality factor of the corresponding resonator, provided that the bending losses do not limit the Q . The waveguide loss is usually described in dB/m, which is equal to $4.343 \times \alpha$.

Another parameter closely related to the quality factor is field enhancement and finesse. Qualitatively, the ratio of cavity photon lifetime over the cavity roundtrip time is a reasonable representative of power enhancement inside the cavity. It can be explained such that the cavity keeps a photon inside for an average τ_0 time scale. Also, at each roundtrip time, photons coherently add up with the continuous stream of coherent light into the resonator from the access waveguide. Therefore, the power enhancement (η) is of the scale of

$$\eta = \frac{\tau_0}{T_{roundtrip}} = \tau_0 \times \text{FSR}_f = \frac{1}{2\pi} \times \frac{Q \cdot \text{FSR}_\omega}{\omega_0}, \quad (35)$$

in which, $T_{roundtrip}$ is the roundtrip time of power in the cavity. To quantify the field enhancement, the finesse is defined as [54]

$$F \equiv \frac{Q \cdot \text{FSR}_\omega}{\omega_0} = 2\pi\eta. \quad (36)$$

As will be discussed in the Chapter 5, this parameter is the main figure of merit (in contrast to Q) for applications in which the enhancement factor defines the performance of the photonic system, as in Purcell effect and microcavity-based optical sensors, to name a few.

For practical purposes, Equation 30 also offers a temporal method to accurately measure the quality factor. However, for many actual cases, the spectral method is favorable as a continuously tunable wavelength setup can provide the frequency response of the system. Also, the temporal method is exceedingly erroneous as the quality factor reduces, while the spectral method becomes more accurate due to the time-frequency duality. The Fourier transform of an envelope function of Equation 30 with the carrier frequency ω_0 has a form of

$$W(\omega) \propto \frac{1}{(\omega - \omega_0)^2 + \tau_0^{-2}}, \quad (37)$$

which shapes a Lorentzian curve with respect to frequency, and Q can be found accordingly through curve fitting.

As suggested by Equation 37, it is expected to observe a single singularity occurrence per resonance in spectral measurements of microcavities. On the other hand, due to the structural symmetry, a microresonator has a degenerate mode at the resonant frequency. Ideally, the clockwise (CW) and counter-clockwise (CCW) modes are orthogonal, and do not interfere with each other. However, in the presence of a perturbation which can occur in the form of a particle, or more generally the non-ideality introduced by roughnesses at the interface can lift the two-fold degeneracy [55,56]. Two modes of standing waves appear, while the excitation is a propagating wave. One of them maximizes the polarization in the perturbation, a symmetric standing wave (SSW), and the other minimizes the polarization, an antisymmetric standing wave (ASW). Correspondingly, the two modes

shift from the ideal degenerate frequency, and a doublet appears in the spectral domain near the resonance frequency.

2.3.2 Coupled Mode Theory in Waveguide Coupled Microcavity Structures

Coupling is a widely used mechanism to incorporate optical interaction between elements of a PIC. In case of the microcavity, a guiding structure placed in the vicinity of it can provide a path to effectively access and couple light to a specific mode. As briefly introduced in Section 2.3.1, the basic coupling structure can be realized as an integrated waveguide-resonator pair which are fabricated simultaneously, therefore the relative spacing can be precisely controlled through lithographic precision of below 5 nm. Another practical method of coupling to larger cavities utilizes a stripped optical fiber core, usually tapered, and puts the fiber close to the cavity to access a mode. Angle-cleaved facet fibers can also support prism-like coupling scheme to couple to a cavity. The latter processes are usually used to couple light into micromachined cavities through manual alignment procedures which makes the process more complex and susceptible to changes of coupling magnitude over time.

In general, a typical coupled structure such as in Figure 8(a) can be used to introduce the coupled mode theory (CMT) and analyze the dynamics of response in presence of an access path. An integral part of resonator-waveguide coupling scheme is depicted in Figure 10(a), in which two guiding structures are placed in the proximity of one another. For each waveguide, the dynamics of field's spatial evolution has a form of

$$\frac{da_1}{dz} = -j\beta_1 a_1 + \alpha_{12} a_2, \quad (38)$$

$$\frac{da_2}{dz} = -j\beta_2 a_2 + \alpha_{21} a_1, \quad (39)$$

in which a_i , $i=1,2$ is normalized so that $|a_i|^2$ is the power in each mode. It is rather straightforward to show that conservation of energy imposes the coupling coefficients to be such that $\alpha_{21} = -\alpha_{12}^*$. Using perturbation theory, it can be shown that

$$\alpha_{12} = -\frac{j\omega}{4} \int_{WG1} (\epsilon_{WG} - \epsilon_B) \mathbf{E}_2 \cdot \mathbf{E}_1^* dA = -j\Delta \quad (40)$$

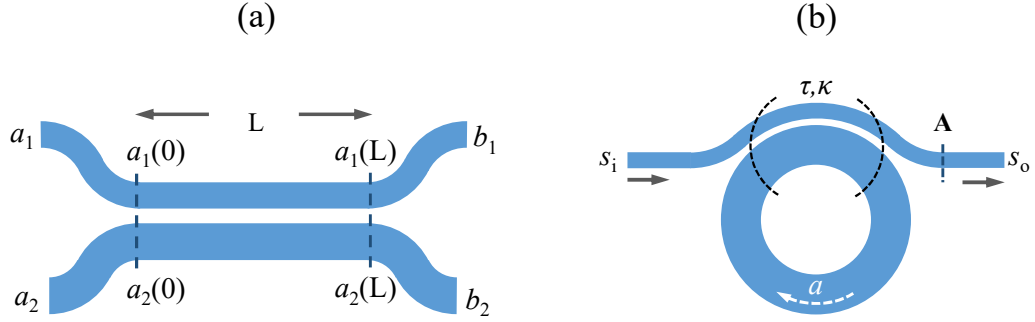


Figure 10: (a) Schematic of a typical directional coupler. (b) Top view of a typical waveguide-coupled microring resonator. The extended coupling length between access waveguide and microresonator can enable coupling to different radial mode orders.

Solving the Equations 38 and 39 for a pair of identical waveguides with an effective length

L of constant coupling, fields are found as

$$a_1(L) = \cos(x) a_1(0) - j \frac{\Delta}{|\Delta|} \sin(x) a_2(0), \quad (41)$$

$$a_2(L) = -j \frac{\Delta}{|\Delta|} \sin(x) a_1(0) + \cos(x) a_2(0), \quad (42)$$

in which $x = |\Delta|L$, neglecting the overall propagation phase in the coupling length ($\exp(-j\beta L)$) for simplicity, as well as any coupling induced phases. Defining τ and κ as $\cos(x)$ and $\frac{\Delta}{|\Delta|} \sin(x)$, a transfer matrix can be defined for the input-output of the Figure

10(a) as ⁴

⁴ In the transfer matrix, τ is defined as a dimensionless through port coefficient, and should not be confused with subscripted time constants in other equations.

$$\mathbf{T} = \begin{pmatrix} \tau & -j\kappa \\ -j\kappa & \tau \end{pmatrix}, \quad (43)$$

Therefore, the overall coupler can be defined by

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} a_1(L) \\ a_2(L) \end{pmatrix} = \mathbf{T} \begin{pmatrix} a_1(0) \\ a_2(0) \end{pmatrix} = \mathbf{T} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}. \quad (44)$$

The structure shown in Figure 10(b) is an example of using such a configuration to define a waveguide-resonator pair, in which the nearby waveguide provides another leakage path for the optical energy stored in the cavity. The new path defines a new loss⁵ process which can be modeled by a coupling Q (Q_c). Assuming P_0 power circulating in the resonator of Figure 10(b) with the perimeter of L_R , it is easy to find that the overall energy stored in the cavity has the form as

$$W = \int_{T_{roundtrip}} dt P_0 = P_0 \frac{n_g L_R}{c}. \quad (45)$$

As Equations 43 and 44 suggest, $|\kappa|^2 P_0 = K P_0$ is the power lost through coupling. Using Equation 29, the coupling quality factor has a form of

$$Q_c = \frac{2\pi n_g L_R}{\lambda_0 K}, \quad (46)$$

from which the cavity coupling decay time is defined as $\tau_c = Q_c / \omega_0$. Overall, a cavity may lose the stored energy due to several different mechanisms, which includes material loss, scattering loss, radiation loss, and coupling loss. Therefore, the overall time constant, or decay time, of a cavity has a form of

$$1/\tau_T = 1/\tau_s + 1/\tau_m + 1/\tau_r + 1/\tau_c = 1/\tau_i + 1/\tau_c, \quad (47)$$

which results in a similar relation to derive the inverse total Q of a cavity as the sum of inverse Q s of loss mechanisms. It is also useful to separate coupling Q from other

⁵ This process is not a “loss” mechanism (as opposed to material loss for instance) in the strict sense of the term, as the optical power is neither converted to another form, nor spatially dispersed. However, it can be modeled in the same fashion.

contributing loss mechanism, and consider the inherent loss mechanisms as the intrinsic Q factor—i.e., Q_i .

To formulate the dynamics of waveguide-cavity response under a forced frequency input, the temporal notation of coupled mode theory is useful. Inside the resonator, the field dynamics can be described by

$$\frac{da}{dt} = j\omega_0 a - \left(\frac{1}{2\tau_i} + \frac{1}{2\tau_c} \right) a + \kappa_c s_i, \quad (48)$$

in which, s_i is defined so that the input power is $|s_i|^2$. Also, a is defined such that $|a|^2$ represents the total energy of the cavity. Similarly, the optical field at an arbitrary cross-section of the output waveguide—e.g., cross-section A in Figure 10(b), has a temporal dynamic as

$$s_o = s_i - \kappa_c^* a. \quad (49)$$

In both Equations 48 and 49, κ_c is the rate of field coupling between the resonator and waveguide, which can be found from Equation 47 as ⁶

$$\kappa_c = (2\tau_c)^{-\frac{1}{2}}. \quad (50)$$

It is worth noting that in the development of CMT, the coupling coefficient appears in three different forms, and according to each a corresponding relation is formulated. One definition is introduced in Equations 38 and 39 to describe the coupling per length (Equation 40). Another notion is utilized to directly relate fields (and energies) of each coupled structure as in Equation 43. The latest format which appears in Equations 48 and 49 defines the coupling as the rate through which the power is transferred, or lost, in an optical structure (Equation 50). Recognizing each coupling coefficient from another, and

⁶ Throughout this work, the time constant is primarily defined for power. The factor 2 multiplied to the time constant is due to κ_c representing the optical field.

appropriate use of each is the key to define a coupled mode relation which properly describes the dynamics.

With an input frequency of ω , the steady-state waveguide-coupled-cavity response can be found by solving the coupled mode Equations 48 and 49 in the frequency domain, from which the transmission of the coupled cavity has a form of

$$T(j\omega) = \left| \frac{s_o}{s_i} \right|^2 = \left| \frac{j(\omega - \omega_0) + \left(\frac{1}{2\tau_i} - \frac{1}{2\tau_c} \right)}{j(\omega - \omega_0) + \left(\frac{1}{2\tau_i} + \frac{1}{2\tau_c} \right)} \right|^2. \quad (51)$$

Replacing the time constants with their corresponding quality factors, the transmission is rewritten as

$$T(j\omega) = \left| \frac{2j \left(\frac{\omega}{\omega_0} - 1 \right) + Q_i^{-1} - Q_c^{-1}}{2j \left(\frac{\omega}{\omega_0} - 1 \right) + Q_i^{-1} + Q_c^{-1}} \right|^2. \quad (52)$$

The relation between the transmission, intrinsic, and extrinsic quality factors determines two different regimes for a coupled microcavity. When Q_c is larger than Q_i , the amount of power coupled to cavity is not high enough to compensate the intrinsic losses, and therefore the cavity is under-coupled. As the result, the overall transmission is nonzero at the resonance, and the outgoing signal is in phase with the input. In contrast, when Q_c is smaller than Q_i cavity receives more power than needed to compensate the intrinsic losses. The cavity is over-coupled, and the output signal is in π phase shift of the input signal.⁷ The transmission amplitude however remains nonzero as in the under-coupled case. The point in which the transmission goes to null is called critical coupling in which quality factors are equal. For the critical coupling, it is trivial to show that

$$Q_i = 2Q_T. \quad (53)$$

⁷ The comment on phase neglects the propagation phase introduced between the input and output.

Figure 11 shows the spectral response of a typical microresonator for different coupling regimes. As briefly introduced in the previous Section, Equation 52 provides a straightforward method to experimentally measure the quality factor. The full-width half-maximum (FWHM) of the transmission can be properly obtained from the recorded spectrally resolved transmission response. Equation 52 shows that the FWHM is related to Q s through

$$\omega_{FWHM} = \frac{\omega_0}{Q_i} + \frac{\omega_0}{Q_c}. \quad (54)$$

Knowing the transmission value at the resonance, the second relation between Q s is

$$T(j\omega_0) = \left| \frac{Q_i^{-1} - Q_c^{-1}}{Q_i^{-1} + Q_c^{-1}} \right|^2. \quad (55)$$

Equations 54 and 55 can determine Q values. However, the absolute value function of the Equation 55 suggests a pair of values for Q_c and Q_i according to under-coupled or over-coupled cavity condition. To find the coupling regime, a coarse simulation can be employed, or the coupling is experimentally swept for the device under test.

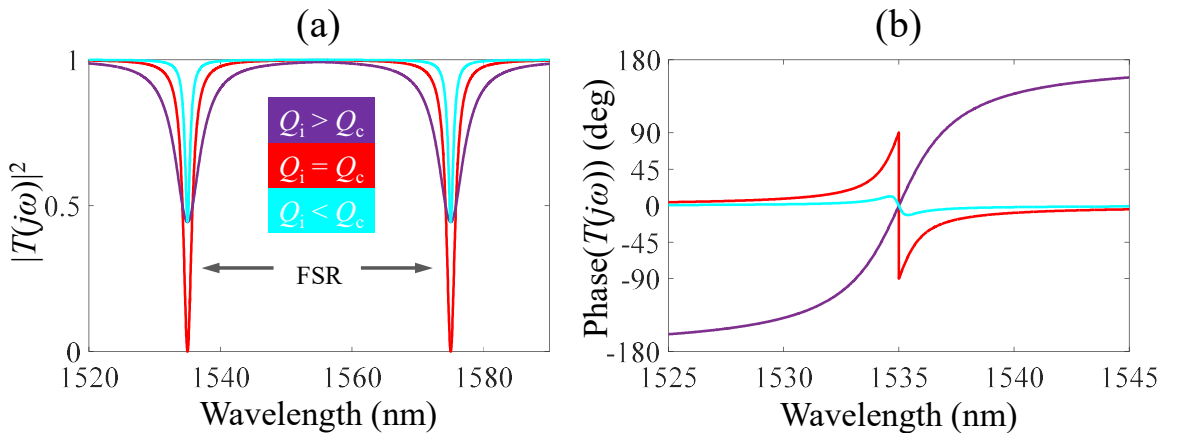


Figure 11: Computed spectral response of a typical resonator. The intrinsic Q is 2×10^3 . (a) Power transmission response of an under-coupled, over-coupled and critically coupled structure. (b) Corresponding transmission phase response in each regime near a resonance wavelength.

It is useful to find the field enhancement through the analysis provided by CMT and confirm the rather qualitative derivation of Equation 35. Solving Equations 48 and 49, the energy inside the resonator has a form of

$$a(j\omega) = \frac{s_i(j\omega) \times 2\kappa_c / \omega_0}{2j \left(\frac{\omega}{\omega_0} - 1 \right) + Q_T^{-1}}. \quad (56)$$

It is also clear that the circulating power in the resonator is the total energy divided by the cavity roundtrip time. At the resonance, the ratio of the power of resonator to the input power—i.e., the power field enhancement is

$$\frac{P_R}{P_i} = \frac{|a(j\omega_0)|^2 / T_{roundtrip}}{|s_i(j\omega_0)|^2} = \frac{(2\kappa_c Q_T)^2}{\omega_0^2 T_{roundtrip}}. \quad (57)$$

Using Equations 36 and 50, the above relation can be rewritten as

$$\frac{P_R}{P_i} = \frac{Q_T}{\pi Q_c} F, \quad (58)$$

which confirms the power enhancement in a cavity is proportional to the finesse.

With the extensive theoretical study presented in this chapter, the basic understanding required for integrated photonic design is properly formulated. The mathematical vision developed here is next used to analyze novel photonic systems, in which extensions of the fundamental relations are employed to design and characterize photonic devices and systems.

CHAPTER III

DOUBLE LAYER SILICON MATERIAL PLATFORM FOR RECONFIGURABLE AND PROGRAMMABLE INTEGRATED PHOTONICS

With the brief overview on enabling and limiting features of Si in Chapter 1, solutions should be sought through material platforms beyond a single-layer Si on oxide. In the current chapter, the reconfiguration in Si photonic is briefly discussed, and limiting factors in single-layer Si platform to enable reconfigurable devices are presented. To address such shortcomings, a universal solution—i.e., double layer c-Si hybrid material platform, is proposed and demonstrated, which can further extend to enable other important applications such as high speed and compact Si-based devices and integrated micro-sensors.

3.1 Tunable and Reconfigurable Integrated Silicon Photonics

The emergence of integrated Si photonics as a viable solution for data transmission has made a strong case to develop and demonstrate different building blocks of optical signal processing on the Si chip. Optical data transmission at high rates is most often implemented through coarse and dense wavelength division multiplexing (WDM) method, as the localized light can make use of a significant bandwidth available in the near-IR telecom band (4.5 THz bandwidth is offered only by C-band), and transmit through several WDM channels simultaneously. To implement WDM schemes optimally, one important requirement is the capability to reconfigure photonic components. In a typical WDM

system, reconfigurable modulation, filtering, switching, and multiplexing are among the basic system requirements, and a considerable amount of research is dedicated to implement such elements in Si platforms. For instance, reconfigurable multiplexer, an essential element in optical networks, has been demonstrated using microring resonators [57]. Another approach is to use arrayed waveguide gratings [58], implementation of which can be extended into SOI platform. There is also an increased level of research to realize reconfigurable multi-channel filters and switches on Si as fundamental blocks of an optical transceiver system [59-64].

Despite the variety of device architectures, system-level design contrasts, and implementation differences, the reconfiguration mechanism of such SiP devices mainly utilizes the thermo-optic effect of Si. For tuning purposes, Si offers a strong thermo-optic effect with the corresponding coefficient of $\frac{dn}{dt} = 1.78 \times 10^{-4} \text{ K}^{-1}$ [65] at the room temperature. To actively control the wavelength of a typical integrated Si device, a micro-heater is fabricated near the structure, usually within 1 μm distance. The heat is primarily generated through resistive dissipation in the microwire, and is delivered to the device through heat conduction of an interface material.

While thermal reconfiguration is the most commonly used mechanism of optical control and fine tuning, it poses several limitations on the overall performance of a PIC. The generation of heat using integrated microheaters often requires high current densities in the resistive section, which triggers electromigration, generates high heat gradients, causes partial melting at hot spots, all leading to increased rate of failure. Also, the incorporation of microheaters to the PIC requires several new fabrication steps, including the deposition of an electrically insulating, thermally well-conductive material on top of Si

with a controlled thickness, successive deposition of highly resistive and highly conductive metals at desired locations to form microheaters, and final cladding of microheaters, each adding a fresh challenge to integration process.

On the other hand, fine tuning of devices due to fabrication deviations in size and shape, as well as natural thermal fluctuations is necessary. For instance, in a silicon microdisk resonator with radius $R = 5 \mu\text{m}$, fabricated in the SOI platform with 250 nm Si thickness, a resonance at 1550 nm would shift about 0.3 nm for each 1 nm change in radius. This is significantly important considering that a typical EBL system has a resolution of ~ 5 nm. Considering other imperfections in fabrication, it is clear that any device with an actual target wavelength requires a tuning mechanism for proper functionality. For many practical applications, the post trimming of the device is a solution which can somewhat mitigate the high scale design versus fabrication discrepancies. However, the fine tuning must be done through active elements such as microheaters. The use of heater to compensate a mismatch to a specific band requires constant current passing through the heaters for extended periods of time, which puts a considerable burden on the overall power consumption of the PIC, as well as its implications on thermal management and reduced lifetime of the chip.

In order to address the reconfiguration and tuning issues, a novel platform based on two thin films of crystalline Si is envisioned. When an insulator such as SiO_2 is placed between the two, a capacitive element is formed and embedded close to the center of optical mode power distribution. On the other hand, Si is a semiconductor and therefore its refractive index changes with the concentration of free-carriers. The underlying physical principle is known as the free-carrier plasma dispersion effect. Si exhibits a strong free-

carrier plasma dispersion at telecom wavelength, and the change in the refractive index can be modeled by Drude theory. Experimental measurements follow the theory with a correction in the relative contribution of electrons and holes, which lead to the refractive index change to have a form of [66]

$$-\Delta n = 8.8 \times 10^{-22} \times \Delta N^{1.05} + 8.5 \times 10^{-18} \times \Delta P^{0.8} \quad (59)$$

in which, ΔN and ΔP denote the change in the electron and hole density (carrier.cm⁻³), respectively. Theoretically, utilizing such an effect in the proposed platform allows the reconfiguration and tuning with zero DC power consumption. Also, active elements can be introduced into the system through capacitive dispersion, results of which will be discussed in more details in upcoming sections.

3.2 Double Layer Crystalline Silicon Material Platform

The 3D schematic of a typical double layer Si (DLSi) waveguide is shown in Figure 12(a), where the low-index material—i.e., SiO₂, is placed between the two layers of c-Si that are extended horizontally. Figures 12(b) and 12(c) show the average power distribution profiles of fundamental modes in a single-mode waveguide formed in the DLSi platform with TE (i.e., electric field parallel to the substrate) and TM (i.e., electric field normal to the substrate) polarizations, respectively. As can be seen in the mode profiles, the TE mode is primarily confined inside Si, maximizing its interaction with changes in Si material. Therefore, the TE mode can support reconfigurable applications with higher efficiency, where the free carrier accumulation and depletion in Si through the capacitive element is used to form optoelectronic devices. On the other hand, the TM mode is highly confined inside the interface material, so it can support applications which demand light-matter

interaction—e.g., coherent light amplification and sensing, thanks to the high field enhancement.

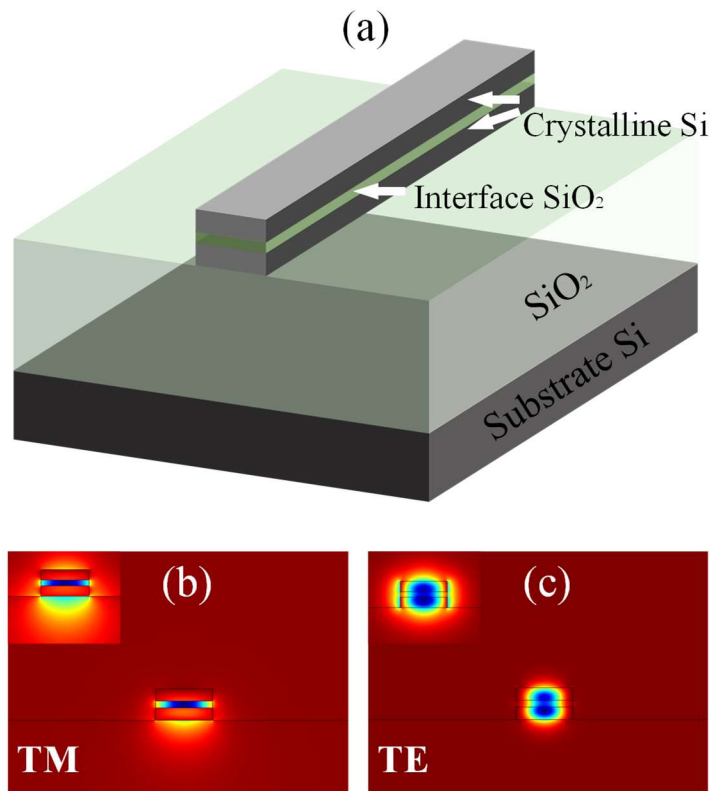


Figure 12: (a) 3D schematic of an integrated single-mode waveguide in the proposed DLSi platform. (b) and (c) Poynting vector distribution profiles of the TM and TE modes, respectively. The insets depict the dominant electric field component (E_y and E_x , respectively), for each mode. In simulations, the thickness of Si layers, the interface oxide, and the width of the waveguide are 110 nm, 60 nm, and 500 nm, respectively.

An additional design parameter in the proposed DLSi structure is the thickness of the oxide layer, as it can control the level of field confinement in Si (TE polarization) or in SiO₂ (TM polarization). For instance, the simulated mode energy distribution indicates that by reducing the oxide thickness from 100 nm to 20 nm, the TE mode confinement increases from 58% to 75%. The same change in the oxide thickness results in the reduction of the confinement of the TM mode in the oxide from 36% to 25%. Therefore, the thickness of interface oxide can be optimized to increase the efficiency for a specific application through mode engineering.

3.3 Platform Development

Figure 13 depicts the envisioned process flow for the DLSi platform, which is based on the bonding of two crystalline SOI dies with a thin oxide interface. The oxide thickness targeted in the proof-of-concept demonstration is 60 nm. The selected oxide thickness value can support good confinement for the TE mode (mainly in the Si regions), yet deliver decent confinement of the TM mode (in the oxide). Nevertheless, a similar platform can be alternatively developed using the deposition of amorphous or poly-crystalline Si on the interface dielectric to form the top Si layer in the DLSi platform [67-69]. In the proposed approach of this work, the integration of c-Si material in both active layers has the significant benefit of minimal additional optical loss (compared to polysilicon or amorphous Si material) to maintain the high material quality of crystalline Si and improve optical performance.

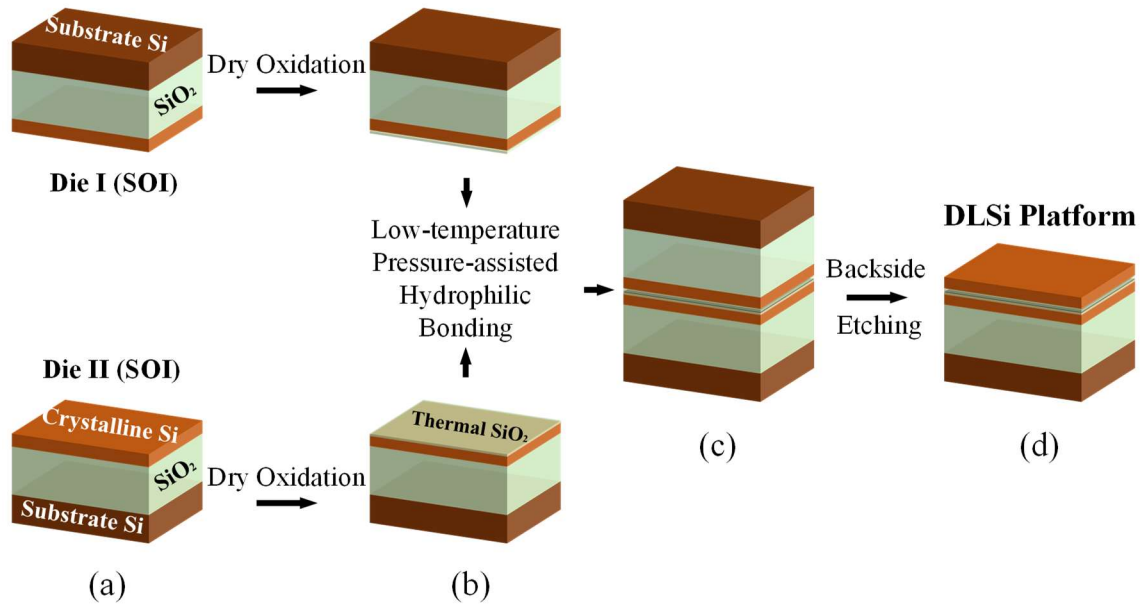


Figure 13: 3D schematic of the process flow to develop DLSi platform. (a) A pair of SOI dies with the same size are diced out of an SOI wafer (b) A thin layer of oxide film (30 nm) is grown on Si through thermal oxidation. (c) Assisted by pressure at an elevated temperature, dies are fused in one. (d) Schematic of the bonded platform after removing the substrate Si and the BOX layers from the backside of the top SOI die (Die I).

3.3.1 Optimization of Thermal Oxidation

Having the target thickness of layers in the envisioned DLSi platform as 60 nm and 110 nm for interface oxide and two Si layers respectively, the thermal oxidation is used to bring down the initial thickness of two SOI dies. The target thickness is met in two steps. First, the c-Si thin film of an 8 inch SOI wafer (250 nm c-Si on top of 3 μ m BOX layer, commercially available from Soitec, Inc.) is needed to be thinned down to 124 nm. The thin-down process is performed by thermal dry oxidation, and subsequent wet etching of the thermal oxide in Buffered-Oxide-Etchant (BOE). Here, 14 nm difference from 110 nm target thickness of Si is intended for the second step—i.e., interface oxide growth. After the initial oxidation step of the thin-down process, the wafer is covered with Red First Contact® polymer (Photonic Cleaning Technologies) and cleaved into 2×2 inch dies. The polymer protects the top surface from cleaving debris, and can be peeled off without leaving any residue after manual dicing. A second thermal oxidation process is used to grow high-quality interface oxide of 30 nm on top of two identical SOI dies. The second thermal dry oxidation reduces the Si thickness from 124 nm to 110 nm target value (with SiO₂ to Si conversion ratio of 2.2). After the two-step oxidation processing, the SOI dies are ready for bonding process.

An important feature of the oxidation process is the surface roughness of the grown oxide layer, since the effect of surface roughness on bonding quality has been theoretically studied and experimentally demonstrated [70, 71]. In general, as the surface roughness reduces, the overall bonding strength and energy increases. Quantitatively, the maximum empirical surface roughness value of 7 Å is found for the bondability regime of SiO₂

interfaces, remaining below which eliminates the need for chemical mechanical planarization (CMP).

Considering the effect of roughness on overall bonding quality, it is of critical importance to control the roughness introduced by all pre-bonding processes. In the DLSi platform development, thermal oxidation is monitored to quantify the roughness level introduced by the thermal treatment. For accurate measurement of roughnesses below 1 nm, Atomic Force Microscopy (AFM) method is used. AFM is an accurate method of measuring the 2D topology of a surface with sub-nanometer accuracy which utilizes a cantilever probe with a nanometer-size tip. The measured 2D map of the surface can be used to produce a value for roughness through statistical analysis.

Figure 14 shows the result of two different oxidation runs with identical values of target furnace temperature and duration. Here, the furnace temperature is fixed at 900° C, and the duration of the main oxidation step is 55 minutes. 4-inch Si wafers are used to perform oxidation and subsequent measurements. Ellipsometry is used after oxidation to generate a map of thickness values over the wafer area, results of which is shown in Figure 14(a) and 14(b) for Run 1 and Run 2, respectively. The average value of the grown oxide in both runs is 31.5 nm, while the standard deviation of the thickness is significantly higher for the Run 2 (2.2 nm) compared to Run 1 (0.28 nm). Figure 14(c) and 14(d) show the AFM phase response measurement of Run 1 and 2, respectively. The computed average roughness of Run 1 and 2 are approximately 2 and 4 Å, respectively. The observation suggests a correlation between average surface roughness and uniformity of oxidation across the wafer area. One explanation can point to the thermal turbulence and gas flow differences across the cross-section of the furnace, which can lead to nonuniform oxidation.

Such fluctuations can result in higher stress induced at the atomic scale and increase the roughness. To mitigate such issues, pre-run calibration of the thermocouples and heaters is needed, as well as ensuring laminar flow of gas inside the tube. Thus, accurate monitoring of oxidation thickness can increase the success rate of bonding and increase the platform quality through roughness reduction.

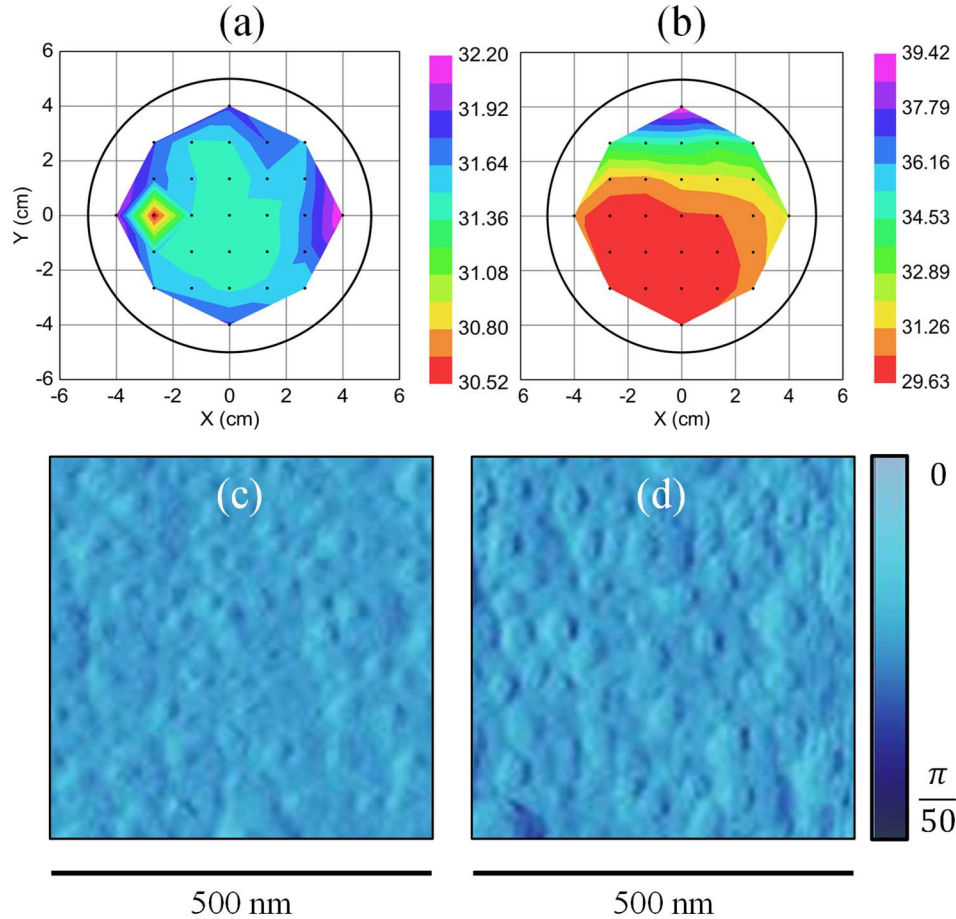


Figure 14: Ellipsometry and AFM measurements of a(n) (average) 315 Å SiO_2 layer thermally grown over two Si wafers in two separate runs: Run 1 ((a) and (c)), and Run 2 ((b) and (d)). The roughness is visibly higher in the Run 2, which has higher non-uniformity over the thickness. For AFM, the phase response of the probe is used to reveal topographic features, since the phase shift is proportional to the amount of inelastic energy transferred from the tip to the sample surface. Such local energy dissipation can be related to surface chemistry changes, visco-elastic changes, and topography changes.

3.3.2 Hydrophilic Bonding and Backside Etching

To ensure strong bonding with minimal voids, the prepared dies are required to be rigorously cleaned, followed by a chemical activation step. The cleaning step starts with 15 minutes of sonication in Acetone, Methanol and Isopropyl alcohol (repeated after changing the solution) followed by a modified RCA process [72] in which the dies are first immersed in SC-1 solution ($\text{H}_2\text{O}:\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ 5:1:1) at 75°C for 20 minutes, rinsed with DI water, then immersed in SC-2 solution ($\text{H}_2\text{O}:\text{HCl}:\text{H}_2\text{O}_2$ 6:1:1) at 75°C for 20 minutes, rinsed with DI water, and finally blow-dried with N_2 . High-quality quartz beakers are used during SC-1 and SC-2 to reduce contamination from alkali metals [72].

The chemical activation process is next used to support a low-temperature wafer bonding. Envisioned steps of the activation process are specifically selected to increase O-H bonds over the surface of the interface oxide layer, which later contribute to the density of bonds over mating surfaces. In the first step, 30 seconds of exposure to O_2 plasma is performed in a reactive ion etching (RIE) tool [73], followed by a dip in NH_4OH to increase hydrophilicity [74]. The dies are blow-dried with N_2 and placed in contact with each other, and bonded in a Karl Suss SB6 bonder (Figure 13(b)). The bonding process is carefully optimized, and the razor-blade test [75] is used to evaluate the bonding strength. After placing the bonding pair inside the bonder chamber, we pump down the chamber to 5×10^{-5} mbar, followed by slowly ramping up the applied force on the mated die to impose 4 bars of pressure at the room temperature. After 30 minutes, the bonder temperature is also ramped up to 400°C and the bonding pair is held for 8 hours to increase the bonding strength. Prior to bonding, SOI dies are handled from the back side using a vacuum tweezer to prevent chipping and particulate contamination.

As shown in Figure 13(d), the substrate Si and BOX of the top SOI die are next to be removed. The backside removal includes the Bosch processing to remove substrate Si, followed by submerging the die in BOE to etch oxide (BOX) layer, concluding the DLSi platform development. Figure 15 shows a processed DLSi die and the corresponding cross-sectional image of the material stack under SEM.

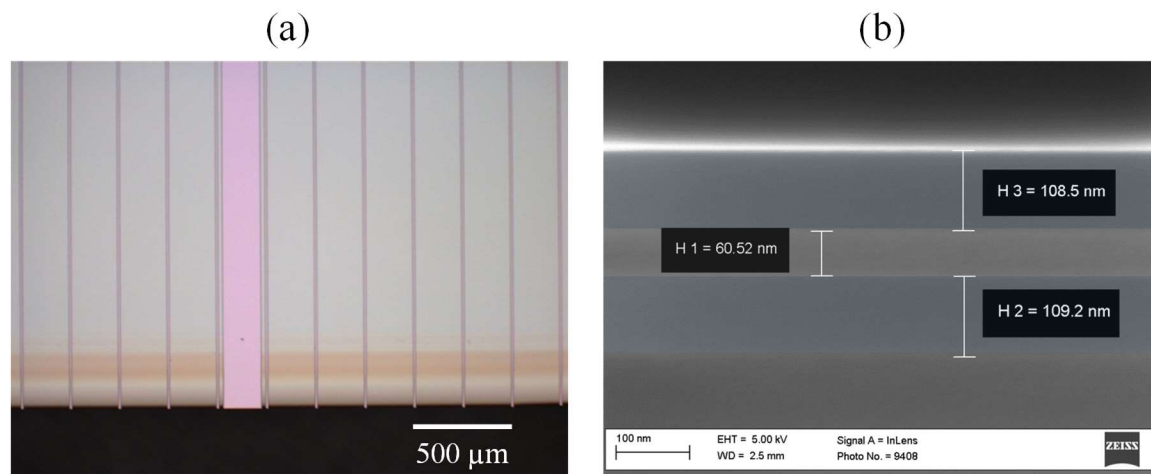


Figure 15: (a) Optical micrograph image of a DLSi sample. Channels are etched in the bottom SOI layer prior to bonding to reduce void formation, which will be discussed in detail in the next Chapter. As can be seen in the microscope image, the bonding yield is close to 100% with no visible void formed. (b) Cross-sectional SEM of the processed DLSi platform. By precise control of the fabrication processes, the thickness of the developed heterostructure has met the target values within ± 1.5 nm margin.

3.4 Proof-of-Concept Devices in The DLSi Platform

Following the successful development of the proposed DLSi platform, the quality of platform development process can be verified through fabrication of nanophotonic devices. A suitable device for such a purpose is the WGM microresonator, as the corresponding Q factor can be readily used to evaluate optical losses, and serve as a figure of merit for the platform and device fabrication. The same device with added electrical contacts to

electrically access the top and bottom Si layers can work as a tunable microresonator to showcase reconfigurability in the platform.

3.4.1 Fabrication and Characterization of High- Q Microresonators

The process flow to fabricate a typical nanophotonic device on DLSi platform (such as microdisk resonators, waveguides, and grating couplers) is based on EBL and dry etching. The patterns are initially defined in a CAD file, which is next transferred to the chip by electron beam lithography (EBL using a JEOL JBX-9300FS system) with a 200-nm thick spin-coated hydrogen silsesquioxane (HSQ) layer (6% from Dow Corning Chemicals), which is a negative electron-beam resist with chemical properties similar to SiO_2 . The top and bottom Si layers of the devices are etched using Cl_2 gas chemistry in an inductively coupled plasma (ICP) system (by Plasma-Therm), and the thermal SiO_2 interface is etched using CHF_3/Ar gas combination in a reactive ion etching (RIE) chamber (by Oxford Instruments). It is particularly important to switch between optimized recipes to etch Si and SiO_2 , as the oxide etching with an unoptimized recipe can adversely affect the etch quality of the bottom Si layer of the DLSi platform and reduce the overall quality of etching. For instance, the ICP etching of Si can etch SiO_2 as well. However, the etch rate selectivity of the Cl_2 -based etch recipe for SiO_2 with respect to Si is high (etch rate measurements: etching time = 180 seconds, Si thickness = 235.5 nm, SiO_2 thickness = 30.8 nm, selectivity (Si/SiO_2) = 7.62). Since the physical etching of SiO_2 in an ICP chamber can introduce roughnesses on the etched surface, the high selectivity amplifies such issue as the etch surface transitions from interface oxide to bottom Si. Alternatively, by switching to an optimized SiO_2 etch recipe—e.g., the recipe with CHF_3/Ar gas combination, the selectivity can be substantially reduced (etch rate measurements: etching time = 120

seconds, Si thickness = 57 nm, SiO₂ thickness = 42.3 nm, selectivity (Si/SiO₂) = 1.35). Using the optimized oxide etching, smoother sidewalls can be achieved, which enables lower optical losses and higher efficiency. After dry etching steps, devices are coated with flowable oxide (FOX-16 from Dow Corning) as the top cladding material. SEM images of Figure 16 depict an aerial view of a waveguide etched in DLSi, with its cross-sectional SEMs for two different bonding efforts, one with target 60 nm overall oxide thickness, and second with target 30 nm.

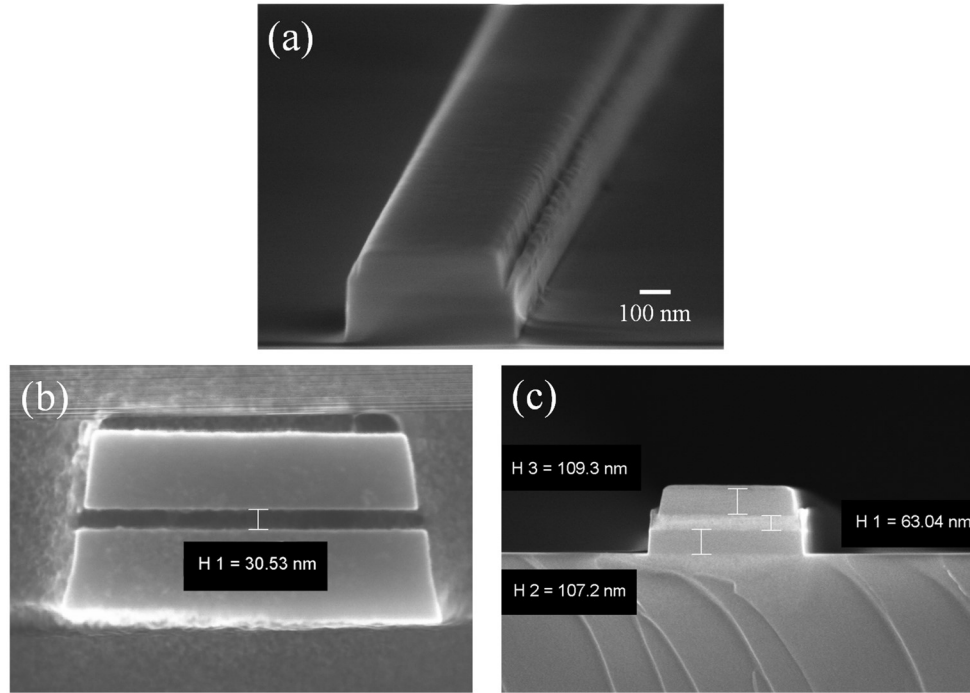


Figure 16: (a) Bird's-eye SEM view of a DLSi waveguide structure at the facet of the chip (the tilt angle is 60°). (b) Cross-sectional SEM of an etched and FOX-coated DLSi waveguide. The thickness of SiO₂ interface layer is reduced to 30 nm in the platform development. (c) Cross-sectional SEM of an etched DLSi waveguide with 60 nm oxide layer.

To assess the optical quality of the DLSi platform and hence the quality of the bonding process, different resonators are fabricated and corresponding Q 's are measured. Microrings with a wide range of radii from 2 μm to 10 μm coupled to access waveguides are fabricated. The fabricated resonators are next characterized by measuring the

transmission spectra of waveguide-coupled microresonators. Most of the resonance-based structures studied in this work are based on the straight waveguide-resonator coupling scheme. The width of waveguides in fabricated devices is 500 nm, and the gap between the waveguides and the resonators is swept between 100 nm to 350 nm to achieve critical coupling. Characterization of the fabricated devices is done using a swept-wavelength transmission characterization setup near 1550 nm wavelength. A fiber polarization controller is used to adjust the input polarization for the characterization. Tapered fibers are used to couple light into and out of the cleaved facets of the bus waveguides. Alternatively, input/output focusing grating couplers are used to couple coherent light in and out of the access waveguides, eliminating the need for facet cleaved edges of the chip. The output light is detected using a variable gain photo-receiver and sent to a computer through a data acquisition (DAQ) card.

Figure 17(a) shows a typical single-mode microring resonator etched in DLSi platform. In Figure 17(b), the experimental spectral response of a 10 μm radius multimode microring resonator (ring width: 3 μm) is shown. The resonator is coupled to an access waveguide with the width of 500 nm, and the gap between waveguide and cavity is 120 nm. Figure 17(c) shows the magnified plot of the transmission for one of the resonances that is close to critical coupling with an intrinsic Q of 2.35×10^5 . The red curve shows a Lorentzian resonance fitted to the experimental data to determine the Q factor accurately. To the best of our knowledge, this is the first demonstration of a high- Q microring on any double layer Si platform. It is also interesting to observe the spectral evolution of different modes of the waveguide coupled cavity. As highlighted by the red dashed ellipses in Figure 17(b), the cavity supports at least 4 radial mode orders with moderate and high Q factors,

repeated in different FSRs associated with each radial mode order, which explains the walk of each mode compared to another in different FSRs of the family.

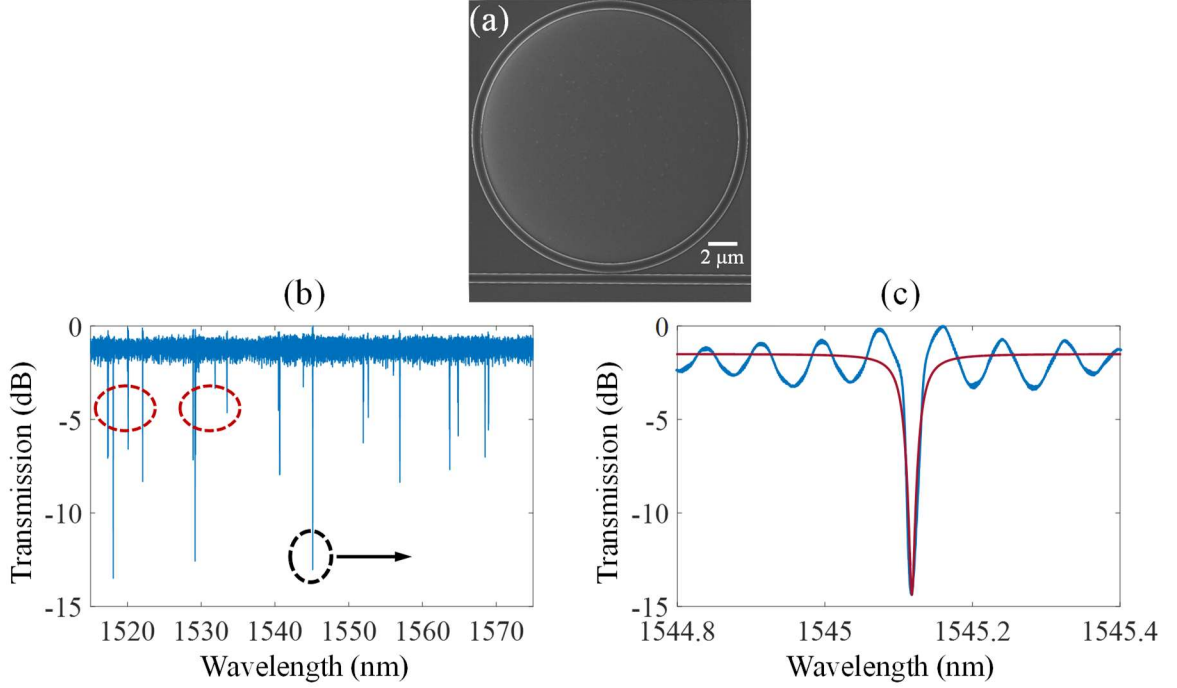


Figure 17: (a) SEM image of a waveguide-coupled single-mode ring microresonator ($R = 10 \mu\text{m}$) fabricated in the DLSi platform. (b) The spectral response of a $10 \mu\text{m}$ radius multimode microring (ring width = $3 \mu\text{m}$) for the TE polarization. The waveguide width is 500 nm , and the waveguide-cavity gap is 120 nm . (c) The transmission spectrum for the resonance marked in (b) with the black dashed ellipse. The red curve shows a Lorentzian function fitted to the experimental data, which confirms $Q_i = 2.35 \times 10^5$.

If the size and area of cavity can be further extended for high Q performance, a $20 \mu\text{m}$ radius multimode microring (ring width: $5 \mu\text{m}$) is an option. The fabricated device is spectrally studied using the coherent tunable setup, and one of the high- Q mode families with an intrinsic Q of 3.2×10^5 is measured and confirmed through curve fitting. This shows a seven-fold increase compared to the previous reported result [76] and is the highest reported Q on any two-layer Si platform to-date, to our best knowledge. On the other extreme where compactness is favored, a microdisk of $2 \mu\text{m}$ radius is simulated using

COMSOL to confirm radiation loss limited Q above 10^6 . As the current state of-the-art fabrication limits the cavity Q below 10^5 for such size scale due to lithography and etching imperfections, a set of $2\text{ }\mu\text{m}$ disks are fabricated in DLSi platform. Characterization of the fabricated devices confirms the intrinsic Q of 3×10^4 for an under-coupled cavity. Such devices can enable a set of novel application including ultra-compact switches and resonant reconfigurable systems, as well as interesting applications in bio-sensing and light-matter interaction devices.

3.4.2 Tunable Compact Microresonator for Reconfigurable Photonics

As mentioned earlier in this chapter, a modification in the concentration of free carriers—i.e., the density of electrons and holes in a semiconductor, can alter the refractive index of the material. For a permanent change, otherwise called trimming, extrinsic carriers can be introduced in semiconductors by implanting donor or acceptor species by ion implantation or thermal diffusion. Another permanent approach is to deposit a thin layer of dielectric material, such as SiO_2 or SiN , and pattern it to achieve the desired tuning level in the device.

Alternatively, in dynamic systems where thermal variations and signaling may affect the devices during the optical processing, a dynamic tuning method, also called active trimming, is of interest. One solution that can enable such reconfigurability can be envisioned by the accumulation of free carriers in a capacitive structure, or carrier injection and depletion in a p-n junction, which can temporarily change the concentration of the carriers. Such an approach provides a fast and reversible method to tune optical devices. This tuning approach can be readily used to reconfigure microstructures fabricated in DLSi platform, thanks to the capacitive element embedded inside the optical mode.

To demonstrate carrier injection approach for tuning in DLSi platform, a compact microdisk structure is a suitable choice. The proposed structure comprises a small microdisk ($R = 3 \text{ }\mu\text{m}$) resonator which is coupled to an access waveguide with 500 nm width, and two focusing grating couplers, all fabricated in the DLSi platform. The fabrication of the passive structure follows the procedure described in Section 3.4.1. However, for the case of tunable microdisk, a 50-nm pedestal is selectively left un-etched around the microdisk on the bottom Si layer through another EBL step using ma-N 2400 (Micro Resist Technology) electron beam resist. To incorporate electrical contacts to the top and bottom Si layers, the sample is first spun with 800 nm of flowable oxide, which is patterned later using an EBL step to include openings to reach top and bottom Si layers. In the last step, Au contacts (with a thin Ti layer to increase adhesion and establish ohmic contact) are defined through e-beam evaporation and subsequent lift-off on a 2- μm thick layer of patterned PMMA. The characterization is performed by applying DC voltage to the capacitive element while wavelength is swept to monitor the resonance shift. Figure 18 shows the characterization results monitoring the first radial mode resonance shift in the waveguide-coupled microdisk. The resonance has an intrinsic Q factor of 7.5×10^3 .

The electro-optical characterization demonstrates the frequency tuning in excess of 100 GHz for the first radial mode of the microresonator. It is also important to consider the reconfigurable functionality is made possible with zero DC power consumption, as experimentally verified ($I_L \ll 3 \text{ nA}$). On the resonance shift of 32 pm at 5 V, it is important to mention the contrast to the next 5 V steps, as the shift increases to ~200-250 pm and follows a rather linear trajectory, as Equation 59 suggests. Since the interface oxide layer is heavily processed during the bonding, an increased level of trapped and charged states

is expected at the interface. In addition, dangling surface states and impurities of oxide can play a role in the reduction of initial free carriers in the Si layer, and therefore reducing the optical resonance shift for the first few volts of input. Another possible explanation can be the contribution of Schottky barrier formation at contacts, which reduces the effective voltage on the capacitive element, reducing the shift at low voltages. Overall, this can be addressed by using a bias point at a rather higher voltage to work in the linear domain, as well as enabling blue and red shift in the tuning.

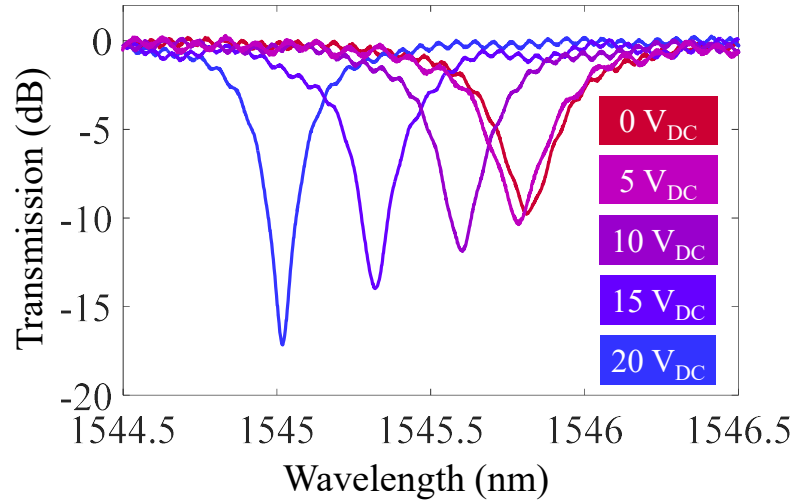


Figure 18: Reconfigurable resonance in a DLSi microdisk resonator ($R = 3 \mu\text{m}$) by free carrier accumulation. Voltage is changed from 0 to 20 V in 5 V increments.

With the demonstration of reconfigurable functionality, the DLSi platform development and quality check is complete. The novel features enabled by this platform can be used in various applications, such as integrated modulators, reconfigurable and programmable optical routers, filters etc. [77-80]. Also by doping the interface, a set of functionalities can be envisioned which includes on-chip lasing and photodetection. As shown in the current chapter, the possibilities offered by DLSi opens a new path toward

functional devices and systems beyond Si to address critical limitations and enhance the state-of-the-art photonic device and system design.

CHAPTER IV

VERTICAL INTEGRATION OF SILICON INTO SILICON NITRIDE PLATFORM

4.1 Cointegration of Silicon and Silicon Nitride

Since its advent in 1990s [81], the success of Si material platform for photonic applications has been critically hinged upon its compatibility with electronic device fabrication processes. Platforms based on Si have been increasingly used in conjunction with CMOS fabrication processes to form a large set of integrated photonic devices and systems. Due to the high refractive index of Si and the resulting high optical confinement, as well as its transparency over the optical telecommunication band (1.2-1.7 μm), photonic devices with submicron features have been successfully demonstrated for generation [82], high-speed manipulation [63,83,84] and detection of optical signals [85] in Si-based platforms. The tight confinement of light in Si leads to realization of compact photonic devices, reduced crosstalk and interference, and high integration density. However, it also makes the Si-based photonic devices more vulnerable to fabrication imperfections—e.g., sidewall roughness [86, 87].

On the other hand, the plasma dispersion effect in Si offers a rather fast way of changing its optical properties, particularly the refractive index [88]. By carrier injection in a forward-biased p-n junction or depletion in a capacitive (or equivalently a reverse-biased p-n junction) element, the refractive index of Si can be altered to realize high-speed modulation and switching [89-91]. In practice, the reverse-bias p-n junction/capacitive

modulation has gained more attention due to its negligible DC power consumption. However, the dynamics of the switching speed is limited by the drift dynamics ($R \times C$ lifetime), which is directly related to Si material through its electron and hole mobilities.

As briefly discussed in the Chapter I, while Si has proven to be an indispensable element for integration purposes, it is not the best solution for all the challenges facing the SiP industry due to its intrinsic shortcomings, some of which critically restrictive to the implementation of photonic systems on a chip. Among the most important is the intrinsic optical loss in Si (due to FCA and TPA), which limits its capability for high-power signal processing and supporting ultra-low-loss photonic devices. Also, Si exhibits optical nonlinearity at much lower optical intensities due to its large Kerr coefficient, which is detrimental to linear resonant optical devices, where the higher field enhancement is highly favored to improve device performance such as power efficiency and device sensitivity.

To address such shortcomings, various materials have been investigated which outperform Si in some of the key optical features (such as linear and nonlinear losses). Among alternatives, silicon nitride (SiN) is a promising platform for integrated photonic applications while being fully compatible with standard CMOS fabrication processes. Thin films of SiN (50 to 1500 nm), grown through the high-temperature, low-pressure chemical vapor deposition (LPCVD), demonstrate ultra-low bulk absorption considerably lower than that of Si in near-infrared (near-IR) and a wide transparency window that extends into the visible range [92]. Recent studies on LPCVD SiN confirm 1-2 orders of magnitude lower optical loss compared to Si at near-IR wavelengths [93-95]. A reasonably high refractive index contrast with the substrate silicon oxide (SiO_2) layer allows tight confinement of the

optical mode while reducing the loss due to fabrication imperfections such as the sidewall roughness, thus enabling the dense integration of photonic devices [96].

On the other hand, due to small nonlinear losses of SiN as a high bandgap dielectric, its high Kerr-nonlinearity figure-of-merit, and its lower dispersion compared to Si, a diverse set of nonlinear applications can be envisioned on the chip. Several seminal works have demonstrated optical parametric oscillation, supercontinuum generation and optical frequency comb generation on SiN platform, which outperforms other available platforms in the power threshold, spectral purity, compactness, frequency span, and ease of integration [97-102]. Especially, the integrated optical frequency comb generation is of practical interest in optical interconnects, transceivers and links. Similar to its off-chip counterpart [103], an integrated comb offers a coherent phase-locked multi-frequency source that can be used in various integrated photonic systems for telecom applications [104,105]. Also, integrated optical comb source offers unmatched practical solutions for on-chip pulse formation and manipulation [106], high-accuracy optical clocks [107], and high-signal-purity RF and microwave sources [108].

In spite of such benefits, SiN lacks some of the key material characteristics required for optoelectronic devices—e.g., lack of a reliable tuning or high-speed modulation mechanism, due to its dielectric nature. One solution to resolve this issue is to develop a heterogeneous Si/SiN material platform, in which, different devices are fabricated in different material layers based on the desired functionalities. Recently, two different approaches for integration of Si and SiN based on 1) the direct deposition of SiN on top of Si [109], and 2) back-end integration of SiN beneath Si [110] have been proposed. In the first approach, after processing the Si device layer of a silicon-on-insulator (SOI) substrate,

the SiN layer is deposited on top of the Si layer (using high-temperature LPCVD), patterned, and annealed at 1100°C in N₂/O₂ ambient to minimize the material loss. This high-temperature step of the fabrication sequence is not CMOS-compatible. Also, the additional oxygen annealing oxidizes the active Si layer uncontrollably and changes the electronic and optical characteristics of the designed devices. Alternatively, the second approach uses a bonding process to transfer a layer of Si on top of a patterned SiN layer after planarization of the sample. While the second approach resolves the issue of high-temperature fabrication process, the reported devices to-date have been based on using a relatively thick—e.g., 600 nm, SiO₂ interface layer. Such thick buffer layers result in weak coupling of the photonic devices in different layers and impose long interlayer couplers (to couple light efficiently between Si and SiN layers) for low-loss applications. For example, an efficient interlayer coupler in such a platform can be 0.3 mm long [110]. On the other hand, such hybrid platforms are only demonstrated for thin SiN layers (40-100 nm) with low light confinement that does not support compact photonic devices. As an example, to achieve a resonator with a high intrinsic quality factor ($Q_{\text{int}} = 8 \times 10^7$), a ring resonator with the footprint of $20 \times 20 \text{ mm}^2$ is needed [111], while a ring of $1 \times 1 \text{ mm}^2$ area does not effectively confine light due to high radiation losses. As the result, such platforms are not suitable for dense integration of optoelectronic devices.

4.2 Crystalline Silicon on Silicon Nitride Material Platform

Considering the complementary features of Si and SiN, an interesting solution is to enable novel functionalities by developing a Si-on-SiN (SON) hybrid material and device platform in which a monolithic crystalline Si (c-Si) layer is integrated on an underlying SiN layer with a thin—i.e., ~50 nm, SiO₂ interface layer. In contrast to previously reported methods,

it is important to develop an approach which covers the entire device fabrication after the development of the hybrid material platform at the wafer-scale. The vision here is to entirely separate the platform formation and the device fabrication from one another, therefore. Such an approach considerably reduces the complexity of the fabrication process, and offers a platform similar to SOI to be used in various end-user defined applications.

4.2.1 SON Platform Development

Figure 19 shows an overview of the proposed fabrication process. In this work, the envisioned method decouples the material platform development from the device fabrication, and therefore is fully compatible with wafer-scale processing. Here the process is done at the chip-scale using smaller wafer pieces—e.g., 2" by 2", for simplicity. The fabrication begins with two wafers (or pieces): an SOI wafer and a bare Si wafer. The SOI piece, “Piece 1” in Figure 19(a), is first thinned down to the desired Si layer thickness (~230 nm) by thermal oxidation and wet etching of the oxide (Figure 19(b)). The thinned Si layer is then thermally oxidized to achieve a 30 nm SiO₂ layer on a 220 nm crystalline Si film (Figure 19(c)). The thickness of the Si device layer is chosen at 220 nm throughout this work to guarantee the single mode operation of Si waveguides. The bare Si piece, “Piece 2” in Figure 19(d), is first thermally oxidized to grow 5 μm of SiO₂. In the next step, 400 nm of stoichiometric SiN is deposited by LPCVD (using a Tystar silicon nitride deposition furnace) at 800°C with di-chlorosilane (DCS) and ammonia (NH₃) precursors at 1:3 gas ratio. The piece is further annealed at 1100°C to improve the quality of the SiN layer.

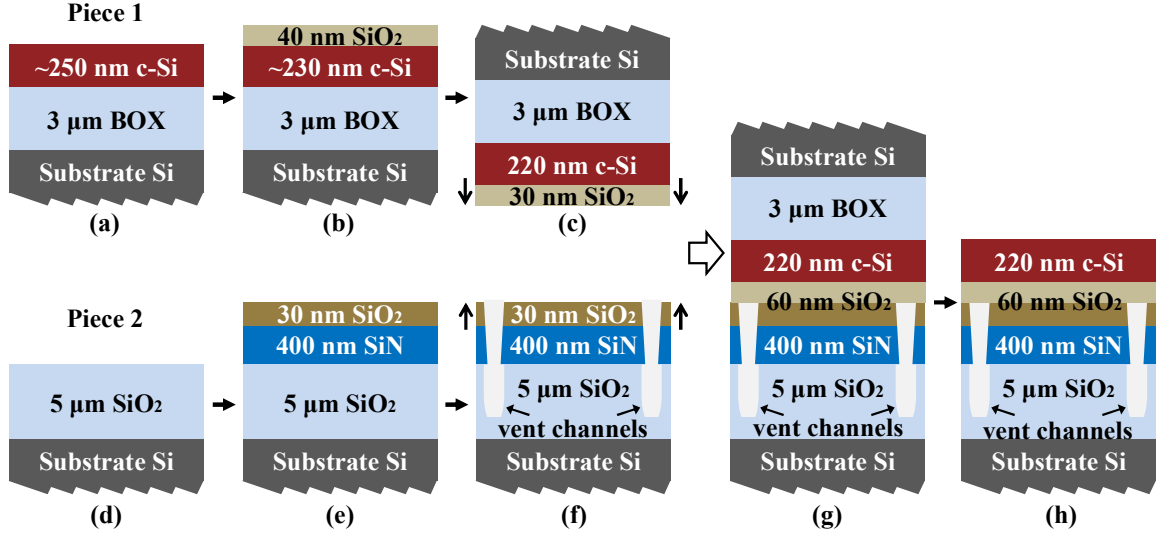


Figure 19: Summary of the SON platform fabrication process. (a) Piece 1, an SOI piece. (b) Dry thermal oxidation reduces the Si thickness. (c) Wet etching of SiO₂ followed by the second dry oxidation. (d) Piece 2, a bare Si piece, goes through oxidation to grow 5 μm of SiO₂. (e) An LPCVD SiN layer is deposited, followed by the deposition of a 30-nm SiO₂ layer using ALD. (f) Vent channels are introduced using optical lithography, dry etching of SiN, and wet etching of bottom SiO₂ layer. (g) Two pieces are bonded using a low-temperature hydrophilic bonding method. (h) Backside removal of the Si substrate followed by wet etching of the BOX layer.

To deposit a thin layer of SiO₂ on SiN (Figure 19(e)), we first test three different oxide deposition methods based on: 1) plasma-enhanced chemical vapor deposition (PECVD), 2) atomic layer deposition (ALD), and 3) hydrogen silsesquioxane (HSQ) spin coating. Since HSQ needs to be annealed in the N₂ ambient to convert to SiO₂, all three samples are annealed at 800°C for 3 hours after deposition. The optical and mechanical quality of the resulting oxide layers are then compared based on two figures of merit: 1) surface roughness, and 2) SiN/SiO₂ interface bond strength. The first parameter is extracted using atomic force microscopy (AFM), and the results are shown in Figure 20. The lowest average surface roughness (R_a) is obtained from HSQ annealing ($R_a = 0.239$ nm), while ALD ($R_a = 0.383$ nm) performs better than PECVD ($R_a = 0.745$ nm). The second parameter is measured by performing hydrophilic bonding on a pair of SiN on Si pieces with a thin–

e.g., 30 nm, SiO₂ layer followed by the blade-crack-opening test, which is a simplified version of the wedge-opening test [112]. The crack depth is measured to be 2.1 mm for the annealed HSQ sample, in contrast to less than 1 mm for the ALD sample. The result confirms that ALD oxide establishes stronger SiN/SiO₂ and SiO₂/SiO₂ bonding interfaces than the HSQ oxide. Therefore, ALD is chosen as the thin oxide deposition method due to its strong interface bond with the underneath SiN layer and a smooth interface layer, which is critically important for atomic-level bonding. In addition, ALD is the most precise method for deposition of a thin oxide layer with a desired thickness.

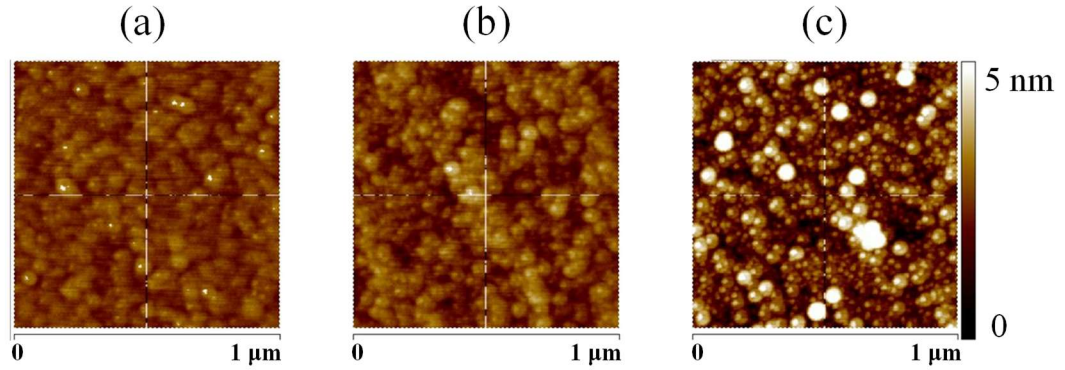


Figure 20: AFM images from the surface of a 30-nm SiO₂ layer on SiN, deposited by (a) HSQ annealing, average surface roughness (R_a) is 2.39 Å; (b) ALD, R_a = 3.83 Å; (c) PECVD, R_a = 7.45 Å.

In the next step, the hydrophilic fusion bonding technique is employed to fuse two pieces into one (Figure 19(g)). Details of the bonding step are similar to the DLSi bonding step, which is covered in the Chapter III. Here, the low-temperature nature of the technique is of particular interest for potential electronic integration. However, when the thickness of the interface oxide is reduced below 200 nm, the quality and yield of the low-temperature bonding drops [113]. SiO₂ is a fairly porous material, which can adsorb and transfer trapped and byproduct gases away from the interface. As the thickness of the SiO₂ is reduced, its

corresponding out-gassing capacity reduces too, resulting in an increased number of voids formed at the interface. To reduce the number of these voids, a set of horizontal vent channels are included and spaced 250 μm apart. As illustrated in Figure 21(a), these channels provide an exit path for trapped air and bonding byproducts to improve the quality of the interface bond. The introduction of vent channels enables void-free bonded interfaces and increases the total yield to close to 100% over the chip for oxide thicknesses as low as 30 nm (Figure 21(b)). It also reduces the mechanical stress in the SiN layer, which allows the wafer-scale bonding.

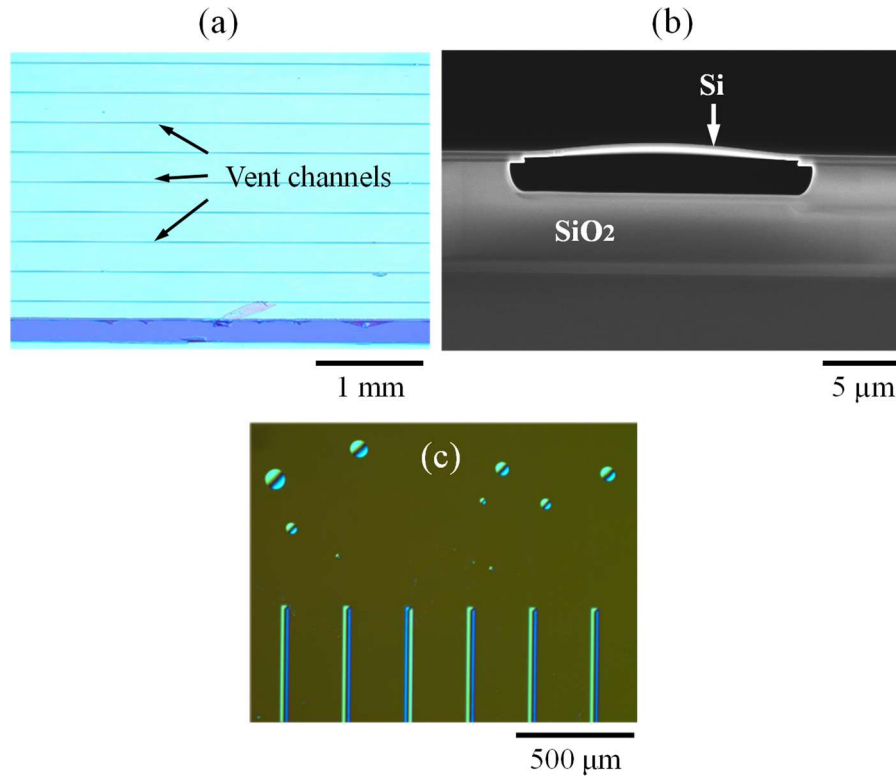


Figure 21: (a) Top view of a void-free bonded SON piece under optical microscope. Lines represent vent channels. (b) The cross-sectional SEM of a typical vent channel after bonding process. (c) A bonded sample at the edge where the vent channels are terminated. Bubbles can be clearly seen in the area without vent channels, while the channeled area is void-free.

Channels are added into the piece 2 after the thin ALD oxide is deposited on the SiN layer (Figure 19(f)). First, a layer of 1813 photoresist is patterned using UV (365nm)

lithography. Then, the SiO₂ and SiN layers are etched using reactive ion etching (RIE). In the next step, the piece is immersed in buffered oxide etchant (BOE) to remove 1 μm of the BOX layer at the bottom of the channels (Figure 21(b)). Finally, the photoresist is stripped away and both pieces go through the hydrophilic bonding process. After bonding the two pieces, the backside substrate of the SOI piece is removed using a sequence of wet and dry etching of Si, in which the SiO₂ layer acts as the etch-stop. The BOX layer is then wet-etched (Figure 19(h)). Figure 21(c) shows an optical micrograph image of the developed SON platform around an edge, where the effect of channels in venting the trapped gases is clearly visible.

4.3 Design of an Adiabatic and Broadband Interlayer Coupler

Moving forward from the single layer optical platform to multilayer platforms, it is necessary to develop a 3D integration approach for various applications. In photonic integrated circuits implemented on hybrid coplanar material platforms, the interlayer coupler with high coupling efficiency is an essential component. Such couplers can route light among different material layers with very small loss, enabling ultra-low-insertion-loss hybrid PICs. The feasible approaches for realization of the interlayer couplers can be categorized into propagating or evanescent field coupling. In the propagating field coupling, the optical power is transferred via a propagating mode. In this category, one method involves the use of reflective surfaces to deflect light beams out-of-plane for chip-to-chip light coupling, which can be tailored to be used for intra-chip layer-to-layer light coupling. Micro-mirrors are fabricated by laser ablation [114], mechanical milling [115], or wet etching [116, 117], and waveguide-to-waveguide coupling losses as low as 2.5 dB are achieved in silicon-on-insulator (SOI) ridge waveguides using wet-etched and

aluminum-coated 54.7° mirrors [117]. While the mirror-based method can offer wide operation bandwidth, the coupling loss due to the mirror surface absorption and roughness is relatively high, and the fabrication processes involved are rather complex, especially for interlayer coupling at the chip-scale. Alternatively, a pair of diffractive gratings at the two layers can be used for efficient coupling. The optimal design and fabrication of on-chip gratings have been extensively studied in recent years, especially to demonstrate efficient fiber-to-chip interconnection [118-121]. For a grating design, the best reported insertion loss (IL) is around 0.62 dB with 1-dB bandwidth of ~ 40 nm [120], and the highest reported 1-dB bandwidth (80 nm) has 1.3 dB IL [121]. The low IL grating includes reflective mirrors, and the high-bandwidth design utilizes a dual-level grating, which makes both approaches difficult to implement in the intra-chip coupler applications. Recently, an intra-chip diffractive grating coupler design with the back reflector has reported 1.94 dB IL and a 3-dB bandwidth of 40 nm [122]. However, the average loss of 1 dB per transition with an average bandwidth of 50 nm would limit the range of achievable on-chip functionalities in hybrid devices, where the light may transition between layers several times. A better engineering solution is needed.

To achieve higher efficiency couplers, the evanescent field coupling is a promising approach, which resorts to the decaying tail of optical modes to transport power from one waveguide to another. The utilization of the confined modes in the evanescent field coupling can inherently reduce the radiation loss compared to the propagating field coupling method. For a pair of phase-matched waveguides, it is possible to transfer all the power from one waveguide to another at a certain length at a given wavelength [123]. However, such couplers are very sensitive to the device geometry. The intrinsic wavelength

dependence of the coupling efficiency (imposed by the fixed coupler length) limits the bandwidth of such couplers. To resolve these issues, inverse tapering of optical waveguides in the coupling zone has been proposed, and IL's as low as 0.2 dB, 0.4 dB and 0.06 dB in the two-layer Si platform [124], the Si-on-SiN platform [110], and the deposited SiN-on-Si platform [125], respectively, have been reported. However, the 3-dB bandwidth of the reported coupler in the hybrid Si-on-SiN platform in [110] is limited to 20 nm, and the demonstrated 100 nm bandwidth device has an IL of 0.8 dB.

To minimize the termination loss, which increases the radiation and scattering losses, we eliminate a deep sub-micron taper end using a new tapering technique. As shown in Figure 22(a), instead of tapering down waveguide 1 while tapering up waveguide 2, we start with a wide multimode waveguide 2 and simultaneously taper both waveguides down to the single-mode width of the waveguide 2. By careful choice of the initial and final taper widths, the coupling to higher order modes can be effectively eliminated.

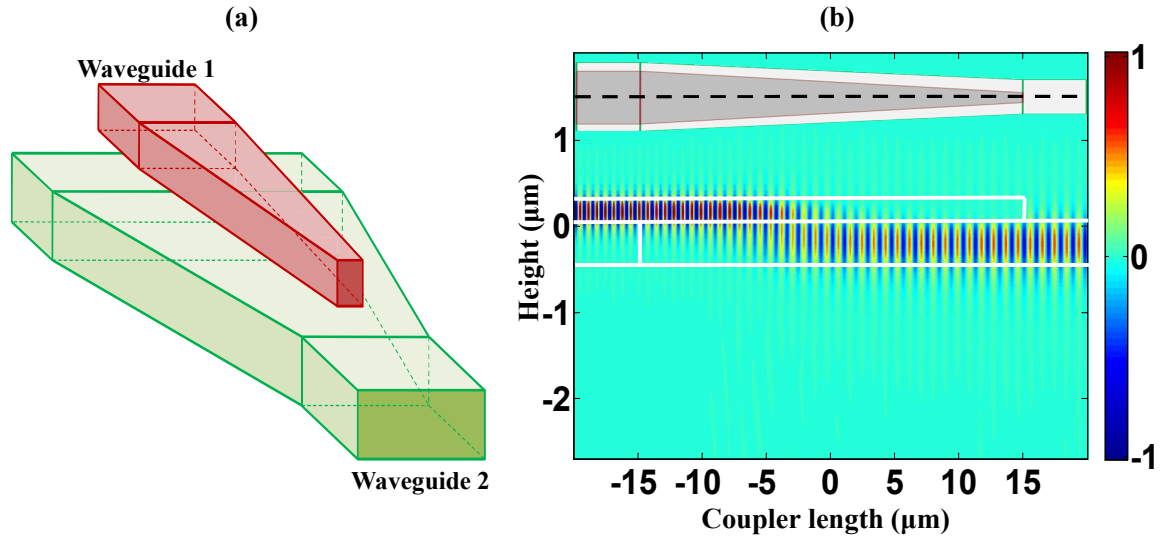


Figure 22: (a) The schematic of the proposed coherent vertical tapering method. (b) The cross-sectional image of the electric field profile along the length of a 30- μm coherent vertical coupler; the inset is the top-view image of the coupler and the dashed line indicates the cross-section surface.

Using the specifications of the developed hybrid SON platform, three-dimensional FDTD simulation (using Lumerical) is utilized to compare the performance of our coherent tapering technique with that of the inverse tapering method. In our platform, the thicknesses of SiN, Si, and the interface SiO₂ layers are fixed at 400 nm, 220 nm and 60 nm, respectively. Waveguide widths of 450 nm and 1 μm are chosen for single-mode operation in Si and SiN nanowires, respectively. The lower bound on the tip of the taper is 50 nm in both Si and SiN layers for reliable fabrication considerations. The upper bound of the tapering length is fixed at 30 μm to facilitate dense integration. An exhaustive search is performed within the defined parameter space to find the optimal tip width for each material layer. The optimal widths at the Si taper end and at the SiN taper end are found to be 160 nm and 1.4 μm , respectively. Figure 22(b) shows the longitudinal cross section of the electric field profile over the 30 μm length of the coherent taper.

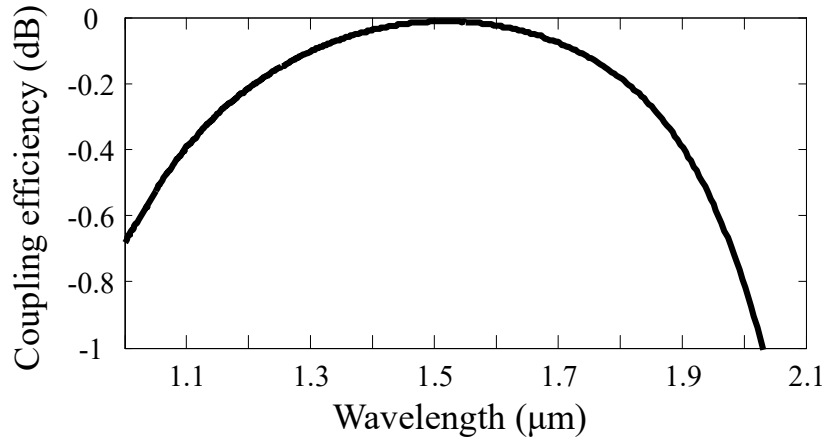


Figure 23: 3D FDTD simulation of the transmission efficiency for the adiabatic interlayer coupler with coherent tapering technique.

The computed coupling efficiency spectrum of the coherent vertical coupler is plotted in Figure 23. The computed total loss of the designed adiabatic coupler is less than 0.02 dB over the 135-nm telecommunication bandwidth (1450-1585 nm), which is a

record-low insertion loss for a coupler to the best of our knowledge. Additionally, the 1-dB bandwidth of the coupler is increased to cover more than an octave in frequency which paves the path for various high-bandwidth applications, such as pulse shaping and self-referenced integrated combs.

4.4 Demonstration of Broadband, Compact and High-Q Functionalities in Si-on-SiN Material Platform

4.4.1 Passive Device Fabrication

Figure 24 outlines the device fabrication steps for implementation of the proposed interlayer coupler on the SON platform. The process begins with patterning the Si layer. The chip is spin-coated by ~ 150 nm of HSQ 6%. As shown in Figure 24(a), the pattern is transferred to the resist through first EBL step. After developing the resist in a tetramethylammonium hydroxide (TMAH) solution, an ICP etching system is used to etch the Si device layer to form Si devices in a Cl_2 -based plasma. The remaining residual HSQ layer is left on the Si devices (Figure 24(b)). The SiN layer is then patterned using a second step of EBL using ZEP520A (by Zeon Chemicals) e-beam resist (Figure 24(c)) and RIE using a fluorine-based (F^-) gas mixture (Figure 24(d)). The residual resist is subsequently removed in piranha solution. In this process, an ESPACER (by ShowaDenko K.K.) is used on the top of ZEP resist to resolve the charge up issue. Figure 24(e) represents a cross-sectional SEM of a Si waveguide in the SON platform using the passive device fabrication procedure.

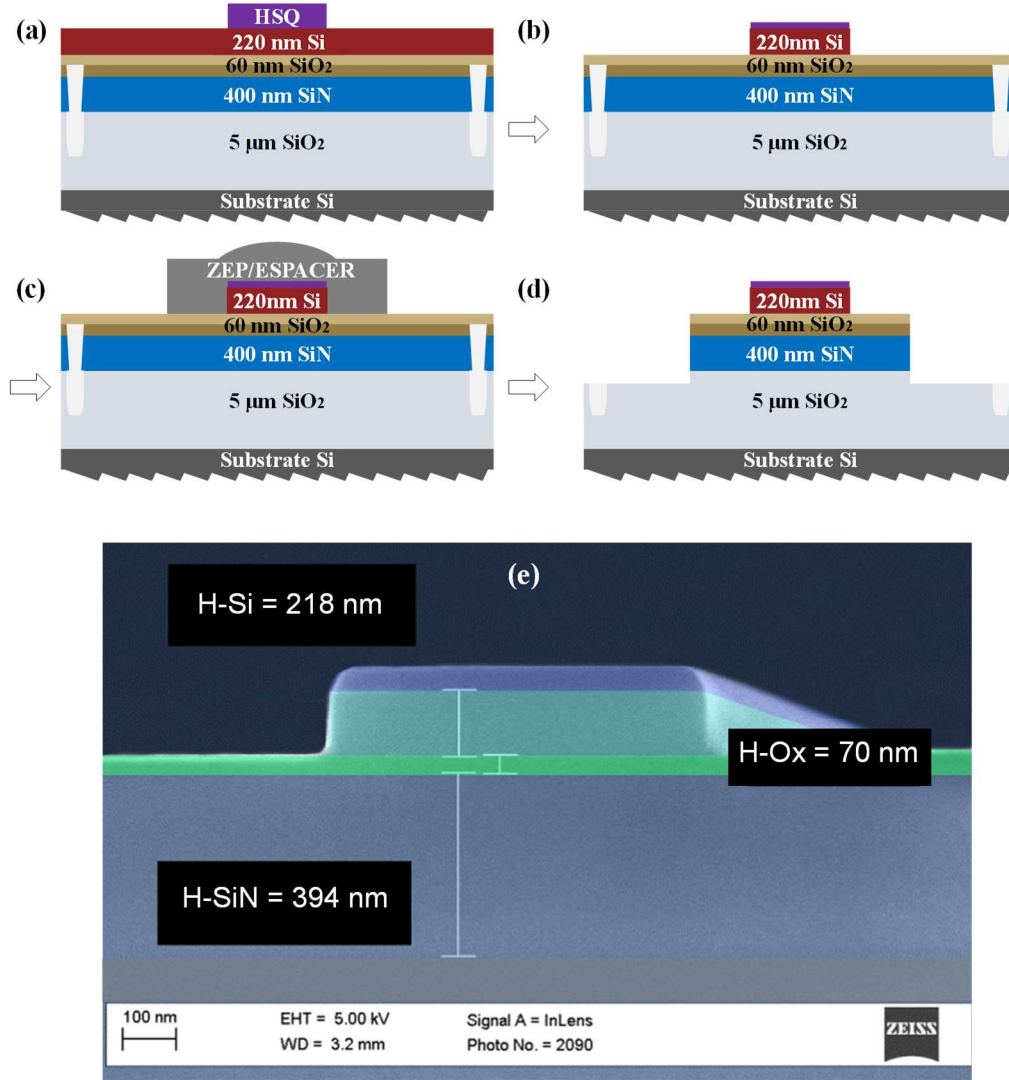


Figure 24: Schematic of the device fabrication process on the SON platform. (a) The first pattern is transferred to HSQ using an EBL machine. (b) The Si device layer is etched to transfer the pattern. (c) The second pattern is transferred to ZEP using the EBL machine. (d) The interface SiO₂ layer and SiN layer are etched to define the aligned second pattern on SiN. (e) False-colored cross-sectional SEM of a waveguide defined in Si layer of the SON platform.

4.4.2 Demonstration of Ultra-Low-Loss Interlayer Coupler

With the passive device fabrication being complete, the characterization of the fabricated devices utilizes a tunable laser (Agilent 8164A) with a tunable wavelength range of

1460–1580 nm. A single-mode fiber (SMF) brings the light to the device, which is mounted on a thermally controlled stage. To control the state of polarization of the light, a 3-paddle polarization rotator is used on the input fiber. The flat-cleaved termination of the SMF delivers the optical signal to the chip, and another flat-cleaved SMF receives the light at the output. The optical signal is then collected by a detector (Thorlabs PDB150C 800–1650 nm), and the corresponding electronic signal is sampled at 2000 samples per nm (wavelength) by a DAQ board (National Instruments PCI 6259).

In the first set of devices, two types of couplers are fabricated. The first type is the adiabatic 30 μm -long coherent vertical coupler, which is optimized for the highest coupling efficiency. The second type is the compact 10 μm -long coupler for dense integration purposes. In order to measure the coupler efficiency, we fabricate a cascaded set of 30 coherent vertical couplers with access gratings at the input and output ports. To distinguish the coupler loss from the loss due to input/output gratings as well as Si and SiN waveguide losses, a modified replica of the cascaded device is fabricated with one pair of vertical couplers. In this device, the corresponding length of the SiN and Si waveguides are chosen to be equal to the total length of the SiN and Si waveguides in the cascaded device, respectively. Using the measurement results of the replica device, the loss of 28 couplers can be isolated from all other losses of the cascaded device. Figures 25(a) and 25(b) show the scanning electron micrographs (SEM) of the fabricated adiabatic and compact vertical coupler devices, respectively. The results of characterization of the two types of couplers are shown in Figs. 25(c) and 25(d). The experimental results in each case agree well with the corresponding theoretical results as seen in the plots. The adiabatic coupler loss is experimentally extracted to be less than 0.03 dB over a wide bandwidth (1530-1565 nm),

which covers the C-band. The measured loss of the compact coupler is less than 0.45 dB in the same band. The inaccuracy of the measured coupler loss is less than ± 0.01 dB, which is mainly due to the variations in fiber-to-chip coupling efficiency. The 0.03 dB loss of the adiabatic coupler in the C-band is, to the best of our knowledge, the lowest reported in any CMOS-compatible hybrid material platform. It shows that the proposed SON platform can be used for realization of practical functional integrated photonic devices with negligible loss due to multiple couplings between different material layers (i.e., Si and SiN).

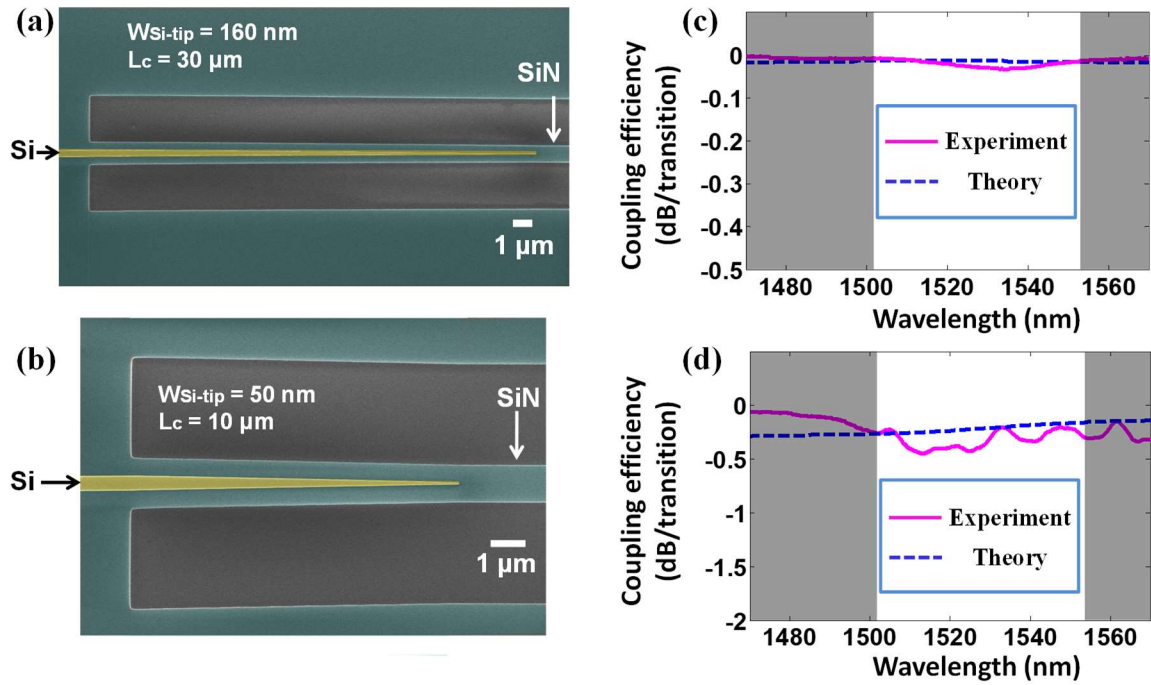


Figure 25: (a) Colorized SEM of the adiabatic coherent vertical coupler; (b) Colorized SEM of the compact vertical coupler. (c) The experimentally measured (solid line, magenta) and theoretically calculated (dashed line, blue) spectra of the coupling efficiency of the adiabatic vertical coupler, and (d) the experimentally measured (solid line, magenta) and theoretically calculated (dashed line, blue) spectra of the coupling efficiency of the compact vertical coupler. The shaded areas in (c) and (d) mark the regions outside the bandwidth of the access input/output gratings.

4.4.3 Demonstration of 3D Optical Path and High- Q Functionality

To showcase the capabilities of the proposed SON platform, we fabricated a prototype device in which a full hybrid optical path is envisaged. As shown in Figure 26(a), the device consists of a pair of access input/output gratings (in the top Si layer) at each end, to efficiently couple light into and out of the integrated device. A pair of coherent vertical interlayer couplers at the two ends transfer the optical signal from the Si waveguide to the SiN waveguide underneath and back to the Si waveguide. The SiN waveguide is coupled (in the SiN layer) to a SiN micro-ring resonator with an outer radius of 60 μm and an inner radius of 56 μm . The gap between the SiN waveguide and the ring is ~ 500 nm to ensure close-to-critical coupling. Figure 26(b) shows the measured transmission spectrum of the prototype device for the TE polarization—i.e., electric field in the plane of the resonator, which is normalized by its maximum value. The characterization results show the intrinsic quality factor of the microresonator to be $Q_{\text{int}} = 3 \times 10^6$ in the SON platform. To draw a comparison between the quality of the low-loss layer (SiN) before and after bonding, an inspection SiN chip was prepared by cleaving a part of the piece 2 after LPCVD SiN deposition (see Figure 19(e)). To maintain the fabrication consistency, the device fabrication on the inspection SiN chip was performed in parallel with the corresponding fabrication steps on the SON chip, as shown in Figure 24(c) and 24(d). Figure 26(c) shows the measured transmission of a microring resonator with 60 μm radius on the SiN inspection chip. The average Q_{int} of the resonator is measured to be $\sim 3 \times 10^6$. This shows no measurable change in the quality of the low-loss SiN layer after the platform fabrication. As it has been demonstrated in [109], the quality factor of resonators can be further

increased by tighter control of the (LPCVD) deposition of the SiN layer to minimize the material loss.

The results presented in this chapter demonstrate the unique functionalities of the SON platform, which can enable new capabilities using such heterogeneous material platform beyond those of the conventional SOI and SiN-on-SiO₂. The possibility of forming a wafer-scale material platform on which the unique advantages of Si and SiN can be combined without adding any tangible loss (either coupling or propagating losses) opens new opportunities in forming functional devices and systems (such as tunable filters, transceivers, and delay lines) with considerably better performance measures compared to conventional substrates. In the SON platform, all devices with ultra-low-loss requirements (e.g., high- Q resonators, delay lines, phase shifters, etc.) can be formed in the SiN layer while all reconfigurable (or tunable) devices and mechanisms are formed in the Si layer. Additionally, SiN waveguides can be used to handle higher optical power compared to Si with minimal nonlinear effects, which can enable a novel set of tunable high-power hybrid devices and systems.

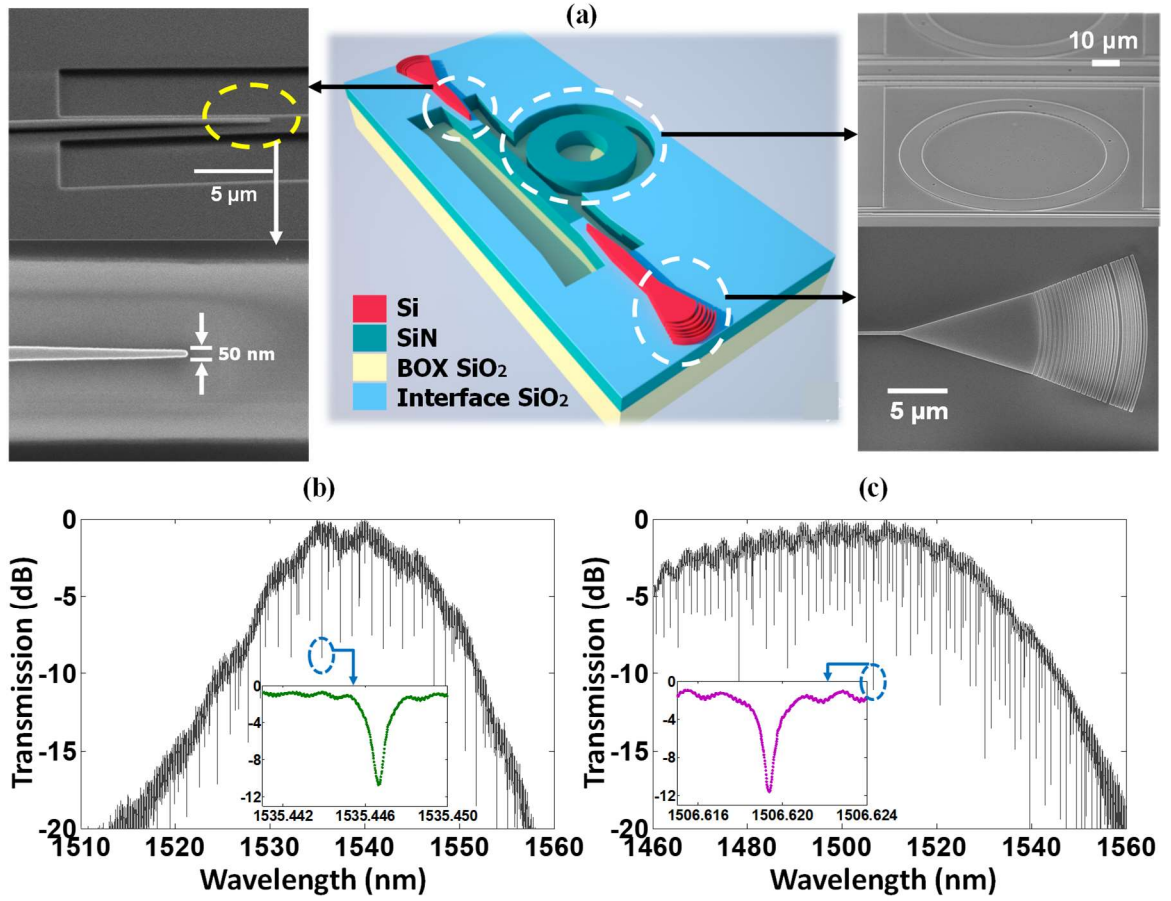


Figure 26: (a) A schematic of the hybrid optical path with SEMs of constituent elements in the path. (b) The transmission spectrum of a 60 μm radius multimode ring resonator fabricated on the SON chip. (c) The transmission spectrum of the same SiN resonator fabricated on the inspection SiN chip. As depicted in the inset figures, the highest intrinsic quality factor in each platform is measured to be $Q_{\text{int}} \approx 3 \times 10^6$. In both measurements, the spectrum is limited by the input/output grating bandwidth (Si gratings in (b) and SiN gratings in (c)).

CHAPTER V

ACTIVE ELECTRO-OPTICAL DEVICES IN SILICON-ON-SILICON-NITRIDE PLATFORM

The SON platform as an enabling ecosystem for photonic integration offers a set of novel functionalities for high efficiency and low-loss operation. A key feature to further develop the platform is to investigate and demonstrate fundamental electro-optical devices and systems with superior figures of merit. In this chapter, the incorporation of active electronic functionality into the photonic platform is studied and demonstrated. More specifically, challenges of active device integration into proof-of-concept devices are described and solutions are presented. In the next step, a novel electro-optical modulator is fabricated and its passive and active response are further studied.



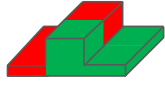


5.1 Design and Optimization of Ion Implantation Plan for Active Functionality in the SON Platform

During the past decade, there has been a significant amount of research dedicated to employ the plasma dispersion effect in Si for fast reconfiguration in photonic integrated circuits (PIC) and high-speed electro-optic modulation in the O and SCL optical telecommunication bands. The underlying principle of such device architecture is to incorporate a PN junction (or otherwise a capacitor) into a waveguide and change its corresponding effective refractive index (n_{eff}) by changing the carrier concentration. The main process for the change is introduced by either carrier accumulation in semiconductor-insulator-semiconductor capacitors (SISCAP) or depletion in reverse-biased PN junctions

for high-bandwidth electrical-to-optical conversion. As an example for the carrier accumulation modulation, we previously designed and demonstrated a SISCAP charge-accumulation-based modulator, which was implemented in the double layer silicon platform. Such a device architecture offers a unique solution for simultaneous high-speed and reconfigurable Si integrated photonics. However, the platform development needs to be redesigned and optimized for integration with SiN in the high-power and high-efficiency applications.

On the other hand, the carrier depletion approach, which is based on the PN junction waveguide to incorporate active electro-optical devices, can be readily applied to the SON platform without additional platform development required for accumulation method. Several architectures can be envisioned for the design of a PN junction inside a rib Si waveguide. As summarized in the Table 1, the PN junction cross section can be lateral, vertical, interdigitated (including zigzag), and U-shaped, among other options. The lateral PN junction, and the PIN junction diode as its extension, can show superior speed performance due to the reduced capacitance across the junction (~ 0.2 fF/ μm), which in turn reduces the carrier lifetime and increases the modulation speed. However, the efficiency of the electro-optical modulation is relatively low for such an architecture, as the plasma-induced modulation in the refractive index interacts minimally with the optical field inside the waveguide. To mitigate the efficiency issue, one solution is to make a U-shaped junction inside the waveguide which has an increased electro-optical overlap cross section, however, the capacitance increases an order of magnitude compared to lateral case, which in turn compromises the speed proportionally.

Table 1: Performance metrics of various active device architectures utilizing high-speed plasma dispersion effect for electro-optic modulation.

	Accumulation	Depletion (PN junction based)			
Interface	Capacitive [80]	Lateral [126]	Interdigitated [127]	Vertical [128]	U-shaped [129]
Device schematic					
Capacitance (fF/ μm)	0.5	0.13-0.34	1.6	0.4-0.9	0.9-2.2
Speed (Gbps)	15	50	10	~30	~20

In order to benefit from the increased electro-optical overlap cross-section as well as enabling the high-speed modulation, the vertical PN junction is a suitable choice. The average capacitance of such an architecture is around 0.5 fF/ μm , which is well below the expected average of U-shaped (~ 2 fF/ μm) and comparable to the lateral PN designs, therefore being suitable for the high-speed and high-efficiency integrated phase shifter designs.

Realization of the vertical PN junction in the Si-layer of the heterogeneous material platform is among the most critical steps of the work. Through an exhaustive numerical search using COMSOL Multiphysics modeling software, the geometry of Si active section

is chosen to be a 600-nm wide, 140-nm high waveguide with a pedestal of 70 nm. This size well confines the field inside the waveguide to interact with the junction, yet it is single mode for practical purposes. Considering such an effective width of Si waveguide, the successful implementation of the PN junction requires a high degree of alignment accuracy for several steps of ion implantation. Our proposed geometry of the PN junction and corresponding ion implantations are depicted in Figure 27(a), along with the computed mode profile of the Si-rib waveguide (using COMSOL, Figure 27(b)), from which the overlap optical power of 51.8% between the PN junction and the mode is calculated. The first three step of the implantation (implant 1 through 3) are done to realize the P side of the junction. Implant 1 is a shallow implant (40 nm target depth), and extends to the 575-nm of the waveguide. This step requires ~ 25 nm alignment accuracy in the EBL, otherwise the implant 5 is affected, and therefore a parasitic PN junction pair shows up at the bottom right edge of the Figure 27(a). Implant 2 is a mid-level implant (110 nm target depth), envisioned to connect the top P region to the pedestal P region self-aligned during the implant step 1. Implant 3 is again a shallow implant (20 nm target depth) but with high doping level, which is designed to establish an ohmic contact with upcoming Ti/Au pad at the final stage of fabrication. The target ion material used for the first three implants is BF_2^+ . Utilization of such compound is superior to using B^+ , mainly due to the reduced channeling effect, as boron itself is a relatively small and light (11u) element, and can easily penetrate through crystalline Si without much collision therefore increase the straggle of the corresponding implant. BF_2^+ ion on the other hand is heavier (49u), which increases the chance of collision and reduces the standard deviation of the implant location. However, using a fluorinated compound adds to the complexity of annealing step as the B-

F bonds are relatively high-energy, requiring higher temperatures for the successful activation of the B acceptors, which is discussed later in the rapid thermal annealing section.

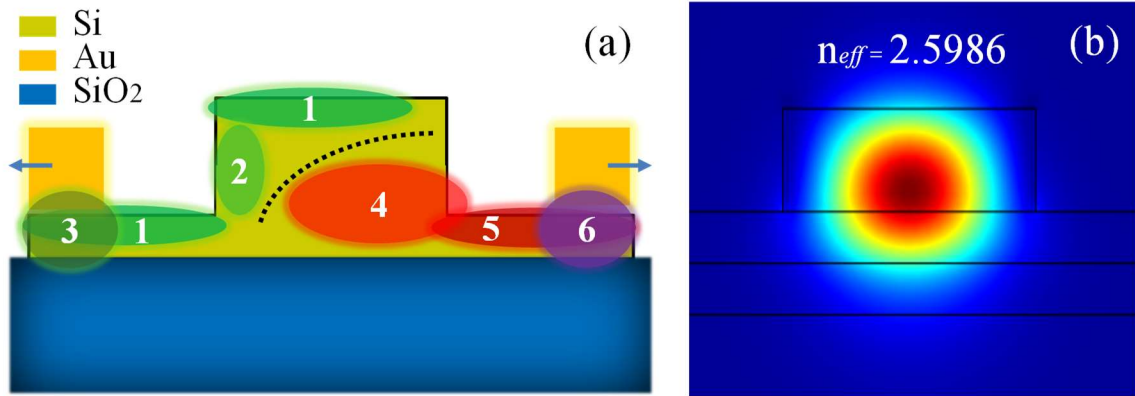


Figure 27: (a) Ion implantation plan for PN junction realization in a Si waveguide with pedestal. Each number refers to an ion implantation step introducing a donor or acceptor material. (b) Computed power flow profile cross-section of the Si-rib waveguide in the heterogeneous Si/SiO₂/SiN (SON) material platform.

For the N region of the junction, ion implantation steps 4 through 6 are performed. Step 4 forms the N region beneath the P region of the waveguide, with the target depth of 175 nm. Step 5 is the shallow version of step 4 with the target depth of 40 nm, to dope pedestal next to the region of implant 4. Both of these implant steps require extreme alignment accuracies below 50 nm, to avoid cross-doping (mainly on regions 2 and 1). Implant 6, like its P counterpart (implant 3), is designed to establish an ohmic contact with the Ti/Au pad. The target ion material used for implants 4 and 5 is As⁺. Implant 6 however uses phosphorous ion (P⁺, not to be confused with P region). P⁺ has a high degree of solubility in Si (10^{21} cm^{-3} at 900°C), and its silicon compound produces a good ohmic contact with Ti, suitable for low-resistivity contacts in the envisioned device.

As the suitable dopants for various steps of implant are chosen and the depth of each implant is determined, the fabrication of active elements in hybrid platform requires two important optimization tasks: 1) optimization of ion dosage and ion energy for each implantation step, 2) optimization of an e-beam lithography process for accurate alignment of fabricated passive devices against active device patterns. To determine the ion dosage and ion energy, a numerical search is performed using Stopping and Range of Ions in Matter (SRIM) software. We first fine-tune the ion energy to set the implant depth, and the output of the SRIM determines the suitable ion dosage required for a specific doping concentration at the implant location. The profile of implant however is set by these two parameters, and further engineering of such profiles requires multiple ion implants, which we tried to optimize through our six-stage implant structure. Figure 28 shows the 2-dimensional profile of a shallow P^+ implant at 40 keV (Figure 28(a)), and a deep As^+ implant of 320 keV energy (Figure 28(b)), corresponding to 39 nm and 181 nm ion implant depth in the N region, respectively.

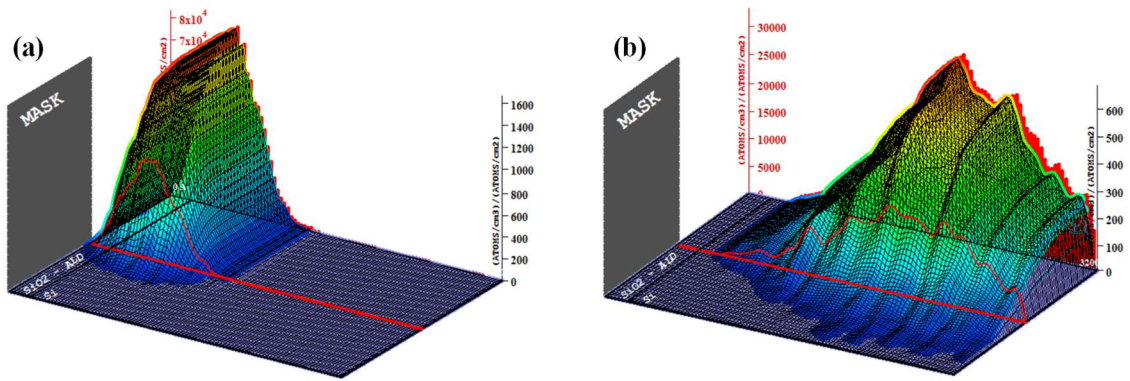


Figure 28: Computed ion range profile: (a) for phosphorous dopant at 40 keV, (b) for arsenic dopant at 320 keV. The 20 nm ALD SiO_2 is included in the simulation, which is originally added for anti-channeling at zero-degree implantation.

As expected, the straggle of the deep As⁺ implant (58 nm) is considerably larger than the shallow P⁺ (23.2 nm). This plot also shows the lateral diffusion of the deeper implants which implies the need for larger clearance of the As⁺ region from the P region, to reduce the impact of this implant on implant 2. Table 2 summarizes the ion energy, dosage and location of each implant for device fabrication.

Table 2: Summary of design parameters and computed ion dose and energies for realization of vertical PN junction on heterogeneous material platforms.

Implant #	1	2	3	4	5	6
Material	BF ₂ ⁺	BF ₂ ⁺	BF ₂ ⁺	As ⁺	As ⁺	P ⁺
Distance from WG-Ped. edge	575 nm	100 nm	1 μm	425 nm	1 μm	1 μm
Alignment accuracy	<25 nm	<25 nm	100 nm	<25 nm	<25 nm	100 nm
Target depth	40 nm	110 nm	20-40 nm	175 nm	35 nm	20-40 nm
Computed ion energy	60 keV	145 keV	35 keV	320 keV	60 keV	40 keV
Ion dosage	1.05×10^{13}	9×10^{12}	3.5×10^{15}	1.9×10^{13}	1.2×10^{13}	5×10^{15}

The ion implantation procedure on heterogenous devices is performed as follows: first, the sample is covered by PMMA with the thickness more than 1.2 μm. The ion implant patterns are next defined through e-beam lithography of the resist which exposes

the bottom layer Si to upcoming step of implantation. However, the PMMA e-beam dose needs to be accurately optimized to avoid parasitic PN junctions and unwanted doping of the neighboring regions during each implant. To accurately assess the e-beam lithography and PMMA, we fabricated some openings on an inspection sample to quantify any source of error or misalignment. Confirmed by an inspection sample test with JEOL 9300 EBL machine, it is possible to align patterns with an accuracy of less than 30 nm by manual marker alignment. Another case of error may arise from the over-exposure of PMMA, as its thickness grows beyond 1 μm . As shown in Figure 29(a), the exposure of PMMA at 700 $\mu\text{C}/\text{cm}^2$ does not well expose the resist at the boundaries, and increasing it to 800 $\mu\text{C}/\text{cm}^2$ totally resolves the issue, which confirms this dose level as the proper dosage for exposure. However, this dose level increases the width of patterns, in our case from 4.1 μm in the design to 4.32 μm on the actual features on the device (Figure 29(b)). This extension of features is then compensated in the designed pattern by $\sim 5.4\%$ shrink to compensate the exposure effect.

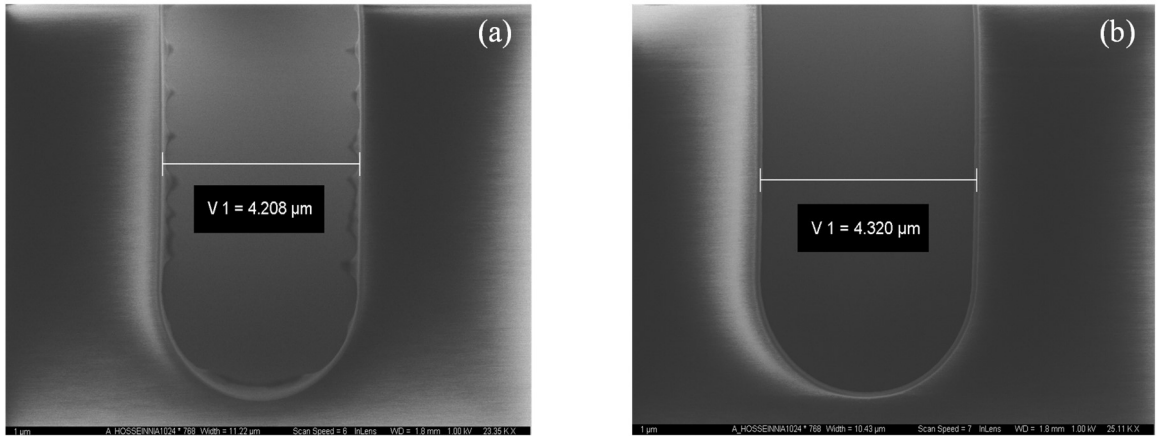


Figure 29: (a) SEM image of an opening on PMMA resist exposed at 700 $\mu\text{C}/\text{cm}^2$, (b) same pattern with 800 $\mu\text{C}/\text{cm}^2$ exposure dose. The width of opening is 4.1 μm in the design.

By accurate trimming of the EBL patterns to address the over-exposure issue, the patterns can be precisely transferred to PMMA resist. The sample is then sent to CuttingEdge™ company where the whole area is exposed to the requested dopant ion for the specified dosage and energy. PMMA protects the covered areas and the desired geometry of PN junction is formed through successive implants. After each step of implantation, the resist is removed in acetone and IPA so that the sample is ready for the next step of implant. This procedure is repeated six times for each implantation steps, with extreme care during alignment and exposure to achieve the required accuracy in fabrication, until the PN junction is defined inside the Si waveguide.

5.2 Rapid Thermal Annealing: Feasibility Study and Demonstration in the SON Platform

Rapid thermal annealing is a well-known process to activate dopant ions implanted into the Si layer. Along with implantation, it has been extensively used in nano-electronic and nanophotonic integrated device fabrication to realize doped areas of the sub-micron scale and lower. However, its extension to hybrid material platforms can cause several unwanted issues. In heterogenous material platforms enabled by bonding, materials of the layered structure exhibit different thermal expansion coefficients. Such thermal expansion gradient can cause detachment of a layer from the other, or deformation and cracking inside a layer due to the thermal stress at elevated temperatures. As part of the active device integration, it is critical to study the effect of annealing on the performance of hybrid integrated devices. Thus, an extensive study was performed to optimize the RTA recipe for hybrid material platforms, with the focus on the SON heterogenous platform. These results can be readily extended to other material platforms with similar properties.

In the context of the current work on heterogenous platforms, it is critical to determine the temperature level that the platform can withstand without major damage. The maximum tolerable temperature is of interest mainly to anneal SiN devices in the platform, as several works have reported that the annealing of SiN devices increases the quality factor and reduces waveguide loss, partially due to the release of hydrogen in the O-H bonds trapped in SiN, and partially due to the reduction of surface states and scattering sites on the waveguide interfaces [94,95,109]. To test the thermal performance, we have fabricated a set of hybrid devices in the SON platform, such as hybrid interlayer couplers and hybrid resonators. The conventional anneal process is next performed on the SON die with fabricated devices. Nitrogen is used as the ambient gas to eliminate unwanted oxidation of Si layer. Our results confirm that there is serious damage to the Si parts of all devices at 1000°C and above. The damage at 1050°C is such that Si devices are totally detached from the SiN substrate layer. Measurement of the Q factor for 40 μm radius SiN disk resonator at 900°C fabricated on the hybrid platform shows that Q increases from 1.7×10^6 to 2.1×10^6 after the anneal. While the increase is overall less than the average reported increase of Q after 1100°C anneal, our experiments confirm that the thermal improvement clearly onsets at 900°C. However, the test also shows that it is crucial to anneal SiN before bonding to reduce hydrogen content, and to keep the anneal temperature of any process on the SON platform below such level.

After assessing the tolerable ambient temperature for the device platform, hybrid devices are tested against rapid thermal annealing. To monitor the potential damage from RTA, a set of 8 pairs of cascaded interlayer couplers is used, which transfer coherent light back and forth between Si and SiN waveguides in corresponding layers. There is also a 40

μm radius SiN disk resonator coupled to the set to monitor the effect of RTA on the resonator Q factor. The input power is fixed at $200\ \mu\text{W}$ at $1550\ \text{nm}$ and the coherent light is coupled into/out of the integrated chip through the input/output integrated grating couplers. The amplitude of the output power is collected by an optical power meter module. The output power is measured before any thermal process for three copies (C1 to C3) of the set of 8 pairs of interlayer couplers. In the next step, the RTA is done to the sample at 600°C for 5 mins in the nitrogen ambient. Solaris 75 Rapid Thermal Processing (RTP) tool from Surface Science Integration (SSI) company is used for the thermal treatment. The device copies are characterized after the anneal. The procedure is repeated on the same set of devices at 900°C and 950°C . Table 3 summarizes the characterization results, which indicates that the loss significantly increases as the temperature rises to 950°C . Further monitoring of the devices under SEM reveals that the deformation of Si waveguides, especially for taper-downs of the interlayer couplers, is deemed to be the main reason for the increase of loss in the fabricated devices. Unlike conventional furnace annealing, no significant change is recorded in the Q factor of resonators after RTA. We believe the difference is due to the duration of annealing in the conventional method (>1 hour) which is longer than RTA average time (<5 mins).

Table 3: Output power amplitude of 8 pairs of interlayer hybrid coupler integrated in SON platform for different RTA temperature treatments.

Output power	No thermal process	RTA 600°C	RTA 900°C	RTA 950°C
C1	250 nW	250 nW	100 nW	7 nW
C2	280 nW	270 nW	110 nW	8 nW
C3	255 nW	250 nW	80 nW	7 nW

Having found the range of thermal treatment for the SON platform, the next step is to find a recipe for RTA which does not significantly damage integrated devices, yet activates the majority of implanted ions for electrical functionality. According to reports on the annealing requirements of As^+ , P^+ , and BF_2^+ , the minimum temperature of activation for 50% threshold of each type of ion is estimated to be 850°C , 925°C and 900°C , respectively [130-133]. The maximum required temperature in our work belongs to phosphorous. However, since it is primarily used for heavy doping of Si at the metal contacts of the N region, we can further compromise on the temperature as the doping level is high and compensates for less than 50% activated ions. Therefore, the trade-off point of loss/activation for the SON platform is determined to be 900°C , and the time of run is maximized to 5 minutes to use the longest allowed RTA run on SSI tool which results in highest activated species. Figure 30 shows the bright field micrograph image of two devices ($3\text{ }\mu\text{m}$ radius disk and $90\text{ }\mu\text{m}$ radius ring) before and after optimized RTA run. As seen in the image, different colors of different implanted areas before the anneal indicates the presence of different material species, i.e. As, P, and BF_2 ions, while the uniform color of the device across all areas after RTA confirms the activation of implanted materials into Si crystal.

Following the RTA step, the contact pads are defined in PMMA resist at the locations of high-dose implantation in the P and N regions, using an aligned EBL run. Dry etching of $\sim 20\text{ nm}$ anti-channeling ALD oxide in fluorine plasma is performed to reach to Si layer at contact locations, followed by an e-beam evaporation of a 470 nm of Au on top of 20 nm buffer layer of Ti, and the subsequent lift-off concludes the device fabrication steps of the integrated hybrid phase shifter device.

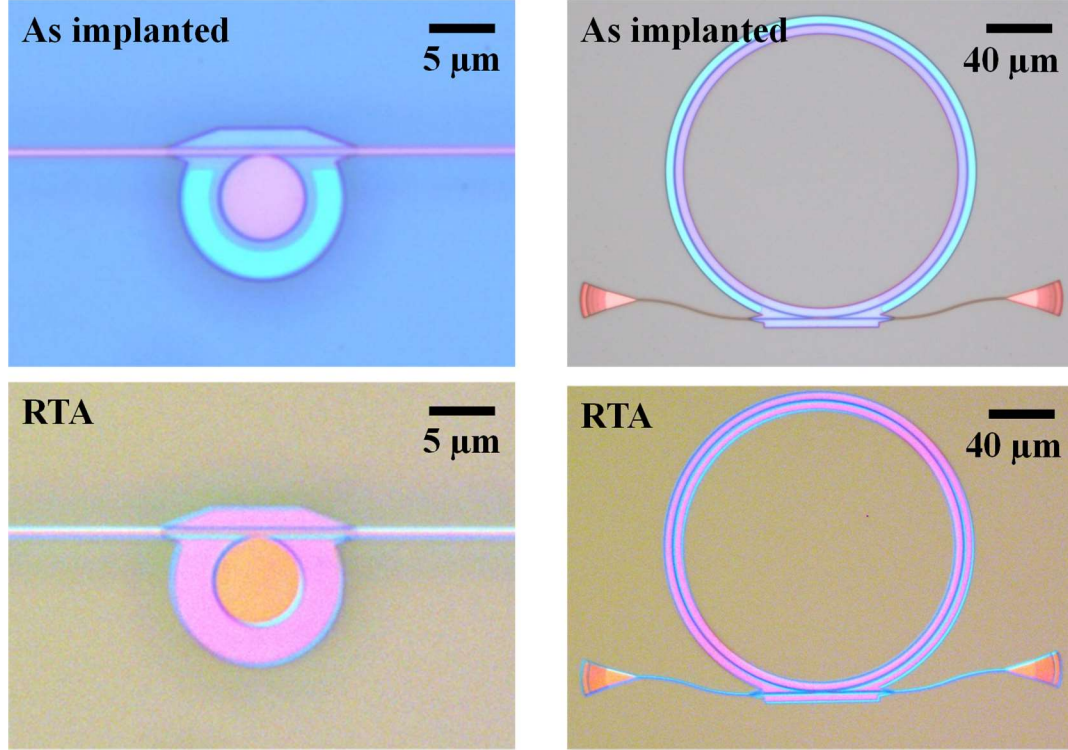


Figure 30: Optical micrograph images of a compact $R=3\ \mu\text{m}$ disk and a large $R=90\ \mu\text{m}$ ring, before and after RTA treatment. Morphing of different implanted areas into a single color is visible.

5.3 High Speed, High- Q Resonant Coupling Modulation in the SON Platform

Among various integrated photonic components, microdisk and microring resonators have been the focus of substantial research to produce low-power, high-speed, and compact integrated modulators [23, 80, 83]. Such modulators are extensively used in different chip-scale applications, including on-chip interconnection, photonic analog-to-digital conversion, and optical pulse-shaping [134]. The main figures of merit for modulators are high speed, high energy efficiency, low insertion-loss, high extinction ratio, and compact size. Such performance metrics can be significantly improved using amplified coherent light in resonance-based structures. In principle, microrings with higher Q 's can offer

higher electro-optical conversion sensitivity and improve all the corresponding metrics. However, there is a fundamental trade-off between the speed of modulation and the cavity lifetime in the majority of resonant-modulation methods. Therefore, the power-efficiency and speed cannot simultaneously increase in such designs

Recently, there has been an increasing attention toward integrated devices based on coupling modulation [135-137]. Such devices share a common modality in which the fundamental limit of speed against cavity lifetime is removed, enabling a set of promising devices for switching, amplification, and modulation. However, the efficient performance of the coupling modulation critically depends on the finesse of the optical cavity. Figure 31(a) shows the schematic of a typical coupling modulator design. As illustrated in Figure 31(b), for a given resonator, the Q factor is directly proportional to the slope of change in the power transmission. Therefore, a higher Q cavity utilizes a higher optical output swing for a fixed coupling swing.

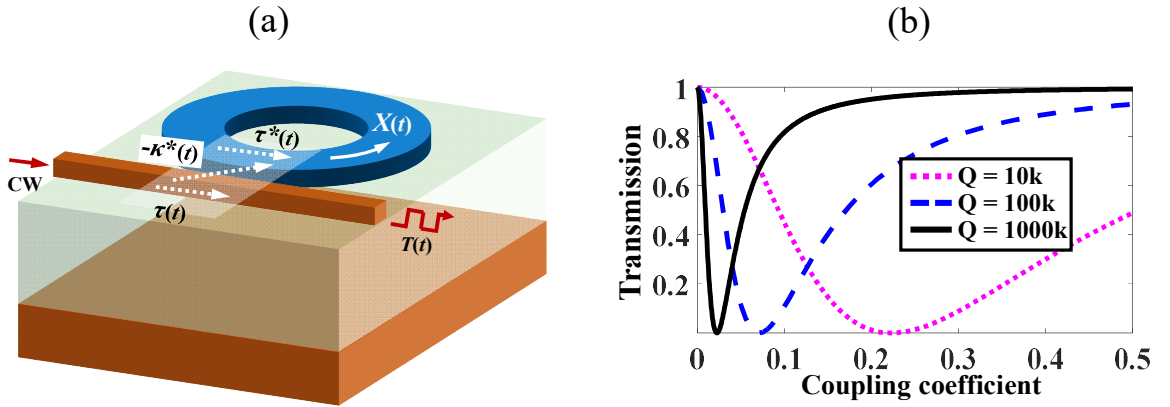


Figure 31: (a) 3D schematic of the resonant device with a hypothetical time-varying coupling coefficient. $\kappa(t)$ represents the field coupling coefficient from the resonator to waveguide. (b) Output power transmission as the function of $|\kappa|$ for three different Q values of a typical integrated resonator. Notice the sharp transition of transmission at low $|\kappa|$ values as Q increases.

Among material platforms to implement the device design, silicon (Si, as in SOI platform) is a natural choice. The electro-optical properties of Si has made it a suitable

choice for such applications. However, the absorption and nonlinearity mechanisms limit the capacity of Si to support high field enhancement in resonators, which is critically important to demonstrate efficient coupling modulators. On the other hand, SiN offers very low intrinsic optical loss and superior linear power handling. However, SiN does not have a reliable tuning or high-speed dispersion mechanism because of its dielectric nature. Therefore, the hybrid SON platform is an excellent candidate for the demonstration of next-generation high-speed high-efficiency integrated coupling modulators.

5.3.1 Device Architecture and Fabrication

To understand the dynamics of modulation, a universal solution of the configuration in the Figure 31(a) is needed. The transfer matrix method is used to find the transmission at each point of time through a recursive formula. Then the method of successive substitution solves such relation to find the overall transmission function—i.e., $T(t)$, which has a form of

$$T(t) = e^{-j\theta} \left[\tau(t) - \alpha \frac{\kappa(t)}{\kappa(t - T_R)} \right] + e^{-j\theta} \kappa(t) \sum_m \left(\alpha^m \left[\frac{\tau(t - mT_R)}{\kappa(t - mT_R)} - \frac{\alpha}{\kappa(t - (m+1)T_{RT})} \right] \prod_{p=1}^m \tau^*(t - pT_R) \right). \quad (60)$$

in which, $\alpha = ae^{-j(\theta+\phi)}$, and a is the attenuation associated with a roundtrip (of time constant T_R) inside the resonator, and ϕ is the propagation phase shift of the roundtrip, and θ is the coupling phase shift. For small signal response of transmission in the high- Q regime of the cavity, and for frequencies that are smaller than $1/t_0$, Equation 60 can be simplified to have a form of

$$T(t) = e^{-j\theta} \tau(t) - \alpha \kappa(t) \times X_0. \quad (61)$$

In the Equation 61, the X_0 factor is the steady-state electromagnetic field amplitude inside the resonator, which is directly proportional to the field enhancement, and finesse of the cavity. Therefore, as the finesse increases, $\kappa(t)$ is proportionally amplified in the output, which confirms the computed results of Figure 31(b).

Building on the insight provided by the coupling modulation theoretical analysis, Figure 32(a) is an illustration of the integrated coupling modulator structure to be implemented in the heterogenous Si-on-SiN (SON) platform. The platform is comprised of a top crystalline Si layer of 220 nm, an interface SiO₂ layer of ~60-70 nm, and a bottom SiN layer of 400 nm. In this device, the modulation of output power is determined by the coupling between the bus waveguide and the micro-ring resonator, amount of which is controlled by a tunable phase-shifter (PS). The PS is coupled to the resonator at two points to enable the time-varying coupling by changing the optical phase. The microring resonator is fully implemented in the SiN layer (dark blue) to enable high Q resonance, while the PS is integrated in Si (dark gray semi-circle) to exploit the high-speed reconfigurability of the material through the plasma dispersion effect. A pair of adiabatic interlayer couplers transfer the light back and forth between waveguides in the Si and SiN layers.

The time-varying coupling coefficient $\kappa(t)$ is realized through two fixed couplers in SiN layer and a pair of interlayer vertical couplers which transfer light from SiN to Si layer. Changing the fixed coupler coefficients in SiN, the power can be balanced between different materials to support an overall high-quality device while enabling the high-efficiency of the modulator. The design of proposed hybrid coupling modulator device is composed of a racetrack SiN resonator with the total perimeter of ~650 μm , two fixed SiN waveguide-resonator couplers with equal (power) coupling efficiency ($|\kappa|^2$) of 0.133, a pair

of ultra-low-loss interlayer couplers, and a Si phase shifter waveguide with an effective length of 250 μm . Figure 32(b) shows the computed response of the device due to the change in the phase shifter arm. Typically, a phase shift of $\frac{\pi}{10}$ gives an output swing of more than 5 dB. The corresponding Q factor of the hybrid Si/SiN resonator is chosen to be $\sim 10^5$ in the simulation. The high Q of the hybrid resonator and high coupling coefficient of each coupler results in high sensitivity of the output optical signal to the phase change in the Si phase-shifter.

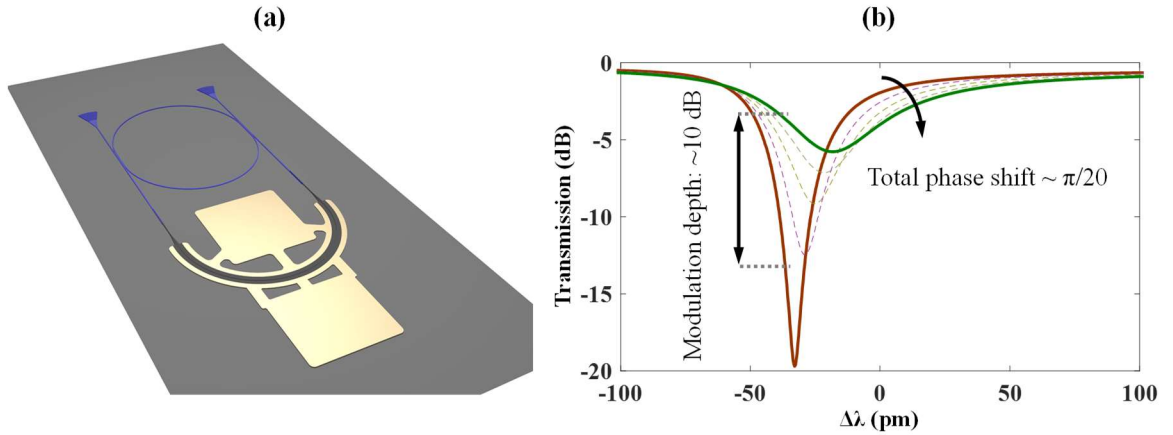


Figure 32: (a) Heterogeneously integrated modulator structure. (b) Computed dynamics of the transmission response with the phase change in the Si waveguide. In the simulations, Q is increased to 5×10^5 to demonstrate high efficiency of the modulation as Q increases.

The passive device is fabricated through the multi-step CMOS compatible fabrication procedure which is discussed in detail in the previous chapter. The active device integration is followed next, according to the process discussed in the Section 5.1 and 5.2. In the last step of device fabrication, the thin SiO_2 layer (~ 20 nm) is needed to be etched away so that the Si layer is exposed to metal which is deposited next to define electronic pads. The reliable and clean process for the oxide removal is through wet etching by BOE. However, since the interface oxide layer between Si and SiN sublayers is also exposed to

the solution, the etching of the interface layer partially releases the Si waveguide, significantly increasing the optical loss and rendering the device inoperable. Dry etching of the SiO_2 is another option. Since the Cl_2 -based dry etching does not actively introduce carbon or hydrogen into the plasma, it is an etching method of preference where the organic contamination is concerned. As the result, a recipe with the Cl_2 chemistry is tested in an ICP etching tool for the removal of ALD oxide layer. As shown in Figure 33, the Cl_2 -based recipe results in a heavily non-uniform etching over the sample (with the variation above 10 nm). This is critically important as the layer beneath ALD SiO_2 is a 70 nm Si pedestal. Since the etch rate selectivity of Si against SiO_2 is measured to exceeds 7 in the Cl_2 -based recipe, such level of roughness can be transformed into the bottom Si layer and totally etch the pedestal.

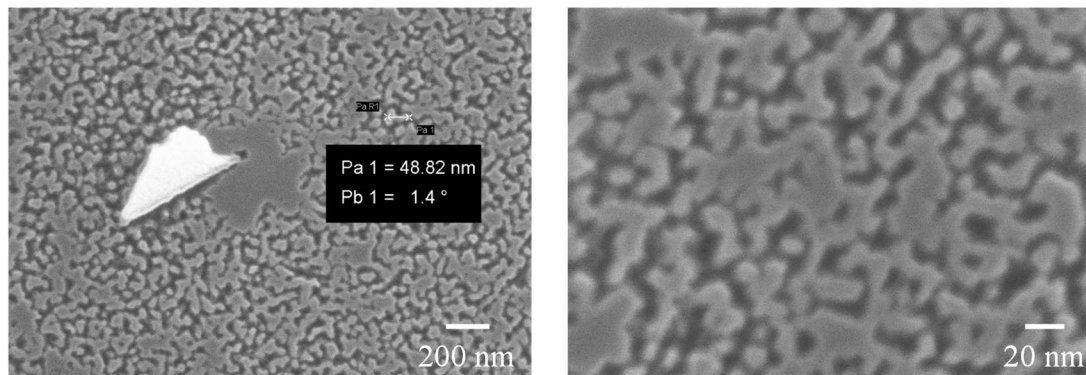


Figure 33: SEM micrographs of a 20 nm ALD SiO_2 on top of Si etched with the Cl_2 -based recipe. The surface is visibly rough after etching with >10 nm variation of the etching profile over the sampled area.

Another option for dry etching of SiO_2 layer is through a F^- -based recipe. Fluorine ion is usually generated in the ICP plasma through CF_4 or CHF_3 compounds, so it is expected to have unwanted organic contamination due to the presence of carbon and hydrogen in the recipe. One solution to the issue is to incorporate O_2 in the gas mix to

assist the decomposing of organic byproducts. After proper optimization on test samples, the etching of ALD oxide was performed and no visible contamination is observed under SEM. Figure 34 shows the dark-field micrograph of the fabricated device in the heterogeneous SON platform after the final electronic pad metallization and lift-off step.

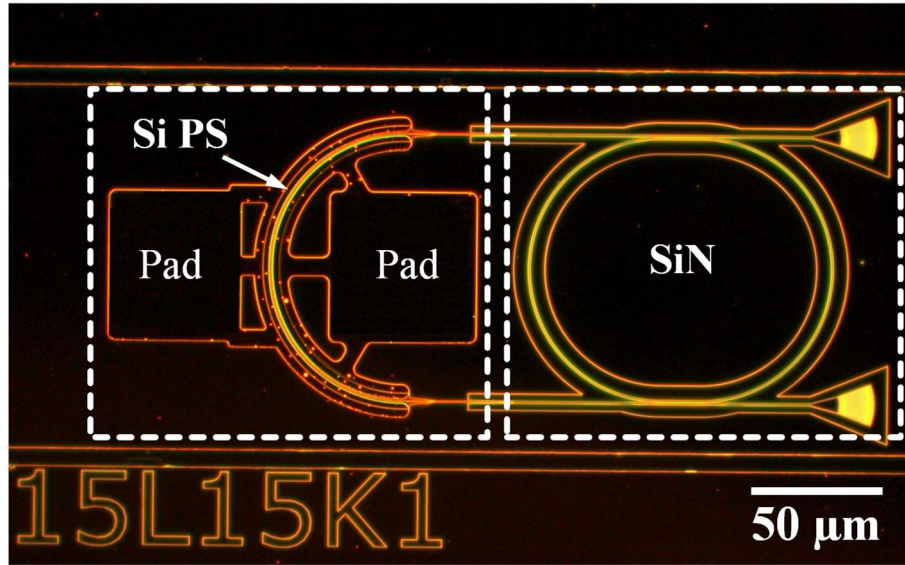


Figure 34: The dark-field micrograph image of the fabricated modulator. Si can be differentiated from SiN due to their different reflected color spectra.

5.3.2 Thermal, DC and High-Speed Characterization

To confirm the functionality of the modulator device in the passive mode, one idea is to use the large thermo-optic coefficient (TOC) of Si in comparison to SiN. At the room temperature, Si has a strong TOC of $1.78 \times 10^{-4} \text{ K}^{-1}$ [65], while the LPCVD SiN has been measured to have a TOC equal to $2.45 \times 10^{-5} \text{ K}^{-1}$ [138]. The large difference of TOC between two materials enables to change the phase of Si phase-shifter arm by heating the whole sample, which effectively changes the refractive index in Si while the change in SiN is negligible. Figure 35 shows that a relatively small change of the sample temperature

(5°C) results in a considerable change in the modulator output spectrum. Such change in the temperature is approximately equal to $0.1 \times \pi$ phase shift in the Si arm. The thermal characterization result in Figure 35 demonstrates that with such a phase change in the Si arm, the extinction of the resonance changes more than 15 dB, which is the signature of coupling modulation. Being based on a nonlocal heating procedure, the proposed thermal method offers a simple way to test and quality check devices before the active device fabrication without any additional device fabrication step, and provides a point of comparison for the active device and its corresponding performance. The Q factor of the passive device is also measured from the spectrum to be as high as 2×10^5 , with the finesse of 242, which exceeds an order of magnitude improvement from the latest coupling modulation in the SOI platform [137].

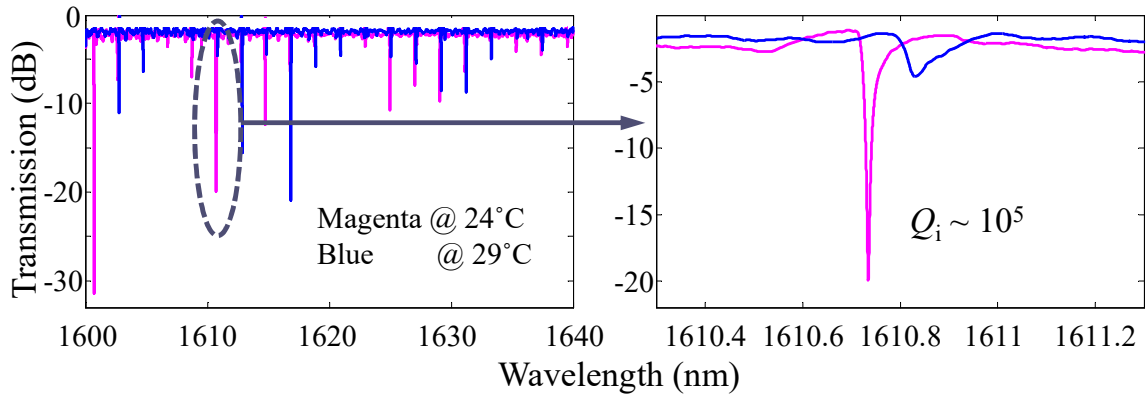


Figure 35: Thermal response of the hybrid coupling modulator. At an appropriate bias point (1610.75 nm for the specified azimuthal order), more than 10 dB extinction is recorded.

As the number of fabrication steps and the tools and processes involved to realize the proposed integrated modulator are quite diverse and not necessarily mainstream, getting a high yield of successful devices is a challenging task. In spite of that, by careful design of experiments on inspection samples and applying corrections to conventional methods

which extended from etching to annealing, we managed to get more than 90% of the devices functional, i.e. passing light in/light out test. Characterized devices have the range of Q_i factors between 7×10^4 to 2.1×10^5 . With the proof-of-concept modulation idea demonstrated in the passive device, the next step is to test the DC electro-optical performance of the structure after the active device fabrication is complete. The electro-optical response of the modulator with applied reverse bias voltage, and the DC i-v characterization of the Si-waveguide embedded PN junction are shown in Figure 36(a) and 36(b), respectively.

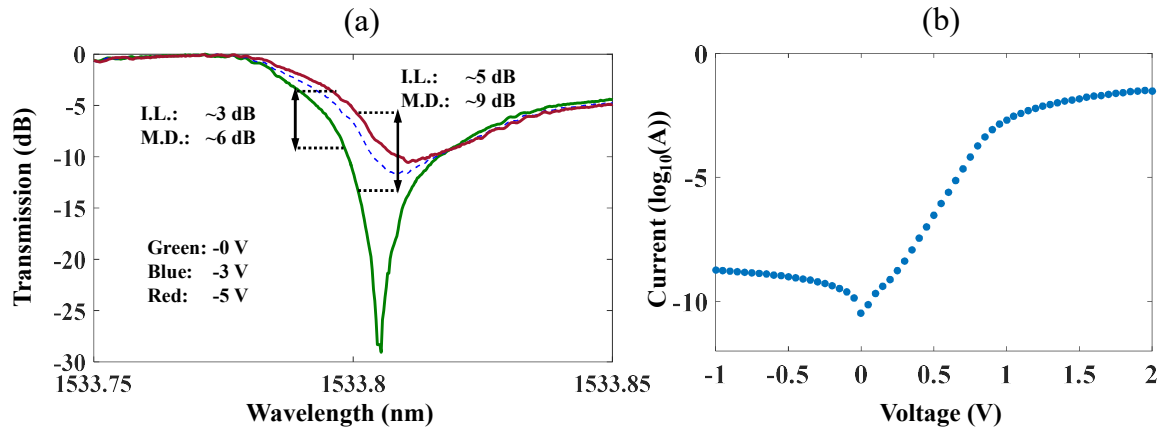


Figure 36: (a) DC electro-optical characterization of the integrated heterogenous modulator. The blue shift of the resonance confirms the free carrier dynamics of the change in effective phase of Si waveguide. (b) Measured DC i-v curve of the PN junction diode integrated inside the Si waveguide.

The results of DC i-v characterization of the PN junction in Si waveguide confirms the functionality of the diode. Three sections of the PN diode can be clearly distinguished in the corresponding i-v curve: 1) the reverse-voltage region with the $I_{rev} \sim 1-5$ nA; 2) the forward bias onset of ~ 0.5 V with the exponential i-v characteristic of the diode; 3) the resistance limited region with the onset of ~ 1 V. The total resistance of the PN junction

device, including the contacts and pads, is measured to be as low as 19Ω . The measured result clearly confirms the success of our proposed process to deliver ohmic contacts of ultra-low-resistivity. Considering the Si waveguide arm with an active length of $300 \mu\text{m}$ in the characterized device, the total capacitance is equal to $\epsilon_r \times \epsilon_0 \times \frac{A}{d} = 11.65 \epsilon_0 \times \frac{0.6 \times 10^{-6} \times 300 \times 10^{-6}}{0.1 \times 10^{-6}} \approx 185 \text{ fF}$ [139]. Therefore, the 3-dB bandwidth of the device is estimated at $(2 \times \pi RC)^{-1} \approx 45.3 \text{ GHz}$.

Figure 37 illustrates a schematic of the characterization setup and the RF power levels for the characterization of the integrated hybrid coupling modulator. The isolated insertion loss of the modulator device is measured to be between 3 to 6 dB depending on the modulation depth level, and additional insertion loss is due to the input/output grating losses, which are not particularly optimized to work at 1550 nm SCL telecom band. The setup is built in the synchronous mode, in which a reference clock synchronizes the bit pattern generator (BPG) and the digital sampling scope. The BPG can generate different PRBS patterns, and for this work NRZ PRBS (2^7-1 pattern) is mainly used with tunable speed through clocking. The electro-optic setup has been successfully built and its issues such as jitter and noise are addressed, and the baseline test of the setup is completed with an off-shelf conventional LiNbO_3 modulator up to 10 Gbps bit rate OOK. As the design of the modulator suggests, the device can be characterized in on-off-keying (OOK) mode, and therefore the detection can be simplified to use a high-speed photodetector directly fed into the sampling scope through a TIA stage for electronic signal amplification and matching.

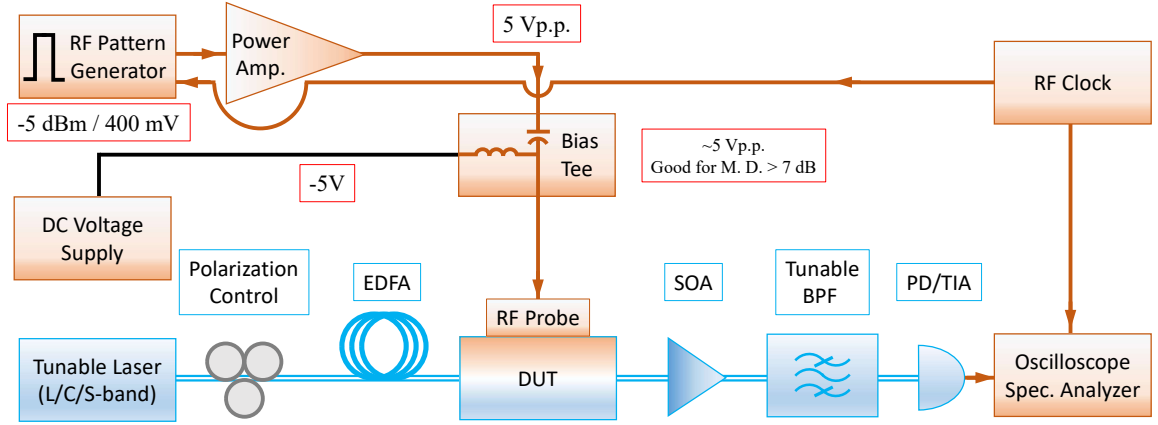


Figure 37: The schematic of the high-speed measurement setup. Blue elements denote optical path and the orange denotes the electrical path and power.

A typical eye diagram result of the device is depicted in Figure 38(a). Here, the measurement is performed at 10 Gbaud/s OOK input signal. The microresonator Q factor of the device under test is measured to be 1.55×10^5 , which leads to the 3-dB bandwidth limit of 1.26 GHz if the cavity modulation was employed. Figure 38(b) shows the corresponding S_{21} measurement of the EO device, in which the 3-dB bandwidth is located well above 10 GHz. This manifests the successful demonstration of coupling modulation for the device, as well as the RC bandwidth of the PN junction exceeding 10 GHz. We believe that the device is capable of working beyond 10 GHz if the RC limit is addressed through revised PN junction design to reduce parasitic capacitances. The issue however can be mitigated with an appropriate design of matching network. BER is also computed through eye diagram Q factor measurements, with the eye Q value of 3.087. The corresponding BER is 1.02×10^{-3} accordingly, which is well below hard decision FEC limit. The increased value of noise is mainly introduced through SOA, which is added to compensate the insertion loss of unoptimized I/O grating couplers. The SOA can be

eliminated if the design of I/O ports is optimized, hence opening the path for PAM modulations and enabling higher signal rates.

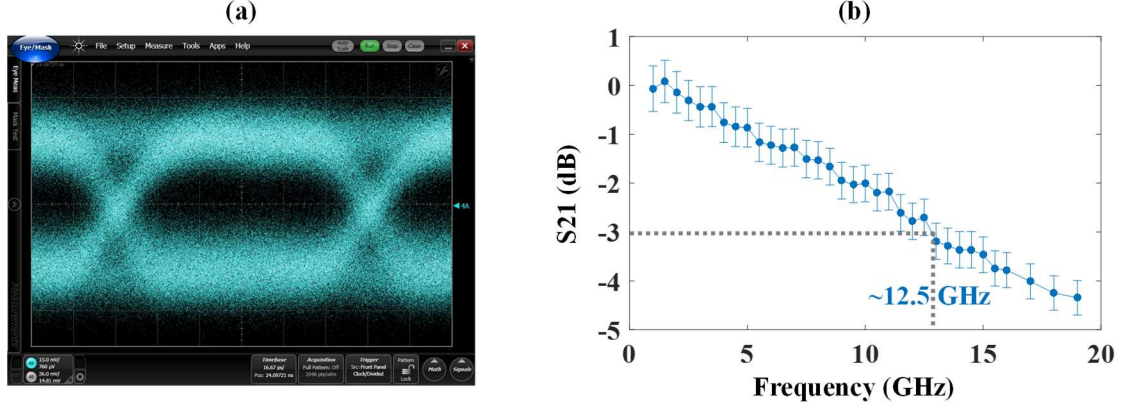


Figure 38: (a) Measured eye diagram of PRBS (2^7-1 pattern) at 10 Gb/s. It is important to mention the rise-time and fall-time suggesting the possibility of higher bit rates for the device. (b) The measured EOE S_{21} of the modulator after direct detection. The curve is normalized to S_{21} value at 1 GHz.

5.3.3 Discussion

Multiple features of device design, fabrication, and characterization can affect the performance of the device, which should be considered to properly analyze the characterization results. Regarding the difference between the calculated bandwidth and the measured 3-dB bandwidth of the electro-optical response from S_{21} parameter, the difference is due to the inclusion of the $50\ \Omega$ source impedance. Taking the source load into account, the overall resistance is updated to $69\ \Omega$, resulting in $(2 \times \pi R_{eq} C)^{-1} \approx 12.42$ GHz, which is in good agreement with the measured S_{21} bandwidth of the loaded device.

An important challenge in characterization of our heterogeneously integrated modulator is caused by the rather high insertion loss of the overall optical path, which necessitates the use of an SOA to restore the signal at the output, and is the main contributor to noise and the subsequent reduction of measured BER. The loss is mainly imposed by

the input and output focused grating couplers ($\sim 7\text{-}10$ dB), which brings the overall loss in excess of 20 dB. There are several reports on optimized grating couplers at loss levels below 2 dB, which can be applied here to significantly reduce the loss. Edge coupling is another option which can reduce the overall back to back insertion loss to less than 3 dB. This eliminates the need for SOA, which reduces the noise figure at the output and demonstrates the potential of the device for low input optical power applications.

To a lesser degree of contribution and importance, parasitic capacitances introduced by successive ion implantations can contribute to noise, as well as parasitic resistances due to imperfections at the ohmic contact locations. On the other hand, there are several characterization setup elements in the optical path which can affect the noise dynamics and also change the device bandwidth, including the SOA, TIA, and photodetector assembly. Such contributions can add up, with higher contribution at the SOA and TIA due to their order in the setup (as Friis formula suggests), and explain increased noise levels.

Another challenge stems from the PN junction series resistance. The measured resistance of the device at $19\ \Omega$ has a non-negligible mismatch with the $50\ \Omega$ standard. The mismatch of the reverse biased diode as the RF load to the standard $50\ \Omega$ line causes power reflection at the load, and reduces the power delivered to load to $\sim 32\%$ of the matched case. In other words, the device is effectively running with $\sim 0.6\ V_{p-p}$ if the delivered power is concerned. However since the device works on voltage drop on the PN junction, this factor can reduce to $0.28\ V_{s,p-p}$, equivalent to $0.56\ V_{p-p}$. The fabricated PN junction is measured to have an average $V_{\pi}L_{\pi}$ of $\sim 1.16\ \text{V}\times\text{cm}$. Therefore, the phase shifter embedded in the Si waveguide effectively produces $0.07\times\pi$ for the applied input voltage. By further optimization of the device toward a matched load, the performance can be significantly

enhanced to reduce the input voltage swing. With the proof-of-concept device functionality established in the SON platform, further improvements for such type of resonant modulation can be considered in the next generation of devices.

CHAPTER VI

EPILOGUE

6.1 Future Work

As it has been the common theme throughout this work, solutions for the next-generation of integrated nanophotonic devices and systems need to be sought through heterogenous material integration. The importance of the material platform as an enabling infrastructure in the design, fabrication and realization of integrated photonic devices and systems will keep pushing Si photonics to include a larger portfolio of materials at its disposal. Therefore, an essential future direction to this work is to add III-V platforms to Si for efficient lasing and detection, which is actively pursued both in academy and industry to improve performance and provide highly efficient and compact electronic-photonic solutions on the Si chip at a lower cost. The critical importance of this work is the fact that it can be readily applied to III-V/Si or III-V/SiN integration, as integration processes developed here meet needs of III-V material processing, including the low-temperature and low interfacial stress requirements.

Another important extension of this work is in the use of SiN material platform for nonlinear photonics and high-power applications. Si can offer high speed data processing and reconfiguration if it is added to the SiN as our heterogenous integration method enables. One interesting idea to pursue is shown in Figure 39, in which the SiN platform is used to generate the ubiquitous optical Kerr frequency combs, and then the comb is transferred to Si by our adiabatic, broadband interlayer coupler to be modulated line-by-line. The idea here can offer a compact solution for integrated optical interconnects at rates

beyond 10 Tb/s. Recently, it has been shown that the comb generation in SiN can achieve conversion efficiencies above 30%, making it a relevant technology for optical communication applications [140].

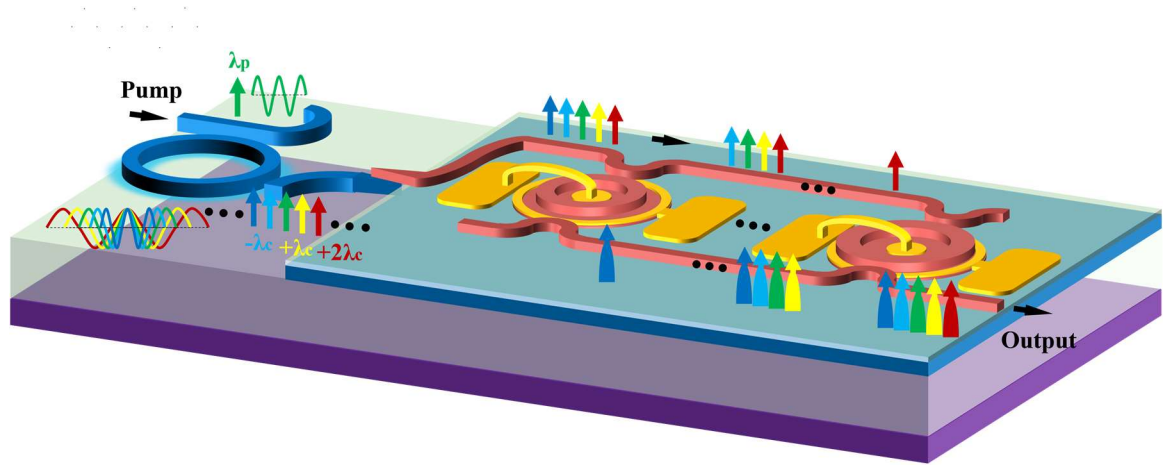


Figure 39: The schematic of an integrated Tb/s interconnect based on Kerr frequency comb generation in a SiN microcavity and high-speed resonant modulation utilizing plasma dispersion effect of Si. Each resonator acts as an add-drop filter and modulator simultaneously. The blue layer is SiN, and the red layer denotes Si.

Considering further developments on heterogeneous platforms, the DLSi on SiN platform is an interesting option to implement the comb-based interconnect idea. It can enable high speed compact modulation through cavity resonance or coupling modulation, each is suitable for an application and can be optimized towards compact and/or low power functionality.

Finally, the optimization of heterogeneous resonant coupling modulator is another interesting direction. In principle, the coupling modulator can reach Q factors as high as 10^7 , which can be used toward extremely efficient modulation. Pursuing that direction requires a thorough revision of ion implantation, interlayer coupler design, and appropriate mitigation of the implantation induced losses in the Si waveguide. If such considerations

are experimentally demonstrated, the SON modulator can work at record low powers thanks to the field enhancement in SiN resonator. Also, in future demonstrations, the input and output couplers can be optimized, or an alternative edge coupling is used to reduce the overall back to back insertion loss. This eliminates the need for SOA, which reduces the noise figure at the output and demonstrates the potential of the device for low input optical power applications.

6.2 Achievements and Contributions to the Field

Integrated nanophotonics for various optical signal processing applications is among the fastest growing fields in the area of electrical engineering and applied physics. In contrast to electronics, where the essential device is a transistor and the dominant material is Si, the toolbox of fundamental materials and devices required for a typical PIC is vast. Therefore, new material platforms beyond single-layer Si are required to host devices and systems, which is the core subject of my Ph.D. work. I have mainly focused on the design, implementation, and characterization of a series of essential integrated photonic elements required for realization of complex nanophotonic applications in heterogenous material platforms.

To meet the demanding features of photonic integration, a substantial portion of this research effort is dedicated to the development of novel material platforms. More specifically, the double layer crystalline silicon (DLSi) platform is envisioned and developed for nanophotonic applications [77, 79, 141]. The quality of platform is checked and controlled through nanophotonic device integration and characterization. A record intrinsic Q factor of 2.35×10^5 in a 10 μm radius multimode microring resonator confirms the quality of device and platform development to match the SOI performance. Also, a

prototype device in the hybrid structure is demonstrated to showcase the reconfigurable capability. The electro-optical characterization demonstrates the frequency tuning in excess of 100 GHz with zero DC power consumption. The platform is further used to demonstrate programmable optical switching and high-speed modulation (exceeding 20 Gbps) with extended tuning capacity [78, 80, 142]. Such demonstration has paved the path to show extensive potentials of such unique material platform, and a similar approach can be adopted for realization of other functional devices and systems, including reconfigurable integrated filters and routers with unprecedented performance and eliminated DC power consumption or need of passive trimming.

With the knowledge gained through DLSi platform and device integration, the silicon on silicon nitride (SON) heterogenous material platform is proposed, developed and used in several important demonstrations pushing the state-of-art a step forward [136, 143-145]. In the first stage of development, challenges of SiN integration with Si is resolved and a successful bonding procedure is developed. The design, implementation, and characterization of an adiabatic ultra-broadband interlayer coupler with an octave of frequency span is a breakthrough for ultra-low-loss and high bandwidth applications. The adiabatic coupler loss is experimentally extracted to be less than 0.03 dB over a wide bandwidth (1530-1565 nm), which is to the best of our knowledge the lowest reported in any CMOS-compatible hybrid material platform. To further showcase the capabilities of the platform, a full hybrid optical path, including a microresonator with $Q_{\text{int}} = 3 \times 10^6$ is demonstrated. By optimization of SiN deposition and etching which is done for this research, it is possible to increase the Q beyond 10^7 .

Another major contribution of this research is through the design, optimization, implementation, and characterization of a resonance-based integrated electro-optic modulator on the SON material. Unlike the majority of resonant modulators, the modulation mechanism envisioned here is based on changing the coupling amplitude, which eliminates the linewidth-speed trade-off limit in the resonant devices while keeping the sensitivity unchanged. Such a design is specifically important as our platform can offer high- Q resonators which face the linewidth limit at Q s exceeding 2×10^4 . The SON platform is also interesting as it can offer high speed plasma dispersion in the Si layer. The fabricated active device has a Q factor of 1.55×10^5 , with the finesse of 181, which exceeds an order of magnitude improvement from the latest demonstration. The S_{21} measurement also confirms the successful demonstration of coupling modulation where the 3-dB bandwidth is close to an order of magnitude higher than the resonance linewidth. The integrated modulator supports speeds in excess of 15 Gbps range without sophisticated optimization. It is rather straightforward to show that modest optimization on the active device fabrication can further increase the modulation data rate up to 50 Gbps. Also, the linearity of the device makes it possible to include PAM-4 modulation which can increase the speed above 100 Gbps.

Finally, the nanophotonic devices and systems demonstrated in different parts of this work utilize carefully optimized fabrication processes tailored to deliver high quality of lithography, etching, and post fabrication treatment to define optical guiding structures and microcavities. Through rigorous design of experiments, various recipes and procedures are developed to enable superior nanophotonic performance, which has a great impact in other

areas of integrated photonic device fabrication beyond the scope of this research effort [146,147].

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