

INTEGRATED FRONT-END ANALOG CIRCUITS FOR MEMS SENSORS IN ULTRASOUND IMAGING AND OPTICAL GRATING BASED MICROPHONE

A Dissertation
Presented to
The Academic Faculty

By

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
in
Electrical and Computer Engineering



School of Electrical and Computer Engineering
Georgia Institute of Technology
August 2009

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DEDICATION

To my loving family ...

ACKNOWLEDGMENTS

First of all, I am thankful to God for giving me the strength to pursue graduate school and survive Georgia Tech's rigorous academic program. I like to express my sincere gratitude to everyone who supported and helped me during this long journey. Without them, I would not have made it this far. I have been very fortunate to work with Dr. Levent Degertekin and Dr. Paul Hasler, both as my co-advisors. I appreciate the time and effort they have put into my thesis work along with my committee members, Dr. Farrokh Ayazi, Dr. Oliver Brand, Dr. David Anderson and Dr. Peter Hesketh. Their dedication to students is inspiring, and I am proud to be a branch on the Degertekin and Hasler family tree.

I give special thanks to professor Alvin Connelly who brought me to Georgia Tech as a Texas Instrument Fellow. I still remember the very first conversation I had with him over phone when I was deciding which school should I pick for graduate studies. Thanks to Dr. Connelly, I have never regretted my decision of coming to Georgia Tech Analog Circuit's program.

I had the great fortune to work on my Master's degree with Dr. Phil Allen. He has been a great source of inspiration to me. He helped me try different areas of research and get my hands dirty with a wide range of topics. He really prepared me for the graduate research that I was about to embark on during my years as a PhD student. Since his retirement, I have always missed his presence.

I believe that for every student in higher education, there is a key person who set's student's future path. In my case, Dr. Jeff Jessing has that distinction. During my undergraduate studies, I had the pleasure to take micro-electronics classes taught by him at Texas A and M University. With his dedication to teaching, he was able to implant the desire in me for taking the non-traditional path in Analog Circuits, in those days when digital was the buzz word.

During my graduate days at Georgia Tech, I had the opportunity to work in three research groups. I started as a rookie in Analog Circuits and Signal Processing group. I am thankful to all the colleagues who sparked my interest to stick around for a PhD. My research involved collaboration between MEMS group MiST in Mechanical Engineering and circuit's group CADSP in Electrical Engineering. Through these collaborations, I gained a lot of knowledge that was simply not possible without them. I am particularly thankful to Dr. Wook Lee, Dr. Neal Hall, Caesar Garcia and Baris Bicen for collaboration on hearing aid project. I was very fortunate to work with Arindam Basu and Dr. Sheng-Yu Peng on the circuits side of things. They had the major contribution to my research work. For the MEMS side, I like to thank Jaime Zahorian and Dr. Rasim Guldiken for spending countless hours in the cleanroom for fabricating CMUT on CMOS.

I am grateful to Texas Instruments for awarding me Master's Analog Fellowship at Georgia Tech. Ron Cox at Texas Instruments was instrumental in introducing me to Georgia Tech's Analog program. Special thanks to Dr. John Bordelon who kept things smooth with my collaborators at Texas Instruments.

To my friends, I thank you for your understanding and support throughout my PhD. My friends from Dhahran, College Station, Atlanta and the Bay Area, have been a key contributor to my studies through out these long years. I thank my officemates for having all sort of discussions that had no direct contribution to the research work, but made the days bearable for so many years. They made my stay pleasant while at school.

Finally to my loving family who has always been there for me regardless what ever path I have taken in life. You all have been asking me "how much longer?" for so many years and now I have an answer. I am grateful to my mother(late) and father for their investment and belief in me. They have supported me through out my studies. I can not imagine to be standing where I am right now, without their support and prayers. I have been fortunate to spend so many holidays with my sister and brother-inlaw in Washington DC. They truly made DC, a home in US for me. There are no words that can express my feelings and

appreciation for them. Last but not least, to my wife Sehar who has been an equal partner in this journey. Your love inspired me through these years. For even my dreams were not as breathtaking as this life came to be with you. Thank you.

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SUMMARY

The objective of this research is to develop and design front-end analog circuits for Capacitive Micromachined Ultrasound Transducers (CMUTs) and optical grating MEMS microphone. This work is motivated by the fact that with micro-scaling, MEMS sense capacitance gets smaller in a CMUT array element for intravascular ultrasound imaging, which has dimensions of 70um x 70um and sub pico-farad capacitance. Smaller sensors lead to a lower active-to-parasitic ratio and thus, degrades sensitivity. Area and power requirements are also very stringent, such as the case of intravascular catheter implementations with CMOS-First CMUT fabrication approach. In this implementation, capacitive feedback charge amplifier is an alternative approach to resistive feedback amplifiers. Capacitive feedback charge amplifier provides high sensitivity, small area, low distortion and saving power. This approach of charge amplifiers is also suitable in capacitive microphones where it provides low power and high sensitivity. Another approach to overcome capacitive detection challenges is to implement optical detection. In the case of biomimetic microphone structure, optical detection overcomes capacitive detections thermal noise issues. Also with micro-scaling, optical detection overcomes the increased parasitics without any sensitivity degradation, unlike capacitive detection. For hearing aids, along with sensitivity, battery life is another challenge. We propose the use of 1-bit front-end sigma-delta ADC for overall improved hearing aid power efficiency. Front-end interface based on envelope detection and synchronous detection schemes have also been designed. These interface circuits consume currents in micro-ampere range from a 1.5V battery. Circuit techniques are used for maximizing linear range and signal handling with low supplies. The entire front end signal processing with Vertical Cavity Surface Emitting Laser (VCSEL) drivers, photodiodes, filters and detectors is implemented on a single chip in 0.35um CMOS process.

CHAPTER 1

ANALOG INTERFACE FOR MEMS SENSORS

Microelectromechanical system (MEMS)-based sensors gather information from the environment through measuring mechanical, thermal, biological, chemical, optical, and magnetic phenomena. The electronics then process the signal information derived from the sensors in the presence of parasitics and noise. Because MEMS devices are manufactured using batch fabrication techniques similar to those used for integrated circuits, unprecedented levels of functionality, reliability, and sophistication can be placed on a small silicon chip at a relatively low cost [1]. Interface electronics becomes challenging with the miniaturization of sensors in the presence of parasitics and reduced sense capacitance. The first part of this research focuses on an alternative approach of using capacitive feedback charge amplifiers to a resistive feedback charge amplifier for addressing these issues. The second part covers interface electronics for optical detection, which is another approach to capacitive detection as used in hearing aid microphones with strict power and supply limitations.

MEMS have the capabilities to manipulate and process signals from the physical world. The micro-scale size of these device increases the relative parasitics with respect to the sense capacitance. In order to mitigate the parasitics and increase the sensitivity of the signal of interest, we make use of a capacitive feedback charge amplifier with pseudo-MOS resistors for stabilizing the DC input node voltage. This capacitive detection technique is used with capacitive micromachined ultrasound transducers (CMUT) for intra-vascular imaging and also with capacitive MEMS microphones. With post-processed CMUTs on a CMOS wafer, we have designed an integrated chip solution for an ultrasound signal transceiver.

However, capacitive detection is not the only approach for sensing MEMS. Optics is

now also becoming feasible for sensing MEMS with the reduction in size of the vertical cavity surface emitting laser (VCSEL). Optical detection is very powerful for high-resolution interferometric displacement sensing. The parasitics and thermal noise of MEMS sense capacitance can also be solved with the use of optics. This approach gives added benefit as the shot noise limit can be reached [2]. In a miniature sized packaging, diffraction-based MEMS membranes can be integrated with VCSEL to form a highly sensitive microphone for hearing aid applications. We have investigated and designed various circuits for a low-power, low-voltage electronic interface with the optical MEMS sensor in microphone applications. These interface electronics consume micro-amperes of current from a 1.5V battery. Furthermore, a 1-bit ADC is also proposed for the front-end interface for optical detection in order to maximize the power efficiency in hearing aid applications.

1.1 Capacitive Micromachined Ultrasound Transducers

MEMS are embedded systems that involve one or more micromachined components or structures. They enable higher level functions, though their utility may be limited. For example, a micromachined pressure sensor in one's hand is useless, but, under the hood, it controls the fuel-air mixture of the car engine. These sensors often integrate several functions together into one package for greater utility (e.g., merging an acceleration sensor with electronic circuits for self-diagnostics). Additionally, the cost benefits of MEMS can come either directly through low unit pricing or indirectly by cutting service and maintenance costs [3]. This section will cover capacitive micromachined ultrasound transducers (CMUT) for intra-vascular imaging.

1.1.1 Intra-vascular Ultrasound Imaging

Intravascular ultrasound (IVUS) is a medical imaging technique that uses a catheter with a built-in ultrasound probe. This makes use of ultrasound to see the inside of the blood vessels. It gives a cross sectional view of the inner wall of blood vessels. IVUS is primarily used in coronary arteries to examine the amount of plaque buildup along the inner

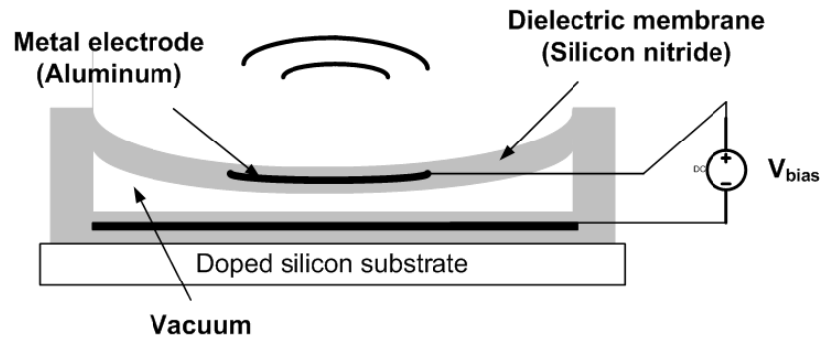


Figure 1.1. Cross sectional view of the Capacitive Micromachined Ultrasound Transducer (CMUT). In transmit mode, the electrodes are actuated with AC signal on a high voltage DC bias. While in receive mode a DC bias is applied on the electrodes and the CMUT is connected with the receive electronics.

walls. Visualizing plaque is the most valuable use of IVUS, since plaque cannot be seen by angiography.

1.1.2 Capacitive Micromachined Ultrasound Transducer

Piezoelectric transducers have long dominated ultrasonic transducer technology; however, CMUTs have recently emerged as an alternative technology, offering advantages such as wide bandwidth, ease of fabricating large arrays, and potential for integration with electronics [4].

CMUTs are essentially capacitors with one moveable electrode. Actuation occurs according to Coulombs Law, as shown in Fig. 1.1. The force of attraction generated between two oppositely charged electrodes causes the moveable electrode to deflect. If an alternating voltage is applied to the device, the moveable electrode begins to vibrate, thus generating ultrasound. If CMUTs are used as receivers, then changes in pressure, such as those from an ultrasonic wave, cause the moveable electrode to deflect, hence producing a measurable change in capacitance.

1.1.3 Challenges in Capacitive Sensing and IVUS imaging

Capacitive transduction is one of the more important and widely used techniques in MEMS, such as in CMUTs. In a typical two-chip hybrid approach there is current leakage along with parasitics to ground. This parasitic capacitance along with the static capacitance of

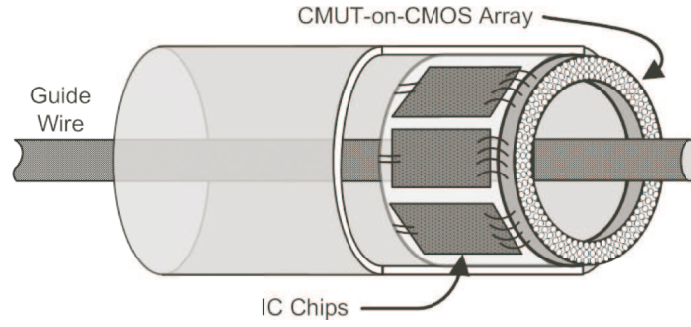


Figure 1.2. Schematic diagram of the IVUS catheter employing the forward-looking annular-ring CMUT array with integrated front-end electronics.

the sensor can be much larger than the capacitance variations to be sensed. This creates many challenges for high sensitivity, high dynamic range detection. In addition, power consumption is also a critical issue in applications like MEMS hearing aids and CMUT-based IVUS imaging.

In intra-vascular ultrasound applications, the piezoelectric transducer technology has prevented effective implementation of systems with diameters below 1 mm. On the other hand, the latest advancements in CMUT technology enable the construction of forward-looking (FL) annular-ring transducer arrays that can be placed in front of the catheter [5]. Because of the small size of each CMUT element in an FL-IVUS array, which is on the order of $100\mu\text{m}$ and is much smaller than that in a non-invasive 1-D CMUT array, the parasitic capacitances introduced by the electrical interconnects can easily overwhelm the device capacitance and impair the achievable signal-to-noise (SNR) ratio. Either integrating the CMUT array with electronics on the die level or building the CMUT array directly on CMOS elements, as illustrated in Fig. 1.2, can avoid the performance degradation caused by the cable losses. Since the probe is located inside the patient's body, power dissipation is another major concern. Because IVUS imaging requires a high resolution and because the imaging depth for vessels is relatively shallow, the transducers usually operate at a high frequency; therefore, low-power electronics are very critical.

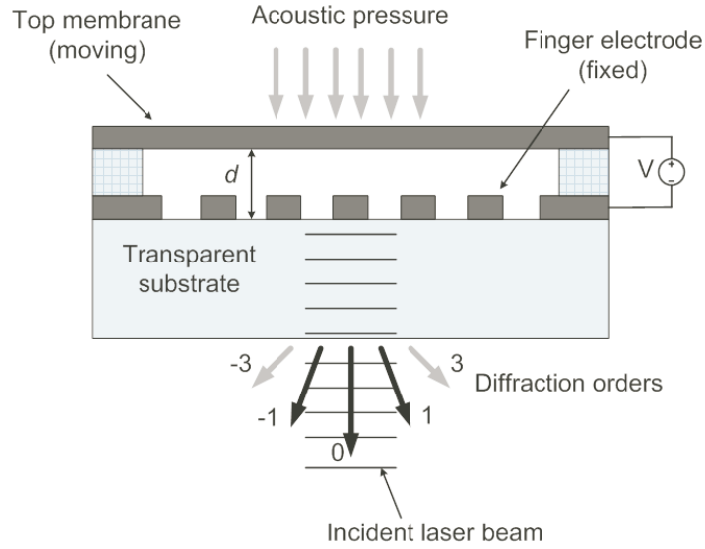


Figure 1.3. Schematic diagram of a micromachined acoustic sensor with a built in phase-sensitive diffraction grating for displacement detection.

1.2 Diffraction Grating Optical Microphone

A simple schematic of the diffraction-based optical displacement detection scheme is illustrated in Fig. 1.3. It consists of a transparent substrate with an optically reflective diffraction grating fixed to the surface. The grating consists of alternating regions of reflective fingers. An optical reflector, whose displacement is to be monitored, is placed behind the substrate. A highly compliant membrane is made part of a phase-sensitive diffraction grating, and the deflection resulting from external acoustic pressure alters the intensities of the diffracted orders, which are monitored with photodiodes [6]. Figure 1.4 illustrates the diffractions orders on the intensity plot [2].

This highly sensitive optical displacement detection method implemented in a small volume and with reduced power consumption has the potential to compete with commonly used capacitance-based methods in micromechanical sensor systems [2]. The traditional capacitive acoustic sensors do not scale down favorably. In other words, reducing the membrane size decreases the ratio of the active capacitance to the parasitic capacitance, thereby requiring a gain in mechanical compliance, which in turn necessitates the use of very thin, low-stress membranes, that are difficult to reproduce in a repeatable manner [1].

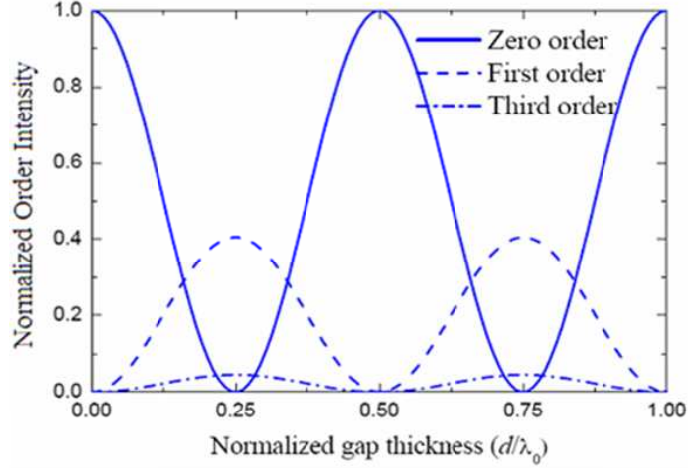


Figure 1.4. Diffraction efficiencies of the zero, first, and third orders.

Reducing the membrane gap to increase the active capacitance can increase the stiffness of the trapped air and reduce the electrical sensitivity by limiting the sustainable electric field [7, 8]. To address these problems, optical techniques are used with diffraction gratings as a method to measure displacement from acoustic pressure in microphones. This hybrid integrated system can be implemented in acoustic-sensor applications using both continuous wave and pulse VCSEL to show reduced power consumption.

1.3 Low Power and Low Voltage Design

There are limitations of integrated circuits when faced with the requirements of low power. Low-noise amplifiers are critical in applications where a large dynamic range is needed. We can express dynamic range as signal-to-noise ratio (SNR). As the standard CMOS technology continues to improve, the power supplies are decreasing and even going below 1 Volts. This reduction comes from the fact that processes are designed for speed and this indirectly affects the breakdown voltages hence the maximum power supply voltages.

Along with noise, we must also take into account the linearity of the amplifiers. If the amplifier is nonlinear, then a pure sinusoidal input signal will create harmonics. Now if the total harmonic distortion (THD) is more than the noise, then in this case, the non-linearity

becomes the limiting factor. It is common to use the notation of signal-to-noise plus distortion (SNDR). This includes noise and the distortion in dynamic range specifications.

When considering low noise design, we start with the single MOS transistor. The equivalent input mean square voltage noise is given by:

$$v_n^2 = \frac{8kT}{3g_m} + \frac{K}{WLC_{ox}f} \quad (1.1)$$

The first part of the equation is the thermal noise and the second part is the flicker noise where k is the Boltzman's constant, T is temperature, g_m is the small signal transconductance, K is the flicker noise, W is the width of the transistor, L is the length of the transistor, f is the frequency in Hertz and C_{ox} is the gate oxide capacitance per unit area [9].

In many respects, the thermal noise of a MOSFET device is equivalent to the thermal noise of a BJT. Unfortunately, the $1/f$ noise is much larger. We note that minimizing the thermal noise of an amplifier is reasonably straightforward. From the first term in (1.1), we see that we want the small-signal transconductance g_m to be large to minimize the equivalent input-mean-square noise voltage. This can be done by large dc currents or large W/L ratios. For the $1/f$ noise, there are at least three approaches to minimizing the $1/f$ noise of CMOS amplifiers. The first is to minimize the noise contribution of the MOSFETs through circuit topology and transistor selection (NMOS vs. PMOS), dc currents, and W/L ratios. The second is to replace the MOSFETs by BJTs to avoid the $1/f$ noise. The third is to use external means, such as chopper stabilization, to minimize the $1/f$ noise.

1.3.1 Total Harmonic Distortion (THD)

If a sinusoidal signal is applied to a linear time-invariant system, it is well known that the output will also be a sinusoidal waveform at the same frequency, but possibly with different magnitude and phase values. However, if the same input is applied to a nonlinear system, the output signal will have frequency components at harmonics of the input waveform, including the fundamental harmonic. For example, if a 1 MHz sinusoidal input signal

is used, the output signal will have power at the fundamental, 1 MHz, as well as at the harmonic frequencies, 2 MHz, 3 MHz, 4 MHz, and so on. The total harmonic distortion (THD) of a signal is defined to be the ratio of the total power of the second and higher harmonics components to the power of the fundamental for that signal. In units of dB, THD is found using the following relation:

$$THD = 10 \log\left(\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \dots}{V_f^2}\right) \quad (1.2)$$

where V_f is the amplitude of the fundamental and V_{hi} is the amplitude of the i 'th harmonic component. Sometimes THD is presented as percentage value. In this case,

$$THD = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \dots}}{V_f} \times 100 \quad (1.3)$$

It should be noted that the THD value is always a function of the amplitude of the input signal, and thus the corresponding signal amplitude must also be reported. Typically first 5 harmonics are used for THD calculations as the higher components falls off very quickly.

1.3.2 Rail-to-rail Input Stages

A very well-known approach for implementing an input stage with a rail-to-rail common mode input range is to place an N-type and P-type differential pair in parallel[10], as shown in Fig. 1.5(a). In this circuit the bias currents are generated by transistors. In each case of the differential pair, the biasing transistor's drain to source voltage should be able to support the current it provides. For the N-type differential pair, this determines the lower boundary of operation range of the N-type metal-oxide-semiconductor (NMOS) differential pair. The upper boundary is determined by the supply voltage and the fact that the gate voltage of a transistor may exceed the drain voltage by only a threshold voltage before it brings the transistor out of saturation. Therefore, the N-type differential pair can operate from a certain common-mode input voltage above the negative supply rail up to a certain

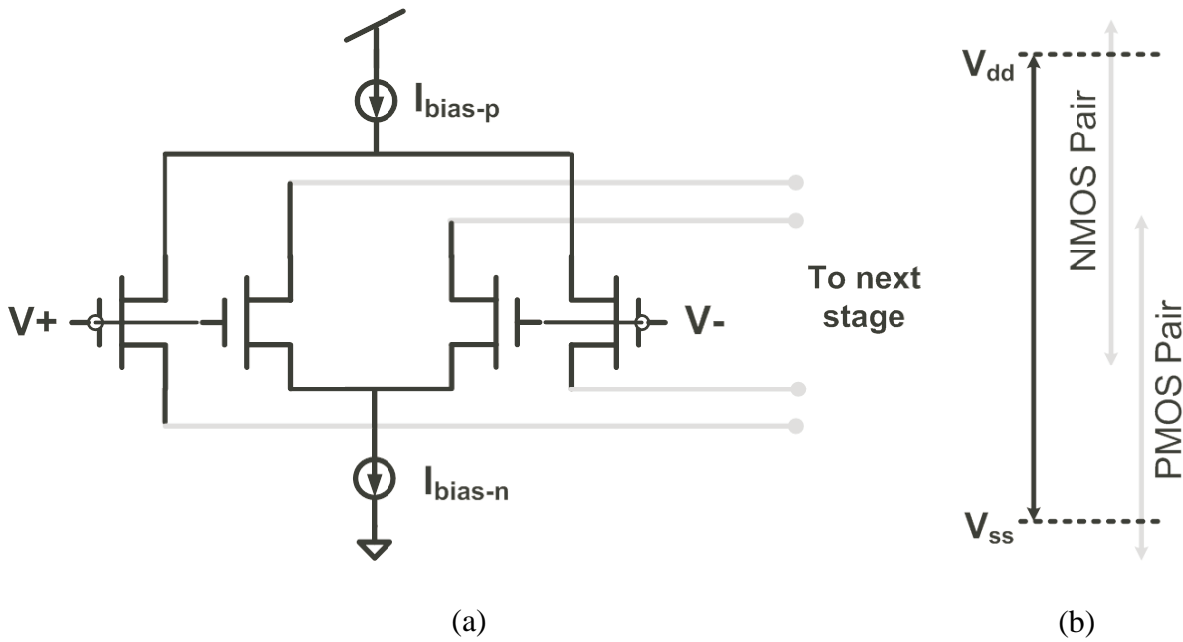


Figure 1.5. (a)Rail-to-rail differential input pair (b)Voltage range of operation

common-mode input voltage above the positive supply rail as indicated in Fig. 1.5(b). For the PMOS differential pair the opposite is true. Thus applying the two complementary input pairs in parallel results in an input stage which has a common-mode input range that can even exceed the supply rails., provided that adequate circuitry is available for combining the output signals of the individual differential pairs.

Three different operation areas can be distinguished:

- The common-mode input voltage is near the negative supply rail; signal transfer will take place only by the P-type differential pair.
- The common-mode input voltage is in a region somewhere in the middle between the supply voltages; both the NMOS and the PMOS differential pairs will be active.
- The common-mode input voltage is near the positive supply rail; signal transfer will take place only by the N-type differential pair.

It is clear that without precautions the transconductance g_m of the combination strongly

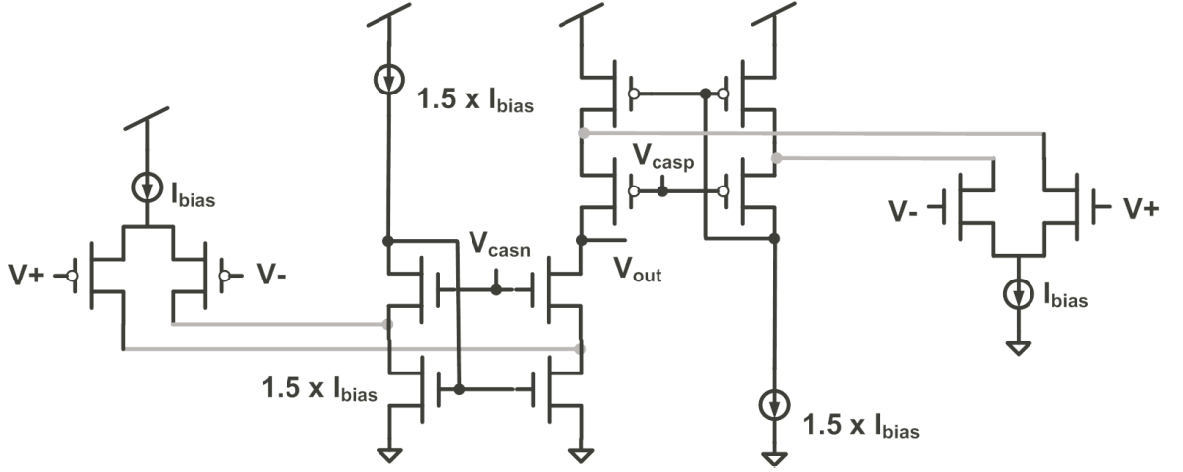


Figure 1.6. Complementary input rail-to-rail folded cascode amplifier.

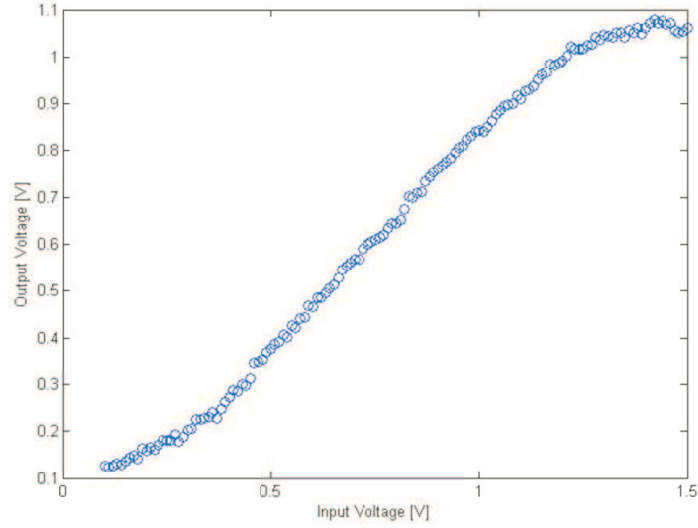


Figure 1.7. ICMR measurement for rail-to-rail input.

depends on the common-mode input level because only in a region somewhere in the middle of the supply voltages will both differential pairs be active. A nonconstant (i.e. a common-mode input voltage dependent) transconductance g_m is undesirable, because a variation in g_m causes a variation in the unity-gain bandwidth of the amplifier and prevents an optimal frequency compensation. This reduces the feasible unity-gain bandwidth of the compensated amplifier. Furthermore, a common-mode input voltage dependent transconductance causes extra distortion.

The ICMR measurement is shown in Fig. 1.7. We see the input common mode of a

a very nonlinear resistor-like characteristics. It is commonly called "tobi element" (after Tobi Delbruck)[12]. It consists of a diode-connected well transistor in one direction and a parasitic vertical bipolar transistor in the other as shown in Figure 1.9. It essentially has two modes of operations, namely bipolar and MOS mode. The mode of conduction when the well voltage is higher than the gate voltage: The structure acts as a diode-connected MOS transistor. The opposite case: The p+/n junction is forward-biased, and the device as a whole acts as a bipolar transistor with two collectors. It can also be looked at like to diodes in parallel with opposite polarity. The current increases exponentially with voltage with either sign of voltage, and there is an extremely high resistance region around the origin. Tobi element now can be used in conjunction with capacitive division in amplifiers. As our microphone is low power and low voltage batttey system, we will make use of linearity maximizing approachs through out receiver electronics.

CHAPTER 2

CHARGE AMPLIFIER FOR CAPACITIVE SENSING

Capacitive detection is a common, and most important method used in microelectromechanical systems, such as in CMUTs. The flexibility of digital data processing systems has sparked significant research efforts to develop new algorithms to reconstruct, enhance, and analyze ultrasound images. However, the ability and usefulness of these algorithms depend on the quality (e.g., SNR, bandwidth, and dynamic range) of the original echo signal, making the transducer and associated front-end electronics the most critical components of ultrasound imaging systems. In this section, we propose a capacitive feedback charge amplifier for front-end analog processing of CMUT sensors.

2.1 Analysis of Capacitive Sensing Charge Amplifier

Fig. 2.1 shows the small-signal model of the capacitive sensing charge amplifier. In this amplifier, the input capacitance, the explicitly drawn capacitance, and all the parasitic capacitances from the floating node to ground are all included in C_w . The amplifier is modeled as a first-order system in the following analysis [13].

The transfer function and SNR expression are summarized below:

Transfer function:

$$\frac{V_{\text{out}}(s)}{C_{\text{sensor}}(s)} = -\frac{V_{\text{bias}}}{C_f} \cdot \frac{1 - sC_f/G_m}{1 + sC_{\text{eff}}/G_m}, \quad (2.1)$$

where $C_{\text{eff}} = (C_o C_T - C_f^2)/C_f$, $C_o = C_L + C_f$, and $C_T = C_{\text{sensor}} + C_w + C_f$.

SNR:

$$SNR \geq C_{\text{eff}} \cdot \frac{2\kappa \Delta V_{\text{lin,max}}^2}{nqU_T}, \quad (2.2)$$

where κ is the subthreshold slope coefficient of transistors, n is the effective number of noisy transistors, q is the charge of an electron, U_T is the thermal voltage, and $\Delta V_{\text{lin,max}}$ is the maximum input linear range of the differential pair. From (2.1), the circuit can achieve

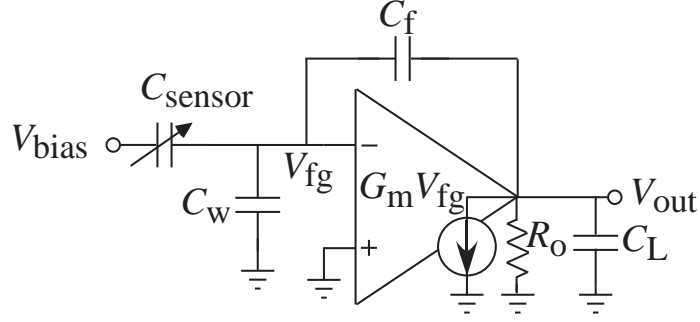


Figure 2.1. Schematics of the small-signal model of capacitive sensing charge amplifier.

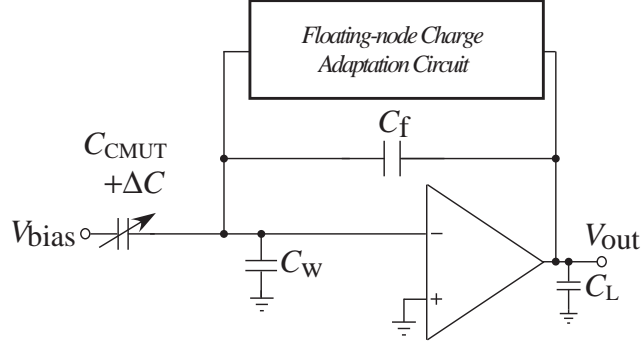


Figure 2.2. A new approach to sensing capacitance change by using a charge amplifier and a floating-gate based charge adaptation circuit.

high sensitivity by choosing a large V_{bias} and a small C_f . From (2.2), a larger G_m can improve the linearity and the SNR.

2.2 Charge Amplifier with Charge Adaptation Feedback

Fig. 2.2 shows the basic topology of capacitive feedback charge amplifier. The charge adaptation circuit can be modeled by a small feedback conductance, g_f , as shown in Fig. 2.3(a).

The transfer function of the sensing circuit can be expressed as:

$$\frac{V_{\text{out}}(s)}{C_{\text{CMUT}}(s)} = \frac{V_{\text{bias}}}{g_f} \cdot \frac{s(s \frac{C_f}{G_m} - 1)}{s^2 \frac{C_T C_o - C_f^2}{G_m g_f} + s \left[\frac{C_f + C_T/A}{g_f} + \frac{C_T + C_o - 2C_f}{G_m} \right] + 1}, \quad (2.3)$$

where A is the amplifier gain. As shown in Fig. 2.3(b), the adaptation scheme creates an extra zero at the origin and an extra low-frequency pole around g_f/C_f , assuming A is large enough. If the transistors are in subthreshold region, we can derive the minimum detectable

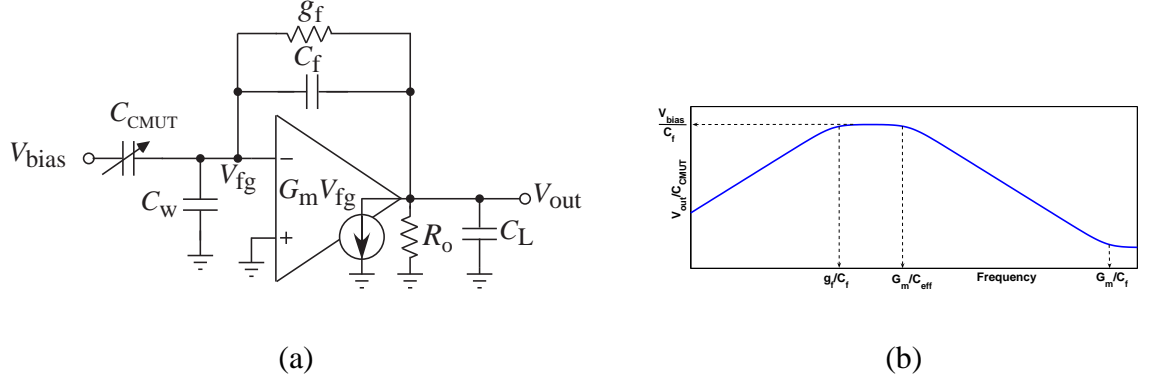


Figure 2.3. (a) The small signal model of a charge amplifier with charge adaptation circuit, which is modeled by a feedback conductance. (b) Simulated frequency response of the circuit shown in (a).

capacitance as:

$$\Delta C_{\text{min,CA}} = \frac{1}{V_{\text{bias}}} \cdot \sqrt{\frac{nqU_T C_T C_f}{2kC_o}}. \quad (2.4)$$

Conventionally, CMUT signals are converted from capacitive currents into voltages by using either resistive terminations followed by amplifiers, common-gate amplifiers, or resistive feedback TIAs as shown in Fig. 2.4 [4]. The first approach suffers from the direct trade-off between bandwidth and input-referred current noise because they both are proportional to $1/R_{\text{in}}$. In the common-gate topology, although the noise can be minimized by maximizing the load resistance and the overdrive voltage of M_2 without affecting the bandwidth, it incurs a reduction in the output voltage headroom. In the last case, because the feedback resistance does not limit the voltage headroom and because the input capacitance can be reduced by the amplifier gain by the "shunt-shunt" feedback, TIA topology is widely used in capacitive sensing applications. However, when the operating frequency is high, the bandwidth can be limited by the parasitic feedback capacitance.

It is interesting to note that Fig. 2.3(a) can also be viewed as a small signal model of a TIA with a parasitic feedback capacitance. The expression of (2.3) can be rearranged to

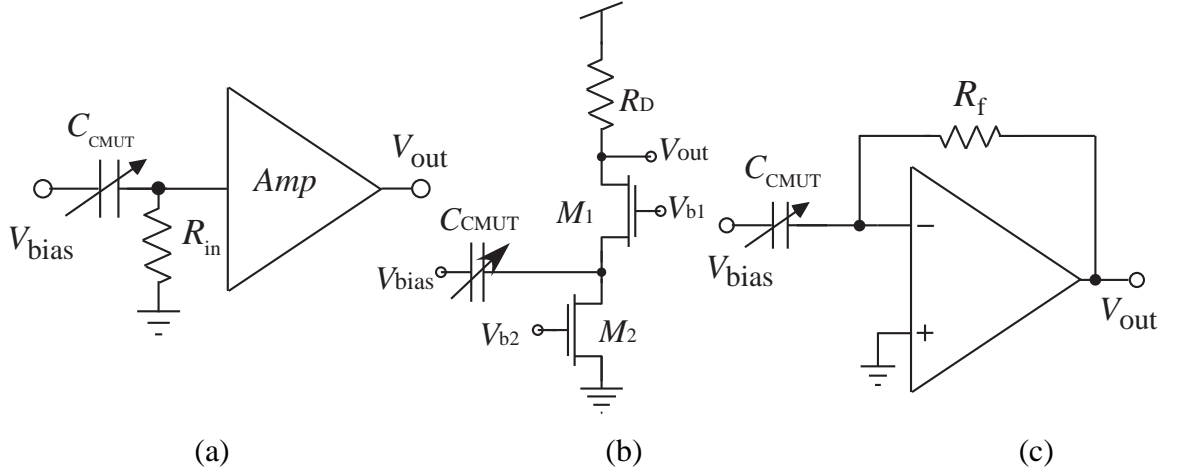


Figure 2.4. (a) Schematic of a resistive termination followed by an amplifier stage. (b) Schematic of a common-gate amplifier. (c) Schematic of a resistive feedback transimpedance amplifier.

describe the transfer function of the TIA as:

$$\frac{V_{out}(s)}{I_{CMUT}(s)} = \frac{V_{out}(s)}{sV_{bias}C_{CMUT}(s)} = \frac{1}{g_f} \cdot \frac{s\frac{C_f}{G_m} - 1}{s^2\frac{C_T C_o - C_f^2}{G_m g_f} + s\left[\frac{C_f + C_T/A}{g_f} + \frac{C_T + C_o - 2C_f}{G_m}\right] + 1}. \quad (2.5)$$

The minimum detectable capacitance of the TIA can be derived as:

$$\Delta C_{min,TIA} = \frac{g_f}{\omega_0 V_{bias}} \cdot \sqrt{\frac{nqU_T C_T}{2\kappa C_f C_o}}, \quad (2.6)$$

where ω_0 is the operating frequency.

Although the topologies of a TIA and a charge amplifier are the same, their design philosophies are different. In a typical TIA design, the operating frequency should be lower than the first pole, which corresponds to the ascendent region in Fig. 2.3(b). The sensitivity-bandwidth trade-off of a TIA is obvious from (2.5) and (2.6). Increasing the bandwidth by increasing g_f decreases sensitivity. On the other hand, using a charge amplifier to sense the CMUT signals can avoid all the dilemmas mentioned before. The sensitivity can be improved by choosing large values of V_{bias} and C_L and a small value of C_f . The bandwidth, corresponding to the second pole, can be extended by using a larger value of G_m .

2.2.1 Design Procedure

With given specifications of minimum detectable capacitance (ΔC_{min}), bandwidth (ω_{3dB}), and SNR, the goal is to optimize the current consumption (I_b), feedback capacitance (C_f),

and load capacitance (C_L). We assume that the known variables include the total capacitance seen from the floating node ($C_T \approx C_{\text{sensor}} + C_w$), the bias voltage of the sensing capacitor (V_{bias}), and the maximum input linear voltage of the transconductance amplifier ($\Delta V_{\text{lin,max}}$). We also assume that the maximum output linear range is not limited by the supply rails but only affected by the nonlinearity of the OTA.

The design procedure starts from the sensitivity expression:

$$\Delta C_{\min}^2 = \frac{nqU_T}{2\kappa V_{\text{bias}}^2} \cdot \frac{C_T C_f}{C_o}, \quad (2.7)$$

where ΔC_{\min} is the minimum detectable capacitance. From (2.7) we can have:

$$\frac{C_f}{C_L} \leq \frac{\Delta C_{\min}^2}{C_T} \cdot \frac{2\kappa V_{\text{bias}}^2}{nqU_T}. \quad (2.8)$$

Since only the ratio of C_f to C_L matters, these two capacitances can be chosen from reasonable and practical values.

The next step is to determine the current consumption for a given C_f/C_o ratio. Assuming that an OTA is biased in subthreshold region, the required current is estimated as:

$$I_b \geq \omega_{3dB} \cdot \frac{2U_T}{\kappa} \cdot \frac{C_o C_T}{C_f} \quad (2.9)$$

$$I_b \geq \sqrt{SNR \cdot \frac{2nqU_T^3 \omega^2}{\kappa^3 \Delta V_{\text{lin,max}}^2} \frac{C_o C_T}{C_f}}. \quad (2.10)$$

The current consumption is usually determined by (2.9).

2.2.2 Setup And Measurement Results

A version of the capacitive sensing circuit is fabricated in a $0.5 \mu\text{m}$ double-poly CMOS process and is tested with a MEMS microphone sensor. The setup diagram is shown in Fig. 2.5. A tunneling junction and an indirect injection transistor are integrated on chip as floating-node charge adaptation circuitry. To measure the characteristics without any auto-zeroing scheme, the charge adaptation circuitry is disabled by shorting the tunneling and the drain voltages to V_{DD} supply. The floating-node voltage settles slowly to an equilibrium

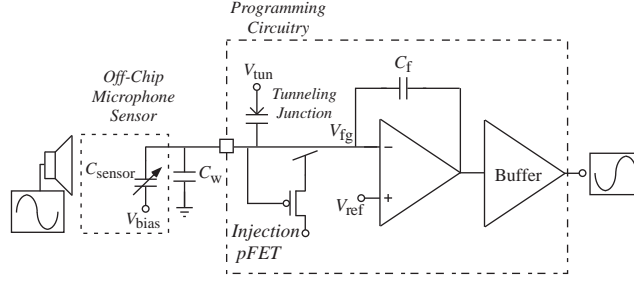


Figure 2.5. Setup of capacitive sensing measurement using a capacitive feedback charge amplifier.

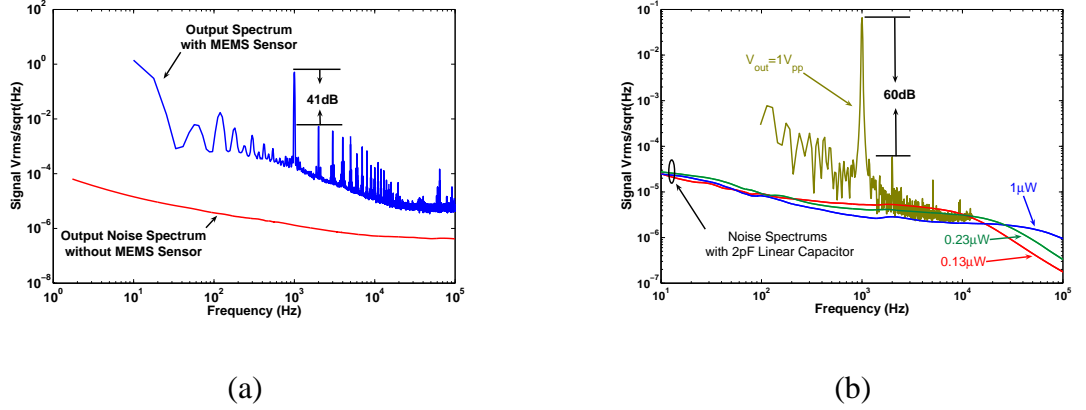
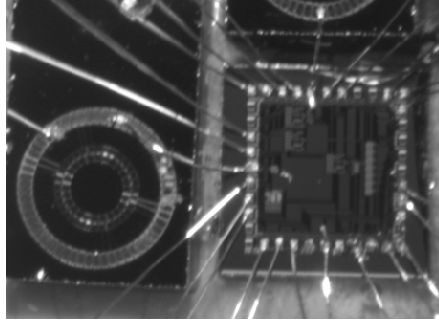


Figure 2.6. (a) The measured output signal and noise spectrums. A card type speaker is used as the 1K Hz acoustic signal source and a MEMS microphone is interfaced with the circuit. (b) Measured output signal and noise spectrums when the circuit is interfaced with a linear 2 pF capacitor.

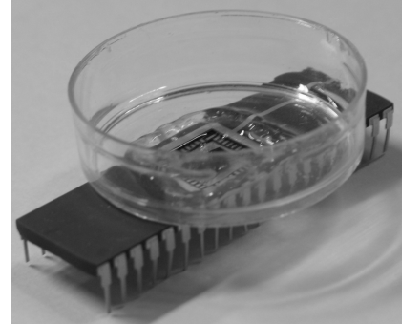
value and the non-inverting terminal voltage can be adjusted so that the output is at the mid-rail.

The spectrum of a 1kHz 1V_{rms} output waveform with -37dB total harmonic distortion is shown in Fig. 2.6(a). The distortion may come from the cascoded output stage, the amplifier offset, and the nonlinearity of the speaker and the MEMS sensor. In the same plot, we also show the noise spectrum of the capacitive sensing circuit without the MEMS sensor. The calculated total noise power of the circuit in the audio band (i.e. 20Hz to 20kHz with uniform weighting) is 115 μ V_{rms}. The SNR of our circuit can be as high as 78.8dB. The minimum detectable capacitance variance in the audio band is 28 aF. The capacitance sensitivity is 0.2 aF/ $\sqrt{\text{Hz}}$ and the minimum detectable displacement is $7 \times 10^{-4} \text{ \AA} / \sqrt{\text{Hz}}$.

To get rid of the nonlinearity from the speaker and the MEMS sensor, the sensor is



(a)



(b)

Figure 2.7. (a) Photograph of a chip wire-bonded to an IVUS annular-ring CMUT array. (b) Photograph of a Petri dish placed on top of a DIP40 package. The circuit and the transducers are immersed in a vegetable oil bath during the measurement.

replaced by a 2 pF linear capacitor. A sinusoidal voltage is applied directly to the linear capacitor. When the output signal is 1 V peak-to-peak, -60 dB total harmonic distortion is measured as shown in Fig. 2.6(b). The even order harmonic may be due to the offset of the OTA instead of the nonlinearity of the transconductance. Noise spectrum with power consumptions of $1 \mu\text{W}$, $0.23 \mu\text{W}$, and $0.13 \mu\text{W}$ are also shown in Fig. 2.6(b). The extracted total output thermal noise over the entire bandwidth is about $575 \mu\text{V}_{\text{rms}}$, which is slightly higher than the estimated value of $370 \mu\text{V}_{\text{rms}}$.

2.2.3 Pulse-Echo Experiment and Results

A version of the charge amplifier that uses a $p\text{MOS}$ transistor as the charge adaptation feedback is fabricated. As shown in Fig. 2.7(a), the chip with electronics is wire-bonded to an annular-ring IVUS CMUT array [14]. The size of each element is $70 \mu\text{m} \times 70 \mu\text{m}$, giving rise to a measured capacitance of 2 pF, including the parasitic capacitance. A Petri dish with an opening at the bottom is glued on top of the package by epoxy. During measurement, transducers and the circuit are immersed in a vegetable oil bath, as shown in Fig. 2.7(b).

By applying different bias voltage to the feedback transistor, the same circuit can be configured as a TIA or as a charge amplifier. Because the charge effect due to the capacitance change is equivalent to that due to the voltage change, the frequency response of the circuit can be performed by applying an AC signal at one of the CMUT terminals. The

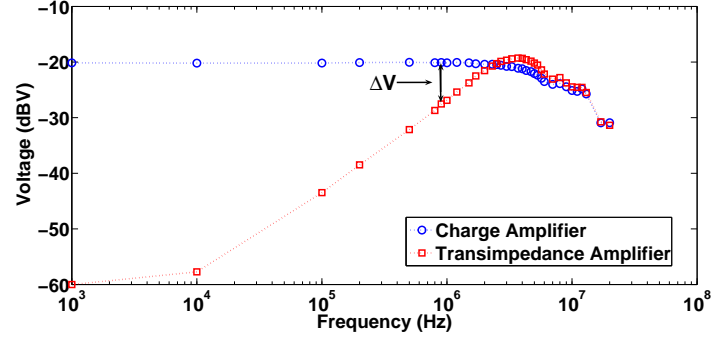


Figure 2.8. Frequency response of a charge amplifier with *pmos* feedback. The input voltage is applied to one of the CMUT terminals. The gate voltage of the transistor can be biased by different voltage to configure the receiver amplifier as a charge amplifier or a TIA. As the operating frequency is below the second pole, the charge amplifier approach can generate larger output magnitude than the TIA approach given the same voltage (or capacitance) variation.

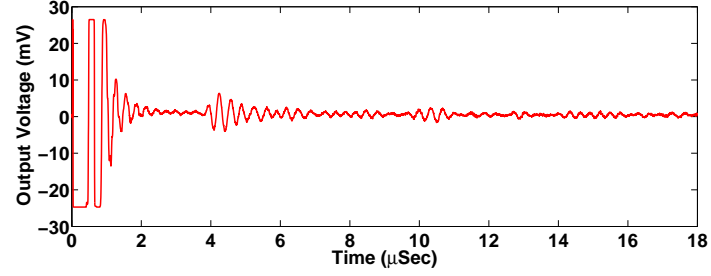


Figure 2.9. Measured pulse-echo response from a charge amplifier. The acoustic source is transmitted from one CMUT device biased by 70V with 20Vpp pulse and the receiver element is bias at 50V. Both devices are immersed in oil. The distance of these two elements is about 3mm. The measured SNR is 16.65dB.

results are shown in Fig. 2.8. As one can see, as long as the operating frequency is less than the second pole, a charge amplifier can obtain a larger output magnitude than the TIA.

The pulse-echo experiment is performed by using one CMUT device as a transmitter and the other element bonded to the circuit as a receiver. The transmitting element is stimulated by a 20V-peak pulse. The receiving device is biased by a 50V DC voltage and the feedback capacitance is extracted as 200 fF. The distance between these two devices is about 6mm corresponding to a pulse-echo distance from a planar target 3mm away. The recorded waveform, shown in Fig. 2.9, indicates a center frequency of 3MHz, which is mainly limited by the amplifier bandwidth. The measured output noise floor is 2.5mV_{rms}

Table 2.1. Performance Comparison

Lit.	[17]	[19]	[20]	[21]	[22]	[23]	This work
Approach	Fig. 2.10(b)	Fig. 2.10(b)	Fig. 2.10(e)	Fig. 2.10(d)	Fig. 2.10(h)	Fig. 2.10(f)	Fig. 2.5
Diff. Cap.	Yes	Yes	No	No	No	No	No
BW (Hz)	2K	100	15K	10K	10K	10K	20K
Noise floor	1.12 aF	3.75 aF	27 dB SPL	$4.8 \mu V_{rms}$	25 dB SPL	$30 \mu V_{rms}$	28 aF
$V_{out,max}$	0.13V	-	0.2V	0.51V	0.5V	0.2V	1V
THD	-60 dB	-	-20 dB	-40 dB	-	-50 dB	-60 dB
SNR (dB)	77	-	93	80	95	54	≥ 78
Power	30 mW	20 mW	$150 \mu W$	$96 \mu W$	$60 \mu W$	$24 \mu W$	$3.3 \mu W$

and the measured SNR from the first received acoustic signal is 16.65dB. The power consumption of the charge amplifier is only $122 \mu W$.

2.2.4 Comparison

One early approach to detecting capacitance change is to use switched-capacitor (SC) circuits containing a charge amplifier, as shown in Fig. 2.10(a). Switches reset the charge on the connecting node. Correlated double sampling (CDS)[15] techniques are also commonly used[16] to reduce low-frequency noise and DC offset. Issues like noise-folding, clock feed-through, and charge sharing need to be taken care of. For applications which require very high sensitivity, lock-in capacitive sensing is one of the most popular techniques[17–19], as shown in Fig. 2.10(b). Because of the modulation scheme, the circuit consumes lots of power, usually in the milli-watt range, and is very complicated. In either SC or lock-in approaches, circuits process the entire charge on the sensing capacitor, instead of only the portion caused by the minute capacitance change. To cancel the effect of large static capacitance, differential capacitor structures are used; otherwise the output dynamic range will be very limited.

For capacitive microphone MEMS sensors, where the differential capacitor structures are not available, traditional approaches usually convert the capacitive current, instead of

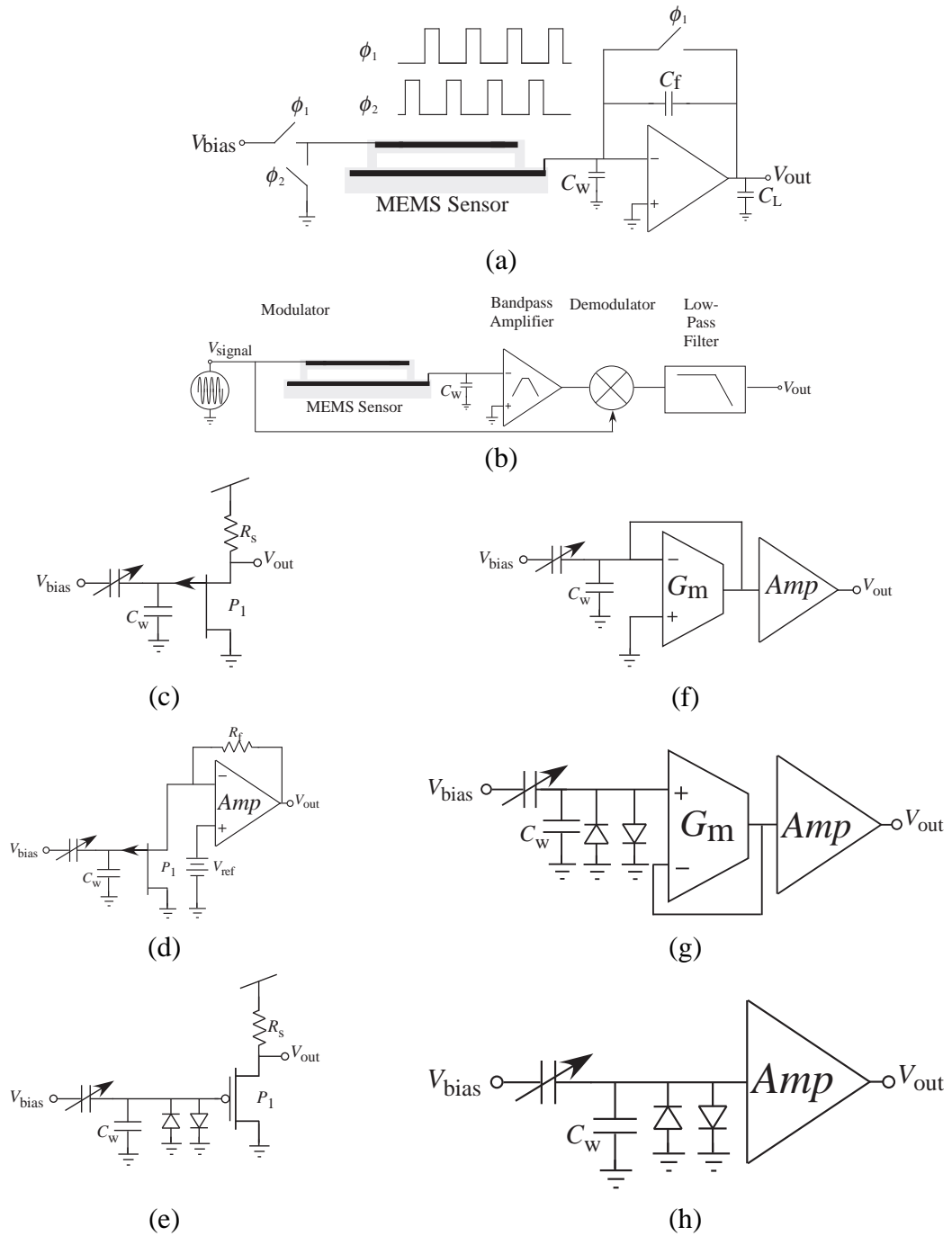


Figure 2.10. Previous approaches to capacitive sensing: (a) Switched-capacitor approach. (b) Lock-in approach. (c) A self-biased JFET source follower as a microphone interface circuit. (d) The current through JFET is sensed and amplified to improve PSRR. (e) to (h) Diodes or linearized OTA are used as a large resistor and the voltage is directly amplified or buffered and then amplified.

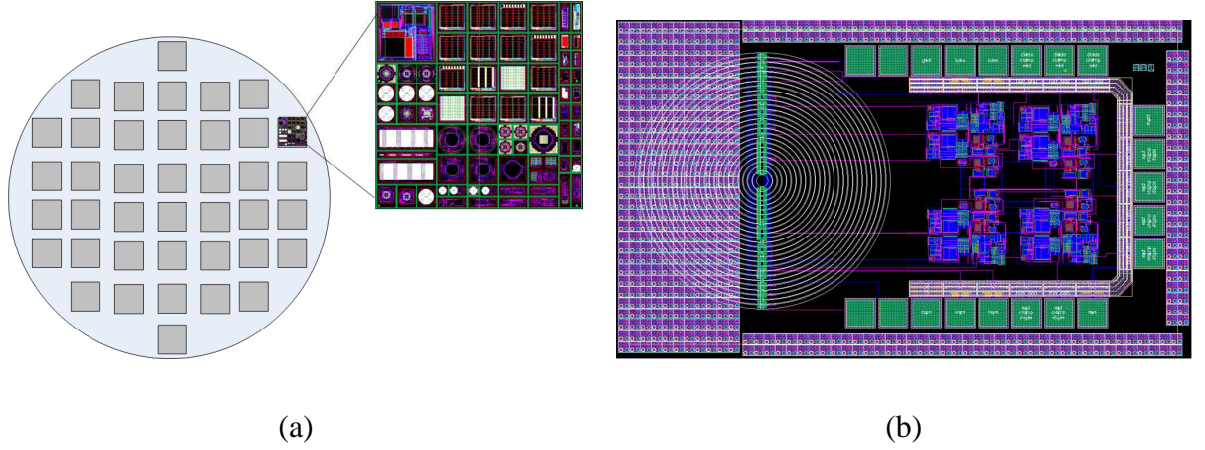


Figure 2.11. (a)Reticle on TSMC 0.35um wafer. (b)Layout of annular array CMUT interface electronics.

the charge, into voltage which will be amplified in the following stages. Because of its high input impedance, a self-biased JFET source follower, as shown in Fig. 2.10(c), is the most commonly used interface circuit for electret condenser microphones (ECMs). However, JFET is not compatible to CMOS process and the source follower has poor power supply rejection ratio (PSRR). In [21], the current through the JFET is sensed and amplified to improve the PSRR as shown in Fig. 2.10(d). Another approach uses diodes[20, 22] or a unity-gain feedback OTA[23] as a large resistor to convert current to voltage. The resulting voltages can be amplified directly or can be buffered and amplified by the next stage, as shown in Fig. 2.10. These approaches usually have much less power consumption compared with SC and lock-in techniques. However, the linearity is usually poor. In this work, we can achieve ultra-low power consumption and very large output dynamic range with high linearity. The comparison results are shown in Table 2.1.

2.3 CMOS-FIRST MEMS Integration for CMUTs

Advancements in the processing and integration of MEMS with CMOS open doors to highly integrated sensors with front-end processing. Figure 2.11(a) shows the reticle submitted to TSMC 0.35 μm fab. Figure ??(b) shows an example of a layout for an annular

array CMUT. The two-chip hybrid approach used until now adds the unwanted parasitics. CMOS-FIRST MEMS integration for CMUTs provides a good solution with reduced parasitics and a one-chip solution. Electronics for three different types of CMUTs with different bandwidths and geometries are being fabricated on the CMOS wafer (listed in Appendix A). Each chip has digital controls for the selection of different CMUT elements. The core amplifiers are a high input swing folded-cascode topology with a high-speed output buffer. These designs will provide experimental verification of a high-sensitivity CMUT interface along with a good comparison of the traditional transimpedance amplifier approach vs charge amplifier with capacitive feedback and pseudo-MOS floating-node stabilization.

To meet the demands of medical ultrasound imaging using high density arrays with CMUT technology, specialized integrated circuits should be custom designed. Because the parasitic interconnect capacitance is a significant factor degrading the SNR, monolithic integration emerges as a viable option. Silicon-based CMUTs enable different array structures and are especially suitable for various levels of electronics integration. Integrated electronics reduces cable count, mitigates parasitic effects and lowers overall cost, and hence is a key factor for successful implementation of catheter-based imaging arrays.

Single-chip or hybrid electronics integration is required for arrays with small element size. Hybrid integration of CMUT array and CMOS electronics through flip-chip bonding is demonstrated in [Wygant (2005)].1]. Single-chip integration of CMOS and CMUT devices includes interleaved CMOS-MEMS integration, where CMUTs are fabricated as an intermediate step in CMOS process flow [Eccardt (1996), Chen (2008)3], and CMOS before MEMS approaches, where CMUTs are fabricated on CMOS electronics [4, 5].

Here we present CMOS design aspects for CMUT-on-CMOS integration. We designed and fabricated 8" wafer using the TSMC 0.35um two-polysilicon four-metal CMOS process. Each wafer contains many chips of size 2 cm 2cm (reticle) containing many smaller IC cells (Fig. 1). We optimized integrated cells with significant design effort to meet the

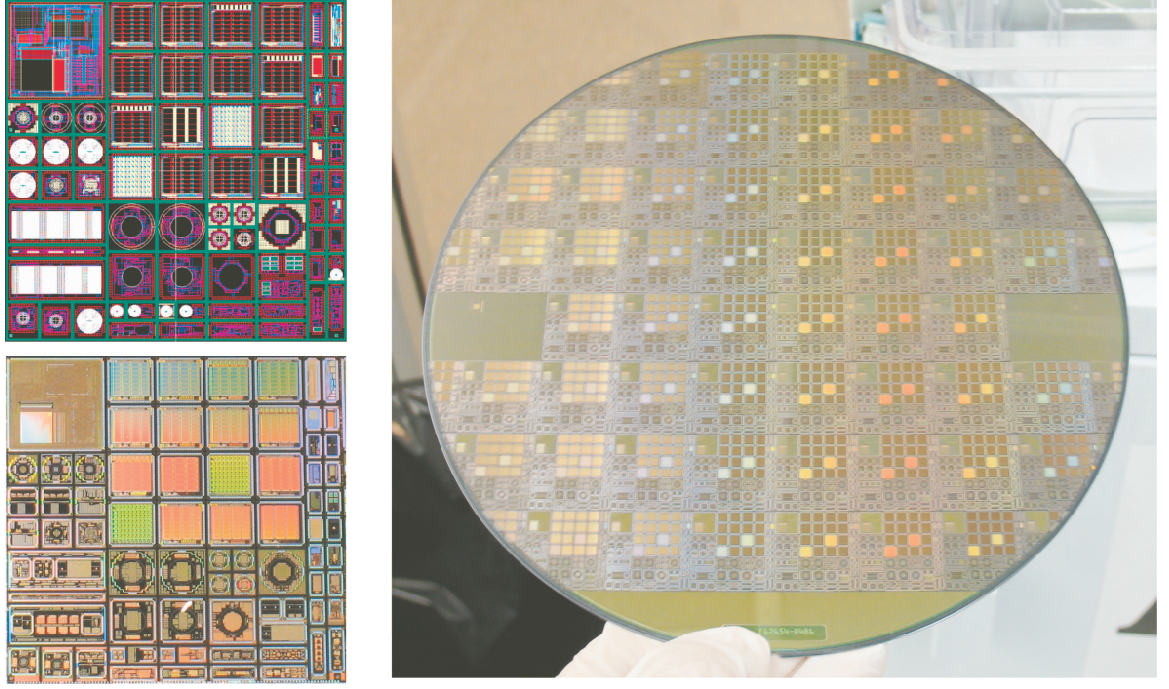


Figure 2.12. Reticle layout and microphotograph (left) and TSMC 0.35um 8'' wafer (right).

Table 2.2. Typical CMUT Parameters for CMUT on CMOS approach

CMUT PARAMETERS			
	Dual Ring Array	Annular Array	Linear ICE Array
# of Elements	32Rx–24Tx 64Rx–48Tx	8Rx 16Rx	64Rx
Operation Freq	15–25 MHz	10–50 MHz	3–13 MHz
Element Area	70 $\mu\text{m} \times 70 \mu\text{m}$	100000 μm^2	172000 μm^2
R_{CMUT}	1 M Ω	53 k Ω	31.25 k Ω
C_{CMUT}	145 fF	3 pF	5.1 pF

specifications for three different arrays designed for IVUS and ICE applications. The number of receive and transmit elements, operation bandwidth and calculated device capacitances of CMUT arrays used in these applications are presented in Table 1. In this paper we focus our discussion to one particular integrated cell to explain the design process.

Our previous dual-ring imaging study [6] included a 32 RX - 24 TX element CMUT array and 4 IC chips surrounding the array, along with a glass layer to help routing. CMUT

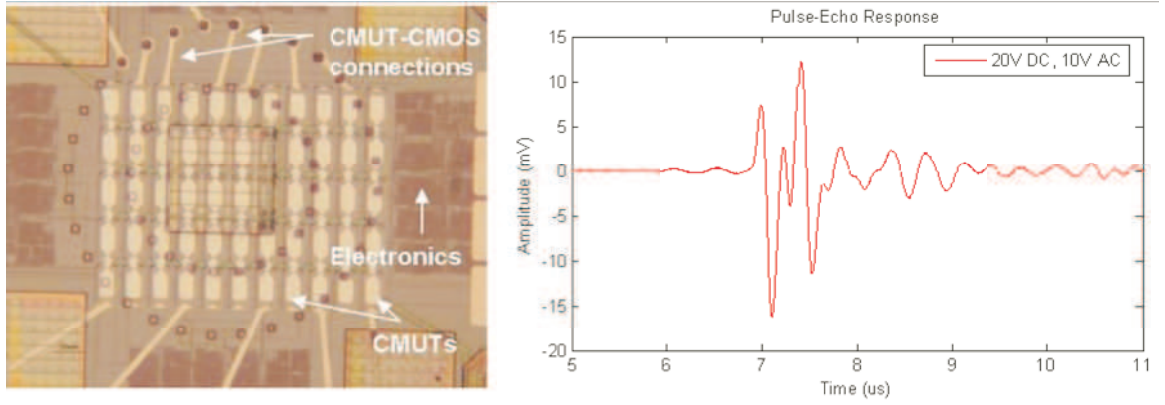


Figure 2.13. CMUT built on CMOS wafer (left) and the received pulse echo data (right).

arrays and IC chips were placed on glass interface chip which was then placed on a 64 pin chip carrier for testing. Such configuration requires more than 100 wirebonds for connections which is quite prone to errors. Hence, CMUT-on-CMOS approach is a remedy for that as it eliminates all those wirebonds. We designed and fabricated an IC chip for monolithic implementation of forward-looking IVUS imaging employing a dual-ring array. A micrograph of this IC is shown in Fig. 2.13. The chip has a die-size of 2 mm \times 2 mm. It includes all the components of the imaging device, such as transmitters, receivers and control logic. It was optimized to interface a dual-ring array with 32 receive and 24 transmit elements. The chip includes 4 sets of pulser arrays, each containing 6 pulsers. Those pulser arrays are connected to 24 CMUT Tx element connections. There are 4 sets of receiver arrays. Each receiver array includes 8 transimpedance amplifiers, one 8:1 multiplexer and a buffer to drive cable and pad capacitances. Chip has total of 4 parallel outputs having one from each set of receiver arrays. Digital control block is designed to synchronize transmit and receive element operations in the dual-ring array. It includes an 8 bit counter that generates control bits for pulser and receiver arrays.

2.3.1 Pulse Echo Results

For initial testing, we performed pulse-echo measurements with a CMUT array on an IC consisting of transimpedance amplifiers, multiplexers and buffers to drive 50 and 12 pico

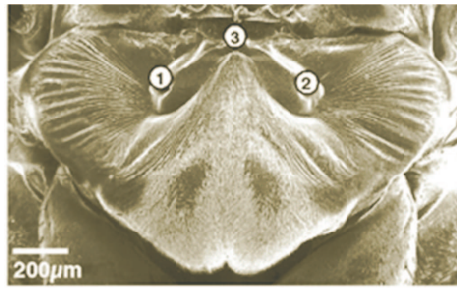
farad cables. The CMUT test array consists of 5 RX and 6 TX elements fabricated on top of this particular cell Fig. 2.13. The electronics shows no degradation after CMUT fabrication. With transimpedance gain of 500 kohm and 3-MHz bandwidth, an echo signal of 28-dB SNR is obtained without any averaging, applying 20-V bias and an external 10-Vpp pulse in a 5-mm deep oil bath. Although used CMUT device is designed for higher frequency operation this test is limited by the low TIA bandwidth that stems from an issue with the fabricated on-chip resistors. We resolved this resistor problem in the new set of wafers and expect to demonstrate higher bandwidth operation.

CHAPTER 3

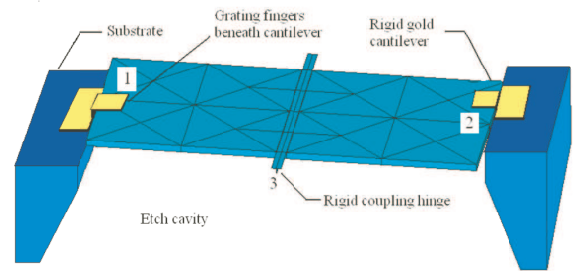
ANALOG FRONT-END FOR BIOMIMETIC MICROPHONE

The biomimetic microphone is inspired by the directional acoustic sensing capabilities of a small fly called *Ormia ochracea* [24]. This fly has an ability to locate the mating singing of crickets in order to lay its eggs on these hosts. When the distance between the ears (1mm apart) of this fly is taken into consideration, the ability of locating sound within 2 degree accuracy is quite challenging. That shows that this fly is able to detect very small pressure differences between the two inlet ports of its ear. The intertympanal membrane of this fly is pivoted from the center by a hinge that couples the two side of the membrane. This ear structure and the design of a diaphragm model that is inspired by this structure can be seen from Fig. 3.1. The coupling effect of the two side of the diaphragm allows this fly to locate the sound without any other information [25].

Fabricated biomimetic gradient microphone chip can be seen in Fig. 3.2. One chip contains two gradient and one omnidirectional microphone diaphragms whose measured directivity patterns are also plotted in Fig. 3.2. The chip is fabricated using silicon micro-machining technology. The differential diaphragm of this microphone structure is made of polysilicon and 1mmx2mm in dimensions. The diaphragm is hinged at the center which allows this structure to do 'teeter-totter' type motion. The gratings and reflective gold



(a)



(b)

Figure 3.1. (a)Ormia ochracea's ear. (b)Design of biomimetic gradient microphone.

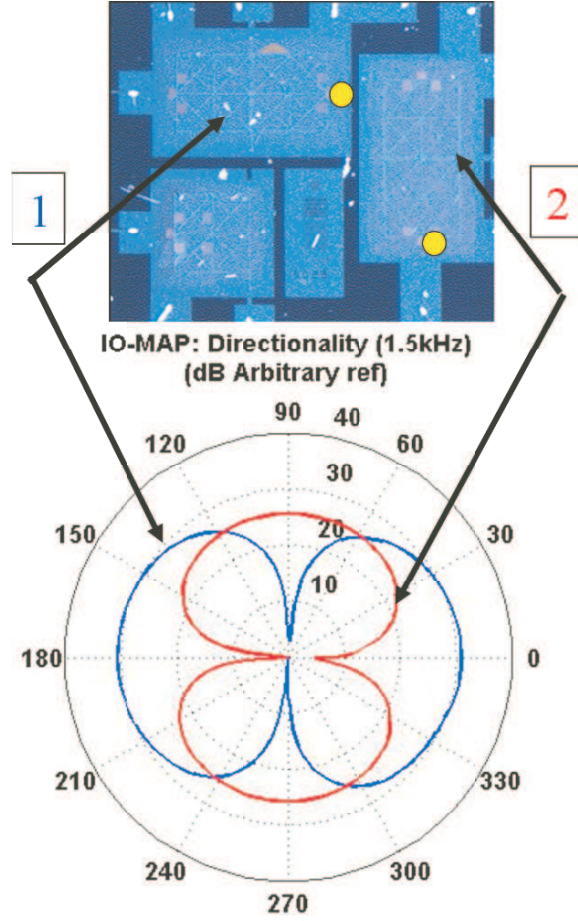


Figure 3.2. Fabricated chip with directionality plots.

backplates are located on each side of the membrane which allows us to use diffraction based optical detection method with these microphone structures [26].

3.1 Diffraction Based Optical Detection Method

The basic operating principle of the diffraction based optical displacement detection scheme is shown in Fig. 3.3(a). In this configuration, the top electrode is the microphone diaphragm which serves as a backplate and the bottom electrode is the diffraction grating fabricated on the silicon substrate. Both these electrodes are electrically conductive and optically reflective. The silicon substrate is etched from the backside so that there is an optical path to reach the reflective diffraction grating. In this configuration the diffraction grating is fixed to the substrate and the microphone diaphragm is moving with the incoming sound wave.

However, moving grating with fixed reflective backplate is also an acceptable design. The overall system forms a phase sensitive diffraction grating [27]. A coherent light source illuminates on the back side of the microphone diaphragm through the diffraction fingers. Some of the light is reflected from the diffraction gratings and some reflected from the microphone diaphragm. The reflected light beam returns as a zero order and the diffracted beam causes higher orders. These orders whose intensities are modulated by the movement of the diaphragm by the sound pressure are captured by photodetectors. Using scalar diffraction theory, the beam intensity of the zero and first diffraction orders can be calculated. These first and zero order intensities vs. the gap height can be seen from Fig. 3.3(b) for 650nm optical wavelength. It is clear from this figure that when the gap thickness is a multiple of $\lambda/2$, the zero order intensity is a maximum and the diffraction grating acts as a mirror. When the gap thickness is an odd multiple of $\lambda/4$, the first order intensity becomes a maximum. To get the highest sensitivity of the diffracted orders, the gap height should be an odd multiple of $\lambda/8$ where the slope of the intensity curve is a maximum. At this maximum sensitivity point, which is the inflection point, this curve is linear. Any factor that causes the shift of the operating point from the maximum sensitivity point results in nonlinearity

There are many different advantages of this optical detection method when it is integrated with a microphone. In this method, sensitivity does not depend on acoustic frequency, the device capacitance or the device size. Because of the fact that the same sensitivity can be achieved with large membrane and grating distance, the gap can be fabricated large enough to reduce the squeeze film damping effect of the air in the gap. Also, different and novel backplate designs are possible to implement since the capacitance of the device is not too critical. The laser intensity noise can be reduced by using the differential detection (first and zero order). With the differential detection, shot noise limits can be achieved ideally [28]. Integration can be made easier with the fabrication of photodetectors with the integrated amplifiers on a silicon wafer that can be integrated with the microphone

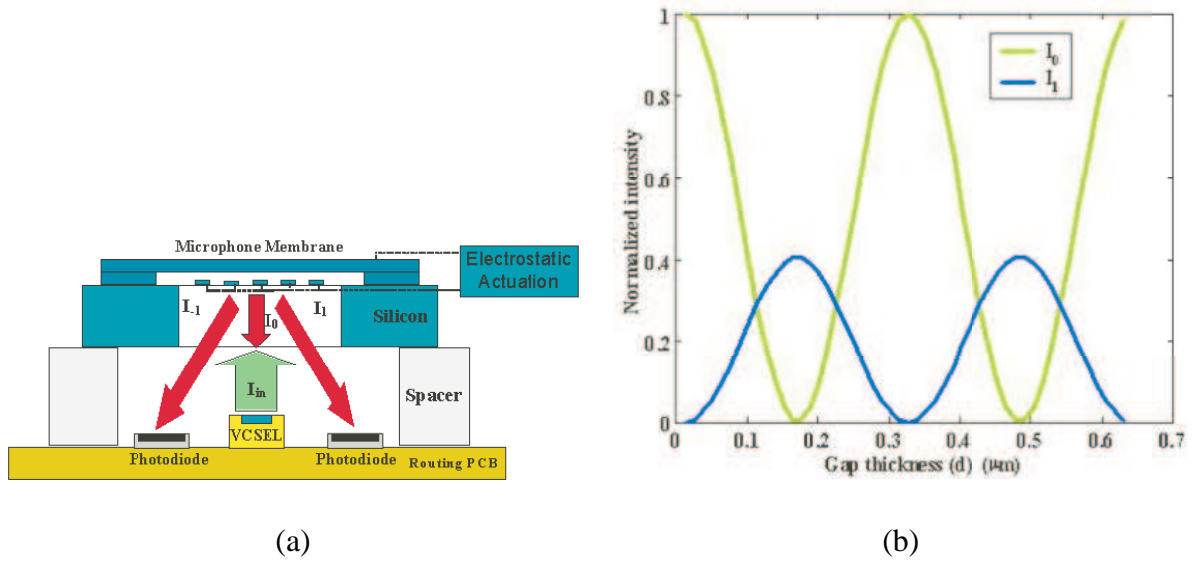


Figure 3.3. (a)Operating principle of the diffraction based optical displacement detection scheme. (b)First and zero order intensities vs. gap thickness curve.

structure. This method also makes the array applications more feasible. The last important advantage of this method is that the electrical port of the microphone is left open. With this port, electrostatic actuation is possible which can be used for tuning the membrane position to get highest sensitivity, tuning the dynamic response of the microphone and applying the force feedback operation to alter the device dynamics in a desired manner.

3.2 Integration of Optical Displacement Detection and Challenges

The highly sensitive optical displacement detection methods implemented in a small volume and with reduced power consumption have the potential to compete with commonly used capacitance-based methods in micromechanical sensor systems. The traditional capacitive acoustic sensors do not scale down favorably. In other words, reducing the membrane size decreases the ratio of the active capacitance to the parasitic capacitance, thereby requiring a gain in mechanical compliance, which in turn necessitates the use of very thin, low-stress membranes, that are difficult to reproduce in a repeatable manner. Reducing the membrane gap to increase the active capacitance can increase the stiffness of the trapped air and reduce the electrical sensitivity by limiting the sustainable electric field. To address

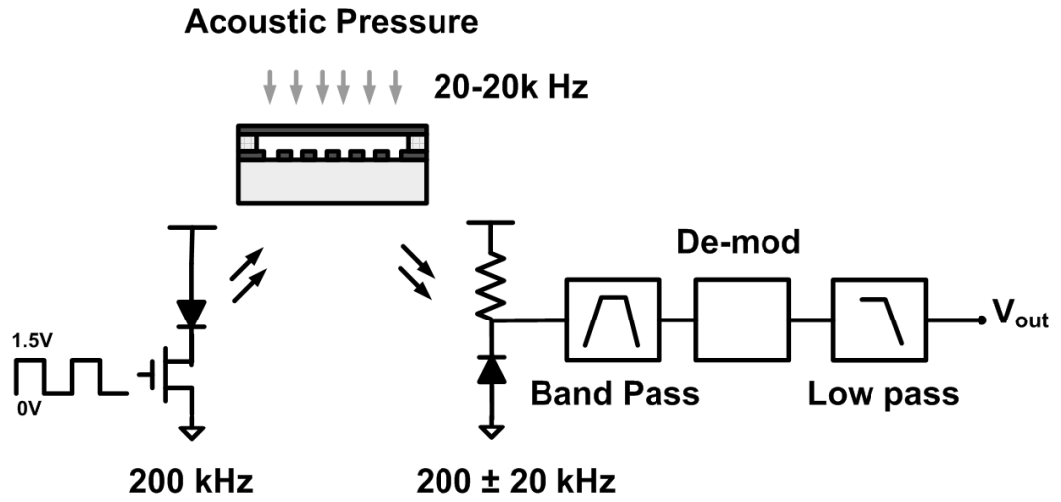


Figure 3.4. System level block diagram for the Optical MEMS hearing aid.

these problems, optical techniques are used with diffraction gratings as a method to measure displacement from acoustic pressure in microphones. This hybrid integrated system can be implemented in acoustic-sensor applications using both continuous wave and pulse VCSEL to show reduced power consumption.

Optical methods have advantages in small displacement sensing applications primarily because the sensitivity is independent of device capacitance. Optical fiber based sensors have been commonly used for optical detection, but integration of optical fibers with micro-machined structures in small volume is quite challenging, and these sensing methods are susceptible to external mechanical noise sources. Recently, diffraction based methods have emerged for compact integration of optical interferometric methods with micromachined structures. Furthermore, VCSELs enables further integration possibilities due to various favorable properties, such as the small chip dimension, out of plane light emission, and low power consumption [2].

3.3 Optical MEMS Microphone Receiver Architecture

Fig. 3.4 shows the receiver system level electronics interface for the Optical MEMS hearing aid sensor. A VCSEL is used to generate the incident optical pulse on to the MEMS sensor. The duty cycle of the VCSEL is minimized to keep the power down on the transmit end.

A simple CMOS switch is used to pulse VCSEL current, which turns the VCSEL on and off with 200kHz input carrier pulse. This incident pulse is modulated with the acoustic pressure in the audio band.

On the receive end of the modulated light, a photodiode is used along with a passive on-chip resistor to do front-end detection. The signal is first cleaned with a bandpass filter centered at 200kHz to remove low frequency content along with undesirable $1/f$ noise. Then the signal is feed into a demodulator to extract our signal of interest in the 20kHz audio band. Finally, the signal is further cleaned with a low pass filter at 20KHz to remove ripples and high frequency contents.

3.4 VCSEL Driver in Standard CMOS

Power consumption is one of the major design constraints for the microphone. The electronics are designed in weak inversion to consume minimum currents with audio frequency bandwidth requirements. The whole receive chain for the continuous time case, can operate for less than 50uA of current from 1.5V battery supply. This leaves us with the power drain at the transmitter side. VCSEL is the most power hungry block in the whole system. One of the main push to use pulsed approach is to cut down average current levels in VCSEL. The reduction in the duty cycle of the pulse can even reduce the average easily less than 1mA.

Typically, VCSELs operate at few milli-amperes of threshold current. This current is required for lasing. Typically, there are two approaches that we can take for biasing the VCSEL. First is threshold-biased VCSEL, and the second is zero-biased VCSEL. The first case is the common approach to achieve above Gbps data rates with out introducing VCSEL turn-on delay. The second approach is viable for us as we are operating at much lower speed where VCSEL turn-on delay is not an issue.

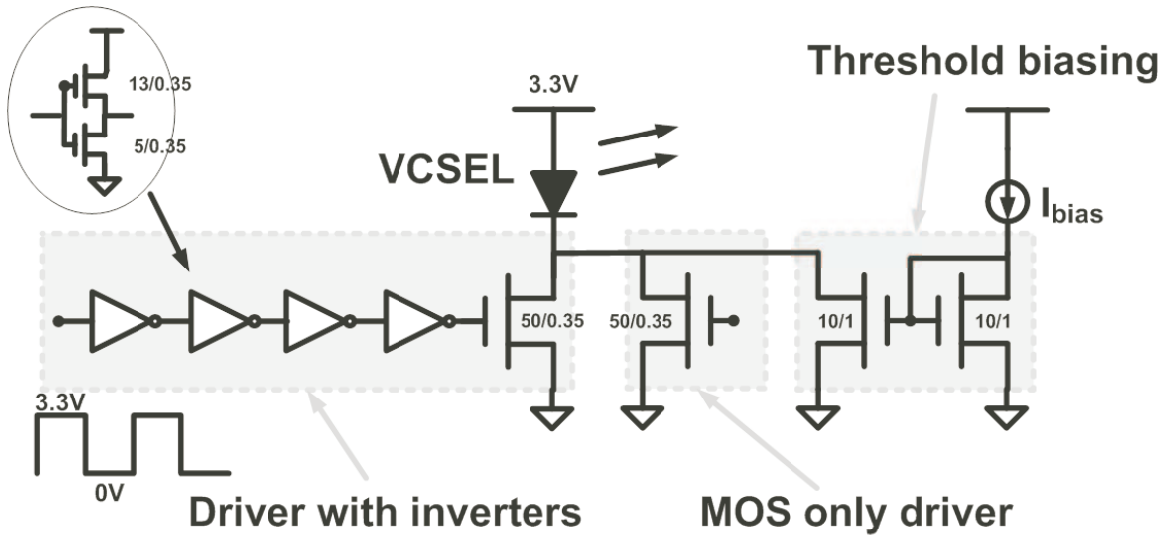


Figure 3.5. VCSEL driver schematic.

3.4.1 VCSEL Driver Design

As we are limited with the current consumption, we do not have the budget for bias current through the VCSEL. We use a simple MOS switch to turn the VCSEL on and off. This enable zero-biased VCSEL operation. This is shown in Fig. 3.5. The MOS transistor is operated as a switch and it simply pulls the n-terminal of the VCSEL to ground when it is on. The MOS is designed to have a minimum resistance when turned on. This gives us minimum drop across the MOS and provides VDD across the VCSEL for its operation.

Figure 3.6 shows the chip micrograph and the driver layout. This design has the option for both zero-biased and threshold bias operation. Two different approaches for driver switch have been integrated as well. First is the simple MOS switch. The second is a switch with inverters to be able to drive big capacitive load of the main high driver transistors. The main MOS switches are designed for high transconductance and speed. They are able to easily drive milliamperes of current. The biasing transistors are relatively smaller in dimension to minimize capacitive loading. The whole driver takes 37um x 25um of area. The usual size of the design chips with complete transceiver is in the range of 3000um x 1500um.

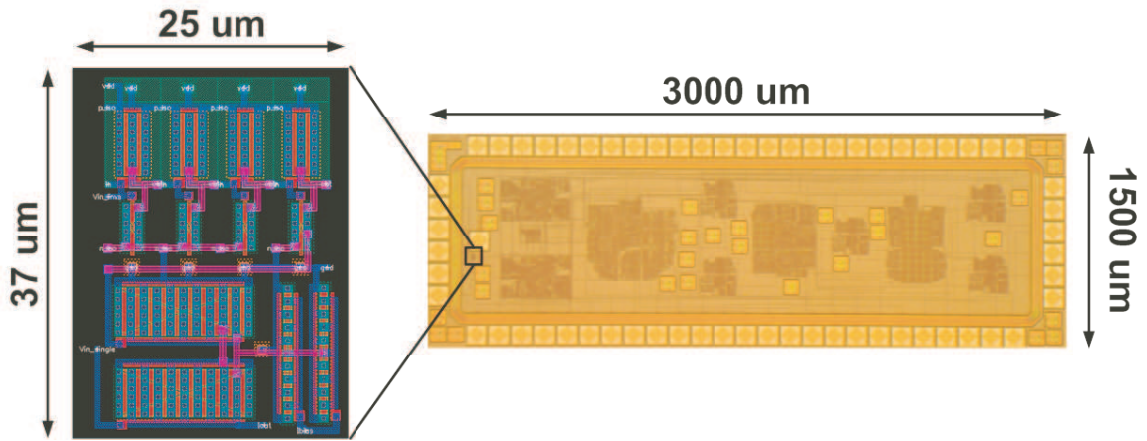


Figure 3.6. VCSEL driver layout.

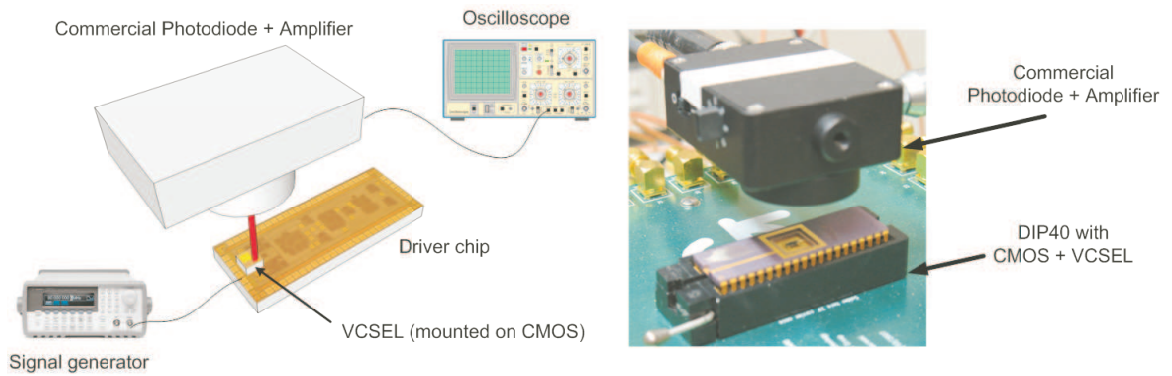


Figure 3.7. VCSEL driver measurement setup.

3.4.2 VCSEL Driver Measurements

Figure 3.7 shows the setup used to measure VCSEL driver. The VCSEL is mounted with conductive epoxy onto the CMOS driver chip. Signal generator is used to generate pulses for the driver. A commercial photodiode amplifier is used to sense the laser with an oscilloscope.

Table 3.1 shows the detailed specification of the VCSEL and the commercial photodiode amplifier used. One important thing to note here is the threshold voltage and current levels. The divergence angle for the current model of VCSEL is low for the overall optical grating microphone design. We can also try a VCSEL with higher divergence angle like ULM 850nm with 1.5V threshold voltage and 0.8mA current. This can provide more power saving for the transmitter and hence hearing aid.

Table 3.1. Specifications for Lasermate VCSEL (VCC-85A1G-IS)

Min. optical power [mW]	2
Forward voltage [V]	3
Threshold current [mA]	3
Wavelength [nm]	850
Divergence [degrees]	8
Size [μm^2]	270×270

Table 3.2. Specifications for Photodiode Amplifier (Thorlab PDA36A)

Detector type	Si PIN
PIN Responsivity @ 850nm [A/W]	0.5
Gain [dB]	0-70
Bandwidth [MHz]	0.0125 - 17

Table 3.3. VCSEL current consumption with varying duty cycle

50%	3.5mA
40%	2.8mA
30%	2.1mA
20%	1.4mA

Table 3.2 shows the specifications of the commercial photodiode amplifier used for measurements. Note that the bandwidth is maximum for the amplifier with minimal gain settings. Also, along with the optical light loss due to the setup, there is also about 50 percent loss from the photodiode from its responsivity at 850 nm wavelength.

3.4.3 Experimental Data and Discussion

We record pulse data for each type of driver for 200 kHz and 2 MHz. Also, each driver is pulsed with threshold bias and zero bias conditions. Reducing the duty cycle also reduces the average current burnt by the VCSEL. The current measurements for various duty cycles are shown in table 3.3.

The pulses in time domain are shown in figure 3.8 to 3.11. The rise time for all the cases is 20ns, which corresponds to 17MHz bandwidth. Now note that the commercial amplifier we are using has a bandwidth of 17MHz. So we are limited in our measurement for the VCSEL driver speed from our detector. But still we meet our requirement of going upto 2MHz pulse rate for sigma-delta approach. Another thing to note is the difference between zero biased and threshold biased measurements. You will note that the only difference is levels of currents. There is no delay introduced for our measurement speeds of 2MHz. Also for the case of threshold biased pulse, we inject current into the VCSEL using the current mirror; as the size of the bias transistor is small, it has large drain to source voltage to operate. Putting this in parallel with the driver switch does not enable the switch to completely turn on. This is evident from the reduced high level current pulse. We observed a delay of 40ns in all the cases of VCSEL pulse. It is likely coming from the commercial amplifier. The amplifier also has ringing issues as we put a pulse with 5ns rise time using the signal generator. In the case of 200kHz pulse, the amplifier is able to settle after ringing; but for 2MHz, the amplifier at duty cycle of 10 percent and lower, does not reach its final high state values.

3.5 CMOS PN Junction Photodiode

The photodetector is an essential element in any practical optical communication system. It converts the incoming optical power into a modulated electrical current that is subsequently amplified and further processed. A good detector has to meet various criteria, of which a good efficiency at the operating optical wavelength and high speed are the most important for telecom applications. The basic detection process in semiconductor photodiodes involves the photogeneration of electron-hole pairs in a region of high electric field strength.

Inherent limitations of photodiode response are due to structure and specific junction

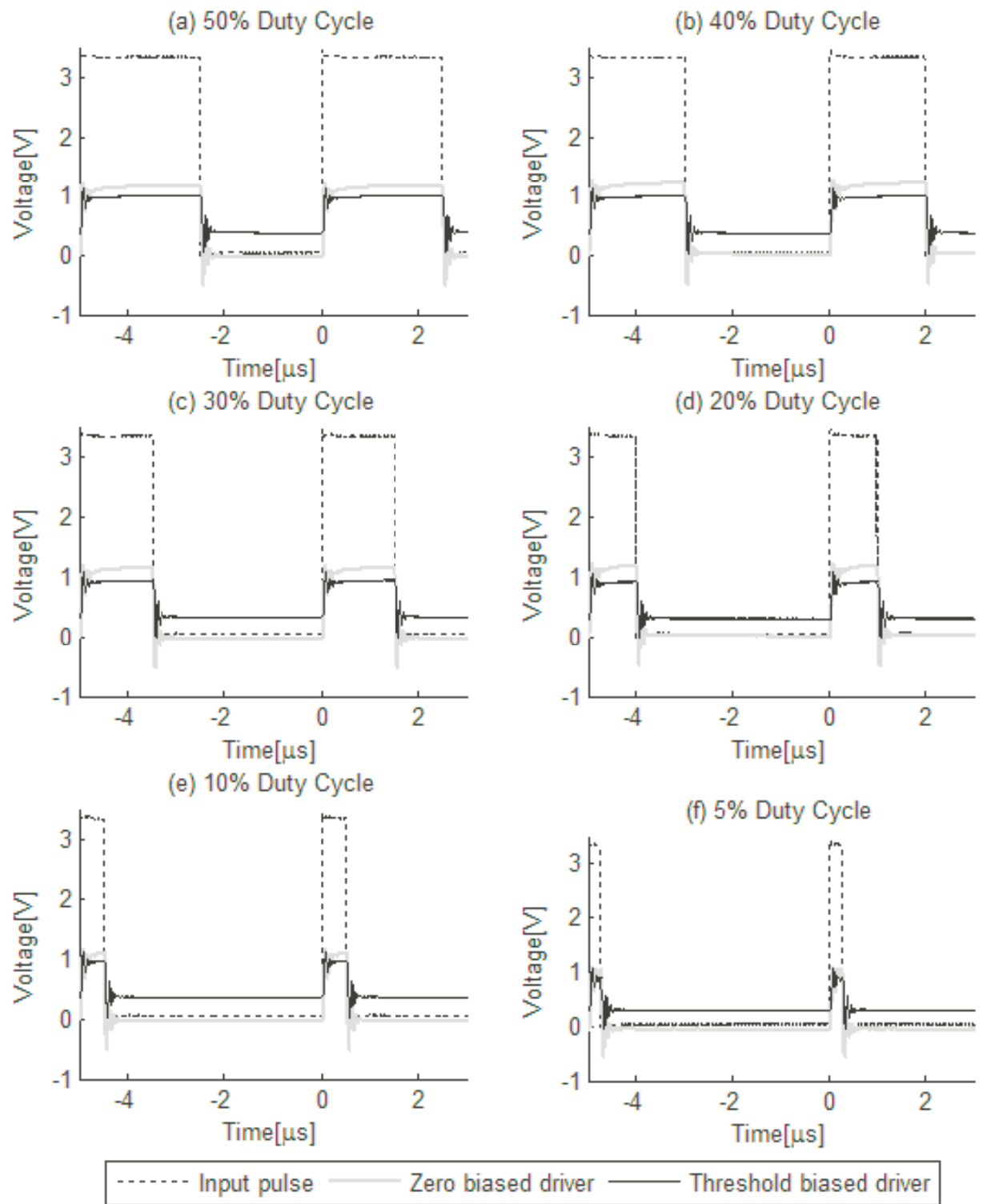


Figure 3.8. Output pulses with MOSFET only VCSEL driver at 200kHz.

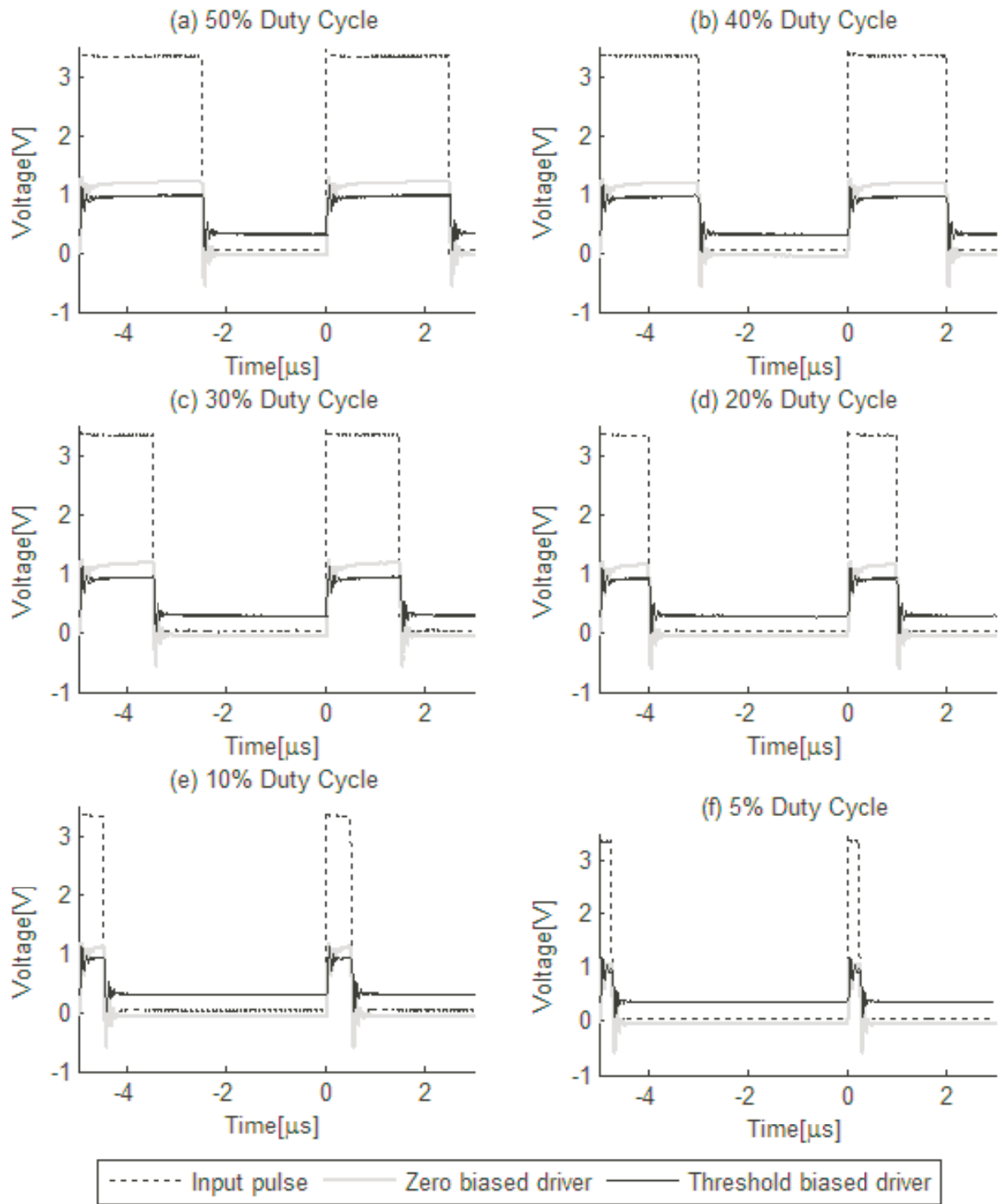


Figure 3.9. Output pulses with inverter VCSEL driver at 200kHz.

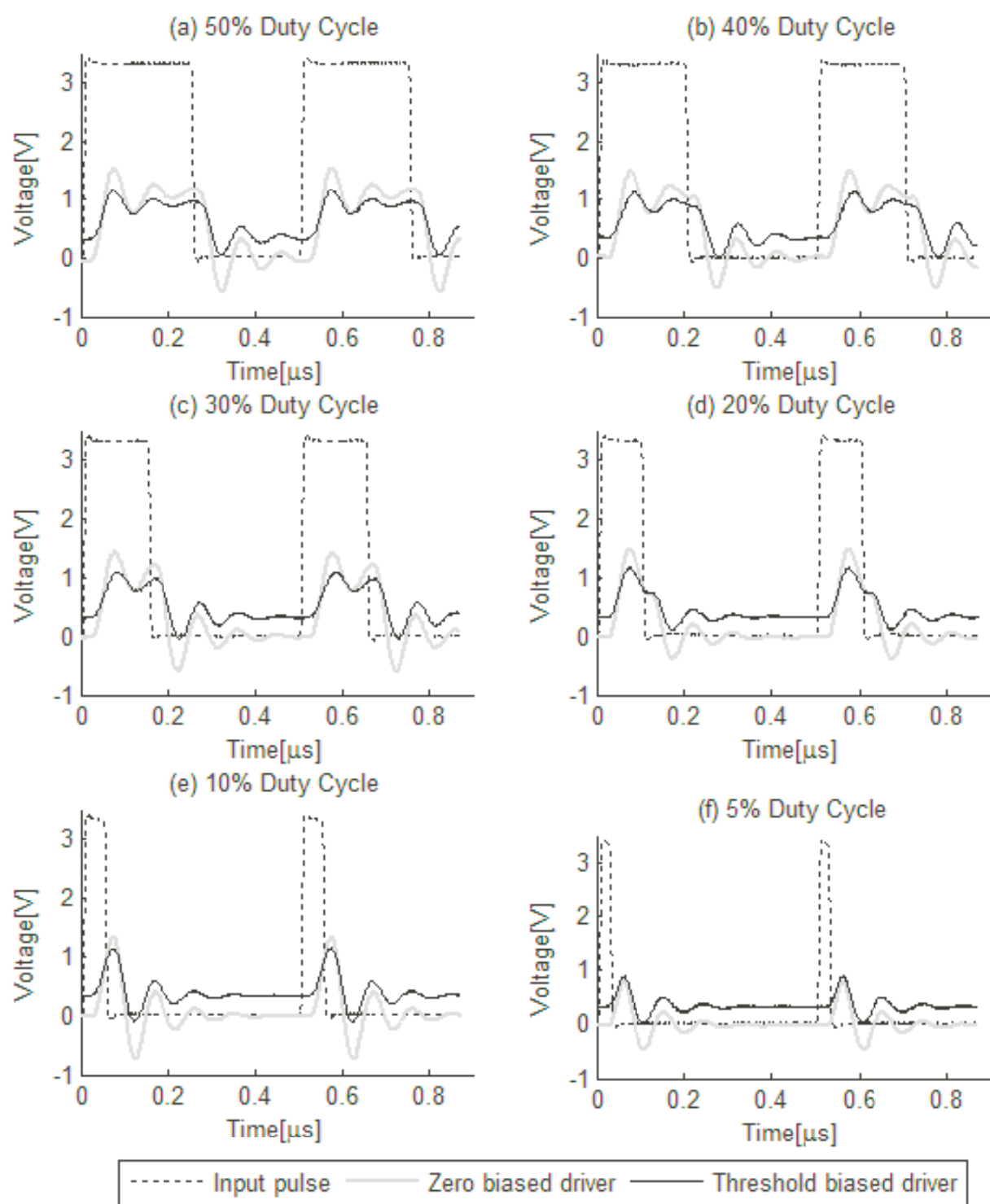


Figure 3.10. Output pulses with MOSFET only VCSEL driver at 2MHz.

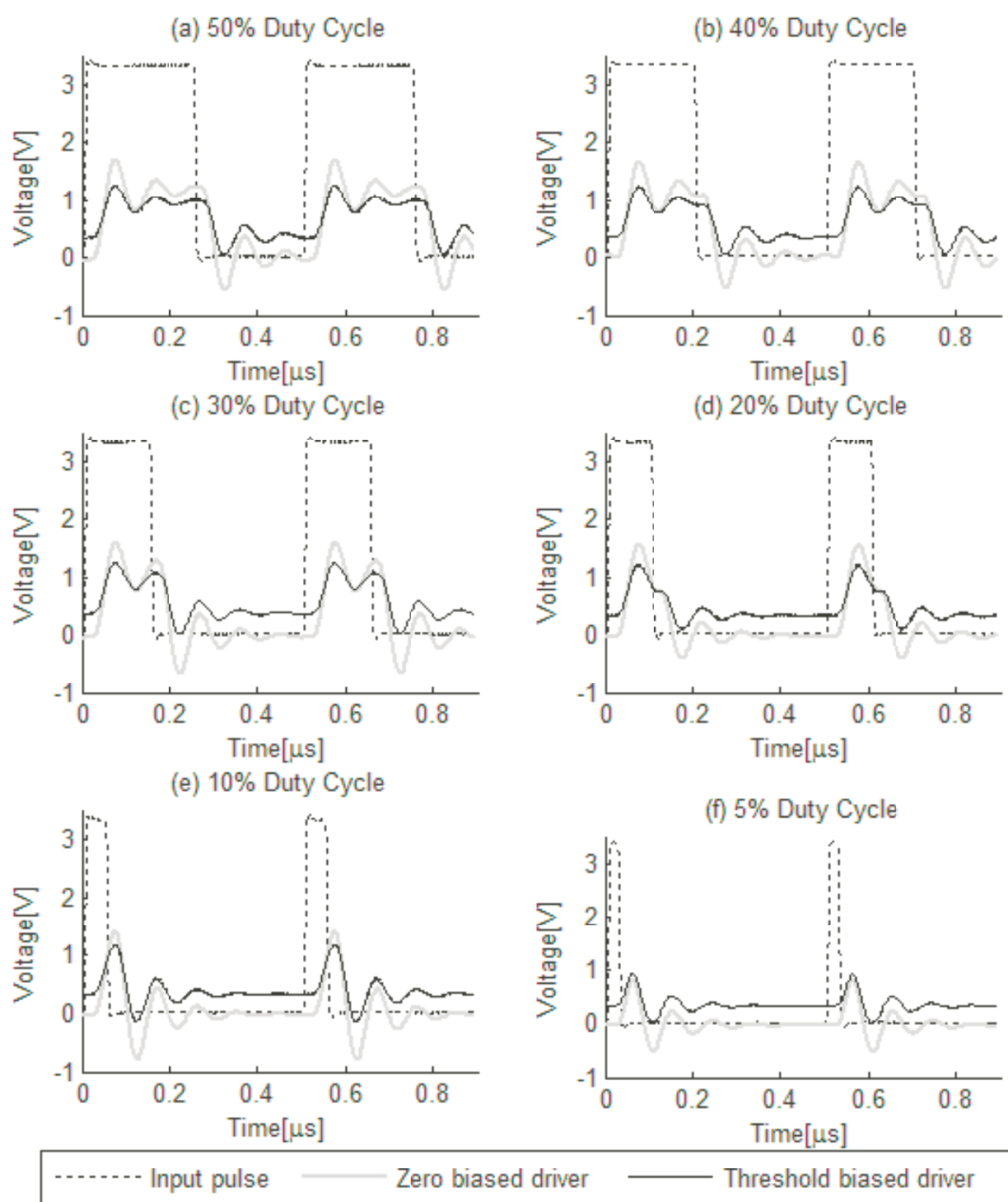


Figure 3.11. Output pulses with inverter VCSEL driver at 2MHz.

Table 3.4. Photodiode Parameters and Measurement Results

PHOTODIODE PARAMETERS			
	N-Psub	Nwell-P	Nwell-Psub
Cross-talk [nA]	32.13	0.65	0.69
Dark Current [pA]	17.21	28.35	22.08
Responsitivity [A/W]	0.3782	0.3783	0.3906
Capacitance @ -2.5V [pF]	28	17	5

design, the presence of an externally applied bias, and the wavelength of incoming radiation. The inherent time constant of a photodiode causes a delay in generated photo current. For silicon photodiodes, this time constant is typically 7 to 15 ns. The P-N junction of a photodiode does not present an infinite resistance to reverse current flow. Consequently, when a reverse bias is applied to a photodiode, a small current flows even in the absence of incident light, as seen in the I-V curve Fig. 3.14. This dark current increases slowly with increasing reverse bias. A large dark current is undesirable since it may represent a significant background above which the actual photocurrent is measured. Furthermore, shot noise associated with the dark current may be significant.

The responsitivity data is shown in Table 3.4. It is clear that Nwell-Psub photodiode gives the best result in terms of responsitivity and frequency response. The dark current is in the range of 20 to 30 pA. This is very reasonable as compared to the big size of these photodiodes (180um x 180um). Cross talk of leakage currents was also characterized for these chips. It varies from 0.6 to 30nA. This can be further improved by isolating the pad frame from photodiodes. This will ground any leakage currents that can leak into the pad frame.

In Psub-N+ CMOS diode, the anode is the p-substrate and the cathode is the n+ diffusion. The junction depth of the n+ diffusion is approximately 0.25um in 0.50um process. The n+ diffusion has a much larger doping concentration than the p-substrate and it is well

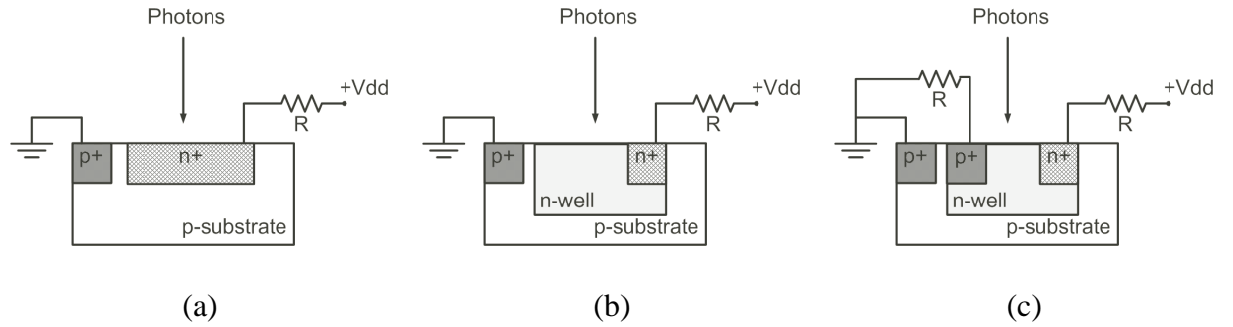


Figure 3.12. (a)Psub-N+ Photodiode. (b)Psub-Nwell Photodiode. (c)Nwell-P+ Photodiode.

known that most of the depletion width will extend into the p-substrate. The p- substrate contact is located within a diffusion length of the n+diffusion contact. For Psub-Nwell photodiode, the anode is also the p-substrate but the cathode is now the nwell. The nwell junction depth is approximately 4.0um. The nwell has a slightly larger doping concentration than the p-substrate, therefore, more of the depletion width will extend into the p-substrate. The p-substrate contact is located within a diffusion length of the nwell contact. The third type of photodiode is Nwell-P+ which allows for substrate isolated optical detectors. The photodiode's anode is the p+ diffusion and the cathode is the nwell. The junction depth of the p+ diffusion is approximately 0.25um. The nwell depth is on the order of 4.0um. The p+ diffusion has a much larger doping concentration than the nwell; therefore, most of the depletion width will extend into the nwell. The nwell contact is located within a diffusion length of the p+ diffusion contact.

A photodiode's first order electrical equivalent is a current source in parallel with its junction capacitance Fig. 3.13. We can model this by its Thevenin equivalent. The current source is replaced by a low impedance signal source in series with a large resistance. This is then loaded with a capacitor representing the diode's junction capacitance. The input current is easily obtained by dividing the applied voltage by the resistor value.

The major disadvantage of integrated diodes in standard CMOS is that this technology is not optimized for optical devices. Their relatively small depletion widths result in a lower efficiency and speed than those of commercial diodes. This might be compensated

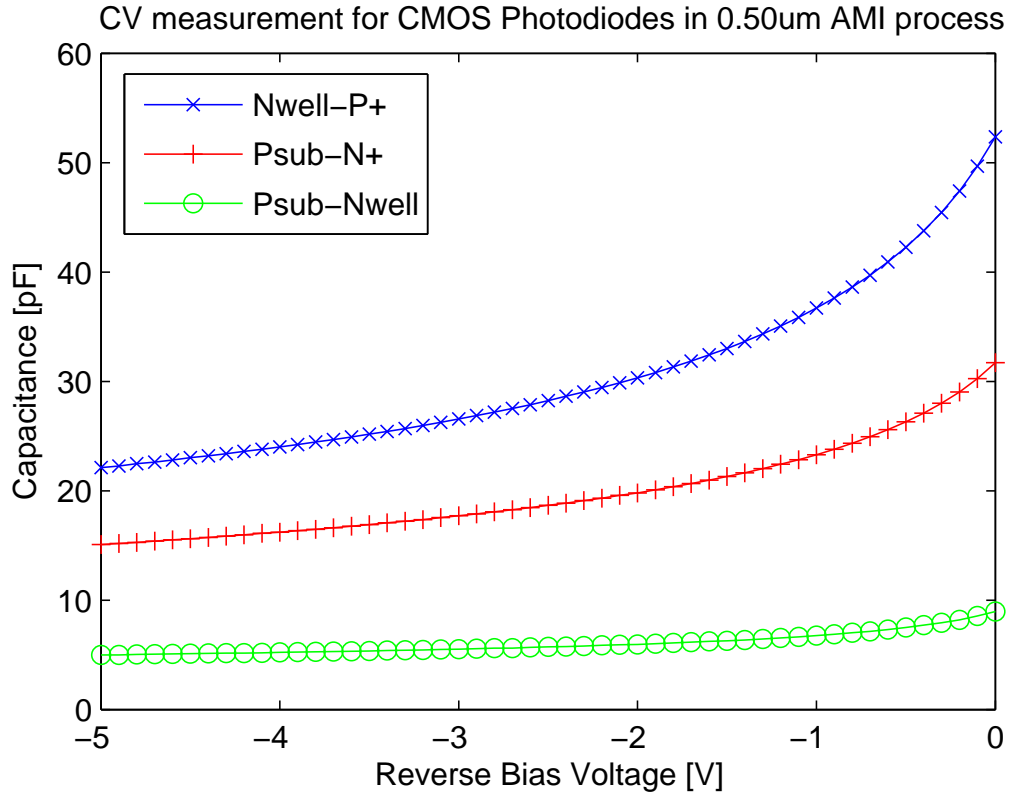


Figure 3.13. CV measurement plot for photodiodes in 0.5um AMI CMOS process.

by slightly modifying the technology, but the resulting raise in cost would probably be unacceptable for large integrated systems.

The limited performance of a photodiode in a standard technology is partly redressed by some important advantages. The integration of such a photodiode on the same chip as the receiver results in a low-cost system with an enhanced yield, thanks to the reduced external components count. Furthermore, an integrated photodiode reduces the total input capacitance by eliminating the parasitics due to the diode's package, the PCB wiring, the IC-package and some bondpads.

This gives the opportunity to increase the transimpedance-bandwidth product for free. The integration of the photodiode is also advantageous for the stability of the receiver with TIA, as its input capacitance, which determines the dominant pole, is well-defined and fixed. Another major advantage of an integrated photodiode is the reduction of noise coupling into the input node thanks to the removal of the bondwires, the package pins and

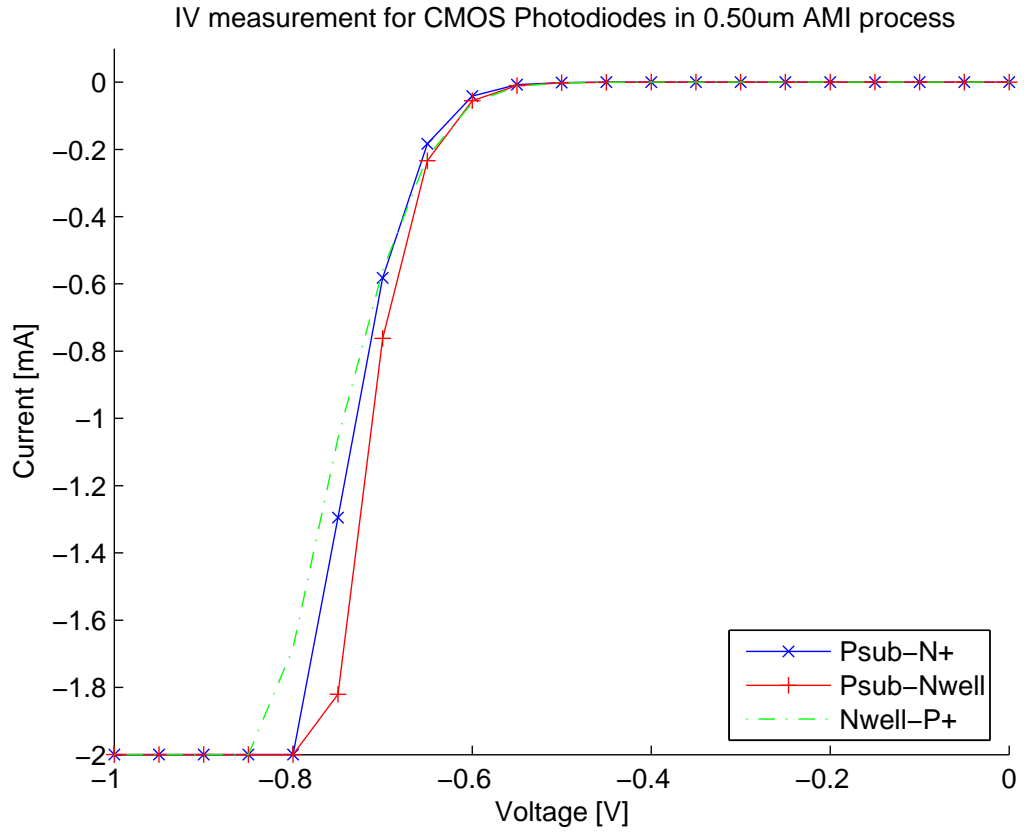


Figure 3.14. IV measurement plot for photodiodes in 0.5um AMI CMOS process.

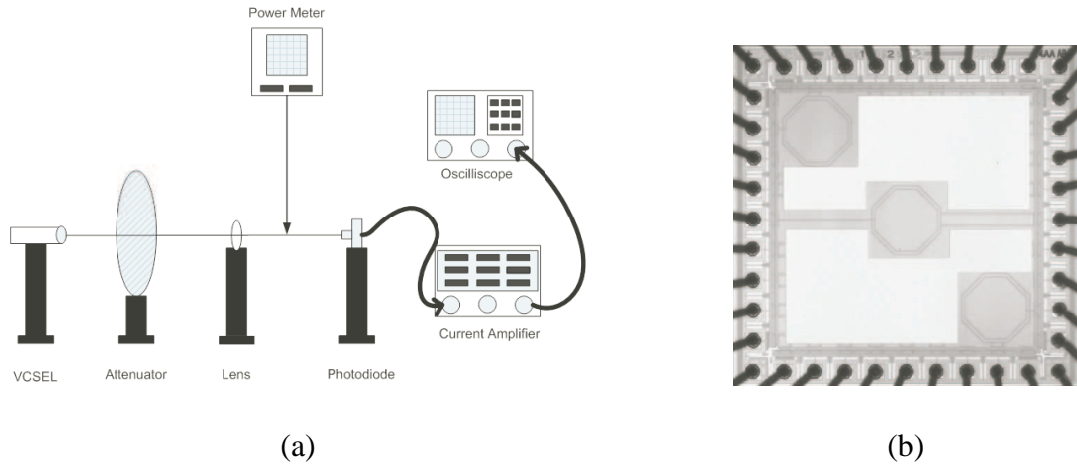


Figure 3.15. (a) Setup for photodiode responsivity measurements. (b) 0.50um AMI photodiode Chip microphotograph (1500um x 1500um).

the PCB paths connected to the node, which otherwise pick up spurious signals from the environment.

3.6 On-chip CMOS Filter

The design of analog filters can be performed with several techniques, such as RC-active, MOSFET-C, OTA-C and SC techniques. The RC-active technique is the most basic implementation technique of filters: The integrator structure consists of a passive resistor, usually polysilicon resistance of a high ohmic resistance, in combination with an opamp with the feedback capacitance. Because the only active component is the opamp, low-voltage filter designs based on this technique are mainly concentrated on the design of low-voltage opamps. The design of low-voltage CMOS opamps can be performed in standard CMOS technologies even down to 1.5V [10]. The only extra requirement compared to OTA-C or SC techniques is that the opamp should be able to drive resistive loads. This last fact is, however, also the drawback of this type of filter, especially if not only low voltage is required but also low power drain. The power drain of the amplifiers and the filter is related to the resistor values in the integrator. However, large resistor values in standard CMOS technologies would result in unacceptable chip areas, and so higher power drains are the result. A second problem with active with active-RC filters is the inaccuracy of the integrator time constant. This is because the time constant is related to the RC product, which depends on the absolute value of the polysilicon sheet resistance and the absolute value of the capacitance. However, those absolute values are not accurate in CMOS technologies. The result is that the cutoff frequency of these filters has only an accuracy of less than 50%.

In MOSFET-C filters the resistor of the active-RC structure is replaced by a MOSFET in its linear region. The advantage is that by controlling the gate voltage, the equivalent R value can now be tuned. Hence the main drawback of active-RC filters can be overcome by integrating an automatic tuning technique on chip [30]. The main drawback of using the MOSFET is that the transistor is a nonlinear component. The distortion can be improved by using fully differential structure. However, this requires not only opamps which can drive resistive loads but also fully differential opamps with a common-mode feedback system. The distortion specification is a function of the gate voltage with respect to the DC input

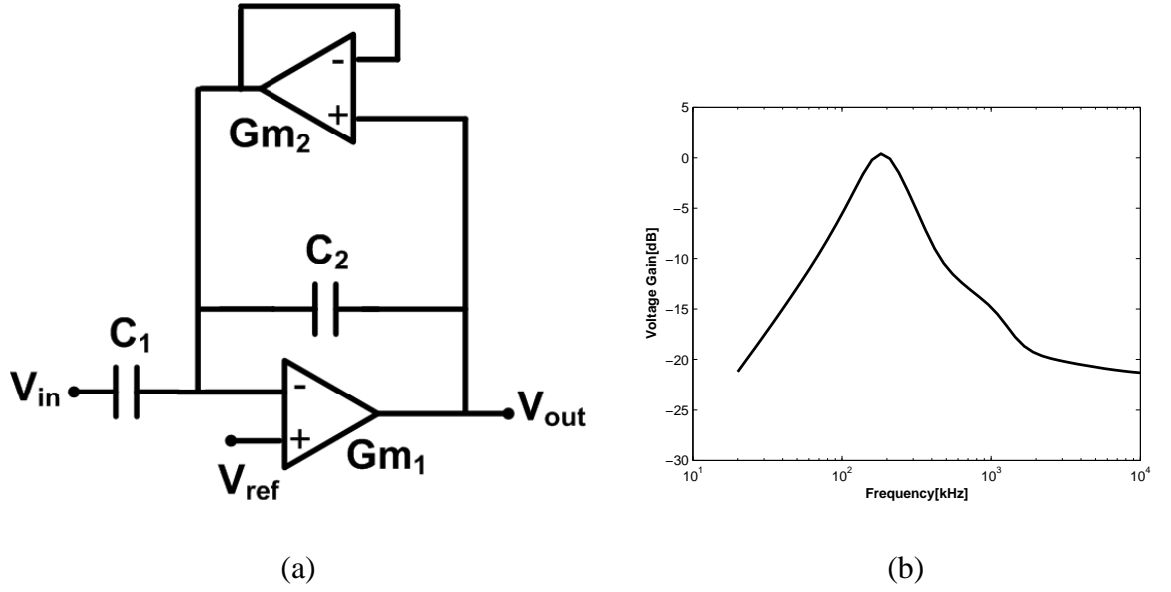


Figure 3.16. (a)Band pass filter topology for independent controls on high and low corners. (b)AC response of the band pass filter(simulated).

voltage and bulk voltage. In order to achieve very good distortion levels of -60dB and better, with big input peak-to-peak signals, high voltage power supplies are required [10].

SC technique is another approach. Usually the operation of frequency is low and the structure requires external clocks signals for switching. On the other hand, the last approach for filtering i.e. GM-C or OTA-C approach can operate at higher frequencies with out the need of external clock signals. This approach is quite common for continuous time filters. Here we will discuss an approach of filtering that is based on capacitively coupled current conveyer circuit. This technique has the potential of having independent control on frequency corners and hence extra flexibility for filter prototyping.

3.6.1 Band Pass CMOS Filter

Fig. 3.16(a) shows the topology used for band pass filter [29]. It gives independent control on low and high corners of the filter. The Gm blocks used here operate in moderate inversion and hence maximize the current efficiency. The corners and the mid band gain is given by

$$f_{LO} = \frac{Gm_2}{C_2}, \quad f_{HI} = \frac{Gm_1}{C_T C_o - C_2^2}, \quad \text{Gain} = -\frac{C_1}{C_2}, \quad (3.1)$$

where $C_T = C_1 + C_2$ and $C_o = C_2 + C_{load}$. The AC response of this band pass filter is shown in Fig. 3.16(b)

This filter can be implemented with only two transistors as shown in Fig. 3.17. This band pass filter is also called Capacitively Coupled Current Conveyor(C4). The C4s corner frequencies are electronically tunable and can be set independently of one another. The frequency response of the C4 is governed by

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} \frac{s\tau_l(1 - s\tau_f)}{s^2\tau_h\tau_l + s(\tau_l + \tau_f(\frac{C_o}{\kappa C_2} - 1)) + 1} \quad (3.2)$$

where the time constants are given by

$$\tau_l = \frac{C_2 U_T}{\kappa I_{\tau_l}}, \quad \tau_f = \frac{C_2 U_T}{\kappa I_{\tau_h}}, \quad \tau_h = \frac{C_T C_o - C_2^2}{C_2} \frac{U_T}{\kappa I_{\tau_h}} \quad (3.3)$$

and where the total capacitance, C_T , and the output capacitance, C_o , are defined as $C_T = C_1 + C_2 + C_W$ and $C_o = C_2 + C_L$. The currents I_{τ_l} and I_{τ_h} are the currents through M2 and M3, respectively in Fig. 3.17. With normal usage, τ_f is very small, and the zero it produces lies far outside of the operating range.

The C4 has the properties of a bandpass filter with first-order slopes and a bandpass gain set by the ratio of the two coupling capacitors as $A_v \approx -\frac{C_1}{C_2}$. The overall time constant of the filter, which gives the center frequency, is

$$\tau = \sqrt{\tau_l \tau_h} \quad (3.4)$$

Transistors M_1 and M_4 can operate in weak, moderate, or strong inversion depending on the desired frequency response. As can be seen from the above equations, the corner

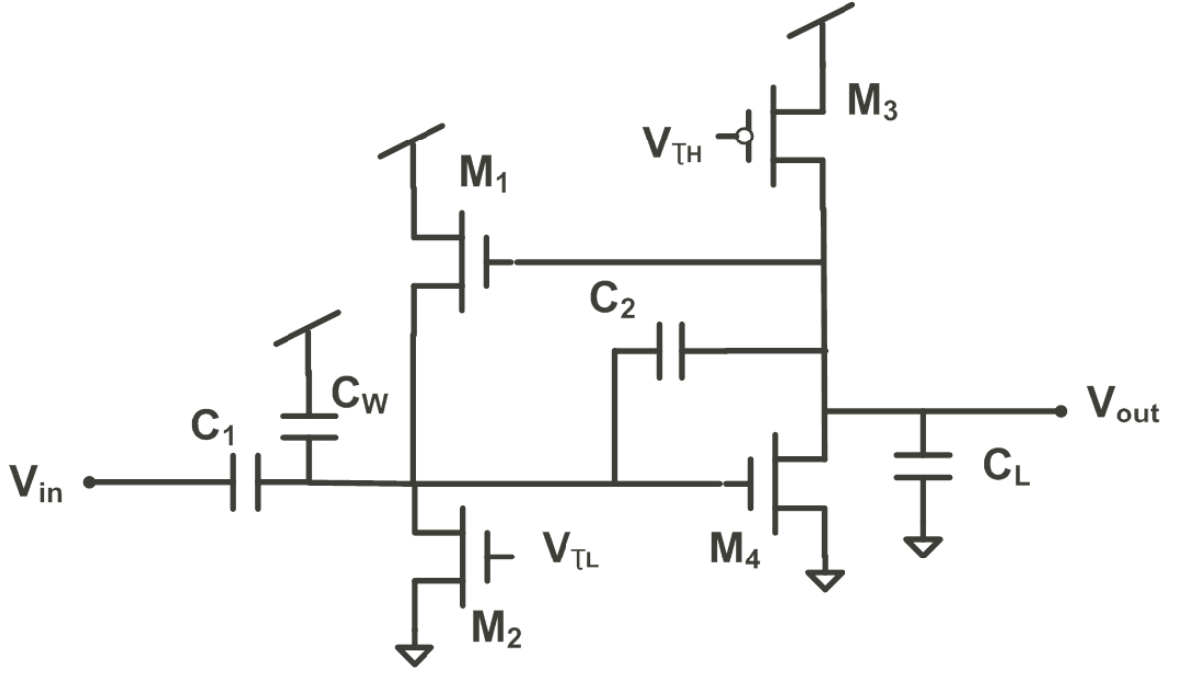


Figure 3.17. Schematic of the capacitively coupled current conveyor (C4).

frequency and the quality factor depend on the transconductances and, therefore, the DC bias current. Thus, the filter element can be easily fine-tuned after fabrication to the desired corner frequencies and Qs by tuning the g_{m1} and g_{m4} .

By tuning the filter such that $\tau_h > \tau_l$, resonance occurs, and the quality factor, Q, is

$$Q = \sqrt{\frac{\tau_h}{\tau_l}} \frac{1}{1 + \frac{I_{d1}}{I_{th}} \left(\frac{C_o}{\kappa C_2} - 1 \right)} \quad (3.5)$$

From the simplified circuit we can estimate the noise and the signal-to-noise ratio (SNR) for this C4 amplifier. The output thermal-noise voltage integrated over the entire bandwidth of interest (set by τ_h) is computed as

$$V_{noise} = \sqrt{q \left(\frac{I_4}{g_{m4}} \right) \frac{C_T}{C_o C_2}} \quad (3.6)$$

where $q = 1.6 \times 10^{-19} C$, and I_4 is the bias current flowing through M_4 . For the wideband case for the complete C4, the noise is divided by a term that is typically close to unity and is

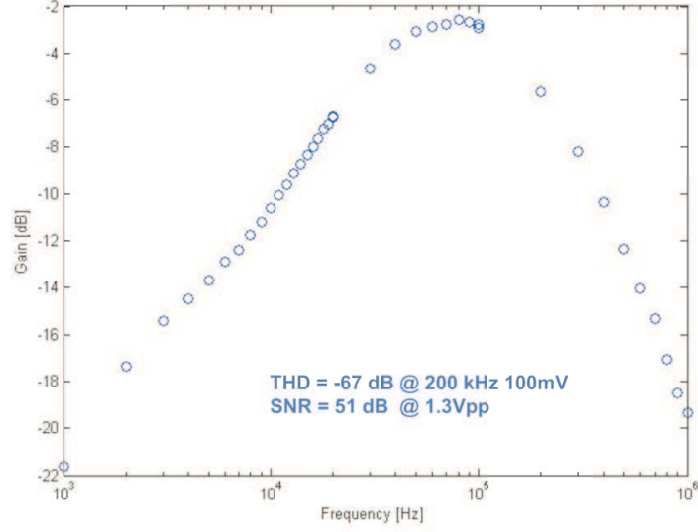


Figure 3.18. AC measurement of band pass filter.

given by $1 + g_{m1}(C_O/C_2 - 1)/\kappa(g_{m4})$. For subthreshold-current levels, the noise takes on the form of kT/C noise where the effective capacitance is $\kappa C_2(C_O/C_T)$. The output-referred linear range is given by $U_T C_T/(\kappa C_2)$ (subthreshold operation) and $V_{on} C_T/C_2$ (above-threshold operation), assuming $C_T C_O \gg C_2^2$ and that $V_{on} = \kappa(V_g - V_T) - V_s$ is the overdrive voltage at the bias condition. The linearity is set by choosing the desired capacitor value for C_W , which results from the capacitive attenuation at the input. Distortion for a differential system is less than -40dB at all points (third harmonic limited) over all frequencies (largest at one-third the center frequency). The resulting SNR for this amplifier is

$$SNR = 10 \log_{10} \frac{1}{q} \left(\frac{I_4}{g_{m4}} \right) \frac{C_T C_O}{C_2} \quad (3.7)$$

The SNR is directly increased by the product of $C_T C_O$ divided by C_2 , resulting in significantly smaller capacitor sizes for a given SNR than can be achieved by using other Gm-C techniques. When designing a C4, the 1/f noise corner frequency should be determined for the given biasing conditions; if the 1/f corner is not in the passband, the the effect of 1/f noise can be neglected.

The AC measurements are shown in Fig. 3.18. The filter is centered at 200kHz to have

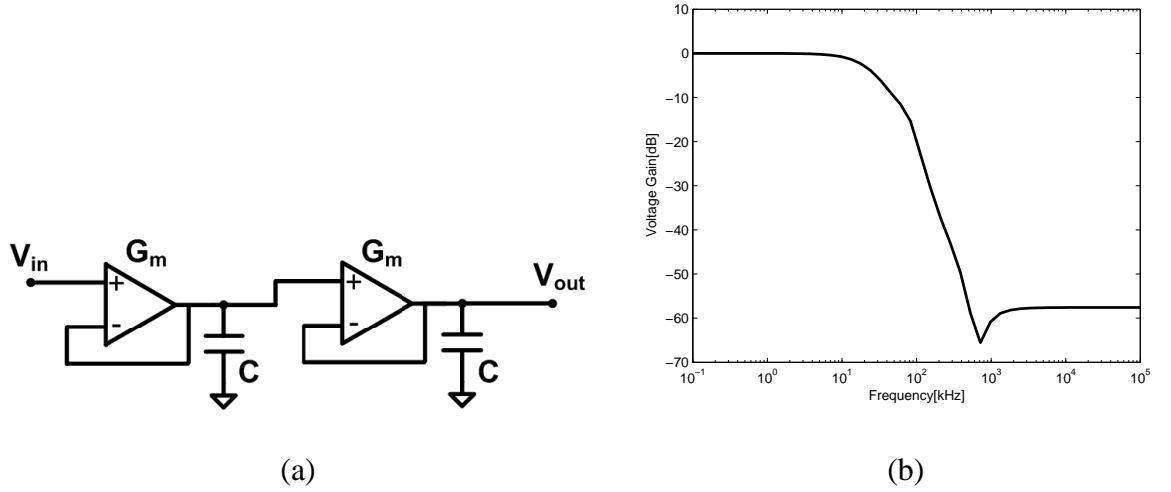


Figure 3.19. (a)Low pass filter topology for audio band. (b)AC response of low pass filter for audio band(simulated).

enough suppression of low frequency noise. The filter has 20dB per decade response for both high and low corners. This filter consumes 17uA of current.

3.6.2 Low Pass CMOS Filter

Fig. 3.19(a) shows the schematic of low pass filter topology used. It is a simple cascade of two follower-capacitor structures based on subthreshold mode amplifier, consuming only few micro-amps of current each. Fig. 3.19(b) shows the simulation AC response with a -3dB cut off close to 20kHz, which is our desired corner for removing undesired high frequency signals. The corner can be easily tuned with Gm/C ratio.

The AC measurements are shown in Fig. 3.20. The filter is corner is at 20kHz to have enough suppression of high frequency signals. The filter has 20dB per decade response and consumes less than 1uA of current.

3.7 AM Demodulators

The audio band signal is basically base band signal. The sound signal occupies the basic lowest frequencies from 20 Hz to 20 kHz. In most of the communication systems, the desired signal is moved higher in frequencies for transmission over the communication medium as shown in Fig. 3.22. We make use of amplitude modulation to shift our frequency

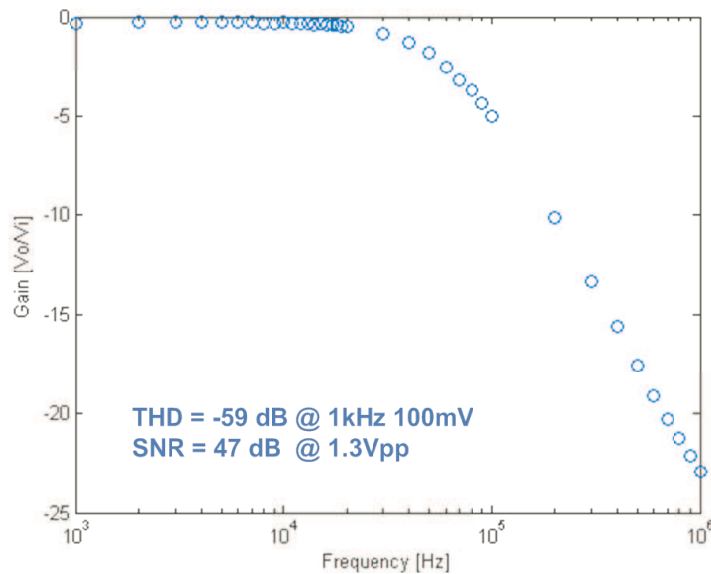


Figure 3.20. AC measurement of low pass filter.

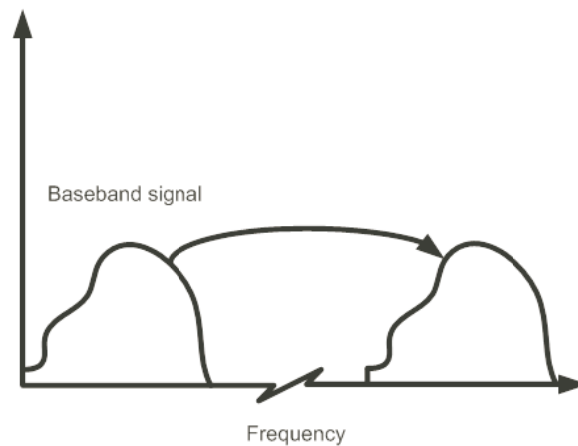


Figure 3.21. A baseband signal is shifted to higher frequency with frequency shifting.

of interest to higher frequencies. Amplitude modulation(AM) can be examined both in time and frequency domain. Modulation is the process where a signal amplitude, frequency, or phase is changed in order to transmit intelligence. In AM modulation, The carrier frequency's amplitude changes in accordance with the modulated voice signal, while the carrier's frequency does not change. The characteristics of the carrier wave are instantaneously varied by another "modulating" waveform. When carrier combined with the signal of interest, the resultant AM signal consists of the carrier frequency, plus UPPER and LOWER

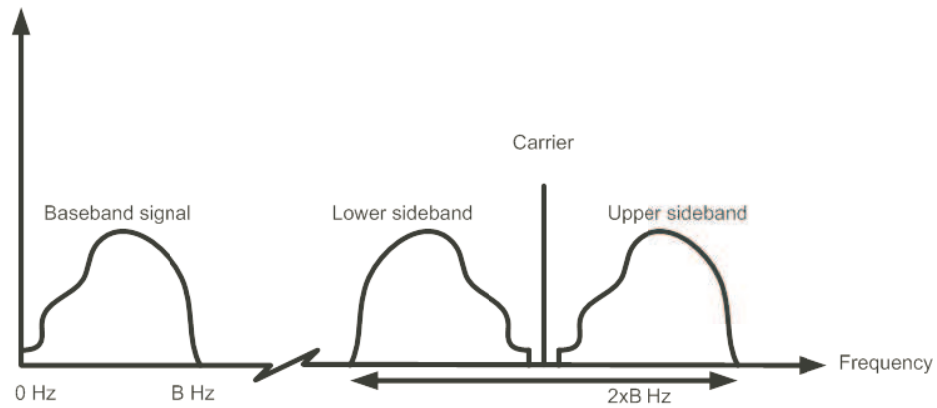


Figure 3.22. Spectrum of AM carrier: Upper sideband is the frequency shifted replica of the baseband signal, while lower sideband is the mirror version. The carrier also appears in the spectrum.

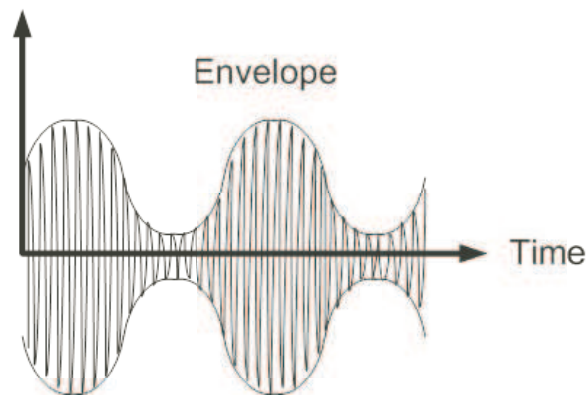


Figure 3.23. The baseband waveform is multiplied by the carrier wave. The envelope has the shape of the baseband signal.

sidebands. This is known as Double Sideband - Amplitude Modulation(DSB-AM), or more commonly referred to as plain AM as shown in Fig. 3.22.

AM is a multiplicative process where the carrier is multiplied with the baseband signal. This results in the peaks of the carrier to take the shape of the baseband signal as shown in Fig. 3.23. These peaks are called the envelope. The effect in the frequency domain is to shift the baseband signal to a range above the frequency of the carrier. If the baseband signal has a maximum frequency of $B \text{ Hz}$, the amplitude modulated carrier contains frequencies from $B \text{ Hz}$ below the carrier frequency to $B \text{ Hz}$ above the carrier frequency. Thus the bandwidth of the amplitude modulated carrier is $2xB \text{ Hz}$.

The process for demodulating a double sideband signal is relatively straightforward

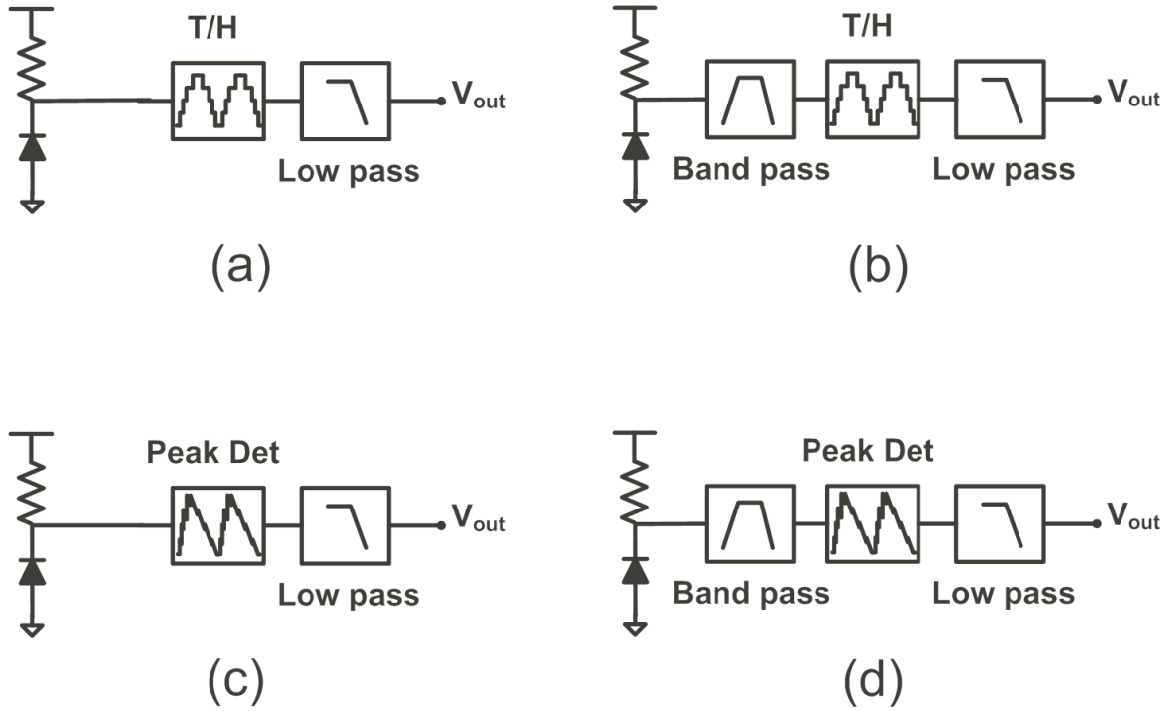


Figure 3.24. Different approaches for Am-demodulation. (a)Track and hold without front end band-pass filter.(b)Track and hold with front end bandpass filter. (c)Peak detector without front end bandpass filter. (d)Peak detector with front end bandpass filter.

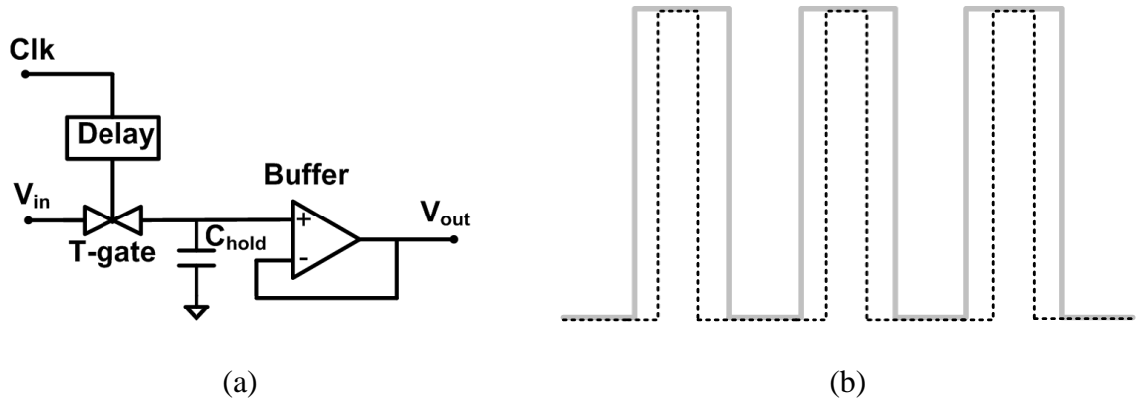


Figure 3.25. (a) Synchronous Detector for AM modulated signal. (b) The clock signal used for demodulation with reduced duty cycle.

because the shape of the baseband signal is contained in the envelope of the modulated carrier. The negative portion of the waveform of the modulated carrier is discarded.

3.7.1 Synchronous Detector

Fig. 3.25(a) shows the simple schematic for the synchronous detector [31]. The clock signal used to generate the input AM modulated signal is also used for demodulation. Fig. 3.25(b)

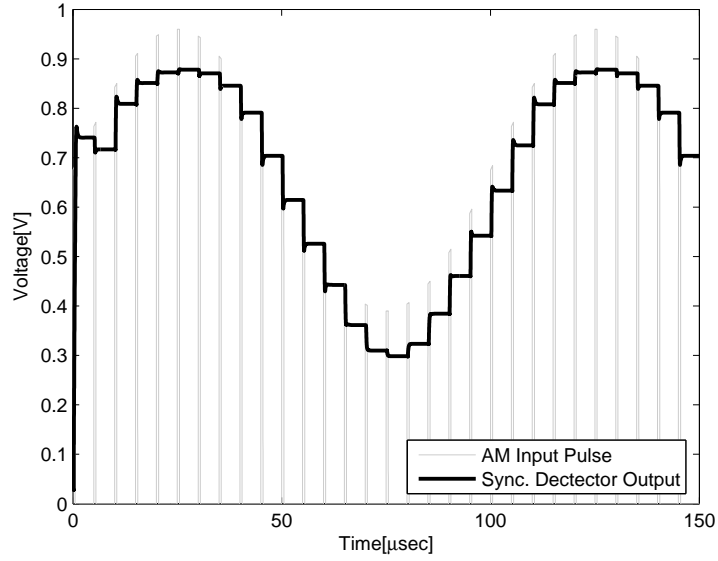


Figure 3.26. Synchronous detector output for AM modulated input pulse.

shows the clock needed for proper detection with reduced duty cycle. When the clock is high, the detector charges the capacitor C_{hold} . Otherwise on low clock, the detector simply tracks the input voltage level that was read on the capacitor. In terms of functionality, this is a track and hold circuit. Combined with the input modulated AM signals, the system behaves as a chopper and reduces the low frequency flicker noise. Fig. 3.26 shows the response of the synchronous detector.

There are mainly two approaches we take in track and hold receiver architecture. Namely it is with and without the bandpass filter in the receiver chain. We will look at the measurement data from each type of receiver and will compare it for SNR for given power.

3.7.2 Track and Hold without Bandpass

This approach is shown in Fig. 3.27. Notice that essentially the main receiver architecture is kept same with track and hold based approach. The only difference is the absence of bandpass filter after current to voltage conversion stage at the front end of the receiver. There are tradeoffs in this approach. The initial intent of using a bandpass filter is the filtering of low frequency noise. Essentially we want to have a highpass filter at the front

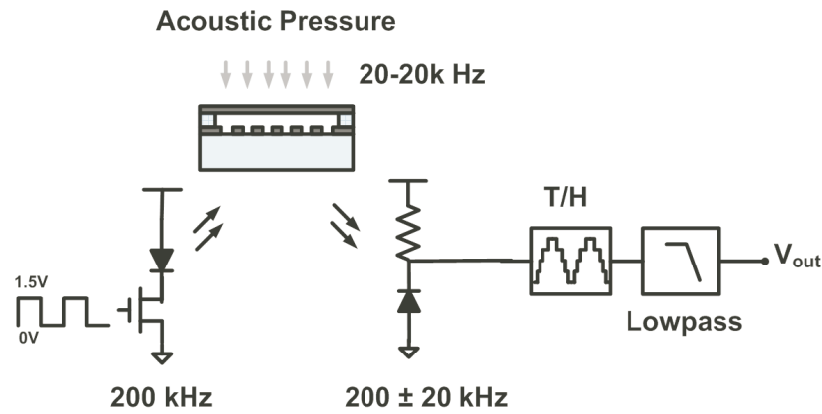


Figure 3.27. Track and hold receiver without bandpass filter.

end. The corner of the filter should be set lower than the carrier frequency of the input modulator. In our case, the frequency is selected at 200kHz. Care has to be taken when making frequency selection for the modulator. As the application is for low power device, the frequency cannot be too high. Having a high carrier frequency translates directly to power consumption. The other concerns is bring in high frequency signals into the receiver specially for track and hold topology. The high frequency clock used can also easily disturb the rest of the receiver blocks by coupling signals into the package leads, wirebonds and also the traces on-chip.

There is one concern with not using a bandpass filter. It is the low frequency noise. There could be a lot of different sources of low frequency noise coming into the receiver. The VCSEL has relative intensity noise. There is also flicker or pink noise. The $1/f$ noise corner is in kHz range. As the audio band for microphone is from 20-20kHz, care is taken in designing low flicker noise electronics. Amplifiers with PMOS differential pairs is preferred as it introduces less noise compared to its counterpart with NMOS differential pairs. The second concern is the control on the signal dc levels. The bandpass has a reference voltage node that is used to optimize the dc levels. Now without the bandpass filter, the front end dc levels right after the current to voltage conversion at photodiode and resistor node are dependent on the optical light input to the photodiode. As the light levels go up, the node voltage drops from the VDD level. Initially there is only dark current in the

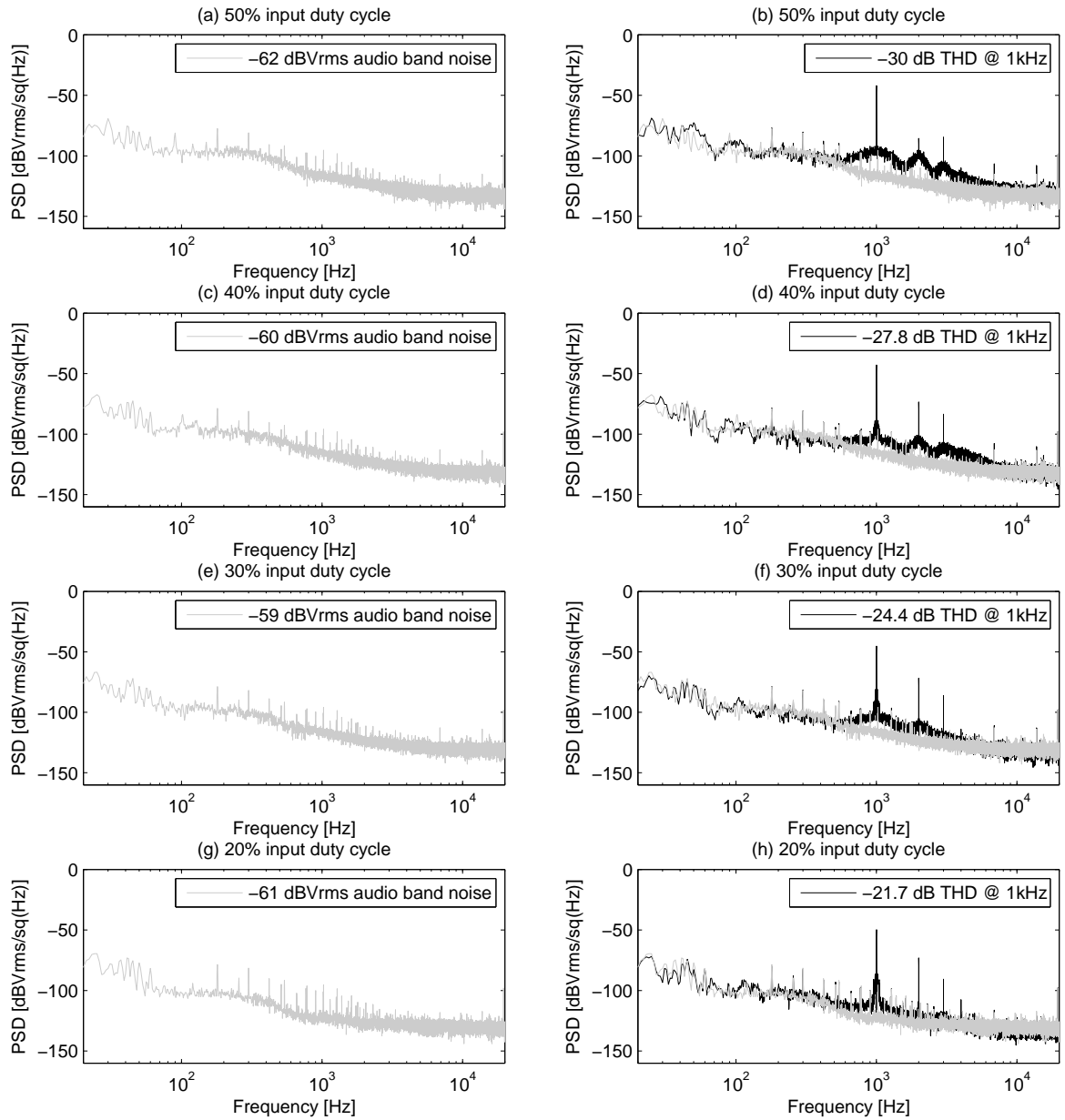


Figure 3.28. Track and hold receiver noise without bandpass filter at various input duty cycles: (a)50% duty cycle noise spectrum. (b)50% duty cycle with 1kHz audio signal spectrum. (c)40% duty cycle noise spectrum. (d)50% duty cycle with 1kHz audio signal spectrum. (e)30% duty cycle noise spectrum. (f)30% duty cycle with 1kHz audio signal spectrum. (g)20% duty cycle noise spectrum. (h)20% duty cycle with 1kHz audio signal spectrum.

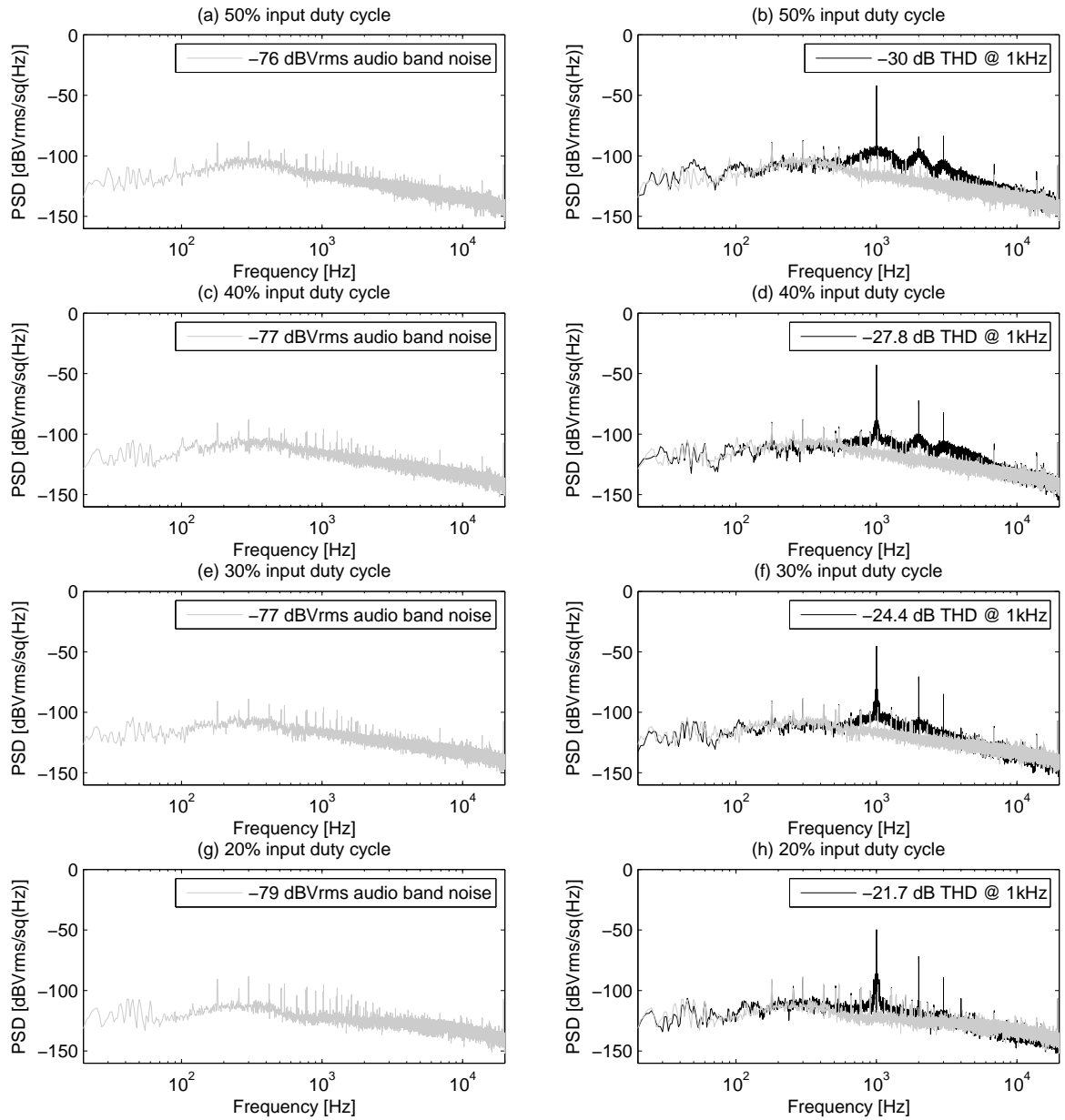


Figure 3.29. Track and hold receiver A-weighted noise without bandpass filter at various input duty cycles: (a)50% duty cycle noise spectrum. (b)50% duty cycle with 1kHz audio signal spectrum. (c)40% duty cycle noise spectrum. (d)50% duty cycle with 1kHz audio signal spectrum. (e)30% duty cycle noise spectrum. (f)30% duty cycle with 1kHz audio signal spectrum. (g)20% duty cycle noise spectrum. (h)20% duty cycle with 1kHz audio signal spectrum.

photodiode. Then as the current level increases, there is an increased voltage drop across the front end resistor. Now notice that the dc level at the front end conversion can change with the optical input. This could have an adverse effect on the dynamic range and hence the linearity of the overall receiver. The noise data is shown in Fig. 3.28. We make use of A-weighting filter for microphone application. The noise with A-weighting filter is shown in Fig. 3.29. The A-weighting filter has a bandpass type shape. It is mainly based on the human ear perception for different frequencies. Most of the emphases is on the low kHz frequency range. This is the range where most of the speech occurs. The total integrated noise in the audio band is about -60dBVrms without the use of A-weight. The noise level drops to about -80dBVrms after A-weighting. The change in the input duty cycle has a little effect on reducing the noise level in measurements. As the track and hold switch is turned on for a shorter and shorter interval of time, this means that the back end of the receiver is exposed to shorter intervals of noisy input signal. The THD is not dependent on the input duty cycle. The changing duty cycle changes the dc level of the receiver. The signal goes from more optimized dc level to a non-linear range.

The time domain behavior is shown in Fig. 3.30. We perform a FFT on the time domain signal to see how the received signal appears on the frequency spectrum. After detection, there is still 200kHz carrier is present in the spectrum. As the on-chip CMOS filter does not have enough suppression, we process the data with an ideal RC 2nd order butterworth filter. This places a corner at 20kHz and hence with 20dB per decade suppression, the 200kHz signal is further minimized.

3.7.3 Track and Hold with Bandpass

This approach is shown in Fig. 3.31. Notice that essentially the main receiver architecture is kept same with track and hold based approach. The only difference is the presence of bandpass filter after current to voltage conversion stage at the front end of the receiver. There are tradeoffs in this approach. The initial intent of using a bandpass filter is the filtering of low frequency noise. Essentially we want to have a highpass filter at the front end. The

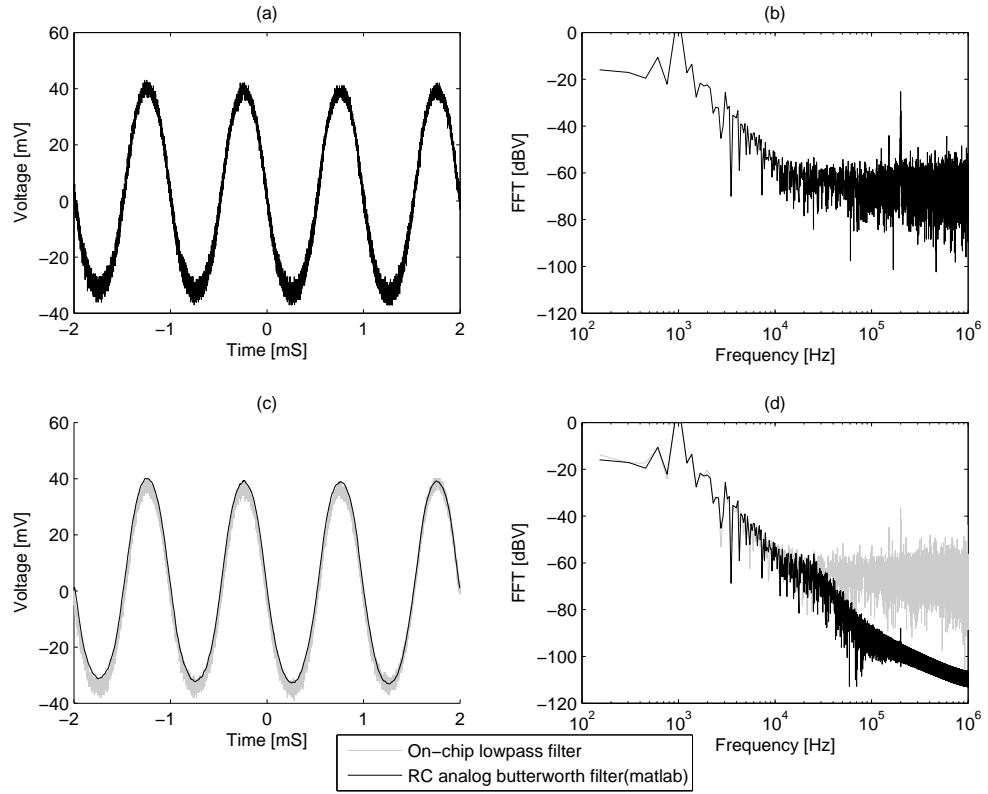


Figure 3.30. Track and hold receiver output without bandpass filter.(a) Output from the detector.(b) FFT of the output from detector. (c) Output after lowpass filter.(d) FFT of the output after lowpass filter.

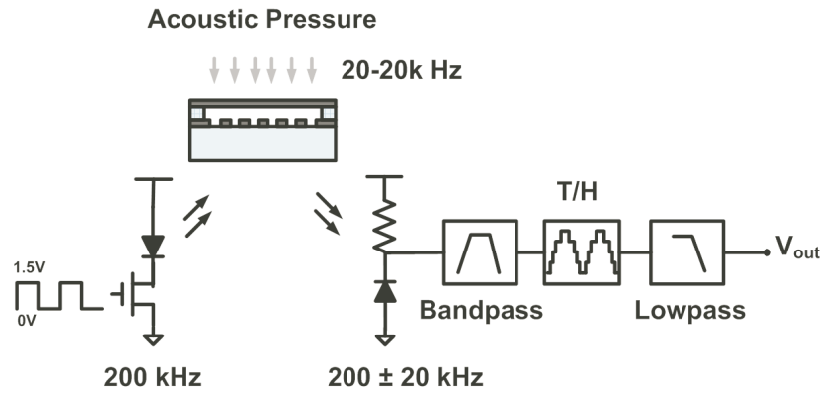


Figure 3.31. Track and hold receiver with bandpass filter.

corner of the filter should be set lower than the carrier frequency of the input modulator. The much of the receiver remains the same. The frequency is selected at 200kHz. Care is taken when making frequency selection for the modulator.

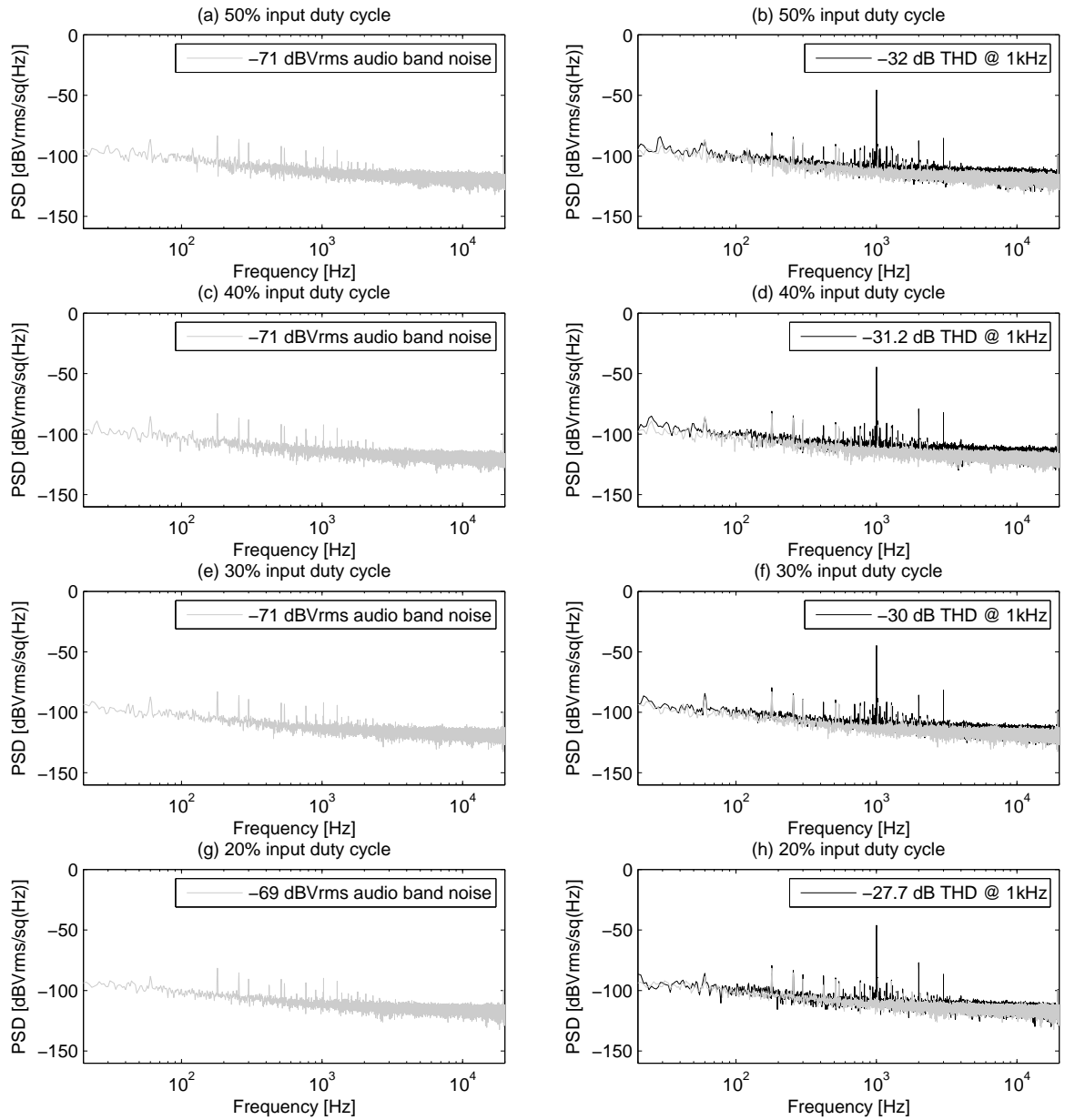


Figure 3.32. Track and hold receiver noise with bandpass filter at various input duty cycles: (a)50% duty cycle noise spectrum. (b)50% duty cycle with 1kHz audio signal spectrum. (c)40% duty cycle noise spectrum. (d)50% duty cycle with 1kHz audio signal spectrum. (e)30% duty cycle noise spectrum. (f)30% duty cycle with 1kHz audio signal spectrum. (g)20% duty cycle noise spectrum. (h)20% duty cycle with 1kHz audio signal spectrum.

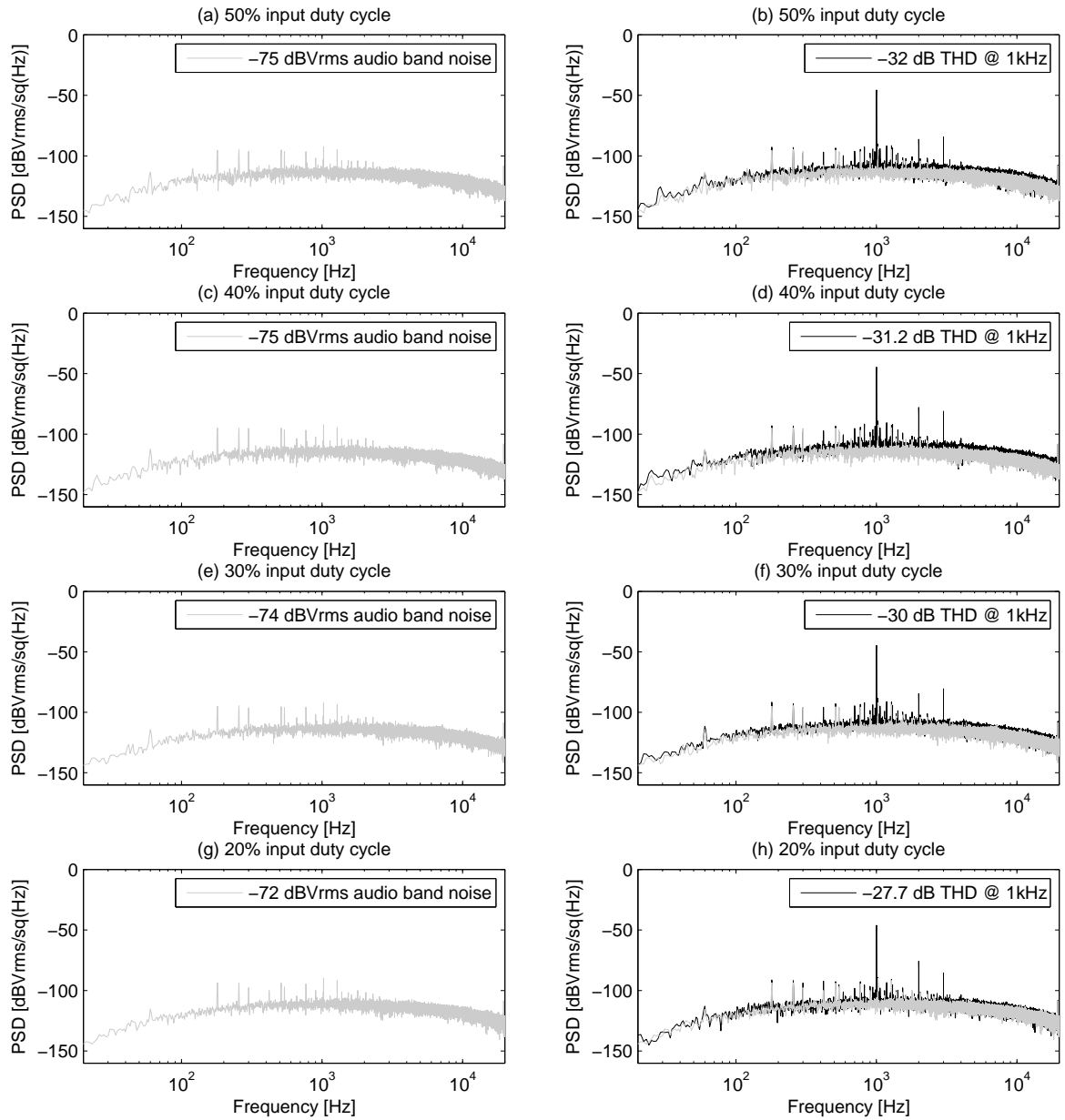


Figure 3.33. Track and hold receiver A-weighted noise with bandpass filter at various input duty cycles:
 (a) 50% duty cycle noise spectrum. (b) 50% duty cycle with 1kHz audio signal spectrum.
 (c) 40% duty cycle noise spectrum. (d) 50% duty cycle with 1kHz audio signal spectrum.
 (e) 30% duty cycle noise spectrum. (f) 30% duty cycle with 1kHz audio signal spectrum.
 (g) 20% duty cycle noise spectrum. (h) 20% duty cycle with 1kHz audio signal spectrum.

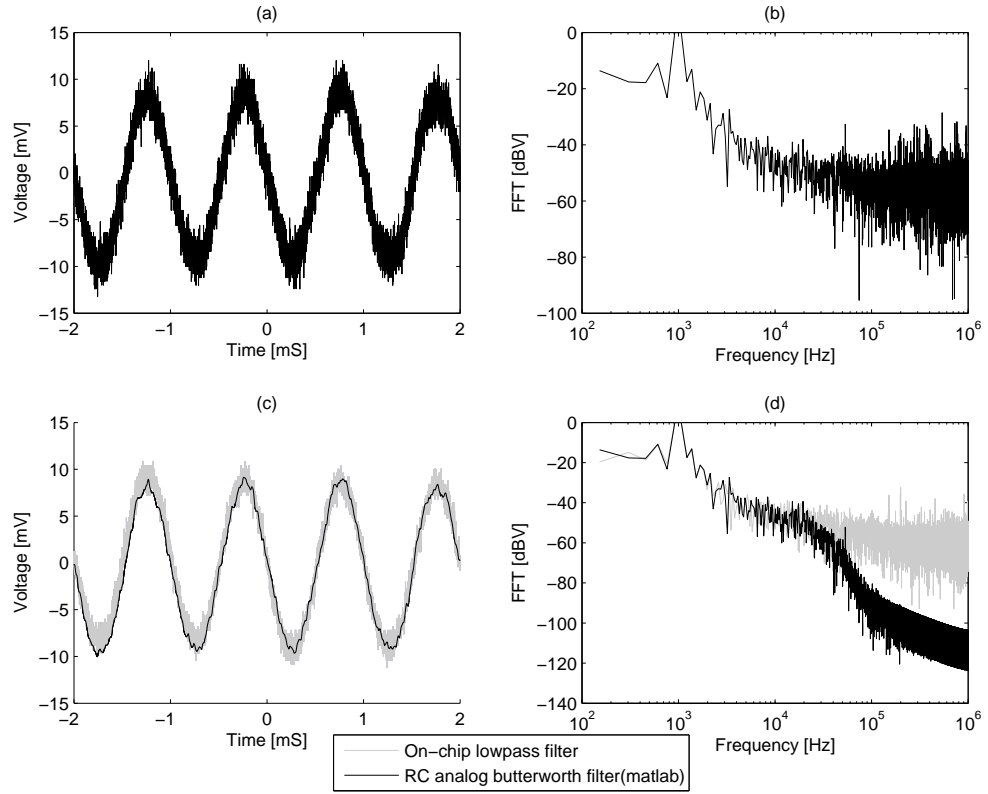


Figure 3.34. Track and hold receiver output with bandpass filter.(a) Output from the detector.(b) FFT of the output from detector. (c) Output after lowpass filter.(d) FFT of the output after lowpass filter.

The bandpass filter filters any low frequency noise present at the front end of the receiver. The VCSEL introduces noise, along with the shot noise from photodiode and the resistor noise. The bandpass has the benefit of providing the control on dc levels after the front end conversion. The second concern is the control on the signal dc levels. The bandpass has a reference voltage node that is used to optimize the dc levels. Now notice that the dc level at the front end conversion can change with the optical input. This could have an adverse effect on the dynamic range and hence the linearity of the overall receiver. The dc control on the bandpass reduces this adverse effect. The noise data is shown in Fig. 3.32. We make use of A-weighting filter for microphone application. The noise with A-weighting filter is shown in Fig. 3.33.

The total integrated noise in the audio band is about -70dBVrms without the use of

A-weight. The noise level drops to about -75dBVrms after A-weighting. The change in the input duty cycle has a little effect on reducing the noise level in measurements. As the track and hold switch is turned on for a shorter and shorter interval of time, this means that the back end of the receiver is exposed to shorter intervals of noisy input signal. The THD is not dependent on the input duty cycle. The changing duty cycle changes the dc level of the receiver. The signal goes from more optimized dc level to a non-linear range. In this case the front end bandpass filter has nonlinearity coming from the change in the input dc levels. With the introduction of bandpass, the front end shift in the dc levels pushes the input signal to a more nonlinear input range of the bandpass with the changing input duty cycle. The nonlinearity is also introduced from the output buffer. In case of PMOS buffer, the ICMR is from 200mV to 800mV. Any shift of DC close the edges will have effect on the THD.

The time domain behavior is shown in Fig. 3.34. We perform a FFT on the time domain signal to see how the received signal appears on the frequency spectrum. After detection, there is still 200kHz carrier is present in the spectrum. As the on-chip CMOS filter does not have enough suppression, we process the data with an ideal RC 2nd order butterworth filter. This places a corner at 20kHz and hence with 20dB per decade suppression, the 200kHz signal is further minimized.

3.7.4 Envelope Detector

The demodulation of an AM signal using envelope detector is highly effective and is widely used in almost all commercial AM radio receivers. In an envelope detector, the output of the detector follows the envelope of the modulated signal. The circuits shown in Fig. 3.35 functions as an envelope detector [32]. On the positive cycle of the input signal, the MOS transistor just like a diode, conducts, and the capacitor C_{charge} , charges up to the peak voltage of the input signal. As the input signal falls below this peak value, the MOS transistor, just like a diode, cuts off. This occurs because the capacitor voltage which is very near the peak voltage, is greater than the input signal voltage, as a result causes the diode connection

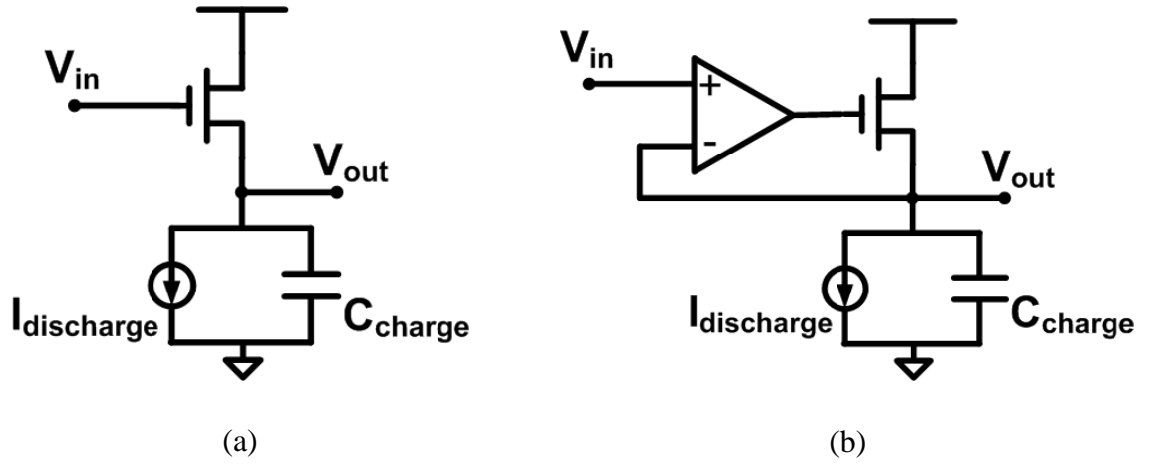


Figure 3.35. (a) Envelope Detector for AM modulated signal with simple MOS transistor. (b) Envelope detector for AM modulated signal with MOS transistor with input amplifier.

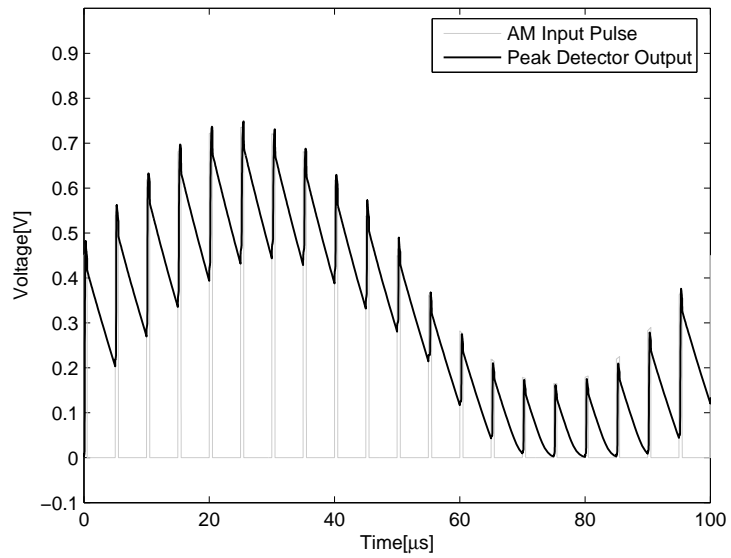


Figure 3.36. Peak detector output for AM modulated input pulse.

to open. The capacitor now discharge through the $I_{discharge}$ current source. Thus the output voltage closely follows the envelope of the input signal. Fig. 3.36 shows the output of the peak detector along with the input AM pulse. Note that the addition of amplifier in this topology removes the V_{gs} drop of the MOS transistor.

However, certain conditions must be met in order for the detector to work. The discharge frequency should be smaller than the sampling frequency of the pulse. It should also be greater than the frequency of interest in the AM modulated signal. The AM signal

must be narrow-band, meaning that the carrier frequency be large compared to the message bandwidth. Moreover, the percentage modulation must be less than 100%. The charging is bounded by

$$\frac{1}{R_c \cdot C} > f_c, \quad (3.8)$$

where, f_c is the carrier frequency, R_c is the impedance at the output node when MOS transistor is conducting, and C is the charging capacitor. This condition ensures that the capacitor charges rapidly and thereby follows the applied voltage up to the positive peak when the MOS transistor is conducting. Now when the MOS transistor stops, the discharging is bounded by

$$f_m < \frac{1}{R_d \cdot C} < f_c, \quad (3.9)$$

where, f_m is the frequency of interest and R_d is the impedance at the output node when MOS transistor is not conducting. This ensures that the capacitor discharges slowly through the discharging load, i.e. from the current/charge sink. The result is that the capacitor voltage or the detector output is nearly the same as the envelope of the AM input signal.

3.7.5 Envelope detector without bandpass

Envelope detector without bandpass filter is shown in Fig. 3.37. The signal after current to voltage conversion at the front end goes directly into the detector stage. Same concerns for dc voltage applies here too. The dc levels are now dependent on the optical input level. Starting with 50% duty cycle, the dc levels are optimized in the middle of the input common mode range. This dc level will change with the changing duty cycle.

The noise data is shown in Fig. 3.38. The noise with A-weighting filter is shown in Fig. 3.29. The total integrated noise in the audio band is about -62dBVrms without the use of A-weighting. The noise level drops to about -67dBVrms after A-weighting. The change

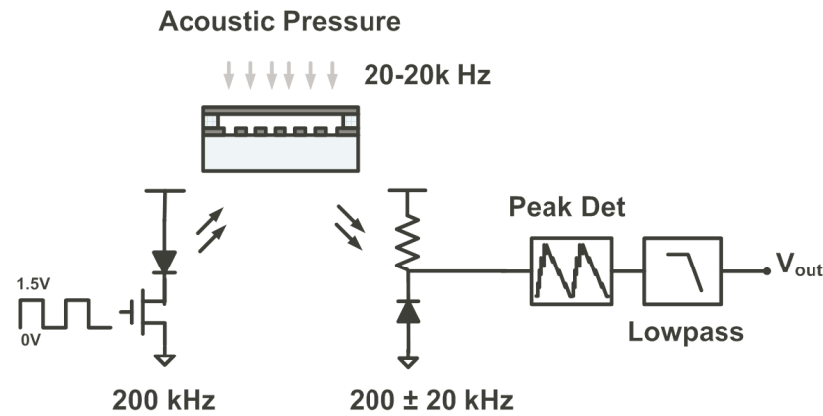


Figure 3.37. Peak detector receiver without bandpass filter.

in the input duty cycle has a little effect on reducing the noise level in measurements. Again the THD is not dependent on the input duty cycle. The changing duty cycle changes the dc level of the receiver. The signal goes from more optimized dc level to a non-linear range. Although the peak detector has more non-linearity coming from the diode like behavior of the transistor. The THD is 5dB worse than the track and hold receiver.

The time domain behavior is shown in Fig. 3.40. We perform a FFT on the time domain signal to see how the received signal appears on the frequency spectrum. After detection, there is still 200kHz carrier is present in the spectrum. We process the data with an ideal RC 2nd order butterworth filter. This places a corner at 20kHz and hence with 20dB per decade suppression, the 200kHz signal is further minimized. Basically what it means that with a 2nd order CMOS filter we can achieve the desired attenuation in our detected signal.

One thing that we notice in case of peak detector receiver. The input to the detector is essentially a square pulse. It has a sinc shape response. Now if we change the duty cycle from 50% down to 20%, ideally the output amplitude for the first lobe of the sinc function goes down. Now more and more energy shifts from the 200kHz band to its harmonics. We notice this behavior in our gain measurements. The gain tends to go down as we change input duty cycle from 50% to 20%. Further discussion is made on this in the topology comparison section of this chapter. The peak detector demodulation is quite different from track and hold detector. Track and hold basically captures the envelope from the synchronized

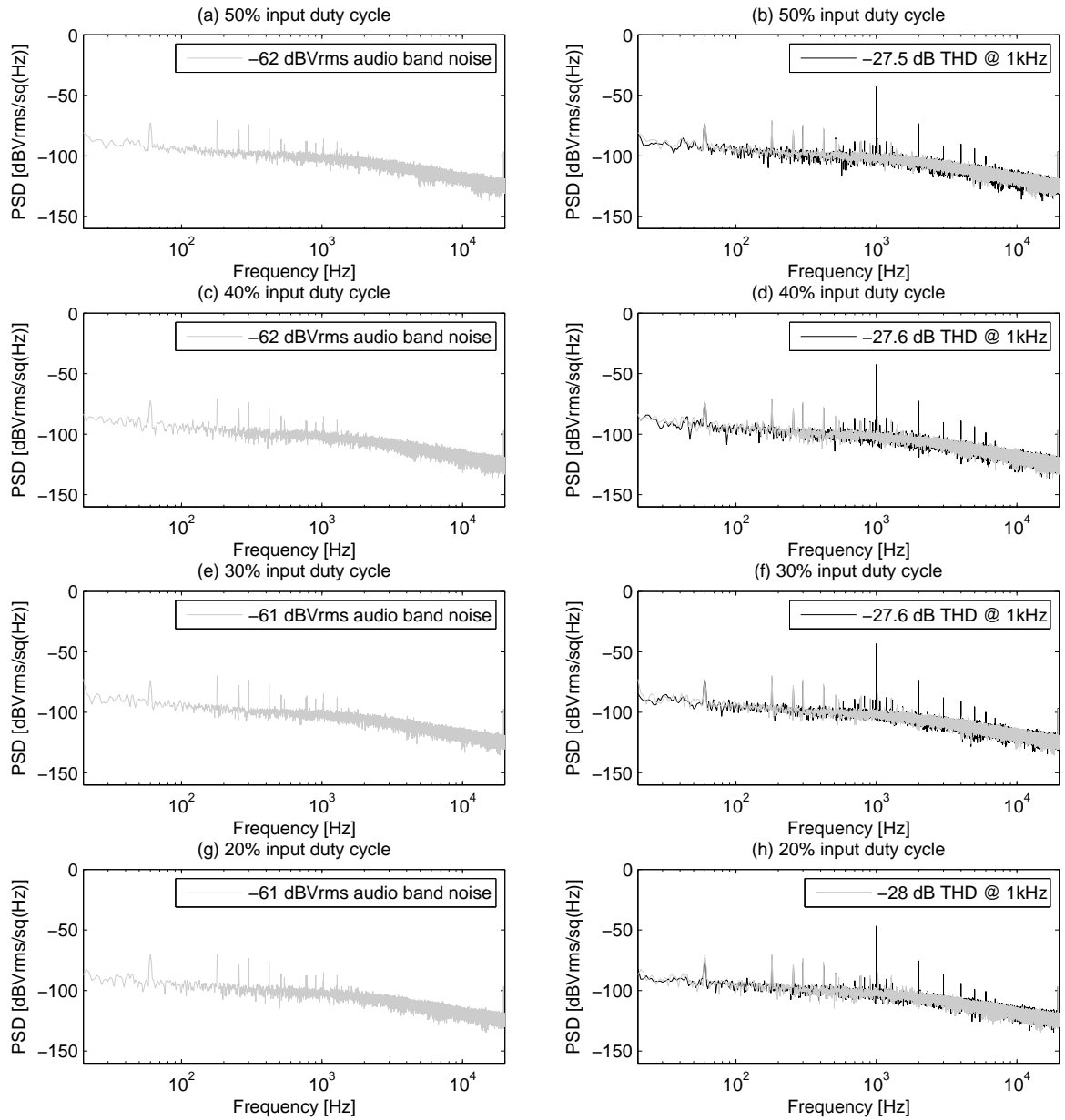


Figure 3.38. Peak detector receiver noise without bandpass filter at various input duty cycles: (a)50% duty cycle noise spectrum. (b)50% duty cycle with 1kHz audio signal spectrum. (c)40% duty cycle noise spectrum. (d)50% duty cycle with 1kHz audio signal spectrum. (e)30% duty cycle noise spectrum. (f)30% duty cycle with 1kHz audio signal spectrum. (g)20% duty cycle noise spectrum. (h)20% duty cycle with 1kHz audio signal spectrum.

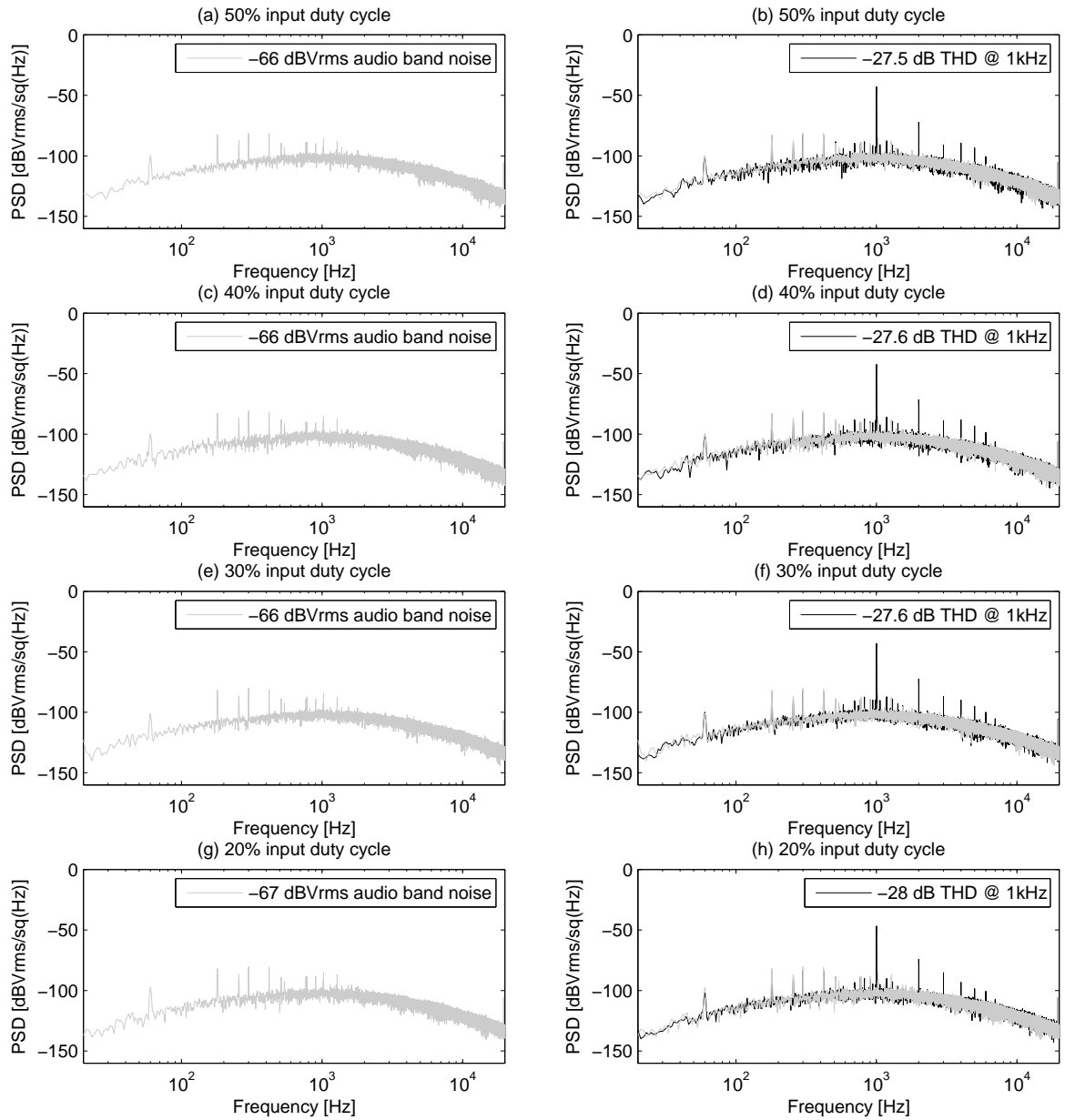


Figure 3.39. Peak detector receiver A-weighted noise without bandpass filter at various input duty cycles: (a)50% duty cycle noise spectrum. (b)50% duty cycle with 1kHz audio signal spectrum. (c)40% duty cycle noise spectrum. (d)50% duty cycle with 1kHz audio signal spectrum. (e)30% duty cycle noise spectrum. (f)30% duty cycle with 1kHz audio signal spectrum. (g)20% duty cycle noise spectrum. (h)20% duty cycle with 1kHz audio signal spectrum.

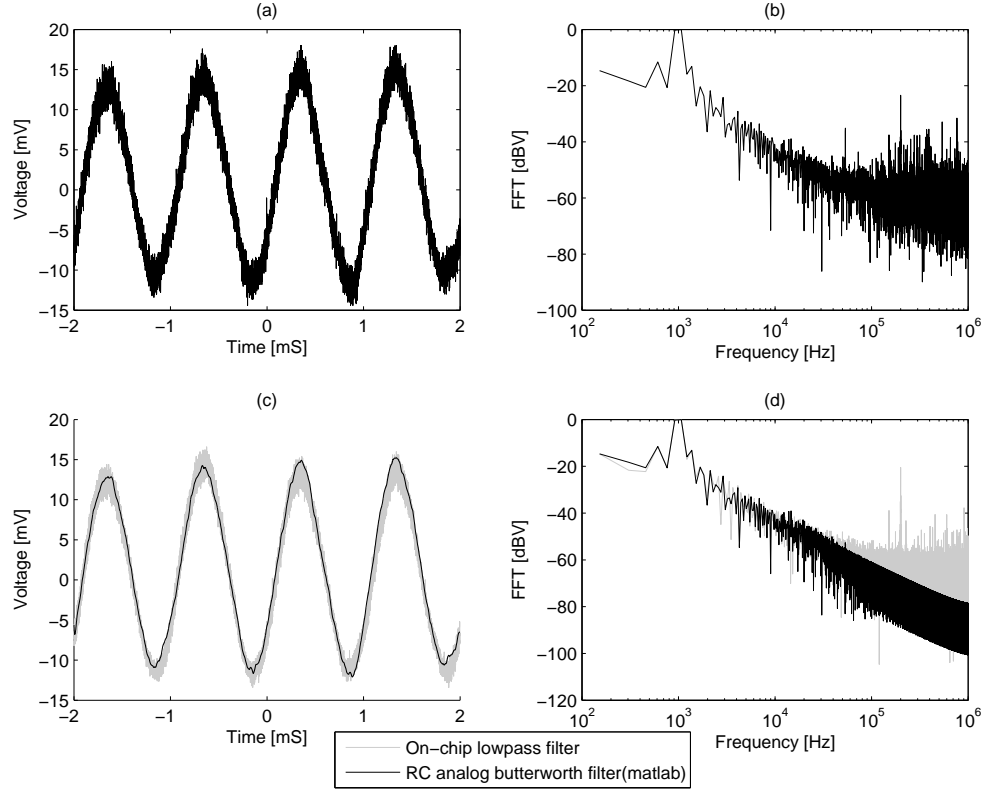


Figure 3.40. Peak detector receiver output without bandpass filter.(a) Output from the detector.(b) FFT of the output from detector. (c) Output after lowpass filter.(d) FFT of the output after lowpass filter.

clock used for the input pulsing. Peak detector on the contrary is designed to capture the envelope of certain frequency with out any clock input. This limits the frequency response. More treatment of this topic is given in AC response comparison.

3.7.6 Envelope detector with bandpass

This approach is shown in Fig. 3.41. The main receiver architecture is kept same with peak detector approach. The only difference is the presence of bandpass filter after current to voltage conversion stage a the front end of the receiver.

Again the bandpass filter filters any low frequency noise present at the front end of the receiver. The bandpass provides the control on dc levels after the front end conversion. The dc control on the bandpass reduces the adverse effect if affecting the dynamic range and signal clipping down the receiver chain. The noise data is shown in Fig. 3.42. We make

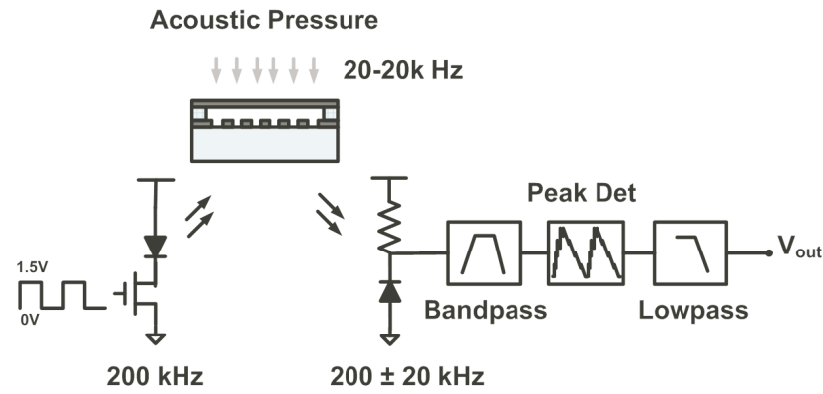


Figure 3.41. Peak detector receiver with bandpass filter.

use of A-weighting filter for microphone application. The noise with A-weighting filter is shown in Fig. 3.43.

The total integrated noise in the audio band is about -64dBVrms without the use of A-weight. The noise level drops to about -70dBVrms after A-weighting. The change in the input duty cycle has a little effect on reducing the noise level in measurements. The THD is not dependent on the input duty cycle. The changing duty cycle changes the dc level of the receiver. The signal goes from more optimized dc level to a non-linear range. In this case the front end bandpass filter has nonlinearity coming from the change in the input dc levels. The nonlinearity is also introduced from the output buffer. In case of PMOS buffer, the ICMR is from 200mV to 800mV. Any shift of DC close the edges will have effect on the THD.

The time domain behavior is shown in Fig. 3.44. We perform a FFT on the time domain signal to see how the received signal appears on the frequency spectrum. After detection, there is still 200kHz carrier is present in the spectrum. As the on-chip CMOS filter does not have enough suppression, we process the data with an ideal RC 2nd order butterworth filter. This places a corner at 20kHz and hence with 20dB per decade suppression, the 200kHz signal is further minimized.

Again the input to the detector is existentially a square pulse. It has a sinc shape response. Now if we change the duty cycle from 50% down to 20%, ideally the output

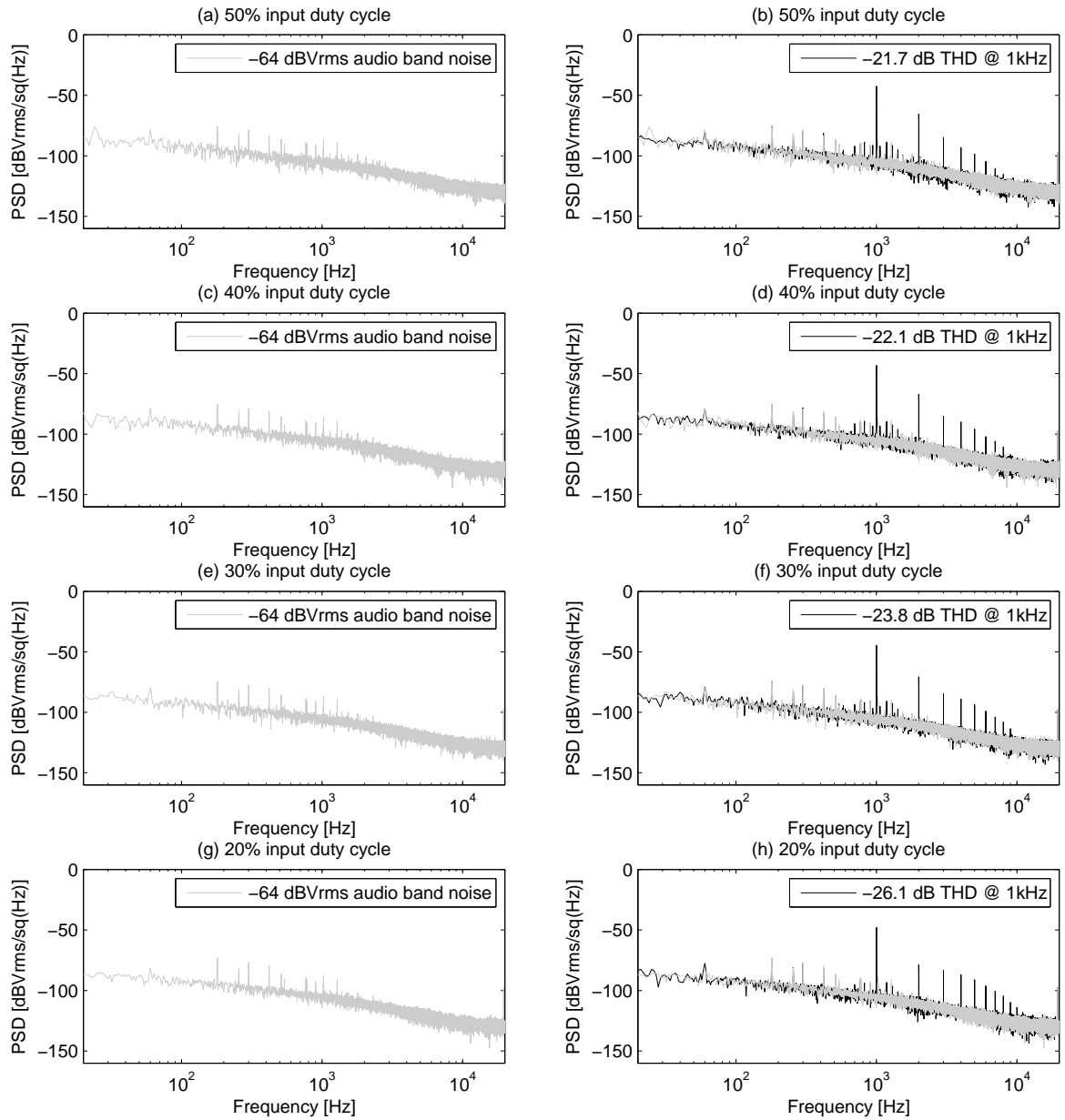


Figure 3.42. Peak detector receiver noise with bandpass filter at various input duty cycles: (a)50% duty cycle noise spectrum. (b)50% duty cycle with 1kHz audio signal spectrum. (c)40% duty cycle noise spectrum. (d)50% duty cycle with 1kHz audio signal spectrum. (e)30% duty cycle noise spectrum. (f)30% duty cycle with 1kHz audio signal spectrum. (g)20% duty cycle noise spectrum. (h)20% duty cycle with 1kHz audio signal spectrum.

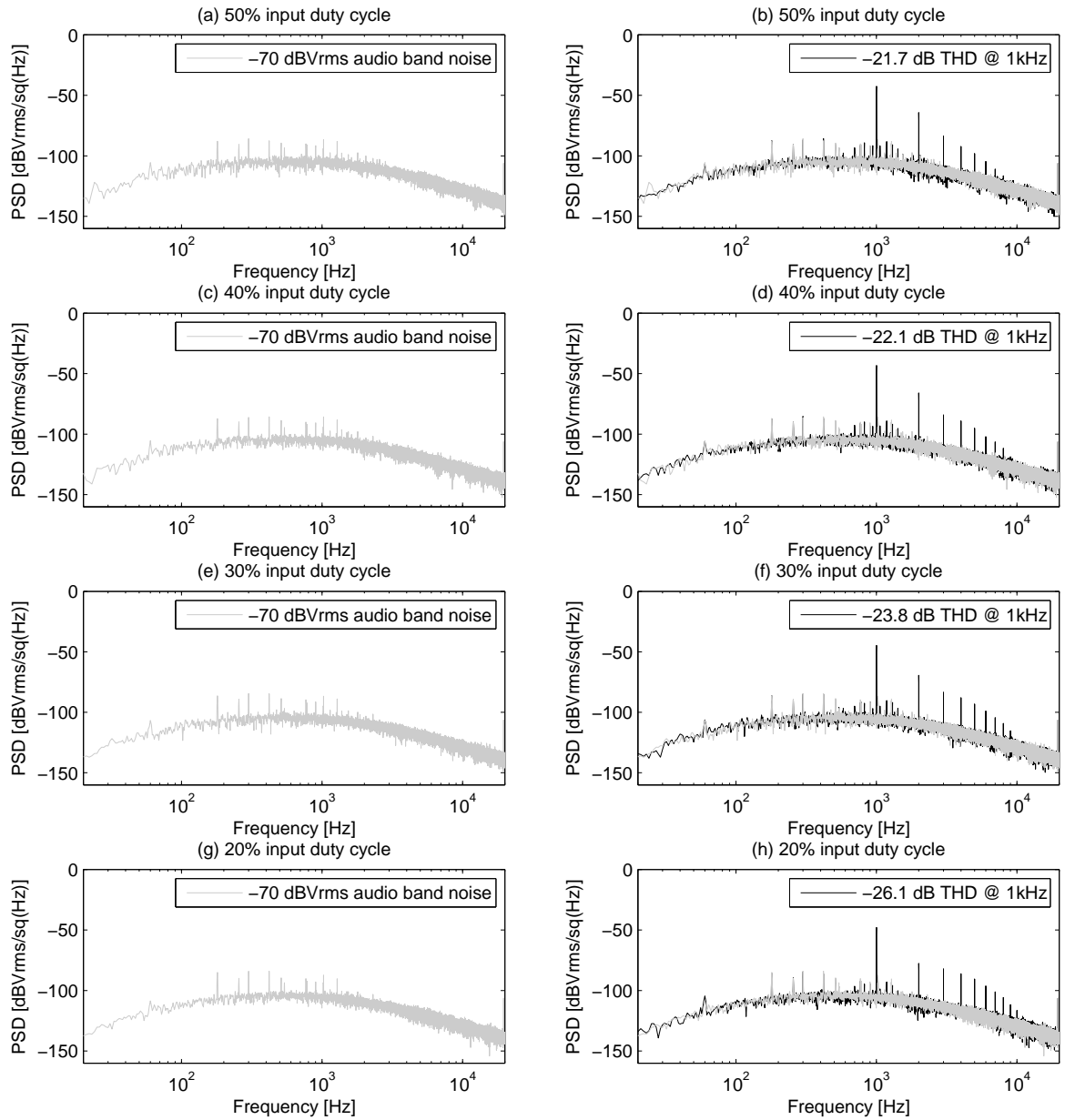


Figure 3.43. Peak detector receiver A-weighted noise with bandpass filter at various input duty cycles:
 (a) 50% duty cycle noise spectrum. (b) 50% duty cycle with 1kHz audio signal spectrum.
 (c) 40% duty cycle noise spectrum. (d) 50% duty cycle with 1kHz audio signal spectrum.
 (e) 30% duty cycle noise spectrum. (f) 30% duty cycle with 1kHz audio signal spectrum.
 (g) 20% duty cycle noise spectrum. (h) 20% duty cycle with 1kHz audio signal spectrum.

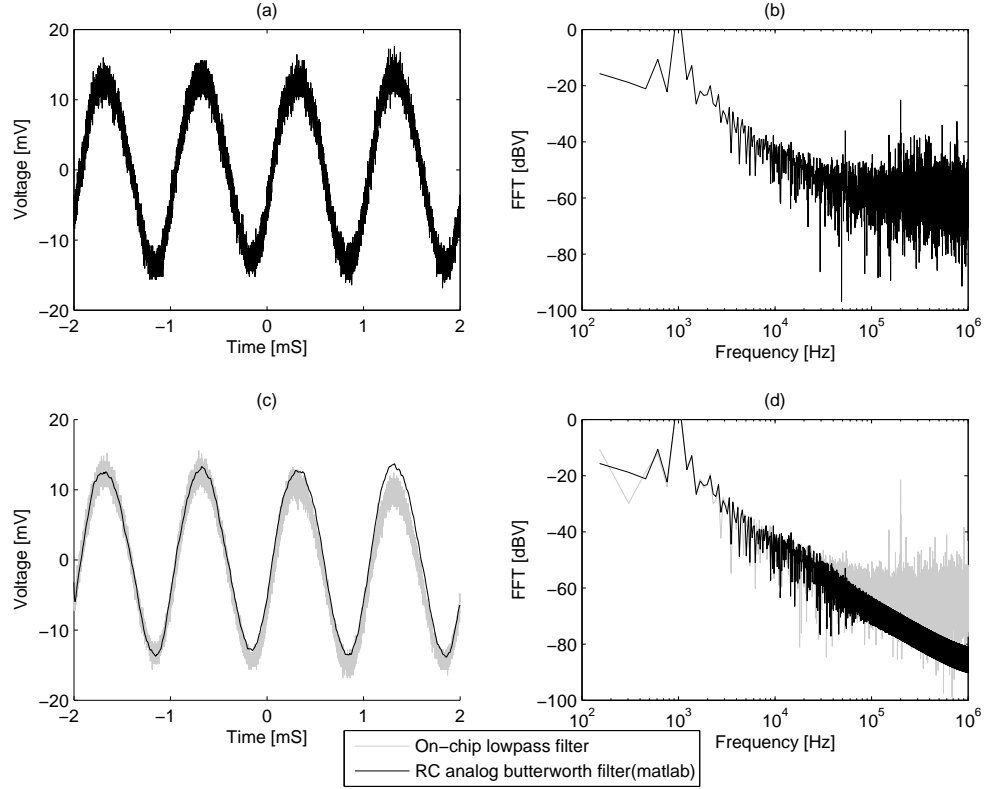


Figure 3.44. Peak detector receiver output with bandpass filter.(a) Output from the detector.(b) FFT of the output from detector. (c) Output after lowpass filter.(d) FFT of the output after lowpass filter.

amplitude for the first lobe of the sinc function goes down. Now more and more energy shifts from the 200kHz band to its harmonics. We notice this behavior in our gain measurements. The gain tends to go down as we change input duty cycle from 50% to 20%. The peak detector demodulation is quite different from track and hold detector. Track and hold basically captures the envelope from the synchronized clock used for the input pulsing. Peak detector on the contrary is designed to capture the envelope of certain frequency without any clock input. This limits the frequency response.

3.7.7 Continuous Mode VCSEL Receiver

Now we discuss the approach of the optical receiver where the VCSEL is kept on all the time unlike pulsed operation. The receiver architecture is quite simple in this case. This is shown in Fig. 3.45. The VCSEL driver gate is set to a fixed dc bias voltage for a pre

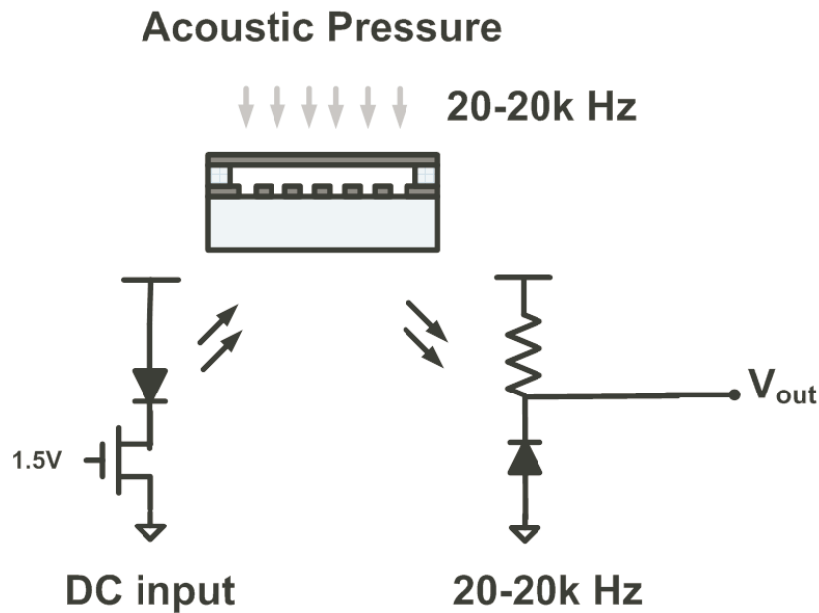


Figure 3.45. Receiver with continuous mode VCSEL input.

determined current levels through VCSEL. For the purpose of better and fair comparison with the pulsed operation, all the operating conditions are kept same in this case too. The average current which is now the dc current in this case is kept above the threshold current of about 3mA and above. The AC signal is feed on the DC bias of the VCSEL driver. The amplitude is kept less than 100mV.

The current to voltage conversion is done with only dc bias power consumption through the front end of the receiver. The dc current is in the range of 50 micro amperes and less. The major contribution for power is now coming from the continuous operation of the VCSEL. As the threshold current is around 3mA, this is the heavy load on the battery for low power microphone application. The noise is shown in Fig. 3.46. Notice that the noise level go higher from the VCSEL relative intensity noise contribution. One of the main advantages here is the linearity of the system. THD is -35dB and better. On the receiver end of the system, the front end is very linear; major source of non-linearity is coming from the PMOS buffer that is used to drive off-chip capacitive load of cables and instruments.

The time domain response is shown in Fig. 3.47. Notice that high frequency noise is very low as compared to pulsed operation. We can use the output buffer to further lower

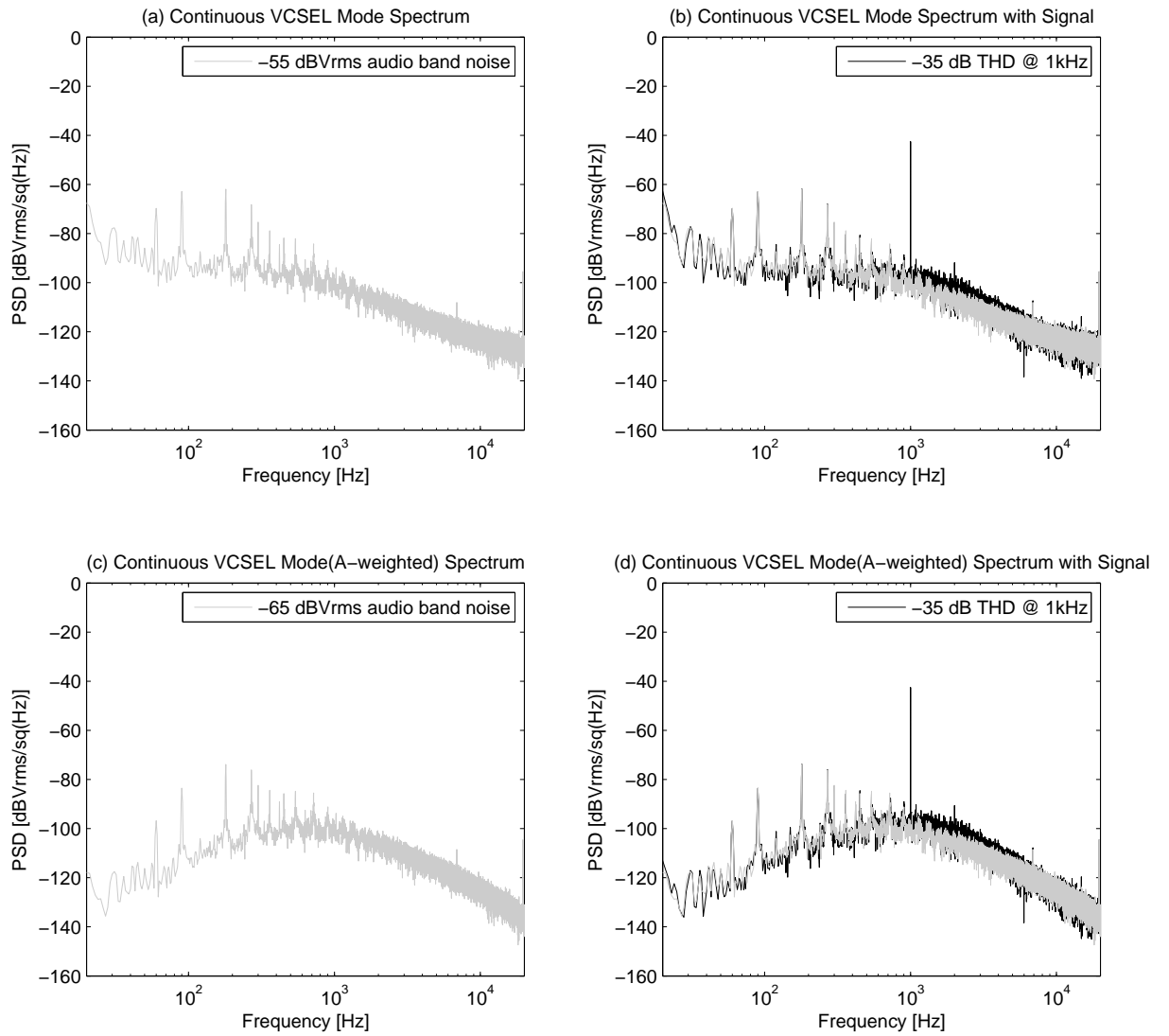


Figure 3.46. Continuous mode receiver noise: (a)Noise spectrum. (b)Noise spectrum with 1kHz audio signal spectrum. (c)A-weighted Noise spectrum. (d)A-weighted Noise spectrum with 1kHz audio signal spectrum.

the frequency corner to save more power. Lowering the current levels can increase the noise levels. Care should be taken for optimizing noise, linearity and power of the receiver blocks.

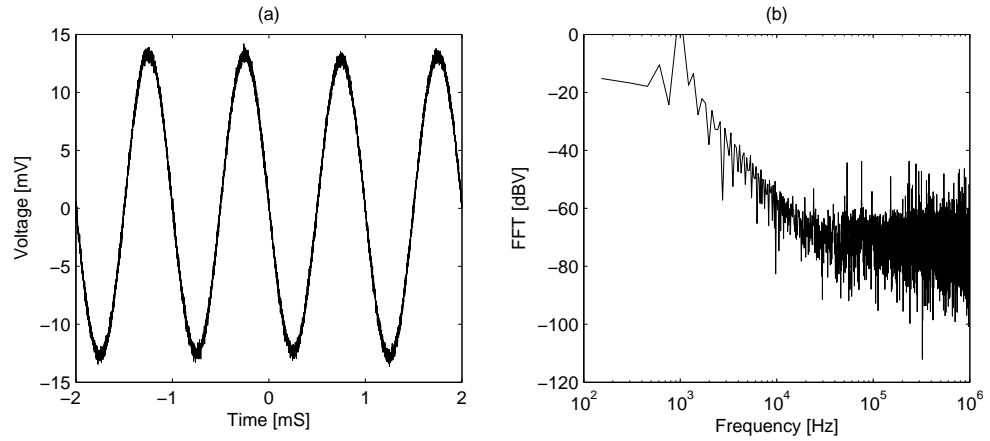


Figure 3.47. Continuous VCSEL mode receiver output.(a) Output from the detector.(b) FFT of the output from detector.

Table 3.5. Measurement results of continuous mode VCSEL receiver

SNR [dB] @ 100mVrms signal	35
A-weighted SNR [dB] @ 100mVrms signal	45
Noise [dBVrms]	-55
A-weighted noise [dBVrms]	-65
THD [dB]	-35
Power [mW]	19.923

3.8 Receiver comparison

In this section we go over the five different topologies discussed earlier individually. Our main basis of comparison is the power consumption and then the SNR for a given power. Let us first look at the more basic comparison between the synchronous and peak detector. The AC frequency response of the modulation input is shown in Fig. 3.48. For the AC comparison, 50% duty cycle at 200kHz pulse and 1kHz modulation is considered.

The response from the continuous mode operation of VCSEL has a flat AC response in the audio band. The main corner that comes is basically from the diode-resistor front end or the output drive buffer, that can be set for a even lower corner for power saving. For the peak detector case, the envelope detection scheme is set to demodulate essentially a desired frequency. The discharge current through the capacitor is set for 1kHz modulation in this case. If the input modulation frequency goes higher, then the peak detector fails to follow

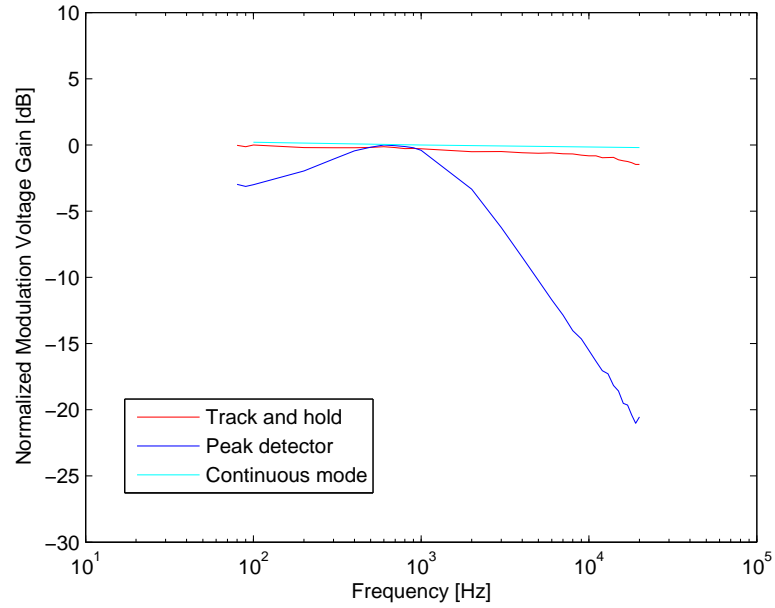


Figure 3.48. AC response of demodulators.

the fast falling modulation on 200kHz pulses. The same is true for lower frequencies as now the peak detector tend to clip the real gain of the output as it has a faster discharge current as compared to what is actually necessary for lower frequency signal detection. Now looking at the response from the track and hold detector, the response nearly flat over the audio frequency band. The track and hold detector is based on phase locking the input with the demodulation clock. With this additional feature, the system follows the input modulation on 200kHz pulse all the way till the corner introduced from the hold amplifier.

Let us look at the noise and SNR first without A-weighting filter. The noise comparison is shown in Fig. 3.49. Notice effect of bandpass filter on the total integrated noise in the audio band. When we introduce a bandpass filter at the front end, the system effectively becomes a chopper amplifier. We are modulating the audio signal on 200kHz pulses. The bandpass filters the low frequency noise in both peak detector and track and hold receiver. The signals are then demodulated and have reduced total integrated noise in the audio frequency band. Introducing a bandpass with track and hold reduces the noise levels significantly as compared to the peak detector as the peak detector already has a bandpass

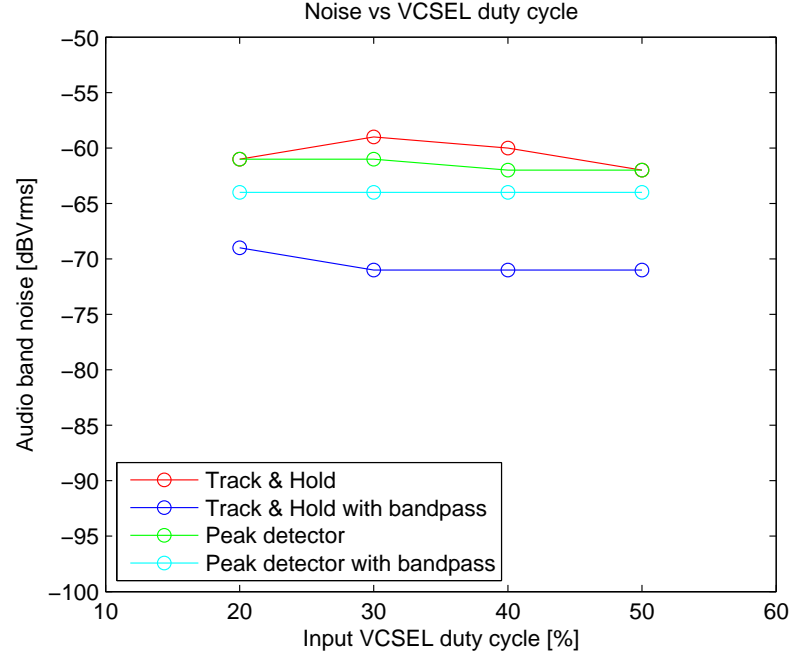


Figure 3.49. Noise reduction with bandpass filter.

shaped response from its structure.

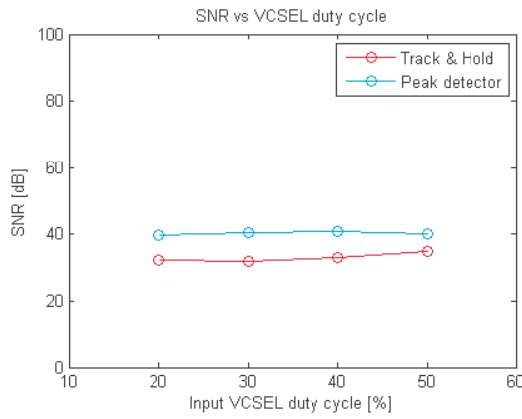
The measurement results from the continuous VCSEL mode receiver are shown in 3.5. The first thing we notice is the power consumption. The VCSEL is burning continuously 6mA of current from a 3.3V supply. That is the most major power hungry part of the receiver. The major benefit that comes with this receiver is the linearity. It is -35dB for the same operating condition of input signal. This linearity goes to -50dB and higher with an optimized signal input and reduced signal amplitude as expected from the optical sensor.

The receiver key parameters are summarized in Table 3.6. The first thing to notice is the fact that just only 17uA of currents in the bandpass filter give 6dB and 3dB SNR improvement. The SNR with the bandpass is better than the one is the continuous time approach. In the continuous time receiver, all the low frequency noise is present, while in our modulated receiver with the bandpass, we reduce low frequency noise.

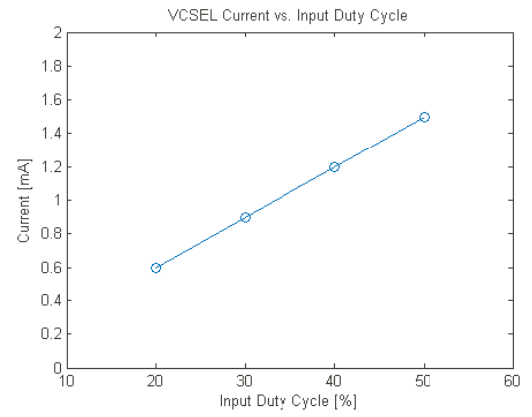
The SNR with input duty cycle is shown in Fig. 3.50(a). As we reduce the input duty cycle, both receivers maintain signal SNR. The demodulators essentially capture the shape of the envelope. That shape remains unchanged with duty cycle as long as our input driver

Table 3.6. Receiver Comparison

	Power [μ A]	Noise [dBV] (Audio band)	SNR [dB] (1kHz @ 100mV)
Cont. Mode	59.06	-55	35
T/H	41.03	-62	34.47
T/H + BP	57.98	-71	39.94
Peak Det.	32.45	-62	37.99
Peak Det. + BP	49.40	-66	40.26



(a)



(b)

Figure 3.50. (a)SNR variation with input duty cycle.(b)VCSEL current consumption with input duty cycle.

has no bandwidth limitations. As shown earlier, the VCSEL driver is tested for at least 17MHz bandwidth. The receiver electronic have fast settling with phase margins more than 60 degrees in each receiver. If we have a square pulse as an input, then we will see the reduction in SNR with duty cycle as the output has a sinc shaped response; but in this case, we have a bandlimited input coming to the demodulator with at least 600kHz corner from the frontend photodiode and resistor.

Now if we look at the THD comparison as shown in Table 3.7, we notice that the continuous mode has the best linearity. First we have to realize that we are using a non-linear MOS switch with AM modulated signal. Ideally, the modulation is supposed to come from sensor. Now at the best we have -35 THD which this limited measurement setup. The

Table 3.7. Total Harmonic Distortion @ 1kHz 100mV input

Continuous mode	-35 dB
Track and hold	-32 dB
Peak detector	-22 dB

Table 3.8. Analog Receiver Comparison

	Knowles	Akustica	This work (T/H+BP)
Supply Voltage [V]	1.5-3.6	1.65-3.6	1.5
Current [μ A]	250	140	57.98
Peak SNR [dB] (1 Pa @ 1kHz)	59	57	64.98*
Type	Omni	Omni	Directional
Directional SNR [dB]*	46	44	64.98

track and hold offer better linearity as compared to the peak detector as it simply holds the envelope value on a capacitor. The peak detector on the other hand is charging and discharging with the input.

As we reduce the input duty, we get benefit in terms of power reduction on the VCSEL side. The current consumption in the pulsed mode VCSEL is shown in 3.50(b). Notice the drop in current as the duty cycle goes down. Now here is the key things to notice between the continuous mode and pulse mode VCSEL receiver. The power goes down at the transmitter by at least 50%. The added electronics consume current less than 60 μ A in each case.

Table 3.8 shows the comparison of this work with commercial analog front ends by Knowles and Akustica. We have picked track and hold receiver with bandpass filter at 50% duty cycle. The SNR values are the maximum values we can achieve ideally with the optical grating microphone. We know the maximum deflection of the sensor along

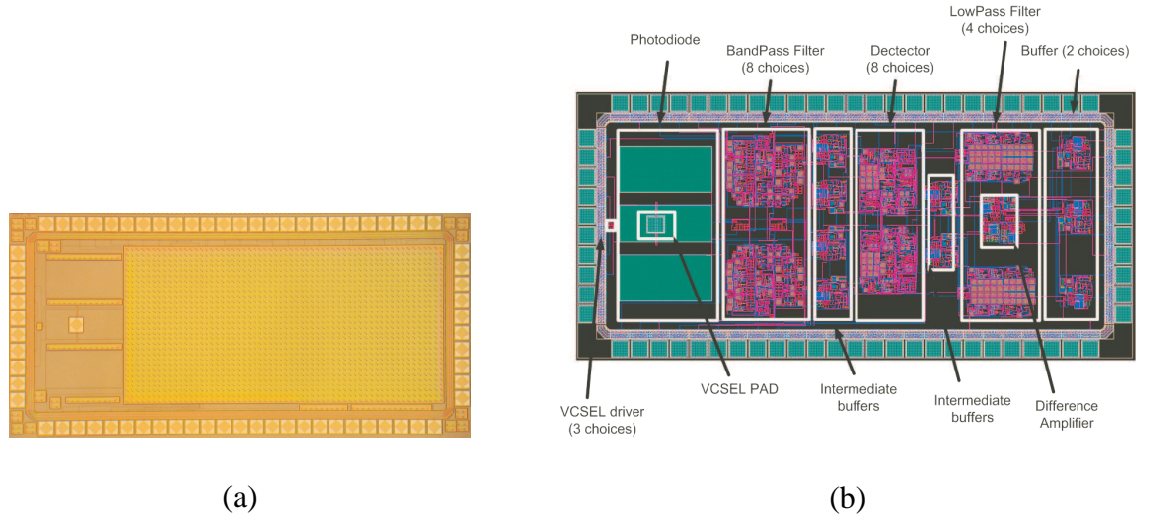


Figure 3.51. (a)Continuous time chip microphotograph.(b)Continuous time chip layout.

with the power on photodiode. Now we know from electrical measurements that the circuits have high linearity and input dynamic range. This gives us 64.98 dB ideal SNR from pulsed mode receiver. In terms of current and SNR, this offer better performance than the commercial analog frontends. Notice that the SNR is for omni-direction microphone for Knowles and Akustica. In our case, the biomimetic optical grating hearing aid is directional by design. If we use two omni microphones to make a directional microphone, typically the SNR degrades by 13dB [33]. The Biomimetic microphone with pulsed mode approach offer exceptional SNR performance for directional hearing aid. Considering the SNR and power, track and hold receiver offer the best choice. The pulse operation adds complexity into the receiver along with chip area. The simplicity of the continuous mode receiver and linearity is desirable in applications where power is not an issue. For low power applications like microphone, pulsed operation offers good SNR for the power consumption.

The continuous time chip is shown in Fig. 3.51. The electronics are shielded with metal layer to prevent optical latch up. The chip area is 1500um by 3000um. The chip offers an integrated approach for the biomimetic microphone electronics in 0.35um standard CMOS process.

CHAPTER 4

DIGITAL FRONT-END FOR BIOMIMETIC MICROPHONE

In a typical hearing aid, the front end preamplifier is the most power intensive block [34]. Figure 4.1 shows the power break down for a typical hearing aid. Notice that 74% of total power is burnt at the front end by the preamplifier and the analog-to-digital converter. The rest of the system has a DSP and then a digital-to-analog converter for the driver of the receive speaker. In the pulsed mode approach of detecting the audio signal, we already have a sampled input. We can use that directly without any preamplifier on the receive side and generate digital bit stream as shown in Fig. 4.2(b).

4.1 Sigma-Delta Analog-to-Digital Converter

A single-bit sigma-delta modulator ADC is chosen because of its inherent linearity, robustness against process deviations, and simplicity. Fig. 4.2(a) shows the block level schematic of the optical front-end with sigma delta. If we want an oversampled data conversion, the sampling frequency should be much higher than nyquist rate to get good resolution. This helps in filtering the output quantization noise that is not in the signal bandwidth and hence, increases the output signal-to-noise ratio. The use of noise shaping places much of the quantization noise outside the input signal's bandwidth. The signal-to-noise ratio (SNR) theoretically improves by 9 dB for each doubling of the oversampling ratio [35]. The use of this shaped quantization noise applied to oversampling signals is commonly

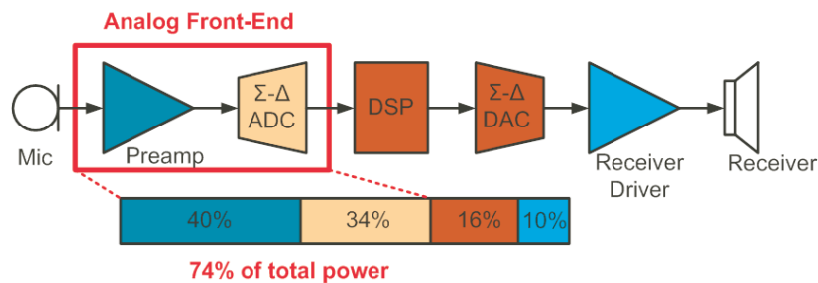


Figure 4.1. Power breakdown of an hearing aid.

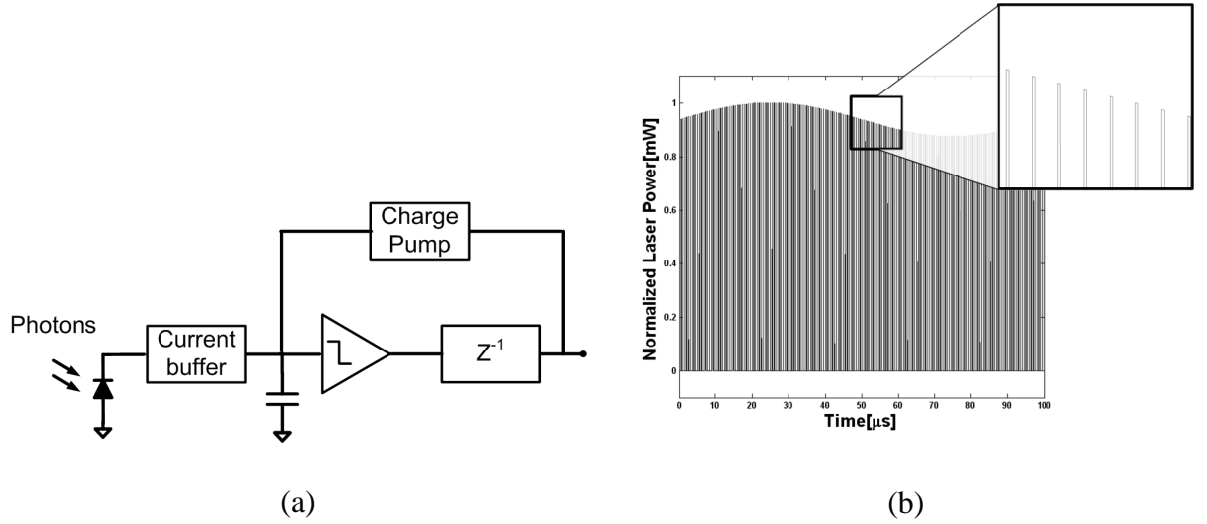


Figure 4.2. (a) System level integration of photodiode and current input sigma-delta.(b) Input PWM signal at the receiver photodiode.

referred to as sigma-delta modulation.

As the photodiodes used here have wide area coverage to capture incident laser from sensor, the capacitance is in the range of couple of pico farads. A current buffer as shown in Fig. ?? is used to isolate this big capacitance of the photodiode from the integrating capacitance of the sigma-delta. The integrating capacitance is much smaller than the junction capacitance, achieving a larger voltage output for the same charge. We have added the capability to digitally control the capacitance for various levels of input current.

4.1.1 First Order 1-bit Sigma-Delta

Fig. 4.4 shows block level architecture of the 1-bit sigma-delta. The circuit mainly consists of three sections: a photodiode and integrator, a one bit A/D converter, and a one bit D/A converter. The photodiode is made from an N-well to P-substrate junction. The photodiode is exposed to the VCSEL light reflected from the diffraction grating based optical displacement sensor, while the rest of the circuitry is covered with metal to reduce the chance of photon induced latch-up. The size of the photodiode was designed to completely capture the laser beam. The duty cycle of the incident VCSEL light is reduced to lower the average

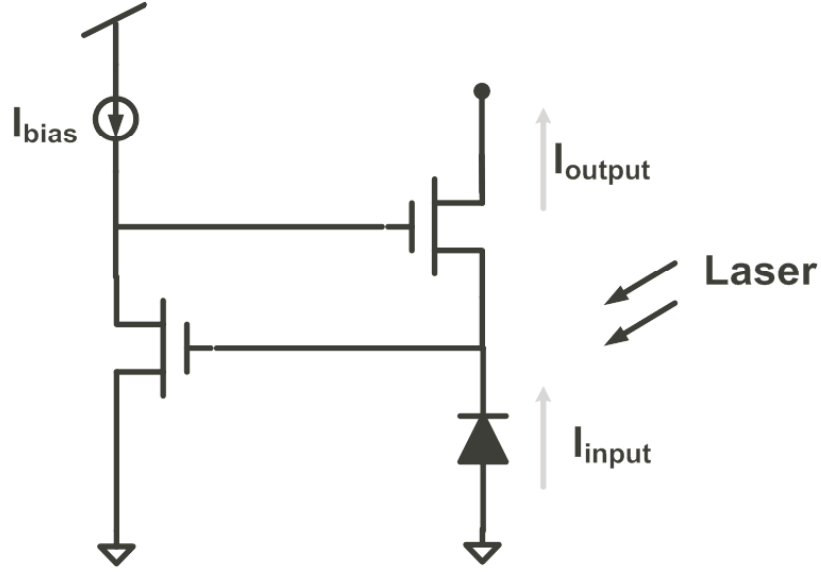


Figure 4.3. Input current buffer for isolating photodiode capacitance from the integrating capacitor.

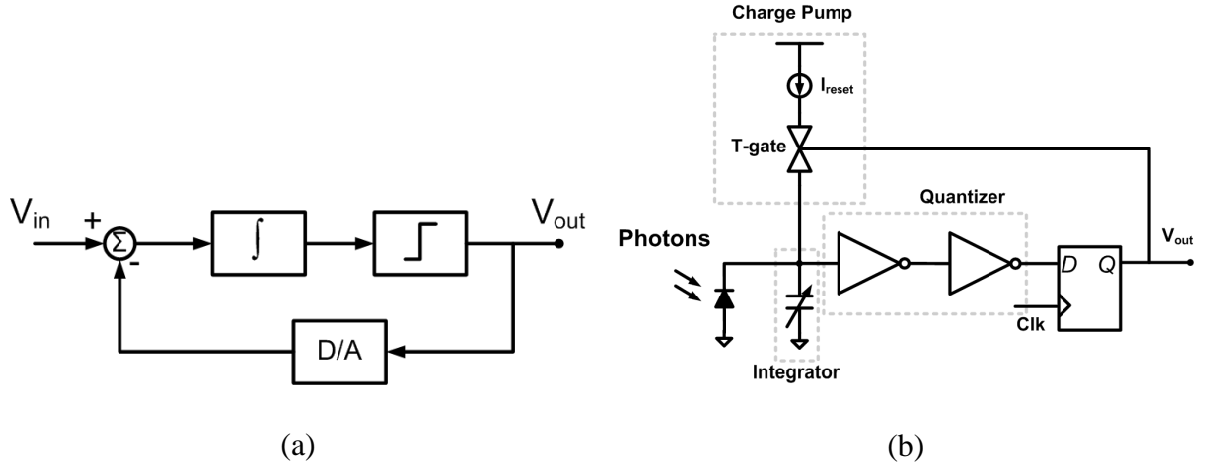


Figure 4.4. (a) System level architecture of 1-bit first order sigma-delta ADC. (b) Circuit level schematic of 1-bit first order sigma-delta ADC.

power consumption and the average photocurrent. This photocurrent is fed to the capacitor which behaves as an integrator. Inverters are used as comparators to mimic two level quantizer. Note that the comparator threshold does not affect the modulator performance [36], and thus the circuit is not sensitive to inverter threshold variations. The output controls the feedback resetting switch which enables a preset bias current into the integrating capacitor. The resulting bit stream along with the integrating voltage is shown in Fig. 4.5. The signal-to-noise ratio is given by

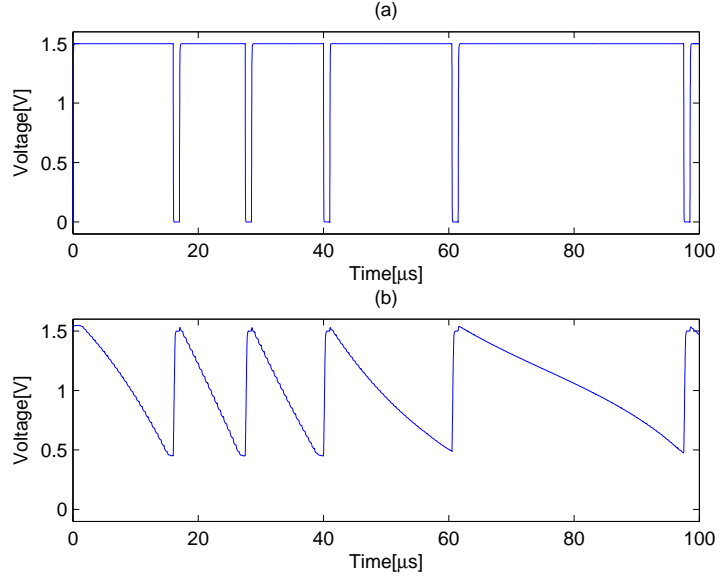


Figure 4.5. (a) Bit stream from 1-bit first order sigma-delta in response to PWM sinusoidal signal. (b) Integrating voltage for 1-bit first order sigma-delta.

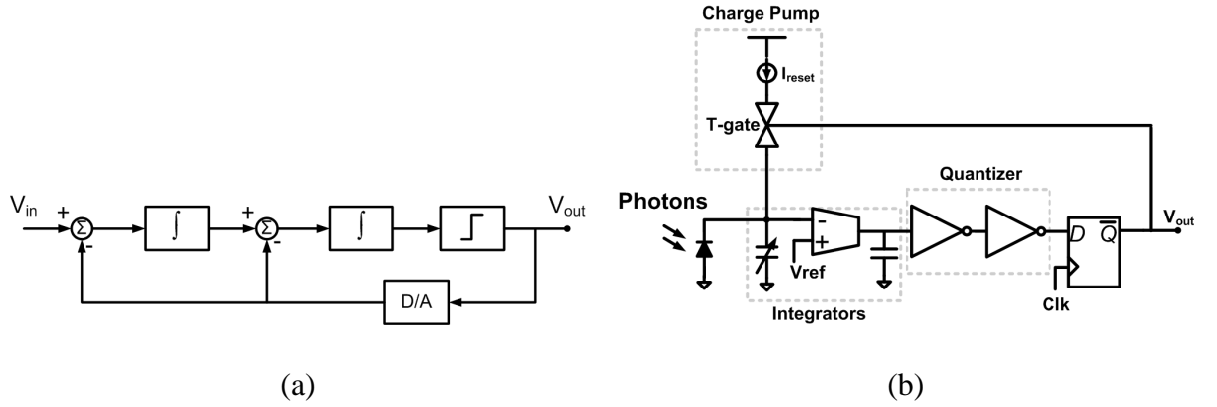


Figure 4.6. (a) System level architecture of 1-bit second order sigma-delta ADC. (b) Circuit level schematic of 1-bit second order sigma-delta ADC.

$$\text{SNR}_{\max} = 6.02N + 1.76 - 5.17 + 30 \cdot \log(\text{OSR}), \quad (4.1)$$

where N is the number of bits for the quantizer and OSR is the oversampling ratio.

4.1.2 Higher Order 1-bit Sigma-Delta

If we use OSR of 64 with the signal frequency of 20kHz as in the audio band, then this sigma-delta will give 9 bits of resolution. A OSR of 64 means sampling frequency of

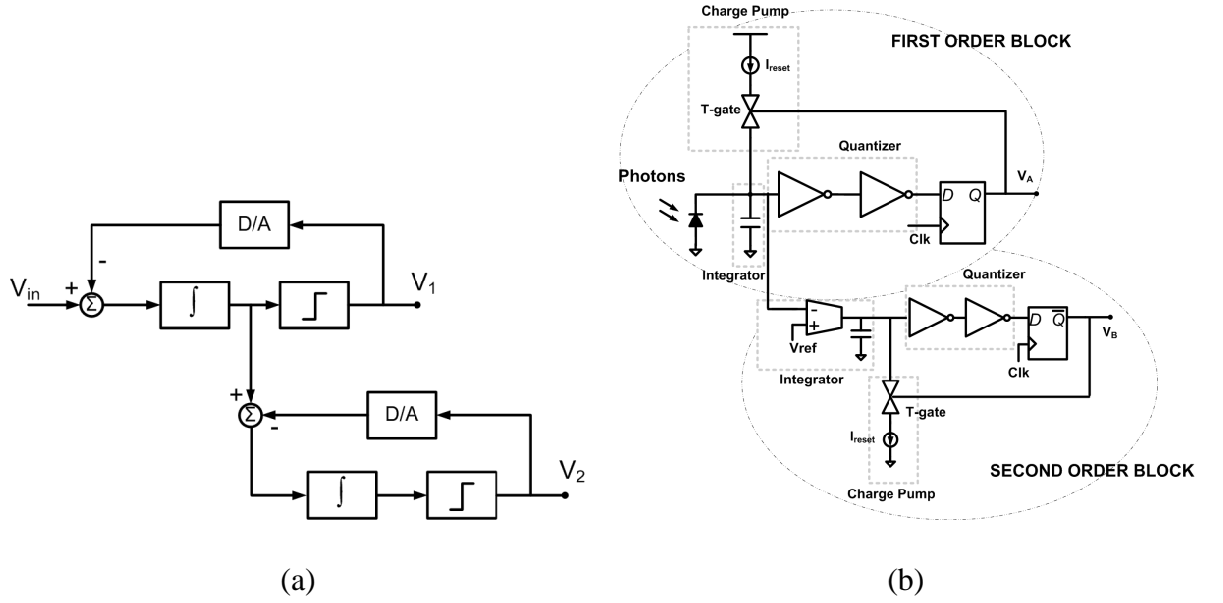


Figure 4.7. (a) System level architecture of 1-bit incremental sigma-delta ADC. (b) Circuit level schematic of 1-bit incremental sigma-delta ADC.

2.56MHz. This sampling frequency requirement can be reduced with higher resulting resolution, if we increase the order of sigma-delta. Fig. 4.6 shows the block level implementations of second order sigma-delta along with the circuit implementation. The second integration is implemented with a transconductor based integrator. The signal-to-noise ratio is given by

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50 \cdot \log(OSR), \quad (4.2)$$

With this implementation we can get a 14 bit resolution with oversampling ratio of 64 and sampling frequency close to 2MHz. The advantage of using second order sigma-delta is evident as resolution increases with lower sampling frequency, for the cost of one additional integrator in terms of power and complexity. One more technique for sigma-delta ADC can be explored as shown in Fig. 4.7. It can provide enough resolutions without the complexity of double integration in a single loop [37].

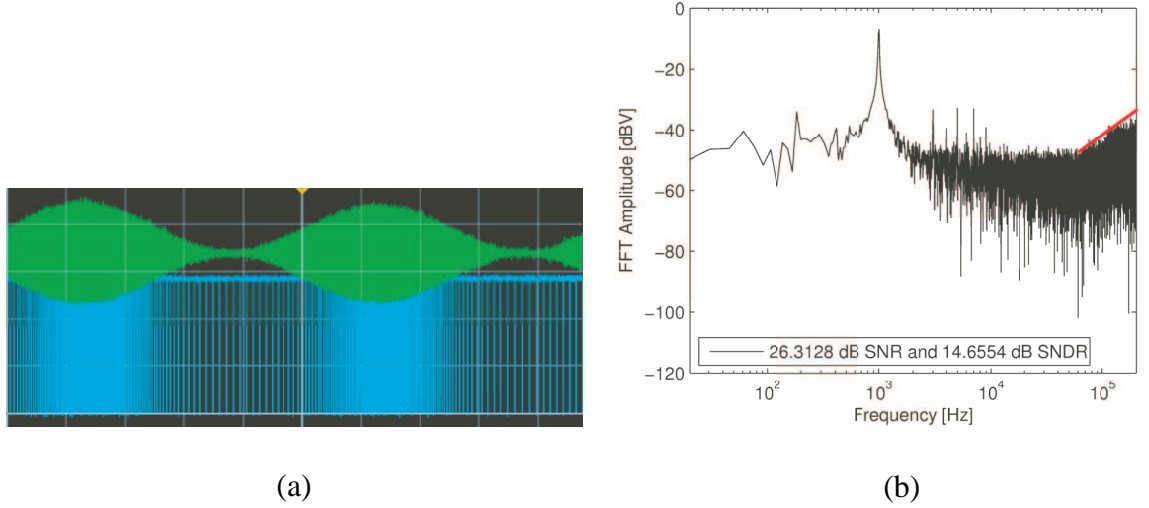


Figure 4.8. (a)Output captured from first order sigma delta converter.(b)FFT of digital bit stream.

4.2 Measurements

The measurement setup is kept same as in the case of continuous time hearing aid electronics. We make use of two chip approach, with the input driver and VCSEL on one chip and the receiver electronics on the second. The input pulses had AM modulation with 1kHz sinusoidal signal. The VCSEL mounted on the transmitter chip is directly inverted over the photodiodes on the second CMOS chip. The digital bit stream from the first order 1-bit sigma delta is shown in Fig. 4.8(a).

Figure 4.8(b) shows the frequency spectrum of the digital bit stream from sigma delta converter. The measured SNR is 26.3dB. That corresponds to 4 bits of resolution as compared to 9 bit of theoretical resolution. The SNDR is 14.6dB which is lower than SNR. Notice the harmonics that appear in the spectrum. The input pulse with AM 1kHz input signal is coming from a single transistor as a VCSEL driver. Remember that the transistor is a non-linear element. If we use it for AM 1kHz signal, then we will have very strong non-linearity coming into the receiver side of sigma delta. The systems is designed to be used with a MEMS optical microphone, in which case, the VCSEL driver transistor will not be used for AM signal. The acoustic signal on the MEMS microphone will modulate the input incident pulse.

Table 4.1. Digital Hearing Aid Comparison

	JSSC 1997 [38]	JSSC 2002 [39]	JSSC 2006 [40]	Knowles	Akustica	This work
Supply [V]	2.15	1.1	0.9	1.6-3.6	1.8-3.6	1.5
Current [μ A]	150.1	172.7	66	600	-	62.8*
Peak SNR [dB] @ 1kHz	77	92	86	56 (1Pa)	56 (1Pa)	62.52** (1Pa)
Technology	0.8 μ m CMOS	0.6 μ m CMOS	0.25 μ m CMOS	-	-	0.35 μ m CMOS
Integration	ADC	ADC	ADC	Frontend +ADC	Frontend +ADC	Frontend +ADC

There are mainly two reasons for reduced resolution in this measurement setup. First we are limited with our setup with the maximum input we can apply on the VCSEL driver. As the input has AM modulation on the input pulse, the signal generator has top and bottom envelopes. In order to keep the input above the ground and keeping the bottom envelope not turning on the VCSEL driver, we have to limit the amplitude that we can place on the input pulse to about 100mV. Now this limit reduces the maximum SNR that we can achieve in this current measurement setup. The second issue is with the input buffer. Remember that we are using the buffer to isolate the huge photodiode capacitance from the integrating capacitor of the sigma delta. Now if we increase the gain of the loop by pushing more current into the buffer, the output transistor will be forced out of saturation and will hinder the next stage of sigma delta inverters. In order to keep the sigma delta in operation, we were forced to reduced the current into the buffer. As the current was reduced, the current noise increased significantly and reduced the overall sigma delta resolution.

4.3 Comparison

The layout and the microphotograph of the sigma delta chip is shown in Fig. 4.9. The electronics are shielded with metal to avoid optical latch up. There are two channel for capturing the two orders from the optical grating. The chip area is 1450 μ m by 1450 μ m. The

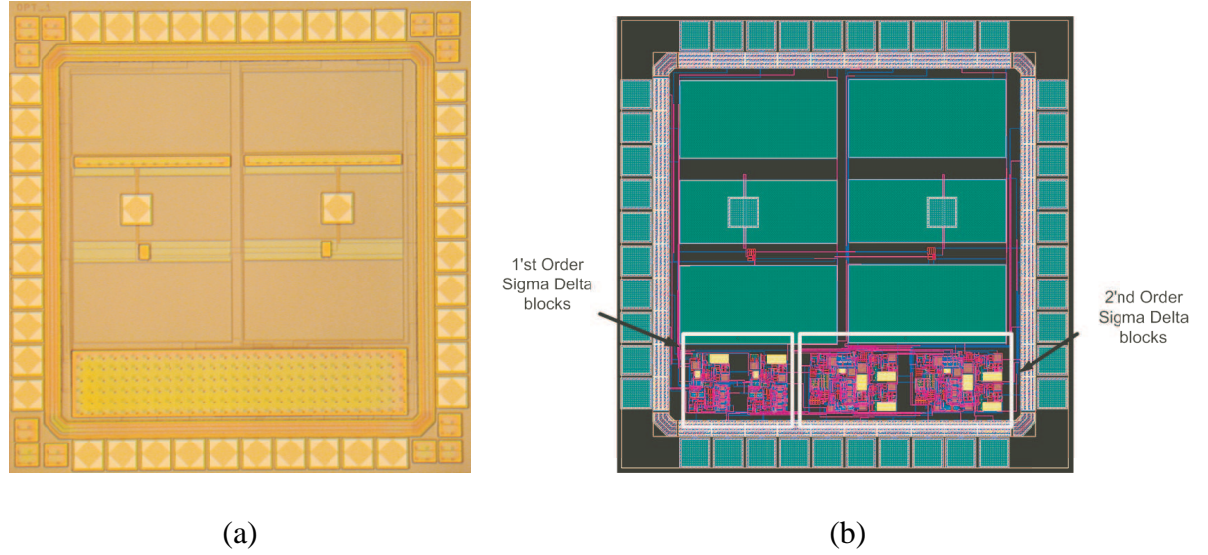


Figure 4.9. (a)Sigma delta chip microphotograph with shielded electronics.(b)Sigma delta chip layout.

actual electronics take very small area. The photodiodes are designed to capture maximum optical input.

In this work, we have presented an integrated digital frontend for the biomimetic hearing aid. A comparison with some recent work in JSSC and also from industry is shown in Table 4.1. Mostly the hearing aids are designed for 1.5 volts of battery. This work shows a very close and even better performance in terms of power and SNR. The SNR value is for the ideal case where we are operating at the maximum on the optical intensity curve. This approach has an integrated frontend as we go directly into digital bit stream and avoiding the frontend preamplifier. The sample signal at the input is directly feed into the current mode sigma delta ADC via photodiode. As the preamplifier is not present in out approach, we offer a more efficient integrated digital frontend for the optical hearing aid.

CHAPTER 5

CONCLUSION

The main goal of this research was to develop and design front-end analog circuits for Capacitive Micromachined Ultrasound Transducers (CMUTs) and optical grating MEMS microphone. This work was motivated by the fact that with micro-scaling, MEMS sense capacitance gets smaller in a CMUT array element for intravascular ultrasound imaging, which has dimensions of 70um x 70um and sub pico-farad capacitance. Smaller sensors lead to a lower active-to-parasitic ratio and thus, degrades sensitivity. Area and power requirements are also very stringent, such as the case of intravascular catheter implementations with CMOS-First CMUT fabrication approach. In order to resolve these issues, we implemented capacitive feedback charge amplifier as an alternative approach to resistive feedback amplifier. Capacitive feedback charge amplifier provides high sensitivity, small area, low distortion and saving power. This approach of charge amplifiers is also suitable in capacitive microphones where it provides low power and high sensitivity.

Another approach to overcome capacitive detection challenges is to implement optical detection. In the case of biomimetic microphone structure, optical detection overcomes capacitive detections thermal noise issues. Also with micro-scaling, optical detection overcomes the increased parasitics without any sensitivity degradation, unlike capacitive detection. For hearing aids, along with sensitivity, battery life is another challenge. We propose the use of 1-bit front-end sigma-delta ADC for overall improved hearing aid power efficiency. Front-end interface based on envelope detection and synchronous detection schemes have also been designed and tested. These interface circuits consume currents in micro-ampere range from a 1.5V battery. Circuit techniques are used for maximizing linear range and signal handling with low supplies. The entire front end signal processing with Vertical Cavity Surface Emitting Laser (VCSEL) drivers, photodiodes, filters and

detectors is implemented on a single chip in 0.35 μ m CMOS process. The core electronics operate from moderate to weak inversion for maximum current efficiency and hence prolonged battery life for bio-medical applications.

5.1 Main Contributions

A low-power approach to capacitive sensing that can achieve a high signal-to-noise ratio has been designed, and tested. The circuit is composed of a capacitive feedback charge amplifier and a charge adaptation circuit. The charge amplifier only consumes 1 μ W and achieves an SNR of 69.34 dB in the audio band. This capacitive feedback charge amplifier also has been used as a receiver circuit for a capacitive micromachined ultrasonic transducer that is designed for forward-looking intravascular ultrasound imaging applications. Compared with conventional approaches, using a charge amplifier to detect capacitance variation avoids the dilemma of sensitivity-bandwidth tradeoff. Pulseecho experiments have been performed in an oil bath using a planar target 3 mm away from the array. The measurement results show a signal-to-noise ratio of 16.65 dB with 122 μ W power consumption around 3M Hz.

Analog front-end low power electronics for biomimetic microphone is integrated on a single chip in 0.35 μ m standard CMOS process. The chip has VCSEL driver, photodiode and receiver electronics all on 1500 μ m by 3000 μ m chip area. We show pulsed mode operation with less than 60 μ A current in the receiver electronics without degrading SNR. A chopped implementation shows better SNR as compared to the continuous mode approach. We can achieve ideally 65dB SNR(1Pa @ 1kHz) that is 20dB better for the direction microphones built by commercial omni-microphones. The electronics are designed with reduced supply of 1.5V in 3.3V process. Wide linear range techniques with dual complementary inputs and pseudo-BJT MOS resistors keep THD levels to -60 dB and better. We have showed integrated approach with low power and low voltage for the biomimetic directional microphone. A power efficient digital front-end is also shown for the biomimetic

directional microphone. We achieve ideally 65.5dB SNR with only 62.8uA of current consumption. We show a direct current mode sigma delta with out the need of any frontend pre-amplifier on 1500um x 1500um 0.35um CMOS. The biomimetic microphone with the digital front end surpasses current state of art in directional microphones.

5.2 Future Directions

The CMOS photodiode responsivity can be improved from 0.1 A/W to as high as 0.5 A/W, by making use of CMOS process for optical applications. The deeper junction depth increase the photon absorption and hence increase the photodiode responsivity. This directly makes the biomimetic optical grating microphone more power efficient, as the input VCSEL power can be reduced.

The optical measurements were limited by the input of the VCSEL driver as AM signal was added on the input pulse at the driver side. Non-linearity of the single transistor and the limited AM amplitude can be overcome by integrating a biomimetic microphone with the CMOS chip. This will also reduce the non-linearities observed in the direct digital ADC approach for the biomimetic microphone. The input buffer for the ADC can be replaced with a single common gate transistor without hindering the switching of next stage inverters as shown in Fig. 5.1. This will improve the achievable resolution of the converter.

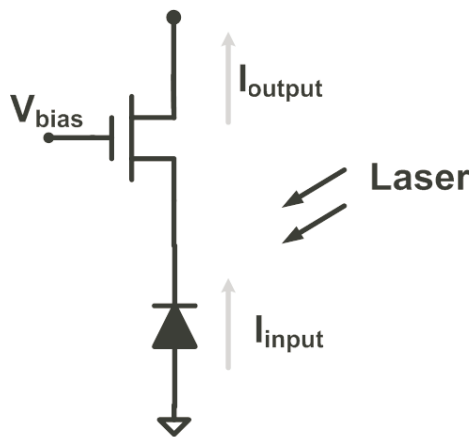


Figure 5.1. Simplified input current buffer.

APPENDIX A

LIST OF ICS FOR CMOS-FIRST CMUT INTEGRATION

The following is the list of chips submitted to the TSMC 0.35um process for CMOS-FIRST MEMS CMUT integration.

Dual Ring Chips (Circular)	
Chip ID	Description
DR2	3mm x 3mm, 64Rx & 48Tx CMUT, transimpedance amplifier
DR3	3mm x 3mm, 64Rx & 48Tx CMUT, charge amplifier
DR4	2mm x 2mm, 32Rx & 24Tx CMUT, transimpedance amplifier
DR5	2mm x 2mm, 32Rx & 24Tx CMUT, charge amplifier
Dual Ring Chips (Square)	
Chip ID	Description
DREL3	3mm x 3mm, 64Rx & 48Tx CMUT, transimpedance amplifier
DREL4	3mm x 3mm, 64Rx & 48Tx CMUT, charge amplifier
P1	2mm x 2mm, 32Rx & 24Tx CMUT, transimpedance amplifier with Pulser
P2	2mm x 2mm, 32Rx & 24Tx CMUT, charge amplifier with Pulser
Annular Array Chips	
Chip ID	Description
AA1	1mm x 1.75mm, 8-element CMUT, transimpedance amplifier and TR switch
AAC1	3mm x 3mm, 8-element CMUT, charge amplifier
AADE2	2mm x 2mm, 16-element CMUT, transimpedance amplifier
AADE3	2mm x 2mm, 16-element CMUT, charge amplifier
P3	2mm x 2mm, 16-element CMUT, Amplifier combo with TR switch
Linear Array Chips	
Chip ID	Description
ICEDE2	2.7mm x 6mm, 64-element CMUT, Amplifier combo with TR switch

APPENDIX B

LIST OF ICS FOR OPTICAL GRATING MICROPHONE

The following is the list of chips submitted to the TSMC 0.35um process for optical grating based microphone.

Optical Grating Microphone Chips	
Chip ID	Description
IC_OPT1	Sigma delta 1 & 2 w/PD
IC_OPT2	Sigma delta incremental w/PD
IC_OPT3	Optical universal RX w/PD
IC_OPT4	Hobbs & force feedback
IC_OPT5	Audio charge amplifier, hobbs, force feedback
IC_OPT6	Sigma delta 1 & 2 w/o PD
IC_OPT7	Optimal RX blocks w/PD
IC_OPT8	Optimal RX blocks w/o PD
IC_OPT9	Optical universal RX w/o PD
IC_OPT10	Stand alone RX blocks sigma delta incremental w/o PD

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