DIGITALLY-ASSISTED, EFFICIENCY ENHANCED, LINEAR RF POWER AMPLIFIER ARCHITECTURES

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Mir Masood

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DIGITALLY-ASSISTED, EFFICIENCY ENHANCED, LINEAR RF POWER AMPLIFIER ARCHITECTURES

Approved by:

Dr. J. Stevenson Kenney, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. P. Douglas Yoder
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. David V. Anderson
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Adeel Khalid
School of Mechanical Engineering
Kennesaw State University

Dr. Azadeh Ansari
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: January 9, 2018

To my parents, and family

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LIST OF SYMBOLS AND ABBREVIATIONS

2G	second generation
3G	third generation
ACLR	adjacent channel leakage ratio
ACPR	adjacent channel power ratio
AM	amplitude modulation
AM-AM	amplitude to amplitude modulation
AM-PM	amplitude to phase modulation
BW	bandwidth
CCDF	complementary cumulative distribution function
dB	decibel
dBc	decibel relative to a carrier level
DPD	digital predistortion
CFR	crest factor reduction
CT	cross-terms

DPD	digital predistortion
EER	envelope elimination and restoration
ET	envelope tracking
EVM	error vector magnitude
FIR	finite impulse response
GHz	giga hertz
Hz	hertz
IBW	instantaneous bandwidth
IIR	infinite impulse response
IMD	intermodulation distortion
LINC	linear amplification with non-linear components
LS	least squares
LUT	look-up table
LTE	long term evolution
MHz	mega hertz
NMSE	normalized mean square error

MP	memory polynomial
MT	memory terms
OBO	output back-off
OFDM	orthogonal frequency division multiplexing
PA	power amplifier
PAR	peak-to-average ratio
PAPR	peak-to-average power ratio
PM	phase modulation
PV	pruned Volterra
QWT	quarter wavelength transformer
RF	radio frequency
VSWR	voltage standing wave ratio
WCDMA	wideband code division multiple access
WLAN	wireless local area network
Wi-Fi	wireless fidelity

SUMMARY

The objective of this research is to use the advanced digital techniques in the development of efficiency enhanced, linearized power amplifier (PA) architectures. The adoption of modern spectrum efficient modulation schemes with high peak-to-average power (PAPR) ratio, constrain the radio frequency (RF) PAs to be operated at higher back-off levels where the efficiency of the PA is low. Therefore, it is desirable to develop the new PA architectures that are efficient and linearizable at the average power levels, operating at back-off from the peak power.

In this research, digital enhancements are used to boost the efficiency of the dual-input Doherty PA. It is shown that the improved phase adjustment and the waveform conditioning for the Auxiliary PA, results in significant improvement in the efficiency of the Doherty PA. This efficiency improvement comes at the cost of degradation in linearity. The conventional digital predistortion (DPD) scheme is found inadequate to linearize the modified Doherty PA in high efficiency mode, when the digital enhancements are applied.

A new segmented DPD architecture is proposed which subdivides the complete dynamic range of the Doherty PA into two power regions, a lower and a higher power region. As the nature of non-linearities exhibited by the Doherty PA are different in these distinct regions, the segmented DPD architecture is found suitable in this scenario. It is shown that by using the segmented DPD architecture, linearity requirements are easily met.

CHAPTER 1. INTRODUCTION

1.1 Motivation

The objective of the proposed research is to investigate new architectures that enable highly efficient, linear operation of the power amplifiers (PAs) in modern wireless communication systems. The ever-growing demand for higher data rates and exponential growth in wireless subscribers has led to the widespread use of spectrum-efficient 3G/4G modulation schemes. These modern complex modulation schemes with a high peak to average power ratio (PAPR) have constrained the radio-frequency (RF) power amplifiers to operate at a significant back-off from the peak saturated power, where the efficiency of the PA is low. Hence, a growing need to explore new linear PA architectures that can achieve higher efficiency when operated at back-off level exists, as PAs with higher efficiency can result in extended battery life in the handset applications and savings in energy costs for the infrastructure applications.

For RF circuit designers, the efficiency versus linearity trade-off is one of the most critical design considerations. The Doherty amplifier architecture is a widely adopted technique [1], especially for the infrastructure applications, because of its simple structure, linearizability, and higher efficiency at average output power levels. The Doherty amplifier in its simpler form is composed of two cells, the main amplifier and the auxiliary amplifier. The main PA is typically biased to operate in Class-AB mode and the auxiliary PA is typically biased to operate in Class-C mode. Using an analog power splitter and a quarter wavelength transmission line, the input RF power is divided into two paths that are separated 90^{o} in phase. The output of the main and auxiliary PA cells is combined using a

quarter wavelength transformer (QWT) by employing a technique called load modulation. In Doherty amplifier technique, the main PA is operating all the time whereas the auxiliary PA is only operating at higher output levels. This technique helps to maintain the higher efficiency throughout the upper 6-dB (typical design parameter) range of operation.

Even though the Doherty PA offers superior performance when compared to the contemporary techniques (such as the envelope-tracking and outphasing PAs etc.); it still suffers from certain performance degradations which are the topic of this thesis. For the ideal power combination, the outputs of the main and the peaking PAs must be perfectly aligned in-phase at all output power levels throughout the frequency band of operation. The auxiliary PA biased in Class-C mode exhibits a large power dependent phase variation (AM/PM distortion) which results in compromising the ideal load-modulation of QWT. Moreover, narrow bandwidth nature of QWT limits the use of the Doherty PA for a wide range of frequency of operation. Unequal power contribution from the main and auxiliary PAs at peak output levels is another issue, which degrades the efficiency in the upper range of the Doherty operation. This unequal power contribution is a result of different biasing schemes of the two PA cells.

This work presents a new modified Doherty PA architecture that uses the digital signal processing techniques to mitigate some of these performance degradations. Instead of using an analog/RF power splitter, a digital power divider is used which provides separate RF inputs for the main and auxiliary PA cells. During the lower range of the Doherty operation, the wasted power input to the auxiliary path can be reduced when the auxiliary PA is not operating. These efficiency enhancement techniques are only useful if the modified Doherty PA is linearizable. The conventional DPD architectures, using single

DPD actuator for the entire dynamic range of operation, significantly suffers by the degradation in performance. The dual-segmented DPD architecture is developed, which uses a separate DPD actuator for the lower range of the PA operation when only the main PA is operating, and the upper range of the PA operation where both the main and the auxiliary PA cells are operating.

Accurate estimation of the PA's non-linear behavior is important in the identification of an effective linearity technique. Another aspect of this research focuses on the development of behavioral models that best describe the mathematical relationship between the input and output of the PA. For the handset applications, a novel modeling technique is developed which uses polynomials along with the infinite impulse response (IIR) basis functions. The non-linearity of the PA is described by the memoryless polynomial component, whereas the IIR basis function proved useful in modeling of the short-term and long-term memory effects of the PA with reduced number of coefficients. For modeling of high-power infrastructure PAs, a new modeling technique is developed where a parallel structure of the IIR basis functions is combined with the pruned Volterra (PV) kernels (new technique called IIR-PV). The characterization of high power class-AB and Doherty PAs validated that the IIR-PV offers superior modeling performance when compared with the contemporary techniques such as Memory Polynomial (MP) or pruned Volterra schemes (PV) of similar complexity.

1.2 Organization of thesis

The thesis is organized as follows.

- Chapter 2 discusses the nature of the non-linearities and memory effects of the PAs. In addition, different PA behavioral modeling schemes are discussed and compared to model the in-band and out-of-band PA non-idealities. This chapter ends with the discussion of contributions of this research towards the behavioral modeling of the PAs.
- Chapter 3 starts with providing an overview of various PA linearization techniques with summary of the pros and cons of various approaches. The digital pre-distortion (DPD) scheme is discussed in more detail. An overview of indirect and direct learning architectures, for calculation of DPD parameters, is also provided.
- Chapter 4 starts with a brief overview of PA efficiency enhancement technique that exist in literature. The Doherty PA architecture is covered in detail. Its basic operation, behavioral modeling and linearity considerations are discussed.
- Chapter 5 presents the architecture of the proposed digitally-assisted, efficiency enhanced, linearized Doherty PA architecture. Efficiency enhancement techniques are presented. In addition, a novel segmented DPD architecture is discussed which is used to linearize the modified Doherty PA. This chapter also summarizes the hardware measurements used to validate the improvements claimed in the proposed architecture.
- Chapter 6 summarizes the conclusions and contributions achieved. Potential areas for the extension of this research are also highlighted.

CHAPTER 2. BEHAVIORAL MODELING OF RF POWER AMPLIFIERS

Power amplifiers are inherently non-linear and they exhibit strong memory effects. Accurate modeling of these non-idealities, is essential in the identification of an optimum linearization technique. In this chapter, few popular behavioral modeling schemes are discussed that exist in the literature. In last subsection, contributions of this research in the development of new PA behavioral modeling schemes, are summarized.

2.1 PA Non-linearities and Memory Effects

The static or memory-less non-linearities of the PA can be modeled by using a polynomial expression [2] shown in (2.1).

$$y = \sum_{n=0}^{\infty} (g_n |x|^n)\, x \tag{2.1}$$

Where, x and y represent the discrete time-samples of the input and output complex envelope voltages, and g_n are the non-linearity coefficients of the series. The even order terms in (2.1) are responsible for introducing the spurious frequency components at the harmonics of the carrier frequency. Odd-order terms in (2.1) are responsible for generating the inter-modulation products (IMDs) that are present close to the desired signal.

The dependency of the output signal on the past samples of the input signal along with the current sample is known as the memory effect. The sources of memory effects in the PA are illustrated in Figure 2-1. These memory effects can be classified as linear or non-linear. Linear memory effects arise from the frequency response caused by the

matching networks. The cause of the non-linear memory effects can be attributed to the non-linear bias networks, thermal feedback, and traps. The memory effect in the PA can be of a short-term or a long-term [3,4] nature. The bias networks, thermal time constants, and trapping effects are attributed to the long-term memory effects, whereas, the matching networks are responsible for the presence of the short-term memory effects.

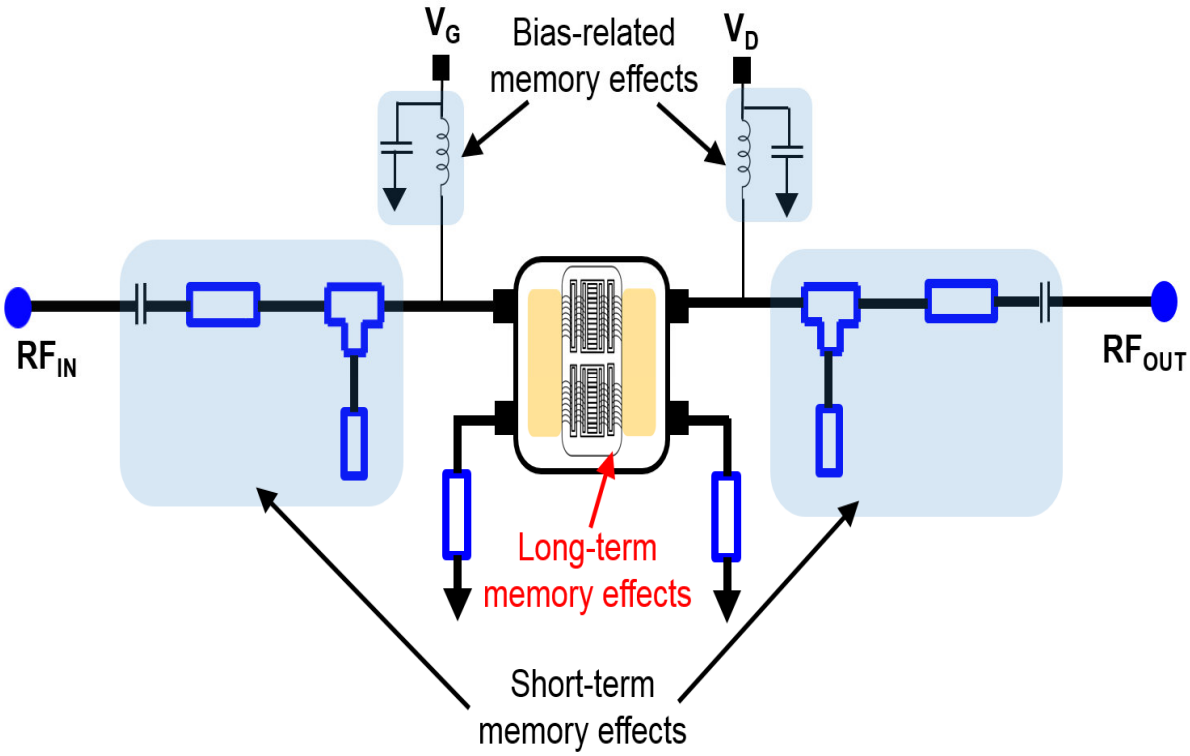

Figure 2-1 - Source of memory effects in the PAs

2.2 PA behavioral modeling architectures

The behavioral models, also characterized as the black-box models, describe the non-linearities and the memory effects of the PA without going into the circuit-level details.

Fundamentally, the extraction of behavioral-model parameters is a nonlinear system-identification problem. Therefore, the behavioral modeling has been studied in different disciplines as nonlinear regression and spline approximation.

The Volterra series [5], which is widely used for PA modeling, is a summation of multidimensional convolutions. Mathematical representation of Volterra series in general form is described in (2.2).

$$V_{out}(k) = \sum_{p=1}^{P} \sum_{i_1=0}^{M} \dots \sum_{i_p=0}^{M} h_p(i_1, i_2, \dots i_p) \prod_{j=1}^{P} V_{in}(k - i_j) \tag{2.2}$$

where, $h_p(i_1,i_2,\dots,i_p)$ is the p^{th}-order Volterra kernel. $V_{in}(k)$ and $V_{out}(k)$ are the complex input and output envelope voltages at the time sample $\boldsymbol{k}$. $\boldsymbol{M}$ is the memory depth. Theoretically, the Volterra series can be used to describe all the different orders of distortion, but the calculation of higher order kernels becomes practically impossible because of the factorial-like increase of the number of coefficients. For this reason, extensive research is being carried out, which focuses on the reduction of the number of kernels/coefficients. The reduction allows faster convergence without losing the modeling accuracy. Depending on the bandwidth of different complex modulation schemes and the fading nature of memory effects present in the PA, the memory depth can be truncated. The work presented in [6] focuses on the truncation of the memory depth without compromising the model fidelity.

As effectiveness of Volterra series modeling, in its general form, is only limited to the weakly non-linear systems, extensive research has been carried out to overcome its

drawbacks. To limit the computational complexity of Volterra kernels, there have been several attempts to prune the Volterra series [7]. Some of its most common variants use simpler cascaded realization for reducing the complexity of the complicated series. Such architecture is called Weiner or Weiner-Hammerstien representation. The Weiner representation uses a cascade of linear system, and a memory-less nonlinearity. The Weiner-Hammerstien system is realized by using a linear system cascaded with a memory-less nonlinearity followed again by a linear system [8]. The Weiner kernels which simplify the realization of Volterra kernels [9] only converge to the Volterra series when the input is Gaussian. With non-Gaussian inputs, the Weiner kernel based solution, no longer offers the reduction in complexity. There are several other schemes that provide functional approximation through other means, which can include polynomials and Laguerre filters [10]. These schemes offer domain specific solutions which may be more efficient in some scenarios.

The artificial neural networks (ANNs) are the systems that have been shown to successfully model the RF power amplifiers [11]. Multi-layer Perceptrons (MLP) is one of the most popular structures of the ANN models. The MLP systems are similar to a general class of feed-forward ANN structure, since the flow of the data is from the input to the output without any feedback. The simpler structure with the back-propagation learning algorithm (BLPA), made the MLP very attractive for the PA behavioral modeling [12,13]. Alternatively, the radio basis function neural networks (RFBNNs) have been employed to model the PA behavior [14,15]. In [14] authors have used the RFBNN with the complex signals in the input layers, which necessitated the complex-valued version of the BPLA.

For the complex-valued BPLA, the training phase is longer than the real-valued BPLA case.

2.2.1 Memory Polynomial Model

The most widely cited baseband behavioral modeling scheme is known as memory polynomial [16] that is used to describe the non-linearity of PA along with the memory effects. The basic block diagram of the memory polynomial model with unit delays, is shown in Figure 2-2. The general form of the memory polynomial model is given as,

$$v_{out}(n) = \sum_{q=0}^{Q} \sum_{p=0}^{P} M_{q,p} |v_{in}(n-q)|^{p} \; v_{in}(n-q) \tag{2.3}$$

where p=1,2,…,P is the polynomial order, q=1,2,…,Q show the memory depth, and $M_{q,p}$ are the complex model coefficients. v_{in} and v_{out} are the discrete input and output complex voltages.

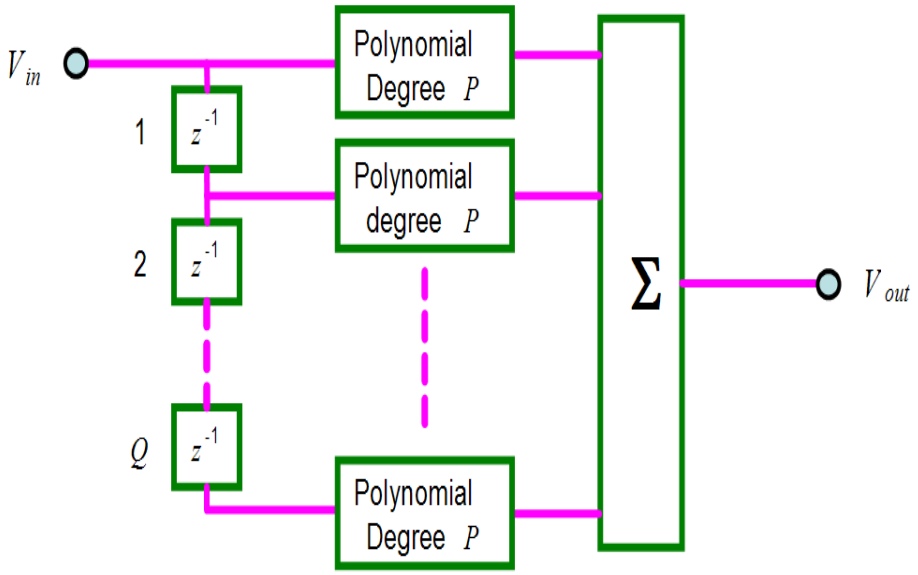

Figure 2-2 - A simplified block diagram of memory polynomial modeling scheme

2.2.2 Pruned Volterra Model using Dynamic Deviation Reduction

Some recent pruning algorithms like the Dynamic Deviation Reduction (DDR) method [17] have shown better modeling performance with the reduced system complexity. This method decomposes the Volterra series into separate static and dynamic components (2.4). The static part is given in (2.5), in which the polynomial order p can be chosen independent of the dynamic part. Equation (2.6) shows the dynamic part where the memory depth M_N can be chosen independently for the different kernels. This helps in reduction of the number of coefficients. This reduction in number of coefficients also results in improving the stability of the system. A simplified DDR-based pruned Volterra (PV) model is shown in Figure 2-3.

$$v_{out}(n) = v_{out,static}(n) + v_{out,dynamic}(n) \tag{2.4}$$

$$v_{out,static}(n) = \sum_{p=0}^{P} \left(a_p \, |v_{in}|^p \right) v_{in} \tag{2.5}$$

$$v_{out,dynamic}(n) = \sum_{p=1}^{P} \sum_{i_1=0}^{M_1} \dots \sum_{i_p=0}^{M_n} h_p(i_1, i_2, \dots i_p) \prod_{j=1}^{P} V_{in}(k - i_j) \tag{2.6}$$

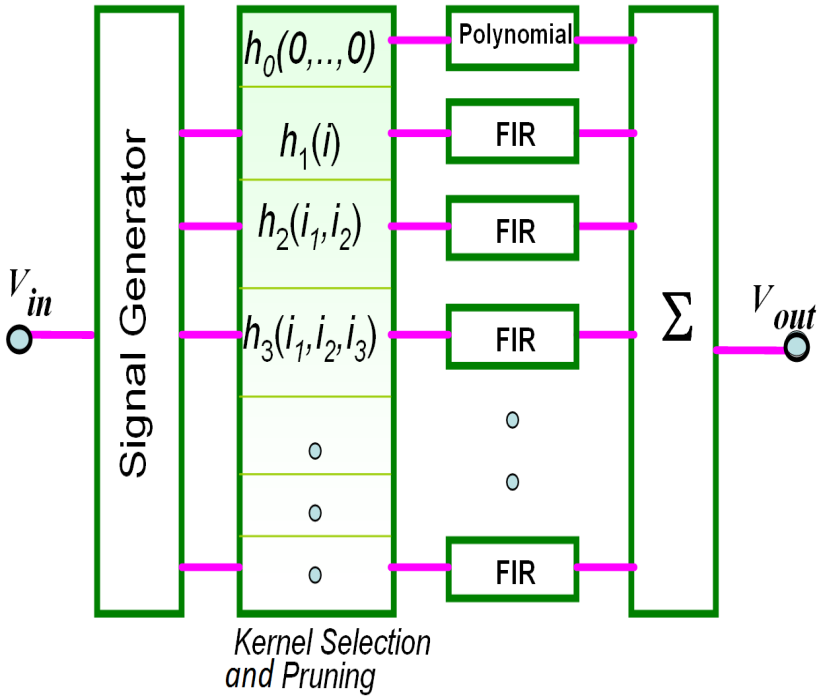

Figure 2-3 – A simplified block diagram of pruned Volterra Model

2.2.3 Generalized memory polynomial scheme

The generalized memory polynomial (GMP) scheme [18] combines the conventional memory polynomial terms with the cross terms between the signal and lagging and/or leading delay terms. Equations (2.7) to (2.10) provide the mathematical description of the GMP modeling scheme. This formulation allows to select a unique polynomial order and memory depth for each of the individual polynomial type as provided in equations (2.8), (2.9) and (2.10).

$$v_{out}(n) = v_{out,static}(n) + v_{out,MT}(n) + v_{out,CT}(n) \tag{2.7}$$

$$v_{out,static}(n) = \sum_{p=0}^{P_S} \left(a_p \, |v_{in}|^p \right) v_{in} \tag{2.8}$$

$$v_{out,MT}(n) = \sum_{q=0}^{Q} \sum_{p=0}^{P_M} M_{q,p} |v_{in}(n-q)|^p \; v_{in}(n-q) \tag{2.9}$$

$$v_{out,CT}(n) = \sum_{r=0}^{R} \sum_{q=0}^{Q} \sum_{p=0}^{P_C} C_{q,r,p} |v_{in}(n-q)|^p \; v_{in}(n-r) \quad , q \neq r \tag{2.10}$$

Equation (2.10) describes the cross-terms as q ≠ r. In literature, many variants of the GMP scheme exist, which are primarily based on different pruning methodologies for the memory and cross-term polynomials. Figure 2-4 shows the simplified block diagram of the GMP scheme. Each polynomial is a non-linear function which can be implemented as a look-up-table (LUT). In many commercial digital front-end (DFE) systems for the infrastructure applications, the GMP model is a popular method of choice for the DPD.

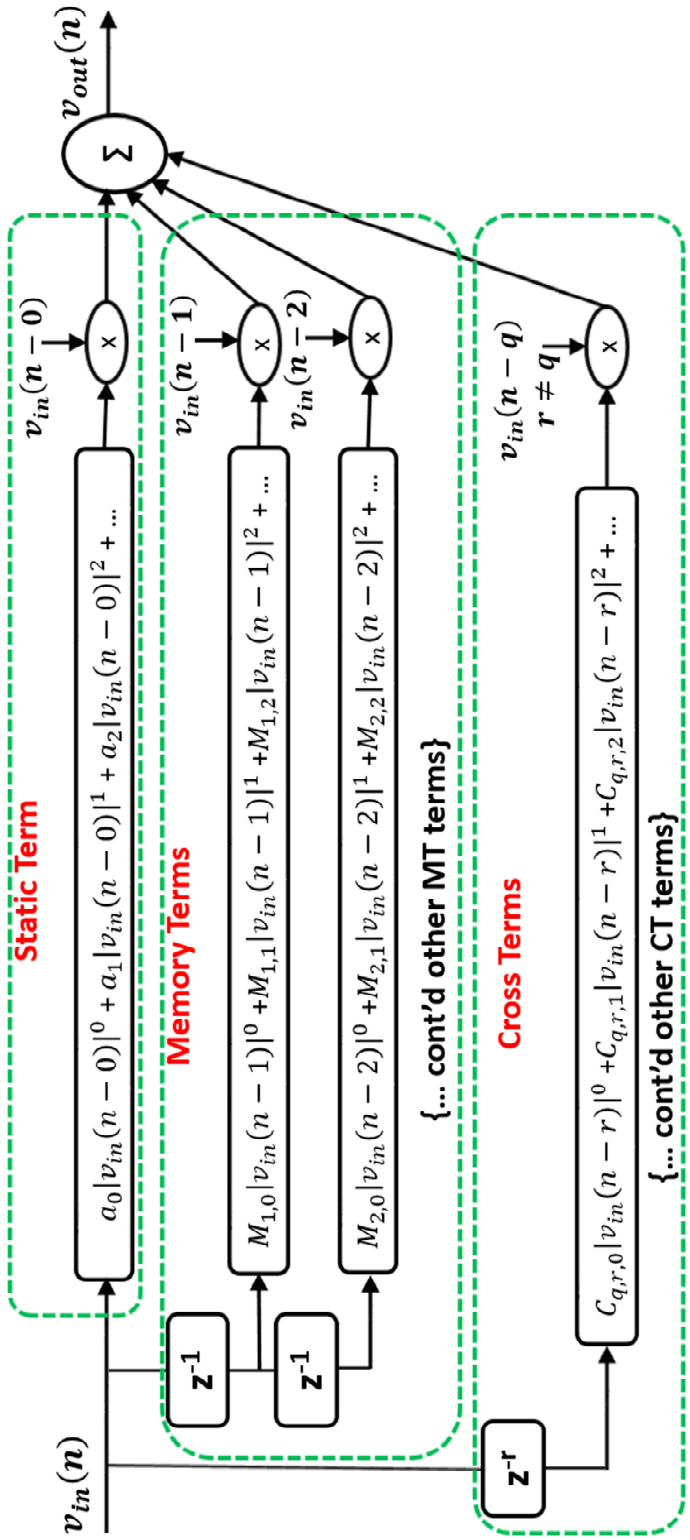

Figure 2-4 The simplified generalized memory polynomial scheme.

2.3 Contributions to behavioral modeling of RF PAs (this work)

2.3.1 Behavioral modeling for the handset PAs

Due to the power overhead and complexity concerns, the traditional behavioral modeling schemes are not used in the handset applications. The modeling work presented here, is based on using a polynomial along with the infinite impulse response (IIR) basis functions [19]. Due to its simpler structure, it is ideally suited for the handset PAs. The general structure of the model is illustrated in Figure 2-5. This modeling scheme has less computational complexity than the other published work. With the use of IIR basis functions, only few parameters are adequate to describe the short-term and the long-term memory effects.

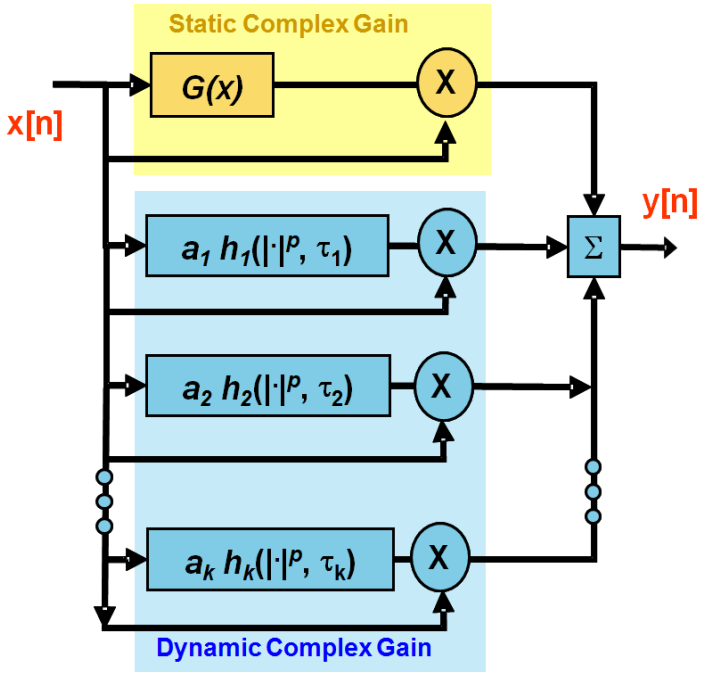

Figure 2-5 The block diagram of IIR based predistorter

Mathematically, the output envelope voltage is given by (2.11),

$$y = [G(x) + a_1 h_1 \otimes |x|^p + a_2 h_2 \otimes |x|^p + \cdots] x \quad (2.11)$$

Where **'x'** and '**y'** represent the discrete time-samples of the input and output complex envelope voltages. The term G(x) describes the memory-less non-linearities in terms of a polynomial expansion (2.12),

$$G(x) = g_0 + g_1|x|^1 + g_2|x|^2 + g_3|x|^3 + \cdots \quad (2.12)$$

To model the PA memory effects, a parallel sum of ***k*** first-order, single-pole, IIR filters, of the transfer functions h_1, h_2,.. h_k, are added with the time constants τ_1,τ_2,.. τ_κ. The time constants (τ_k's) correspond to the sparse delays that best characterize the underlying memory effects of the PA. Each h_k, filters the magnitude (p=1, *bias-related*), or the magnitude-square (p=2, *thermal-related*) of the input. The z-transform of h_k, denoted by $H_K(z)$ is defined by:

$$H_K(z) = \frac{\frac{1}{\tau_K F_s}}{1 - z^{-1}\left(1 - \frac{1}{\tau_K F_s}\right)} \quad (2.13)$$

Where, F_s is the sampling frequency.

A nominal 2W PA, designed for a 2.5G wireless handset, operating at 824 MHz is used to illustrate the validity of the model. Additionally, the PA is biased in deep Class-AB so that it exhibits expansion prior to compression. This PA is selected because it exhibits both the short-term and the long-term memory behavior. As presented in Figure

2-6, the power spectral density plot shows that exceptional agreement is found where the error (red curve) between model and the measurement is better than -50dBc.

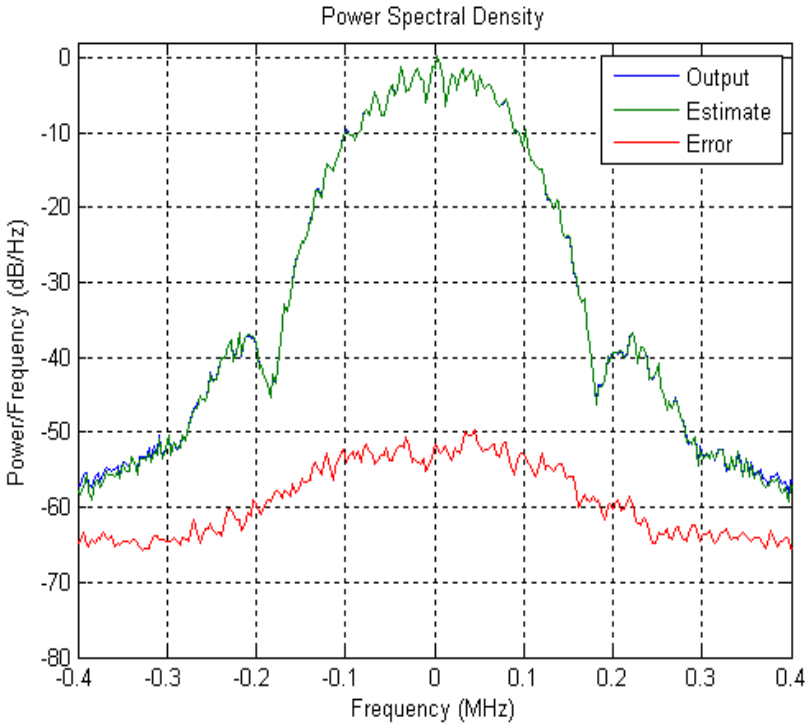

Figure 2-6 - Polynomial with IIR basis functions, validation using 2.5G handset PA

In [20], the polynomial with IIR basis function scheme is extended to model the PA for three-port applications. Most of the existing research on PA modeling is focused on the developing the two-port PA model for the fixed-bias voltage. This technique [20] models the bias port of the PA, along with the input and output ports. A simplified block diagram is shown in Figure 2-7.

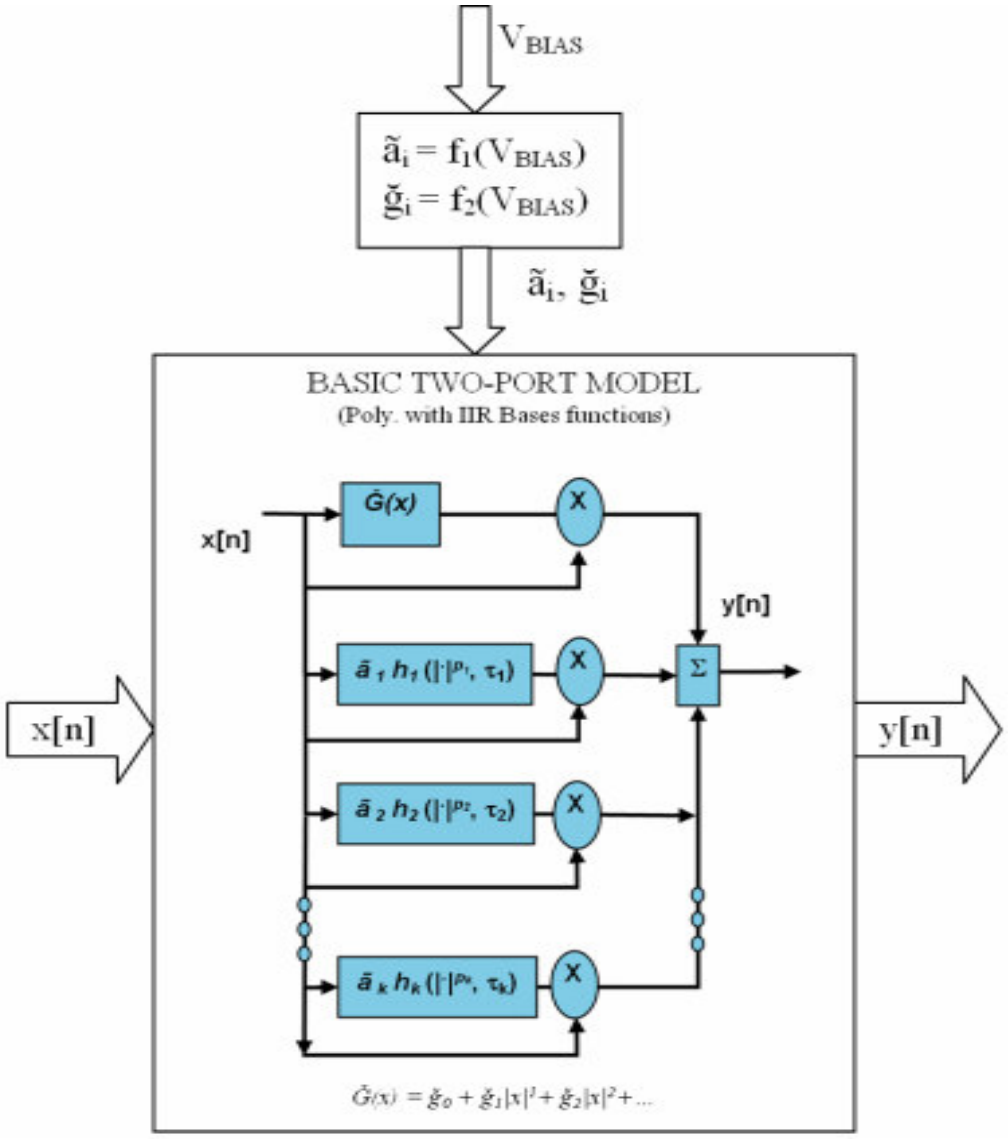

Figure 2-7 Modeling for 3-port applications, polynomial with IIR basis function

2.3.2 Behavioral modeling for infrastructure PAs

Pruned Volterra Model with IIR basis functions (IIR-PV)

As discussed in previous section, several pruned Volterra (PV) based architectures exist in literature for the behavioral modeling of high power infrastructure PAs. A modification to such schemes is illustrated in Figure 2-8, where along with the pruned

Volterra kernels, a parallel structure of infinite impulse response (IIR) basis functions is added [21]. The pruned Volterra based architecture presented in [17], decomposes the Volterra series into separate static and dynamic components. The inherent finite impulse response (FIR) based architecture of the pruned Volterra scheme makes it difficult to model both the short-term and long-term memory effects with reduced number of parameters. Inclusion of IIR basis functions, solves this problem by modeling the long-term memory effects with very few numbers of parameters.

In IIR-PV, the parallel sum of k, first-order, single-pole, IIR filters of transfer functions h_{IIR_1}, h_{IIR_2},…,h_{IIR_k} (with time constants τ_1, τ_2,…, τ_k) are added. The time constants τ_k's correspond to the sparse delays that best characterize the underlying memory effects of the PA. Each h_{IIR_k} block, filters the magnitude (p=1, bias-related) or the magnitude-square (p=2, thermal-related) of the input. A simplified block diagram of IIR-PV scheme is shown in Figure 2-8.

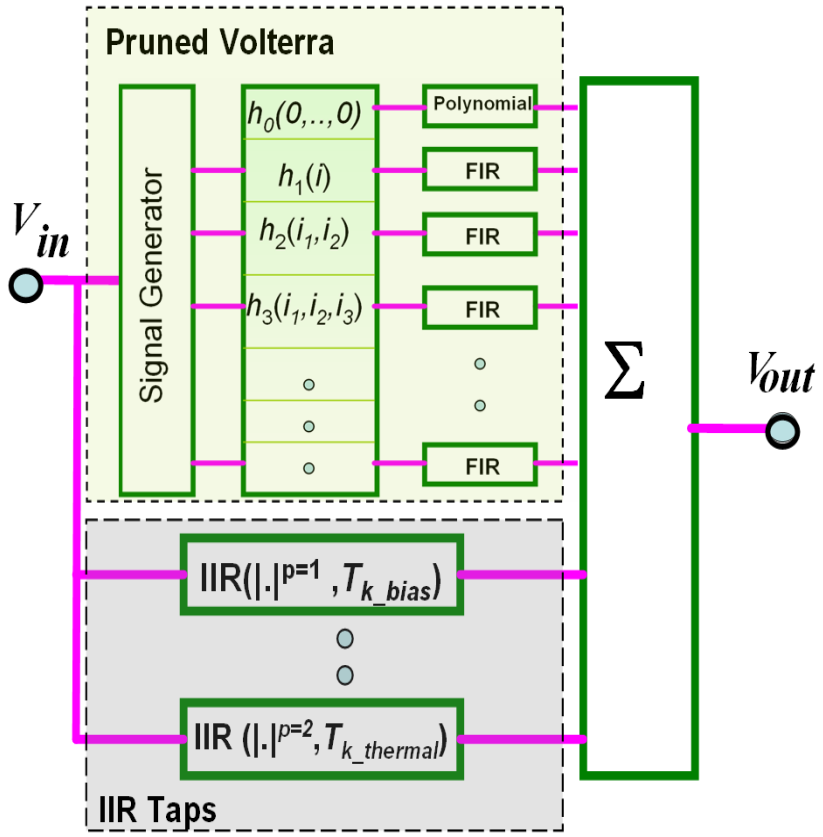

Figure 2-8 – Simplified structure of pruned Volterra model with IIR basis functions

The performance of the IIR-PV architecture is validated by using Class-AB and Doherty power amplifiers, operating at 2.14 GHz, with the average output power levels of 43dBm and 49 dBm, respectively. A multi-carrier WCDMA-1001 test signal of 20 MHz bandwidth is used for the characterization of the PAs. The modeling performance is presented in Figure 2-9 (Class-AB PA) and Figure 2-10 (Doherty PA).

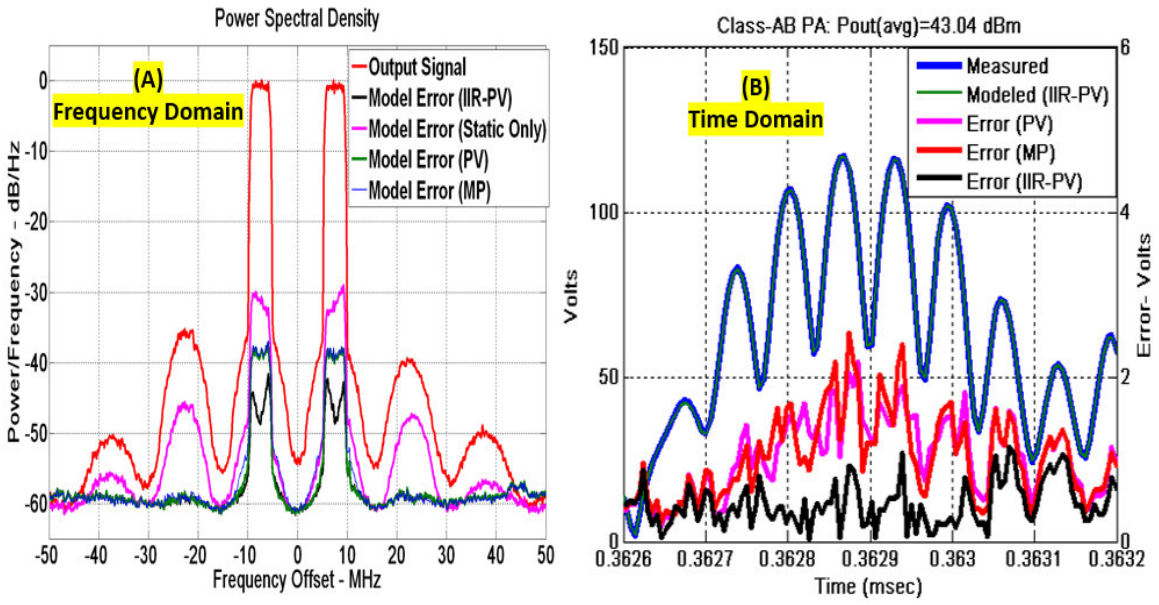

Figure 2-9 - IIR-PV performance using class-AB PA, A) PSD and B) time-domain.

Performance of the new IIR-PV scheme [21], is compared with the original dynamic deviation reduction method based pruned Volterra (PV) scheme [17], and the memory polynomial (MP) scheme described in previous section. For all these modeling schemes, same polynomial order of "11" is selected to model the static non-linearities of the PA. Figure 2-9 shows the power spectral density (PSD) function of the modeling performances of MP, PV and IIR-PV schemes along with the time-domain snapshot. With the addition of only two new parameters, the IIR-PV scheme shows significant reduction in the normalized mean-square error (NMSE) over the PV scheme. Figure 2-10 shows similar trends with the Doherty PA. Table 1 provides the performance summary.

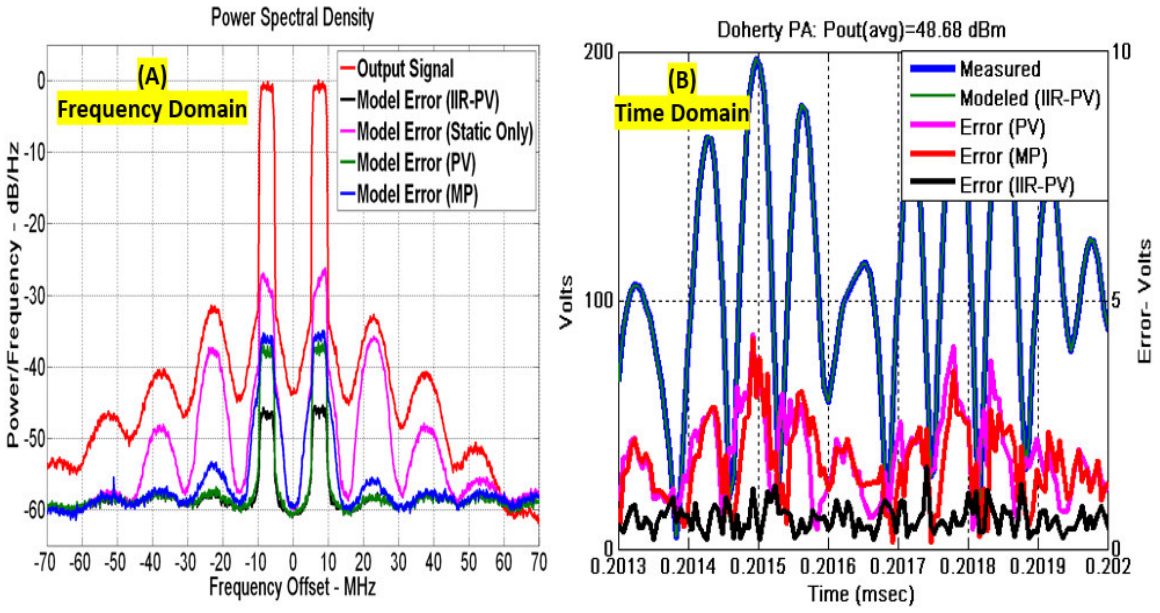

Figure 2-10 - IIR-PV performance using Doherty PA, A) PSD and B) time-domain.

Table 1 - Modeling performance comparison

Model Type	No. of Coeff	NMSE(dB) Class-AB	NMSE(dB) Doherty
Static	11	-30.13	-26.17
MP	44	-36.76	-34.04
PV	47	-37.44	-36.11
IIR-PV	49	**-41.66**	**-42.14**

2.4 Summary

Since a universal PA modeling scheme does not exist, an overview of existing PA modeling schemes is discussed. Each modeling scheme offers advantage in some respects in figure-of-merits such as, reduction in NMSE, in-band performance, out-of-band performance, model complexity and stability. A novel polynomial based modeling scheme with inclusion of IIR basis functions is also discussed. When combined with the pruned

Volterra scheme, the IIR-PV showed improved modeling performance with addition of very few parameters.

CHAPTER 3. POWER AMPLIFIER LINEARIZATION

One of the major challenges to the designing of radio frequency (RF) power amplifiers is its linearity requirement. Worldwide regulatory bodies such as Federal Communications Commission (FCC) and European Telecommunications Standards Institute (ETSI) place stringent limitations on the allowable spurious emissions outside the allotted bandwidth. In addition, the spectral leakage to the adjacent channels in the allotted frequency is also restricted. In this chapter, an overview of various linearization methodologies, with the discussion regarding their advantages and limitations, is provided. In last section, the digital predistortion technique is discussed in detail as it is a widely adopted linearization scheme for the base-station applications.

3.1 Linearity measurement metrics

PA non-linearities are exhibited as distortions, both in-band as well as out-of-band. The Error Vector Magnitude (EVM) and the Adjacent Channel Power Ratio (ACPR) are the two widely adopted metrics for measuring the linearity conformance of a power amplifier.

The EVM measures the in-band distortion and it can be calculated using (3.1) and (3.2). Figure 3-1 illustrates a reference vector and an error vector, with respect to an ideal and a measured constellation point. Figure 3-2 shows an example of the EVM improvement achieved using the PA linearization technique.

$$EVM\ (\%) = \sqrt{\frac{P_{err}}{P_{reference}}} \times 100 \tag{3.1}$$

$$EVM\ (dB) = 10\ log_{10}\left(\frac{P_{err}}{P_{reference}}\right) \tag{3.2}$$

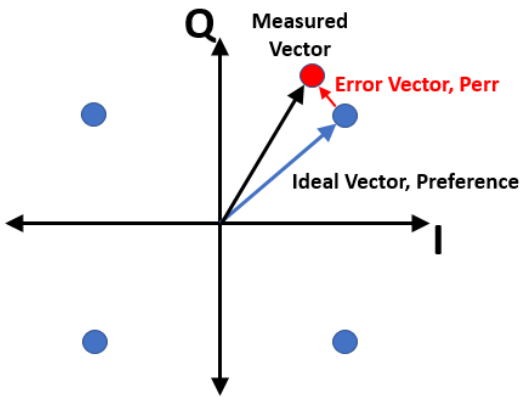

Figure 3-1 - A QPSK constellation

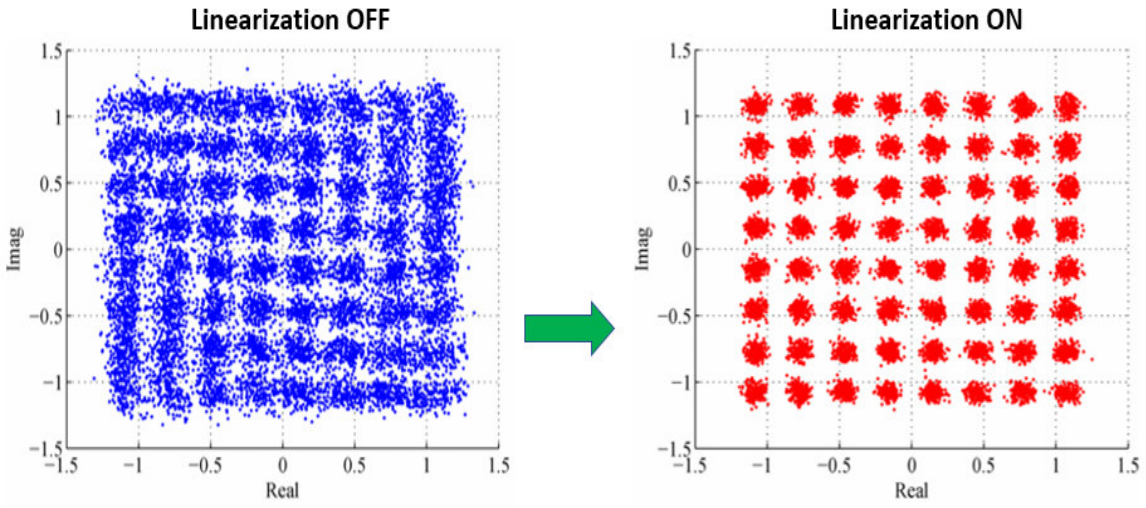

Figure 3-2 - Linearization improves the EVM

The ACPR characterizes the PA non-linearities that contribute to the out-of-band distortions. It is defined as the ratio of the total power delivered in the adjacent channel to the total power over the channel bandwidth. Figure 3-3 shows an example of the PSD plot

of the output of the PA, with and without the linearization. It also shows the spectral emission mask.

$$ACPR\ (dBc) = 10log_{10}\left(\frac{P_{adj}}{P_{ref}}\right) \tag{3.3}$$

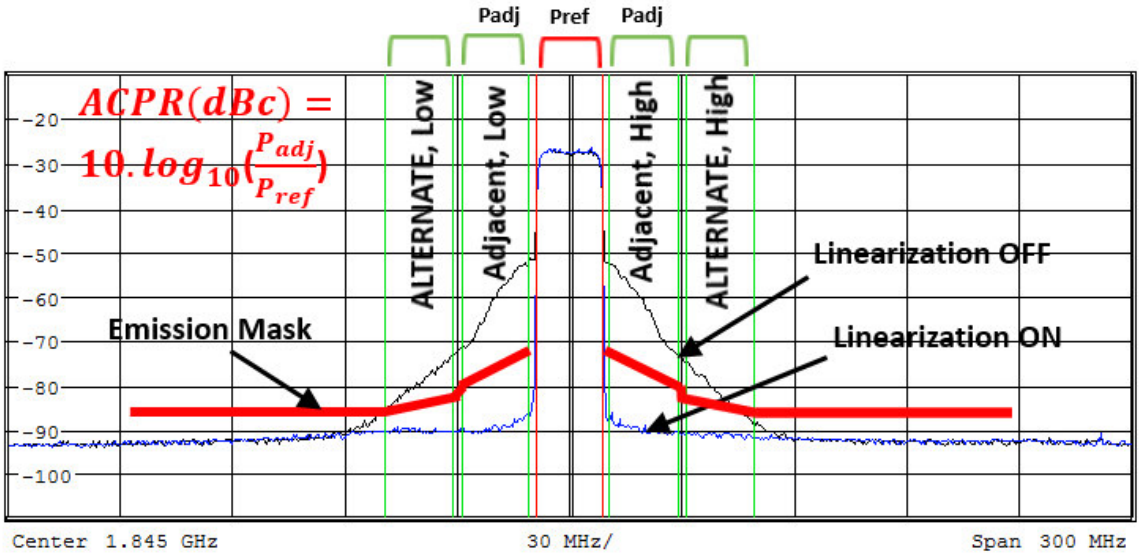

Figure 3-3 - ACPR measurement example

3.2 Crest Factor Reduction (CFR)

Crest factor reduction is a technique used to reduce the peak to average power ratio (PAPR) of the signal under the system constrains of allowable in-band distortion. Reduction of PAPR, allows the PA to operate at the reduced back-off which results in improvement of efficiency of the PA. Several CFR methods exist in literature, most common methods are: clipping and filtering, peak windowing, and peak cancellation. Figure 3-4 illustrates an example of time-domain clipping and its resultant complementary cumulative distribution function (CCDF).

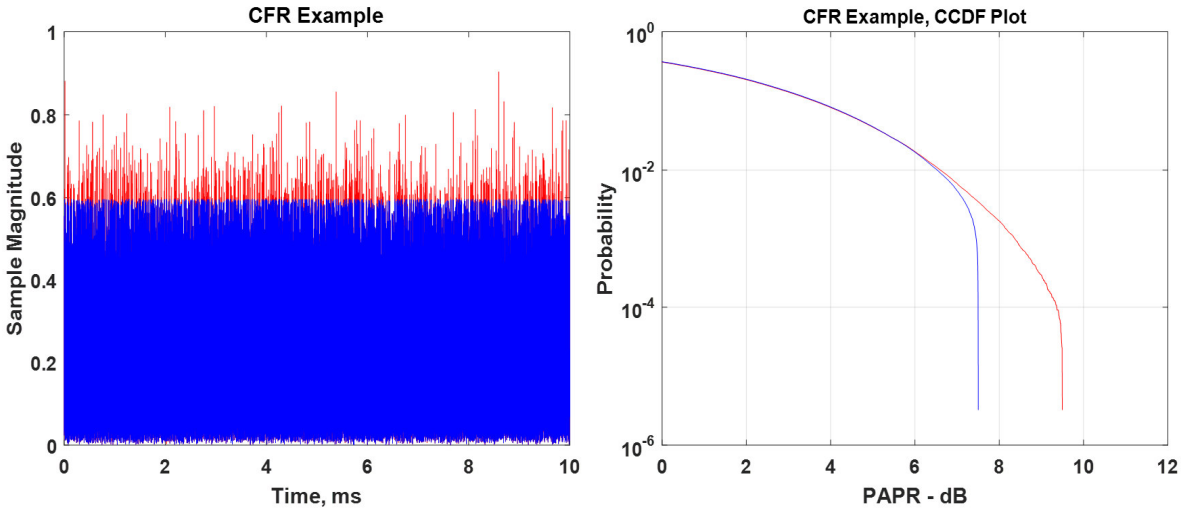

Figure 3-4 – A CFR example

3.3 Linearization Techniques

Several linearization techniques are reported in literature that aim at the improvement of non-linearities and compensation of memory effects of the PAs. These techniques can be broadly characterized as system level, or circuit level. The system level techniques are more popular for the infrastructure applications.

3.3.1 Feed-forward linearization

In feed-forward scheme, originally proposed by Harold Black in [22], a delayed input signal is subtracted from the output of the PA. This error signal is amplified back to original output power level of the PA, and then combined with the delayed output of the PA. This is illustrated in the simplified block diagram shown in Figure 3-5. In practice, the feed-forward systems suffer from many limitations which degrade the linearity performance. This open loop cancellation scheme is quite sensitive to the delay

mismatches, and the gain/phase variations of the error amplifier over the frequency and the temperature. Some modifications exist in literature that aim at improving these limitations by using additional circuitry, but this comes with the increment in cost and degradation of the power efficiency

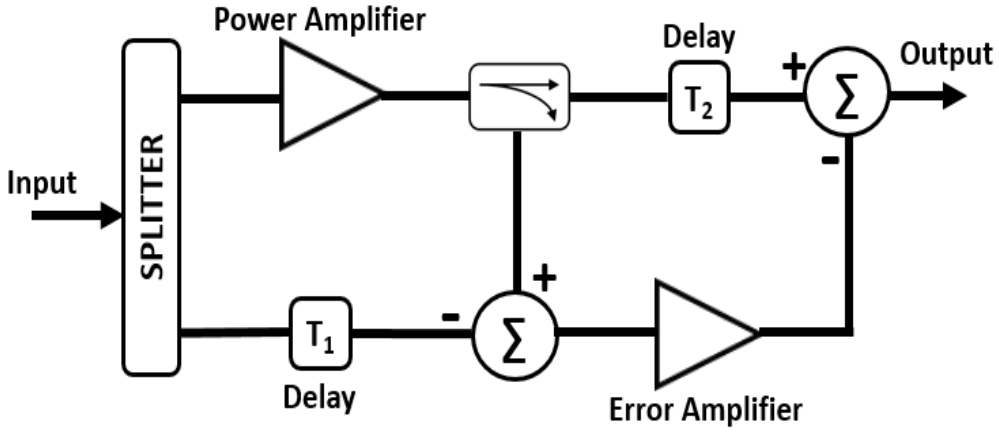

Figure 3-5 - Block diagram of feed-forward linearizer

3.3.2 Feedback Linearization

The feedback linearization system aims at compensation for the non-linear distortion of a PA by implementing a feedback loop which compares the PA output signal to the desired output signal. A transfer function of a simplified feedback closed loop system (Figure 3-6) is given in (3.4).

$$H = \frac{G}{1 + \beta G} \tag{3.4}$$

Where, composite gain of the PA is denoted as *G,* and β represents the transfer function of the feedback loop. Although, the feedback scheme is quite simple to implement but its

efficacy is limited at the frequencies in GHz range. At higher modulation bandwidths, the electrical delays in the feedback loop significantly degrade the quality of linearization achieved.

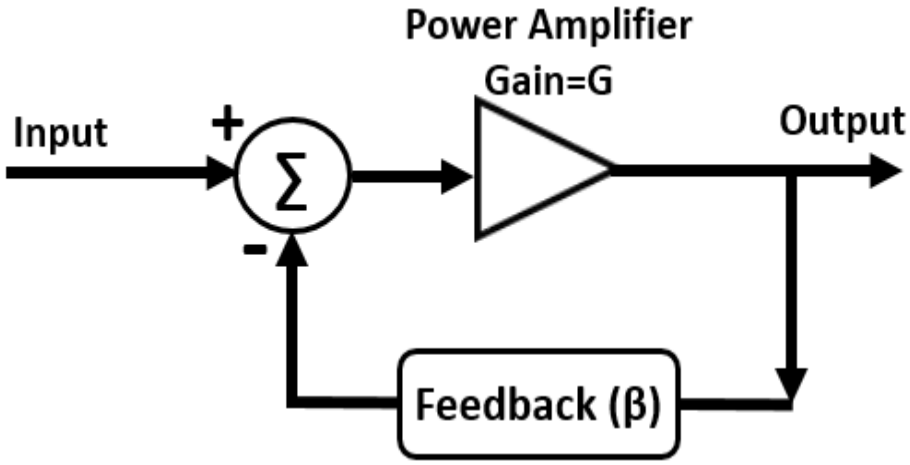

Figure 3-6 - Simplified feedback linearizer

The indirect feedback based linearizer was originally proposed by Harold Black [23], but the proposed design had limitations when used at higher frequencies and bandwidths. A more advanced version is based on cartesian feedback (CFB) architecture [24]. Although, the CFB architecture has been demonstrated to work at higher bandwidths, but still it is most suitable for the narrowband signals where it achieves good cancellation of the IMDs. In addition, the stability of the CFB architecture reduces with increasing band of operation with higher center frequencies.

3.3.3 LINC Linearizer

In linear amplification using non-linear components (LINC) technique [25], a varying envelope signal is subdivided into two or more signal components of constant envelope, which are separately amplified using two highly efficient, but non-linear PAs. The outputs

of these PAs are later combined to achieve an amplified output signal with minimized non-linearities. For instance, take an input signal in (3.5)

$$s(t) = a(t)\, cos(wt + \emptyset(t)) \tag{3.5}$$

The signal is split into $s_1(t)$ and $s_2(t)$, where

$$\begin{aligned} s_1(t) &= a_{max} cos\big(wt + \emptyset(t) + \gamma(t)\big) \\ s_2(t) &= a_{max} cos\big(wt + \emptyset(t) - \gamma(t)\big) \end{aligned} \tag{3.6}$$

Where, $a_{max} = \max(a(t))$ and $\gamma(t) = \cos^{-1}\left(\frac{a(t)}{a_{max}}\right)$. After combining the output of two identical PAs we get,

$$\begin{aligned} s_{out}(t) = G\times\Big\{&\frac{a_{max}}{2} cos\big(wt + \emptyset(t)\big)cos\big(\gamma(t)\big) \\ &- \frac{a_{max}}{2} sin\big(wt + \emptyset(t)\big)sin\big(\gamma(t)\big) \\ &+ \frac{a_{max}}{2} cos\big(wt + \emptyset(t)\big)cos\big(\gamma(t)\big) \\ &+ \frac{a_{max}}{2} sin\big(wt + \emptyset(t)\big)sin\big(\gamma(t)\big)\Big\} \\ &= G\times a(t)\, cos(wt + \emptyset(t)) \end{aligned} \tag{3.7}$$

Where, G is the matched gain of the two PAs. The simplified block diagram of the LINC system is shown in Figure 3-7. The LINC linearizer is very sensitive to the mismatch in two signal paths. Moreover, constant envelope waveforms require the two PAs to operate at a larger bandwidth which is another challenge in realization of the LINC.

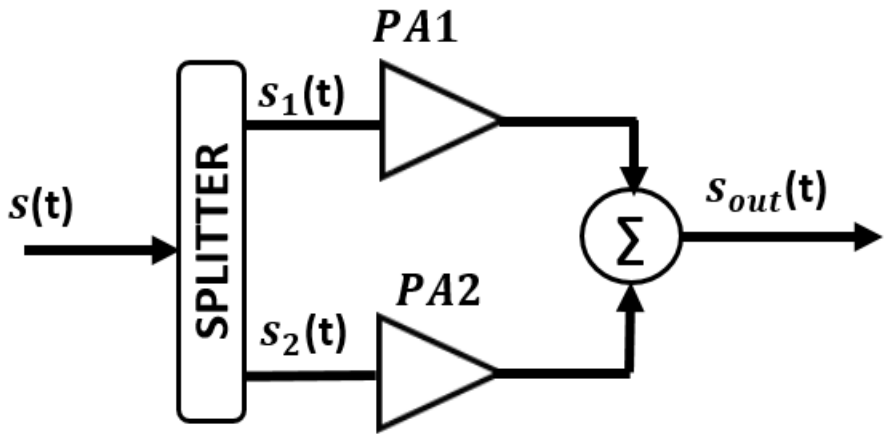

Figure 3-7 - LINC linearizer

3.3.4 Digital Predistortion

The digital predistortion (DPD) scheme, initially reported in 1983 [26, 27], is the most commonly used linearization technique for the infrastructure applications. The DPD can be classified into many variants, for example, the data or signal predistortion, the baseband/IF or RF predistortion and an adaptive or non-adaptive predistortion. The digital baseband signal predistorter is the most widely adopted architecture because of its superior performance in cancellation of both the in-band and the out-of-band distortions. As this predistorter architecture is independent of the band of the PA operation, hence, it provides the maximum system flexibility.

The basic principle of the DPD system, in its open-loop form, is illustrated in Figure 3-8. The predistorter modifies the input signal to power amplifier such that it counteracts the nonlinear characteristics of the PA, resulting into a linear over-all operation. The AM to AM and AM to PM plots represent the magnitude and phase response of the output of

the PA in terms of the magnitude of the input. The plots shown as an example in Figure 3-8 are 'output-power' referred.

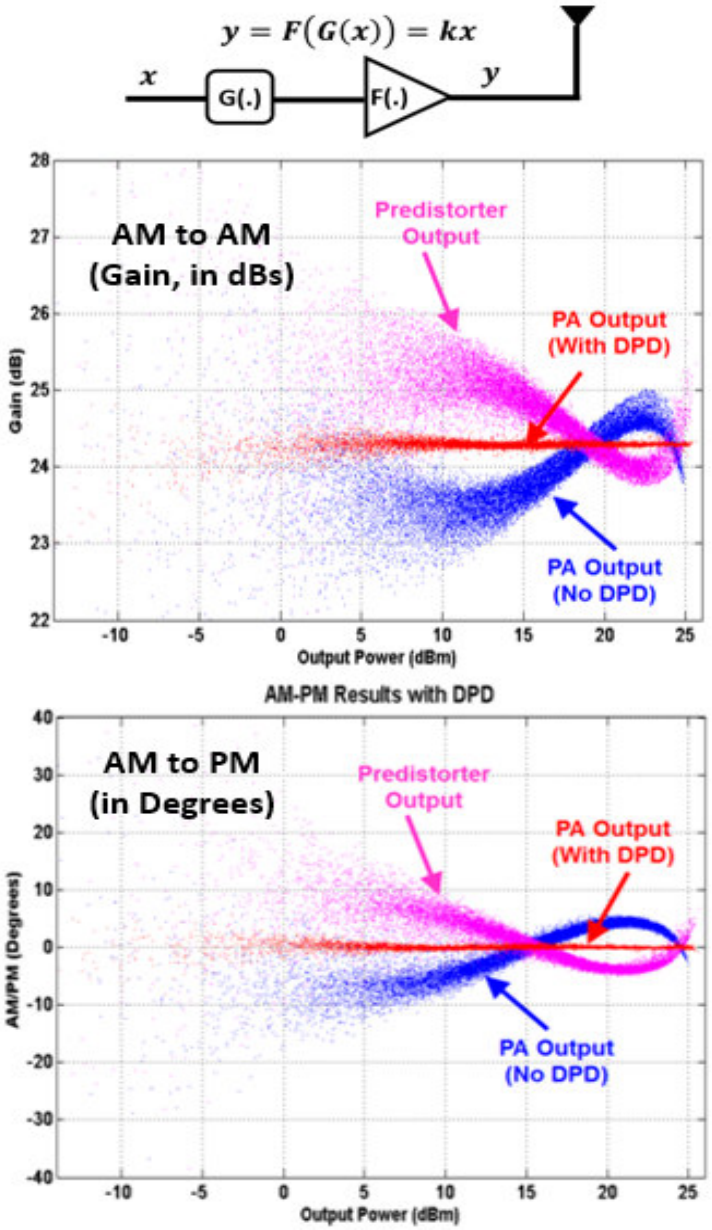

Figure 3-8 - Basics of a DPD system.

3.4 Real-time adaptation of coefficients for a DPD system

For the real-time calculation (*or learning*) of DPD coefficients, two architectures are most popular in the literature, the indirect learning architecture (IDL), and the direct learning architecture (DL).

Indirect learning architecture (IDL)

The basic block diagram of an IDL architecture [28] is illustrated in Figure 3-9. In this scheme, the post-distorter is calculated first by comparing the complex-gain compensated feedback of the output of the PA, shown as $z(n)$, with the predistortion signal $x(n)$ after the proper delay adjustments. This postdistorter function represents the inverse model of the PA. When the IDL system is working properly, the feedback $y(n)$ is a linear replica of the input waveform $u(n)$, and the output of postdistorter $\hat{x}(n)$ matches with the output of the pre-distorter $x(n)$. Hence, the post-distorter and the pre-distorter are essentially the same.

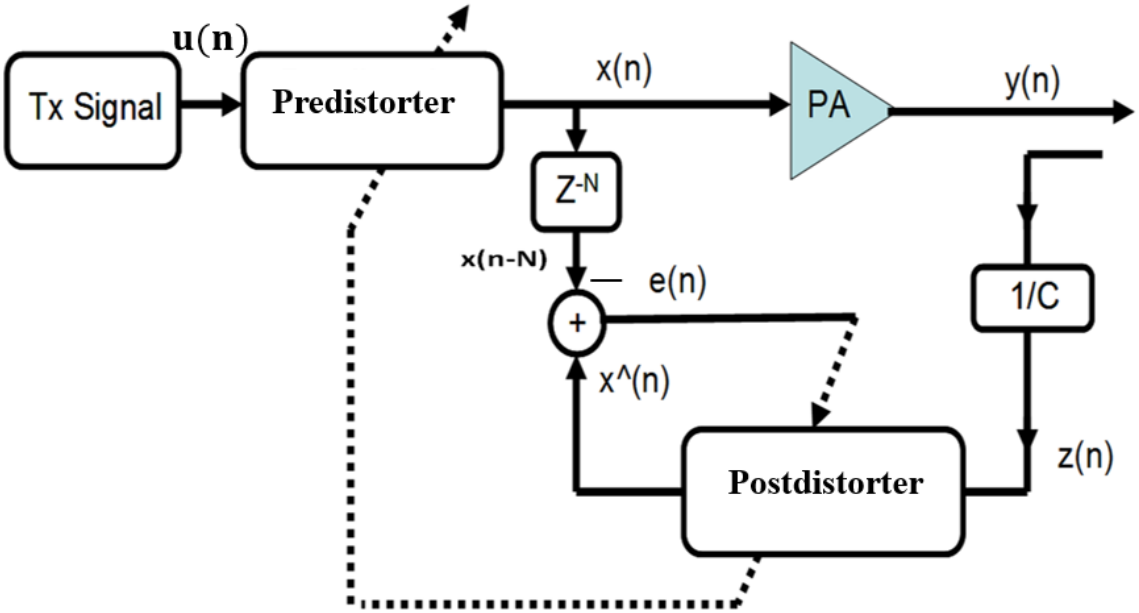

Figure 3-9 - The indirect learning architecture.

For simplicity, let's assume that the memory polynomial scheme is used for the behavioral modeling of the PA, and mathematically it can be represented as,

$$x(n) = \sum_{q=0}^{Q} \sum_{p=0}^{P} a_{q,p} |u(n-q)|^p \; u(n-q) \tag{3.8}$$

Where, $u(n)$ and $x(n)$ are the inputs and the outputs of the pre-distorter. The order of polynomial is given as P and the memory depth of the model is represented by Q. The coefficients of the memory polynomial scheme are given as $a_{q,p}$. In vector notation, the non-linear function in equation (3.8) can be represented as a function which is linear in parameters or coefficients $a_{q,p}$, shown as vector $\boldsymbol{a}$ in equation (3.9). For other modeling scheme, such as the PV, the IIR-PV or the other Volterra based models, the formulation of vector notation will be similar.

$$\boldsymbol{x} = \boldsymbol{U}\boldsymbol{a} \tag{3.9}$$

Similarly, (3.10) provides the post-distorter function. Where, matrices U and W are based on an identical memory polynomial model. As explained earlier, when the IDL system has converged, $\hat{\boldsymbol{x}}$ approaches $\boldsymbol{x}$, and $\hat{\boldsymbol{a}}$ approaches $\boldsymbol{a}$.

$$\hat{\boldsymbol{x}} = \boldsymbol{W}\hat{\boldsymbol{a}} \tag{3.10}$$

As $\boldsymbol{W}$ is not a square matrix, a simple pseudo-inverse approach shown in (3.11) might not be useful to calculate the coefficients $\hat{\boldsymbol{a}}$. Instead, the least-square (LS) solution is usually employed for the calculation of coefficients, as provided in (3.12)

$$\hat{\boldsymbol{a}} = \boldsymbol{W}^{-1}\hat{\boldsymbol{x}} \tag{3.11}$$

$$\boldsymbol{a} = \hat{\boldsymbol{a}} = (\boldsymbol{W}^{\boldsymbol{H}}\boldsymbol{W})^{-1}\boldsymbol{W}^{\boldsymbol{H}}\hat{\boldsymbol{x}} \tag{3.12}$$

Where, $(.)^{H}$ represents a complex conjugate transpose.

Direct learning architecture (DL)

A direct learning (DL) architecture [29] is a classic example of a self-tuning controller shown in Figure 3-10, where input signal $u(n)$ is "directly" compared with the feedback signal $z(n)$. When the predistorter is optimally converged, the complex-gain compensated feedback of the output $y(n)$, shown as $z(n)$, is a linear replica of the input $u(n)$. The pre-distorter function based on a simple memory polynomial based scheme can be expressed as [30].

$$x(n) = \frac{1}{\beta_o(|x(n)|)}\left(u(n) - \sum_{q=1}^{Q-1} \beta_q(|x(n-q)|).x(n-q)\right) \quad (3.13)$$

Where, $\beta_o = \sum_{p=1}^{P} a_{p0}\,|u(n)|^{p-1}$. In the first iteration, $x(n)$ and $x(n-q)$ are replaced with $u(n)$ and $u(n-q)$ in both β_o and β_q.

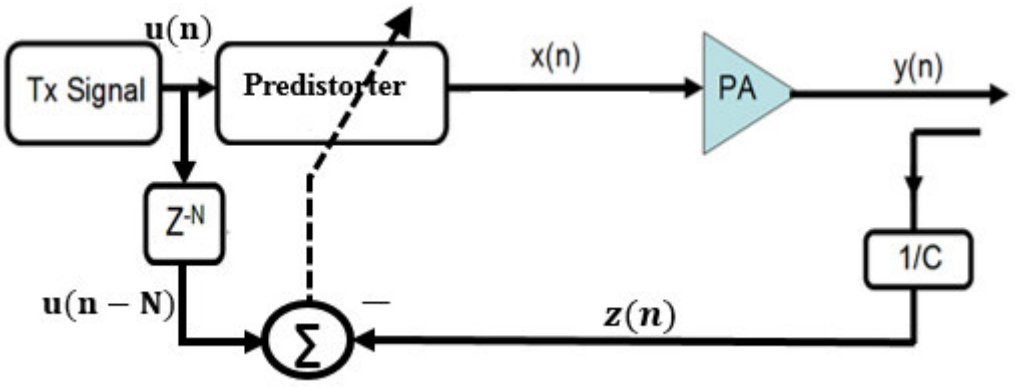

Figure 3-10 - The direct learning architecture

3.5 Digital Predistortion: Latest trends and challenges

- Gallium Nitride (GaN) transistors: The long-term memory effects exhibited by the GaN transistors, generally attributed to trapping effects, pose a challenge for a digital predistortion system. These non-idealities of GaN transistors contribute to the in-band and out of band distortions.
- Multi-band PAs: The imperfections in impedance terminations at the baseband and the difference frequencies, add to the complexity of the DPD systems. In the presence of higher order intermodulation distortion (IMD) products near the desired

band, the extraction of an equivalent baseband model of the PA becomes quite complex. An example of the linearization performance of a dual-band DPD system is shown in Figure 3-11.

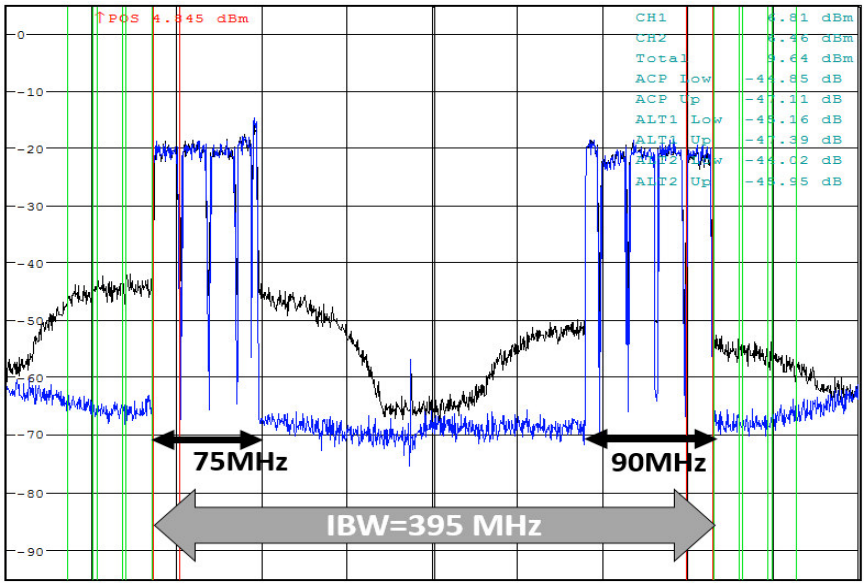

Figure 3-11 - DPD Performance for a Doherty PA operating in 3GPP bands 3 and 66. Use case has instantaneous bandwidth of 395MHz and signal bandwidth of 165MHz (7-carriers LTE20MHz, 2-carriers LTE10MHz, 1-carrier LTE5MHz). The DPD characterization is performed in NXP lab

- WLAN PAs: WLAN PAs are now designed for use with the DPD systems. With IEEE 802.11ac standard, the correction bandwidth of DPD can be 2 to 3 times higher than 160MHz channel bandwidth. To achieve higher efficiency, these PAs operate at reduced back-off levels from the saturation Power (P_{SAT}). The pre-distorter function for such cases, is designed to operate in deep compression (or close to it). In these scenarios, special considerations need to be taken to ensure the stability of the DPD system.

CHAPTER 4. EFFICIENCY ENHANCEMENT OF RF POWER AMPLIFIERS

For the modern transmitter systems, several efficiency enhancement schemes and their derivatives exist in literature. An overview of some of the popular efficiency enhancement techniques is provided in this chapter. These techniques include the Doherty power amplifier, Outphasing amplifier, envelope elimination and restoration (EER) scheme and the envelope-tracking (ET) scheme. The ET scheme is the recent derivative of an EER scheme. Based on contributions of this thesis, a detailed discussion is dedicated for the Doherty PA, since it is the topic of this research.

The drain efficiency or simply the efficiency of the power amplifier, given in Equation (4.1), is the ratio of the output power to the input DC power. Where, P_{RFout} is the average output power of the PA. The power added efficiency (PAE) is given in Equation (4.2). Where, P_{RFin} is the average input power to the PA.

$$\text{Efficiency} = \eta = \frac{P_{RFout}}{P_{DC}} = \frac{P_{RFout}}{V_{DC} \times I_{DC}} \tag{4.1}$$

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout} - P_{RFin}}{V_{DC} \times I_{DC}} \tag{4.2}$$

4.1 The Outphasing Amplifier

The outphasing amplifier, initially proposed by Chireix in 1930s [31], in its idealized implementation claims to hold the efficiency close to maximum for nearly 10 dB of the upper output power range. Although, the outphasing amplifier is capable of linear power amplification (using highly efficient non-linear PAs), but the complexities in realization of compensating reactances, drive signal generation and the DSP correction requirements cause the deviation in the performance from the ideal. Several authors have reported [32, 33] the methodologies to improve the efficiency of the outphasing PAs. Another methodology was reported in [34], where authors have shown the improvement in the efficiency of the outphasing PA by using pulse modulation of the input signals. The block diagram of the outphasing PA scheme is illustrated in Figure 4-1.

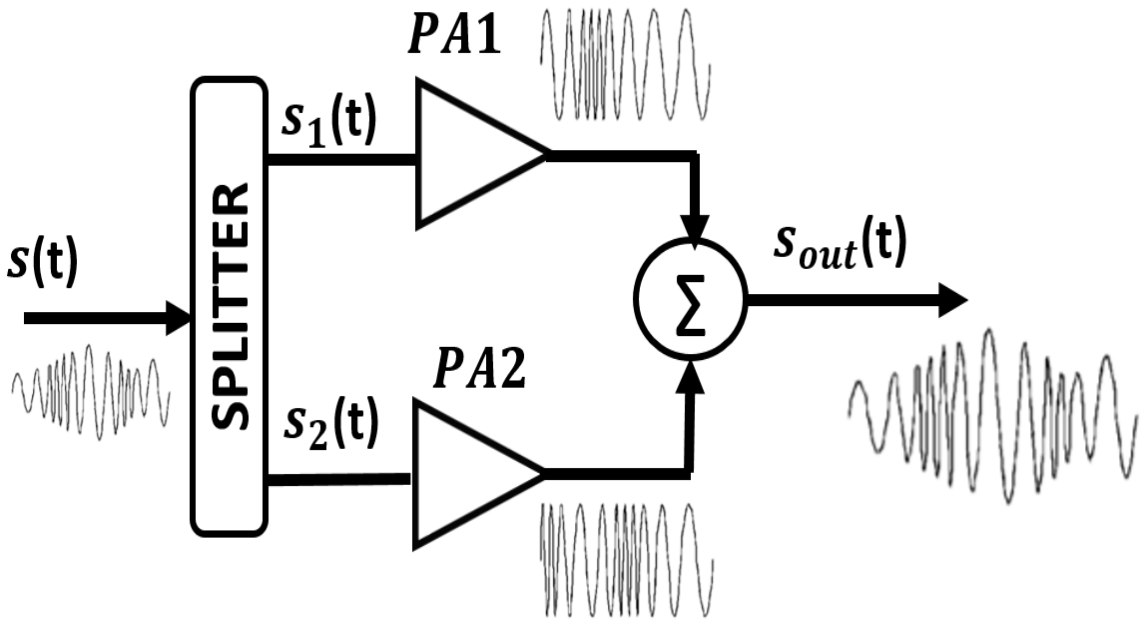

Figure 4-1 The simplified block diagram of outphasing operation

4.2 The envelope elimination and restoration (EER) scheme

The envelope elimination and restoration (EER) technique (illustrated in Figure 4-2), initially proposed by Kahn in [35], can theoretically achieve high efficiency but this technique requires highly efficient power supply modulator. In practical, the realization of highly linearized power supply modulator for wideband applications is still a huge problem. Several authors have reported the hybrid architectures to improve the efficiency of the PA while maintaining the linearity for higher bandwidth signals [36, 37].

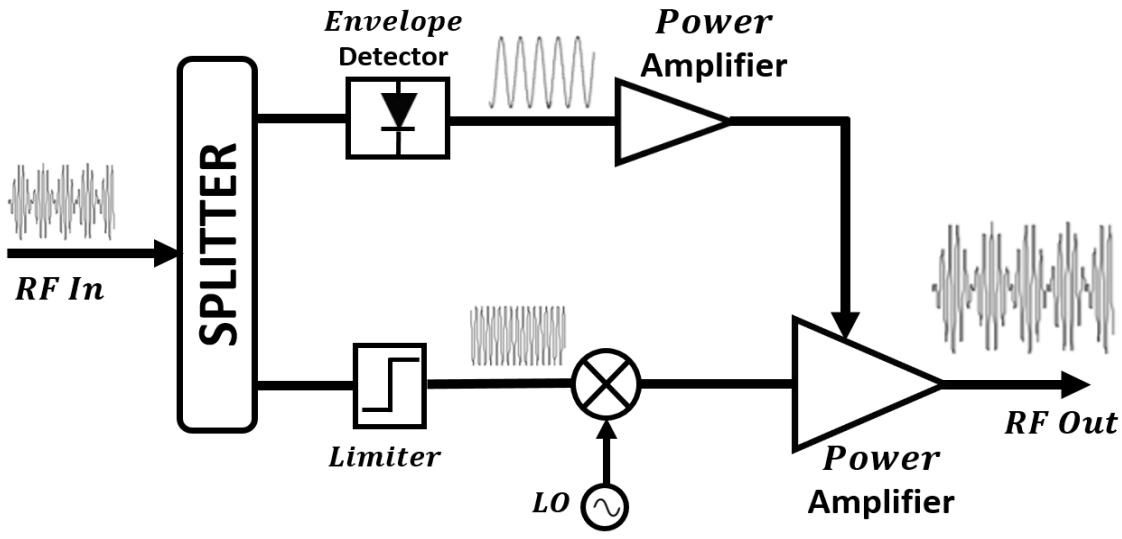

Figure 4-2 The EER scheme for efficiency enhancement

4.3 The envelope tracking (ET) scheme

The envelope tracking (ET) technique [38] is more widely used variant of an EER scheme. Unlike the EER approach, drain bias modulation of the ET amplifier avoids going

to the very low voltages by adding an offset level. The offset voltage in low-power region is typically adjusted to be larger than the "knee" voltage of the transistor. By operating above the knee region, the PA can reduce the extreme nonlinear behavior. The drawback of the improvement in linearity with the ET approach is the lower efficiency, as compared to that of an EER scheme. Like an EER architecture, the ET scheme also requires a wideband power supply modulator which is quite challenging as the bandwidth of the envelope signal can easily become 3~5 times the bandwidth of the input signal. In [39], authors utilized the signal processing techniques in conjunction with analog hysteric feedback to achieve the supply modulator with higher bandwidth capabilities. The simplified block diagram of the ET amplifier is shown in Figure 4-3.

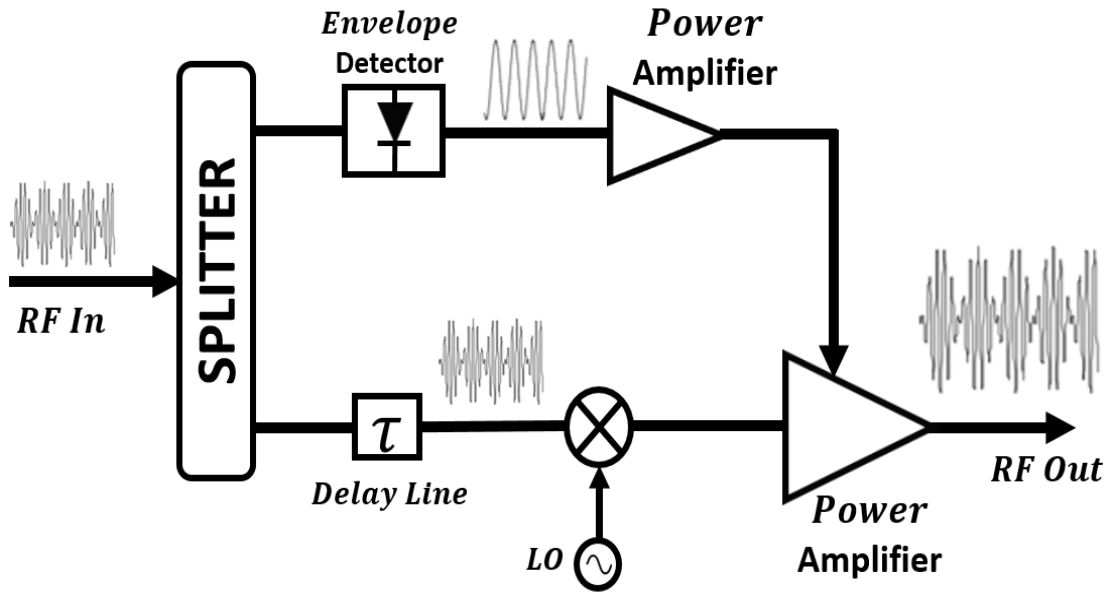

Figure 4-3 The block diagram of ET transmitter

4.4 The Doherty power amplifier

The simplified block diagram of the Doherty amplifier, initially proposed by William H. Doherty in 1936 [1] is illustrated in Figure 4-4. Using the Doherty architecture, several authors (such as in [40]) have reported higher power-added efficiency (PAE) of the PA, for the infrastructure applications. In [41], authors have used a dual path Doherty architecture, where they have shown the improvements in the power added efficiency (PAE) using the adaptive phase alignment scheme for the main and the auxiliary PA paths.

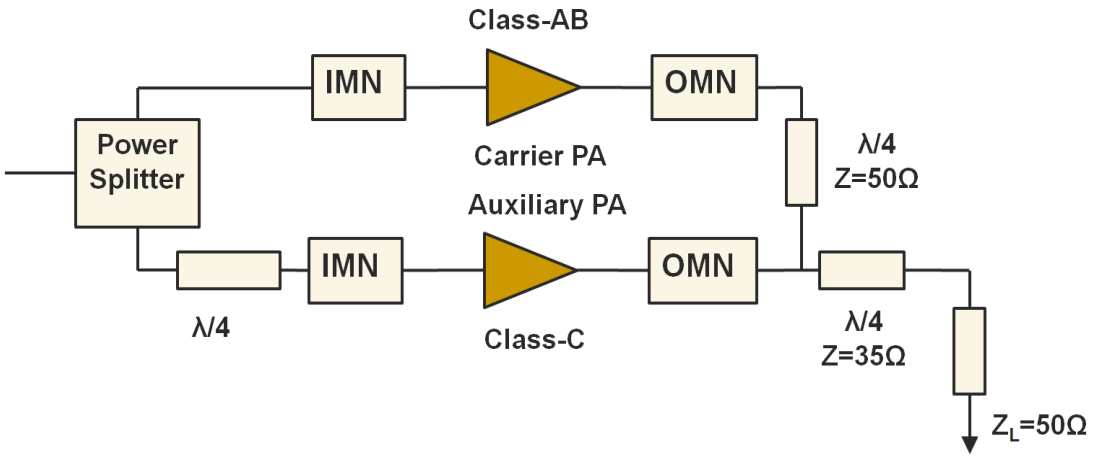

Figure 4-4 – Simplified block diagram of a Doherty power amplifier

The Doherty amplifier is mainly composed of two components, the main (or carrier) amplifier and the auxiliary (or peaking) amplifier. The main PA is typically biased to operate in Class-AB (or Class-B) mode and the auxiliary PA is biased to operate in Class-C mode. The input RF signal is equally split by a power divider, to each amplifier with a difference of 90^o in phase. After the signals are amplified, the signals are recombined using a quarter wavelength transformer (λ/4). In addition, the input matching networks (IMN) and output matching networks (OMN) are also used.

The basic operation of the Doherty PA is illustrated in Figure 4-5. For the low input signals, the auxiliary PA remains off and the main amplifier is presented with load impedance (100 Ω) which enables higher efficiency. However, as the input signal increases in power, the Class-C auxiliary PA gradually turns on and both the main and the auxiliary PAs are presented with load impedances that enable maximum output power. At the peak output power, both the PAs are presented with 50Ω load impedance where the main PA is operating at near saturated efficiency and the auxiliary PA is also operating at high efficiency as it is biased in Class-C mode. This variation of impedances seen by the main and auxiliary PAs with the increasing input power is illustrated in Figure 4-6. This effect is known as 'active load-pull'.

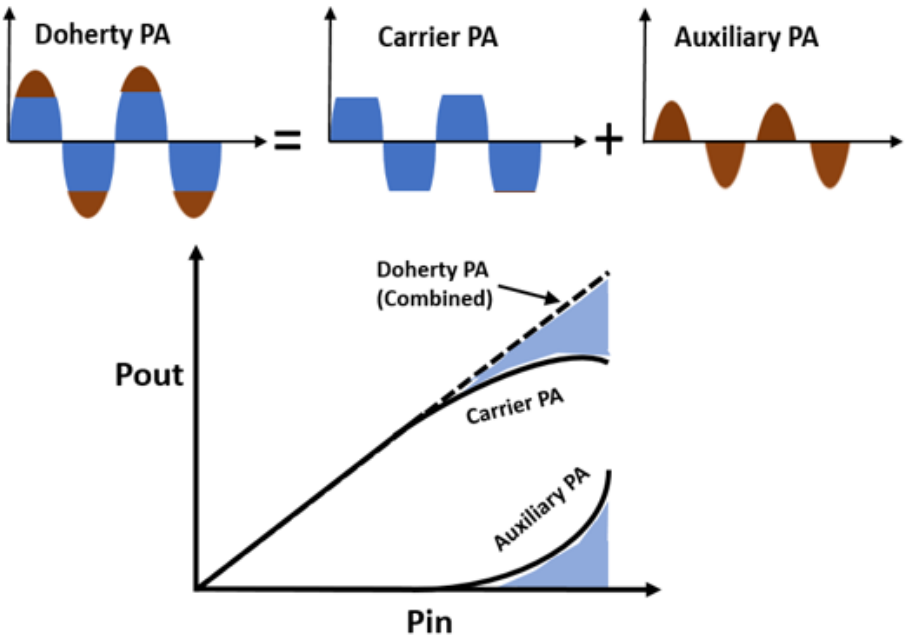

Figure 4-5 - Basic operation of a Doherty PA

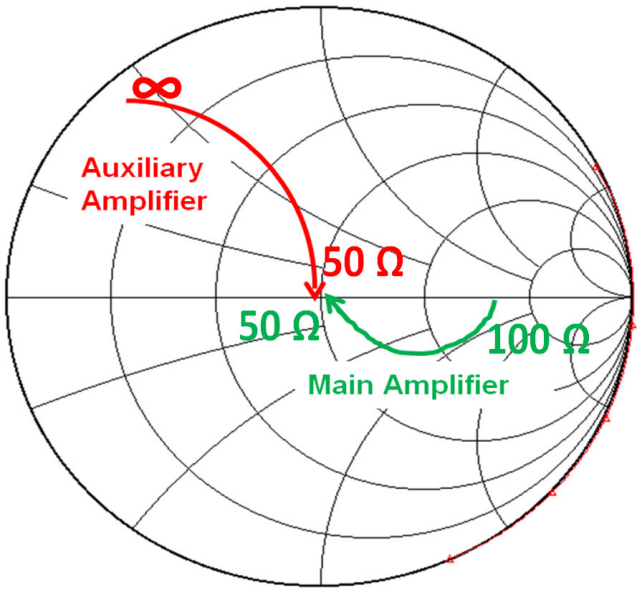

Figure 4-6 – The active load-pull in the Doherty PA. Impedances with increasing power

In a 'classic' Doherty configuration, an impedance inversion factor of 0.5 is selected that means that the main PA is presented with load impedance of 100Ω when the auxiliary PA is off. This impedance inversion factor selection results in saturation of the main PA at 6-dB back-off from the peak output power, where the output voltage of the main PA starts clipping. The auxiliary PA biased in Class-C mode, turns on at 6-dB back-off from peak output power and starts complementing the saturated main PA. The current and voltage waveforms of the main and auxiliary PAs of a typical Doherty amplifier are illustrated in Figure 4-7. As seen in the voltage waveform plot, voltage output of the main PA starts clipping at the onset of the auxiliary PA operation.

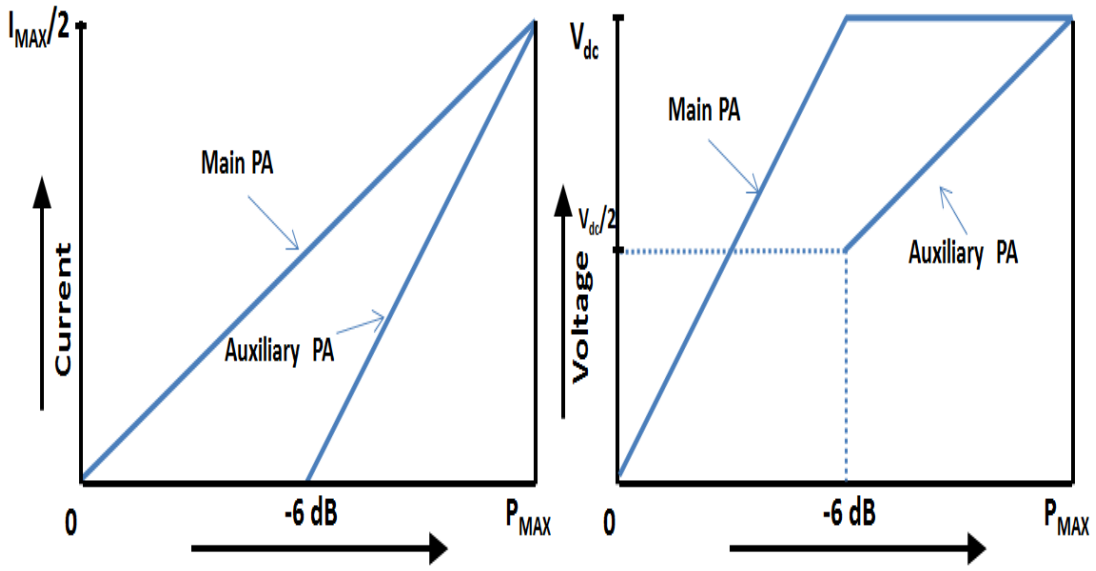

Figure 4-7 - Current and voltage waveforms of the main and auxiliary PAs of a typical Doherty PA

Modern complex modulation schemes inherently have high peak-to-average power ratio (PAPR). Hence, it is desirable to have the second peak in the efficiency curve (at 6-dB back-off) of the Doherty PA near 'P_{SAT} – PAPR'. Ideal efficiency characteristics of the Doherty PA and Class-B PA are compared in Figure 4-8, where second efficiency peak achieved at 6-dB back-off from the peak output power, makes the Doherty PA obvious choice for the modern transmitters employing complex modulation schemes.

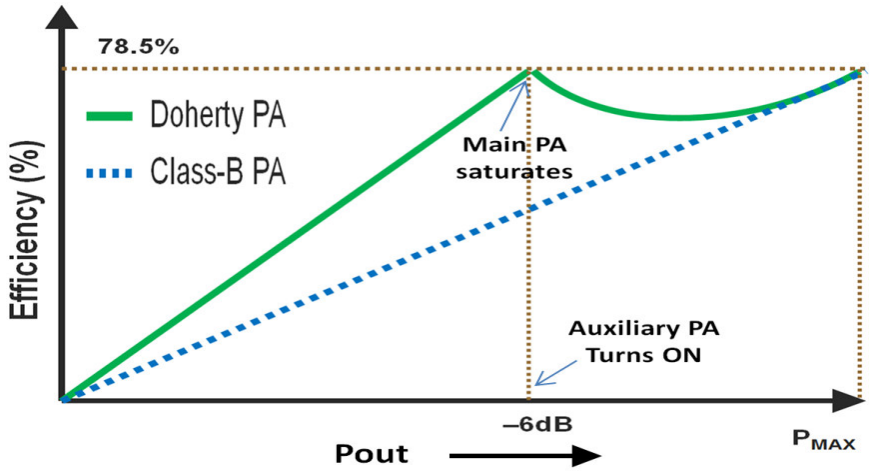

Figure 4-8 – Ideal efficiency characteristics of a class-AB and a Doherty PA

*4.4.1 Linearity considerations of the Doherty Amplifier (**this research**)*

The Doherty PA is highly non-linear and exhibits strong memory effects especially for the high-power infrastructure applications. In this section, various aspects of the linearity of a Doherty PA are presented.

4.4.1.1 Doherty PA: Non-linearities and memory effects

Figure 4-9 shows the measured AM-AM and AM-PM characteristics of 80W class-AB and class-C PAs, whereas Figure 4-10 shows the AM-AM and AM-PM response of a 240W Doherty PA. Most of the non-linearity of the Doherty PA is attributed to the auxiliary PA, which exhibits high AM-PM and AM-AM distortions when operated in Class-C mode. The static non-linearities of the high-power Doherty PA can be modeled with the polynomial of order up to 11.

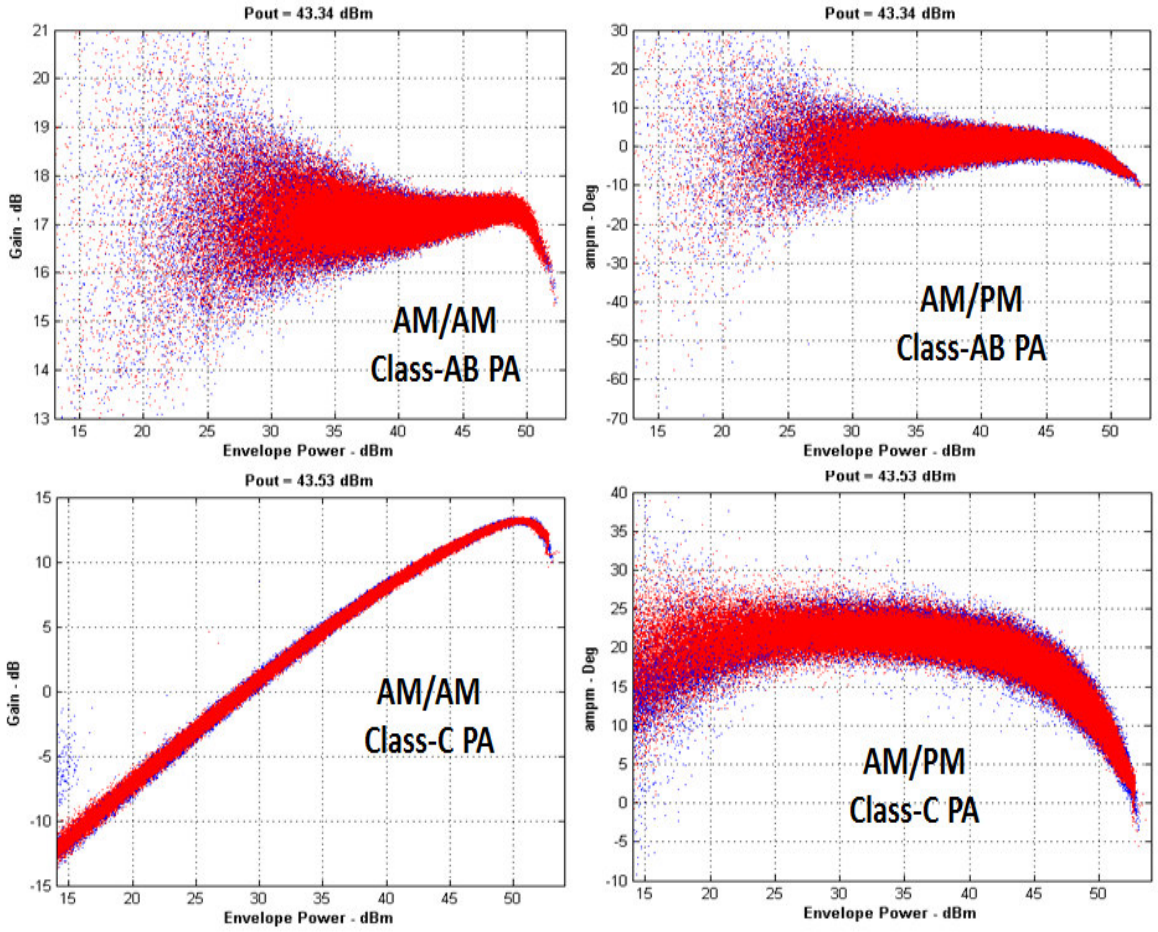

Figure 4-9 AM-AM and AM-PM characteristics of the class-AB, class-C PAs

The Doherty PA is also known to exhibit significant short-term and long-term memory effects. These memory effects can be classified as linear or non-linear. Linear memory effects mainly arise from the frequency response caused by the matching networks. The cause of non-linear memory effects can be attributed to non-linear bias networks, parasitics, thermal feedback, and traps. Accurate identification of the non-linearities and memory effects of a PA is of crucial importance in the development of predistorter model with acceptable linearizability.

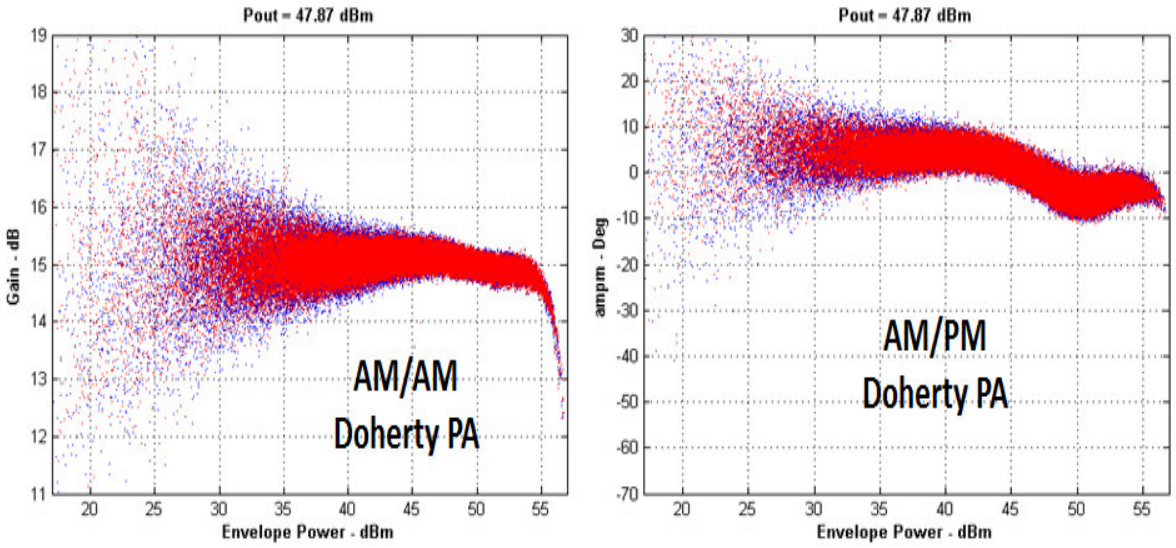

Figure 4-10 - AM-AM and AM-PM characteristics of a Doherty PA

4.4.1.2 Memory residuals (MRs) and two-tone characterization

The Memory Residual (MR) concept, initially presented in [49], is a figure-of-merit (FOM) which indicates the amount of memory present in a PA. When the PA is operated with signals of different bandwidth, this FOM provides a useful insight to the designer about the linearizability of the PA. A two-tone signal of increasing tone spacing and varying power is used for the envelope simulation with large signal model of a Doherty PA circuit. From the time-aligned complex input and output voltages (*Vin* and *Vout*), the modeled static output voltage ($Vout_{Static}$) is calculated using the series expansion shown in (4.3).

$$Vout_{Static}[n] = \sum_{p=1}^{P} \alpha_p V_{in}[n] \left| V_{in}[n] \right|^{p-1} \tag{4.3}$$

Where, α_P's are complex model coefficients. P is the maximum polynomial order. Mathematically, the MR is defined as

$$MR = 20 \cdot \log\left(\frac{rms(Vout_{memory} - Vout_{Static})}{rms(Vout_{memory})} \right) \tag{4.4}$$

Where, $Vout_{memory}$ is the modeled output with the inclusion of the memory effects. Equation (2.3) introduced in Chapter 2, can be used to calculate $Vout_{memory}$. The MR calculated for a nominal 80W Doherty PA (Figure 4-11, left) shows that the MRs have increasing trend with increasing tone spacing which indicates that the Doherty PA exhibits strong memory effects with the increasing power as well as the increasing tone-spacing. The constant MR contours (Figure 4-11, right) show that same MR performance for wider tone-spacing is only possible at lower output power levels. It is shown in [49] that MR trends illustrated in Figure 4-11 are directly related to the linearizability of the PA when operated with the (3G/4G) modulated signals.

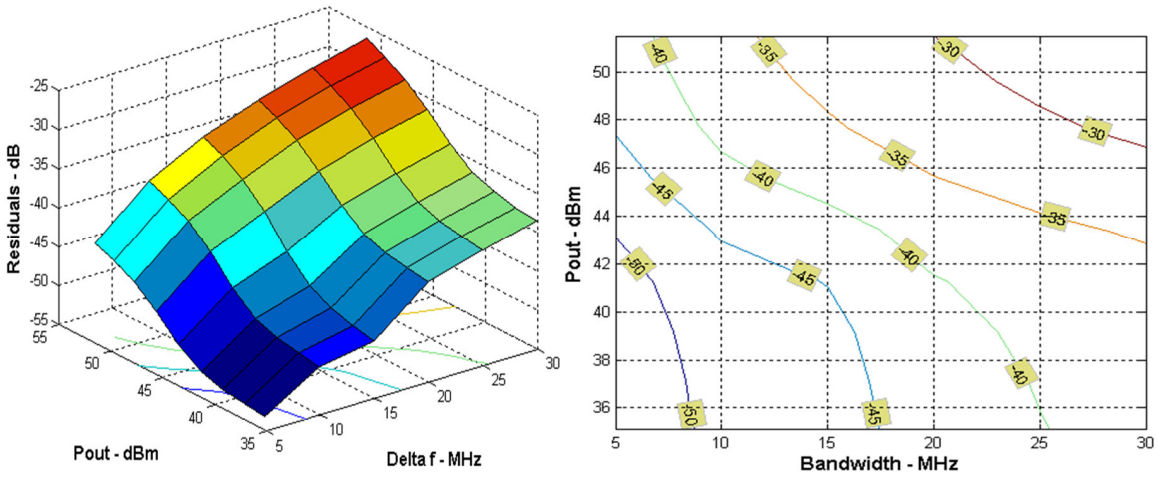

Figure 4-11 - Two-tone characterizations. MR is dB, constant MR contour plot

4.4.1.3 Linearization using digital predistortion

The memory polynomial (MP) scheme and the pruned Volterra (PV) scheme introduced in earlier chapter, are used to linearize a nominal 80W Doherty PA operating at 2.14 GHz. The digital predistortion (DPD) characterization is performed using WCDMA test signals of increasing bandwidth (5~20 MHz, WCDMA-010 ~ WCDMA-1001). For measuring linearity, the adjacent channel power ratio (ACPR) is measured at the offset of 5MHz from the carrier frequency using a spectrum analyzer. The measured ACPR performance as shown in Figure 4-12, compares the performance of the MP and the PV predistorters. The PV predistorter includes carefully selected (pruned) Volterra cross-terms which improve the linearizability performance. It is shown in [49] that with increasing signal bandwidths, the degradation in the linearity performance of the PV scheme is significantly lower than that of the MP scheme.

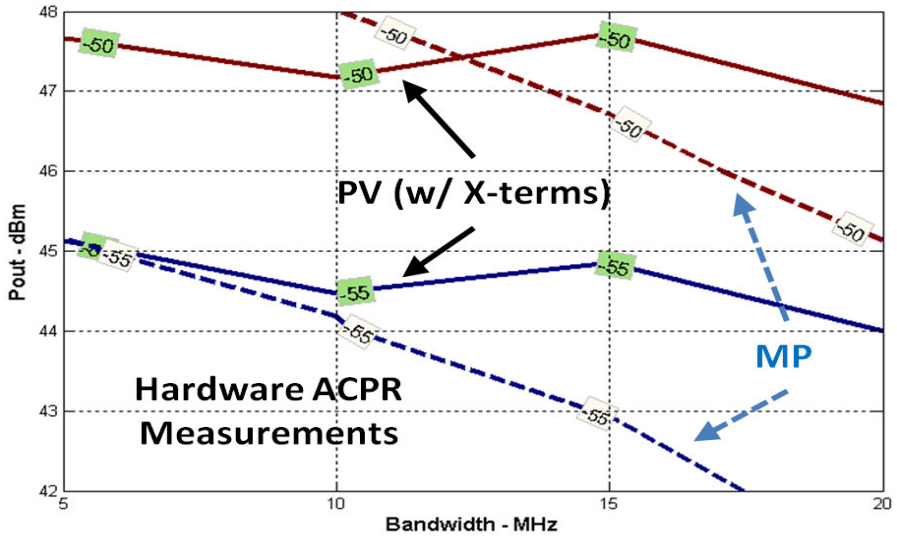

Figure 4-12 - Measured DPD performance: PV with Volterra X-terms compared with MP [42].

4.5 Efficiency enhancement: Impact of crest factor reduction (CFR) and digital predistortion (DPD)

Modern spectrum efficient modulations scheme such as 3G/4G exhibit high peak-to-average power ratios (PAPR). This constrains the PA to be operated at large back-off regions. A power amplifier is most efficient but highly non-linear near the peak powers. To meet the linearity specifications without the DPD and CFR, a PA must be operated at large back-off region from the peak power, which results in very low efficiency of operation. Both the DPD and CFR help in reduction of the back-off from peak power, where the PA can meet linearity conditions at higher average powers. This results in improvement of the efficiency of operation.

To demonstrate the impact of DPD, example plots of the power-added efficiency (PAE) and the ACLR performance plots are shown in Figure 4-13, reproduced from [43], where authors claim 1.9 dB reduction in the back-off with the DPD, which improved the efficiency by ~9%.

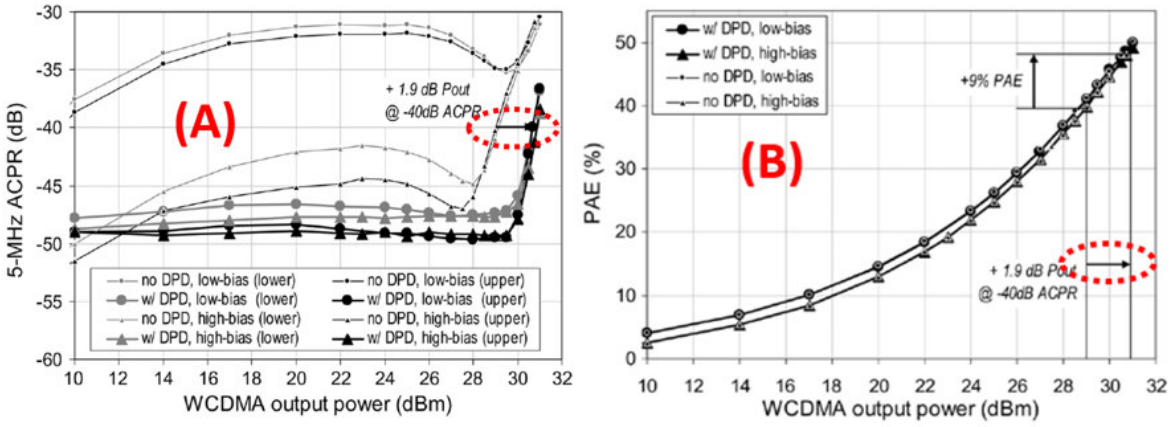

Figure 4-13 Example plot showing the impact of DPD on back-off reduction. (A) ACLR Performance, (B) PAE performance [43]

The CFR offers the reduction in PAPR by limiting the peaks in the waveform; hence the PA can be operated at higher average powers with reduced back-off from peak power (see example in Figure 4-14). This results in improving the efficiency of the PA. The reduction in PAPR comes at the cost of additional in-band distortions, which degrades the EVM. This puts a maximum limit up to which a PAPR reduction can be achieved, without violating the specifications for EVM.

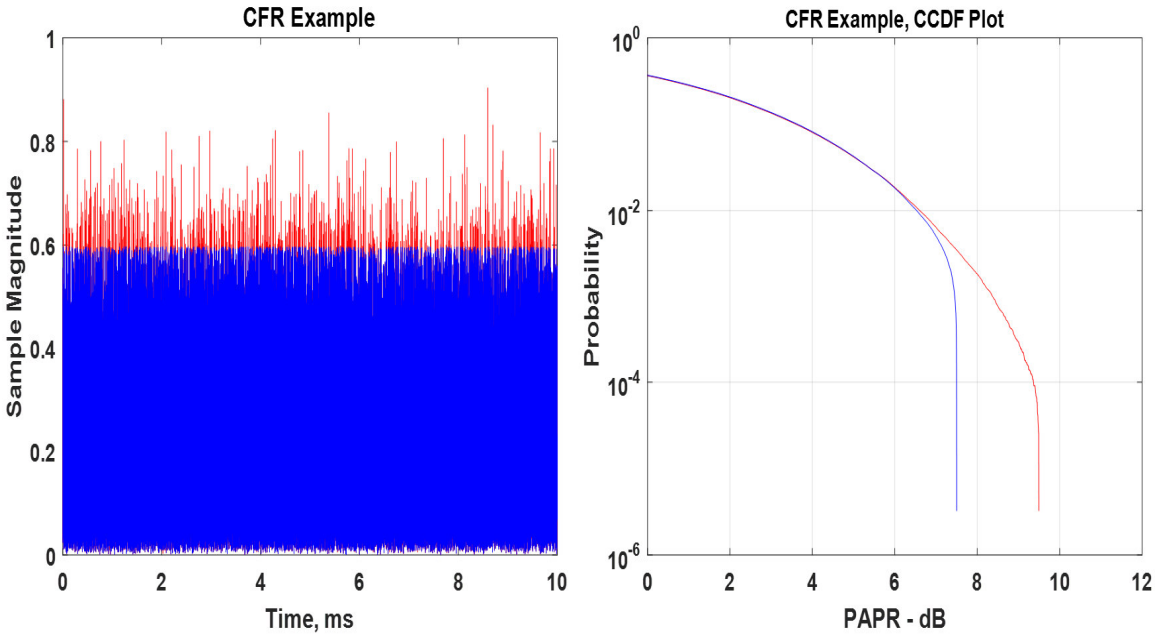

Figure 4-14 An example of PAPR reduction using CFR

CHAPTER 5. DIGITALLY-ASSISTED DOHERTY POWER AMPLIFIER

The Doherty power amplifier (PA) architecture is a widely adopted technique, especially for the infrastructure or base-station applications, because of its simpler architecture, linearizability and improved efficiency at average power levels. The Doherty PA in its simplest form is composed of a Main (or Carrier) PA and an Auxiliary (or Peaking) PA. The Main PA is typically biased to operate in class-AB mode and the Auxiliary PA is typically biased to operate in Class-C mode. In a conventional Doherty PA, an RF splitter and a quarter wavelength line is used to split the input RF signal into two paths that are separated by 90° in phase. These signals are fed to Main and Auxiliary PAs. The outputs of Main and Auxiliary PA cells are combined using quarter wavelength transformer using a technique called load modulation. Because of the differences in biasing, the Main PA is operating all the time but Auxiliary PA is only operating near peak output levels. This technique helps maintain the higher efficiency at the average power levels, backed off from peak power.

In previously proposed digitally assisted Doherty PA architectures (as shown in Figure 5-1), rather than simply splitting the input signal in analog fashion, separate RF input signals for the Main and Auxiliary PAs are digitally created [41,44]. The flexibility to process the input signals of the two PAs separately allows more accurate adaptive phase adjustment between the input RF signals fed to Main and Auxiliary PAs. This results in improved load modulation allowing for higher efficiency operation. In addition, wasted

power into the Auxiliary path can be reduced for lower power levels, thus further improving the efficiency of the PA.

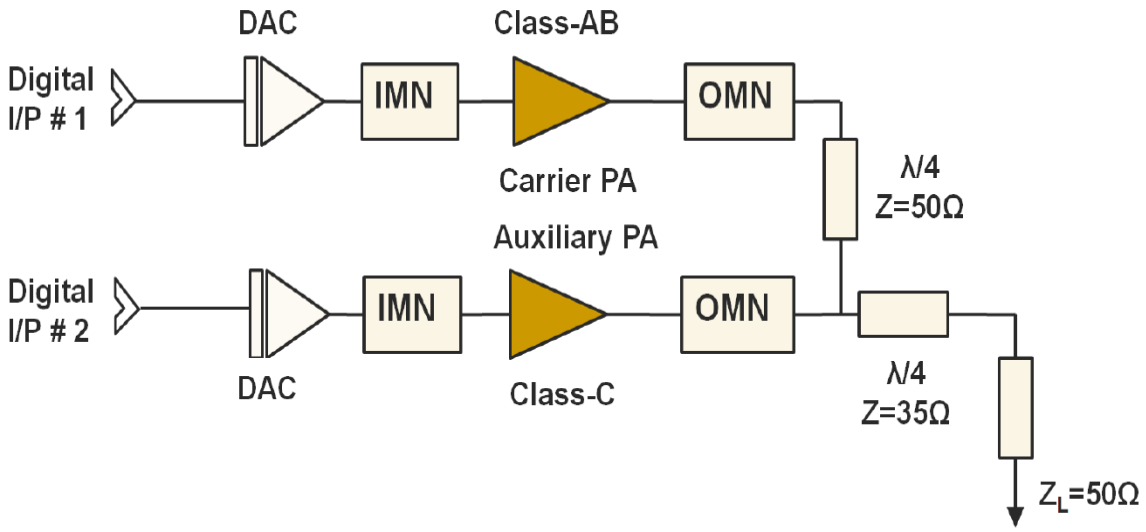

Figure 5-1 – Simplified structure of digitally-assisted Doherty PA

In [41,44], the authors discuss efficiency enhancement technique using a Digital Doherty scheme, but did not address improved optimization of linearity through DPD techniques specifically adapted for the digital architecture. The research presented in this thesis, demonstrates for the first time an improved DPD linearization solution for digitally assisted Doherty PAs. This new architecture includes digital thresholding to provide "soft" thresholding, and segmented linearization to allow the use of greater complexity only when required at high power levels. As a result of these modification, the new architecture demonstrates increased bandwidth for higher power (>90W avg.) PAs designed for macro cell infrastructure applications.

5.1 Efficiency Enhancement

Efficiency enhancement is achieved by using two methods which are described below.

5.1.1 Phase Optimization

In a conventional Doherty configuration, an RF splitter is used to split the input waveform into two signals, separated in phase by 90°. These are fed to Carrier and Auxiliary PAs (symmetrically or asymmetrically based on sizes of Carrier/Auxiliary PA cells). As previously reported in [41], this phase split may not result in most efficient operation of a Doherty PA.

For the PA used for validation (Symmetric LDMOS Doherty PA, Centre Frequency=1845MHz), phase characterization is carried out using single carrier LTE20MHz waveform with PAPR of 10dB. The PAPR compression is the metric used to assess the linearity of the PA. For simplicity, only symmetric power split case is shown where equal power is provided to the Carrier and Auxiliary PA cells. The trends shown in Figure 5-2 will be typical for the most Doherty PAs. The target phase adjustment offset for the best efficiency is shown in Figure 5-2. But this efficiency improvement is achieved at the cost of linearity degradation which is discussed in a later section.

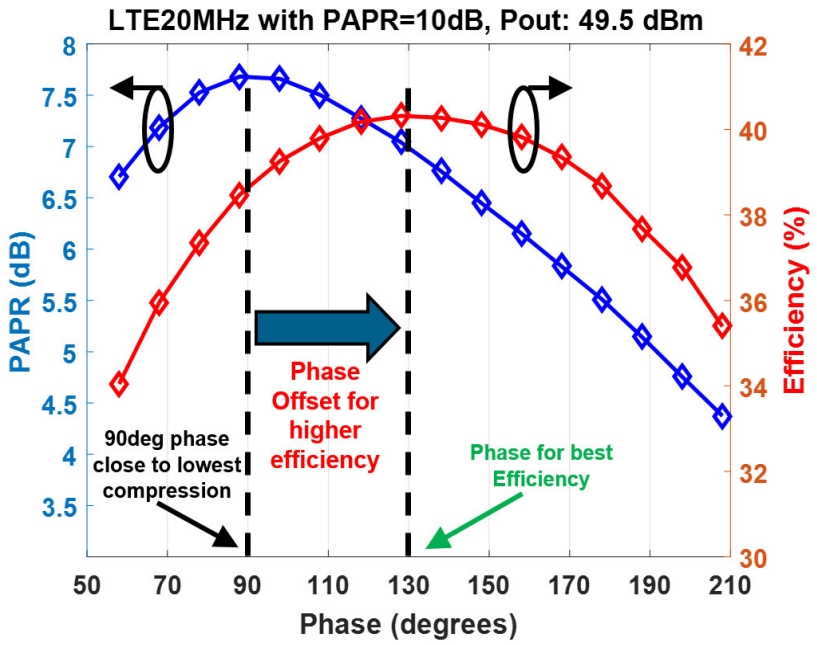

Figure 5-2 – PA characterization for optimum phase (Delta: 30~40 Degrees)

5.1.2 Soft Thresholding of the Auxiliary PA Waveform

In conventional Doherty architecture, Auxiliary PA is biased to operate in Class-C. Ideally the Auxiliary PA should only operate during the peaks, but in practice it starts conducting earlier which causes some degradation in efficiency. With digital thresholding of the input waveform to Auxiliary PA, its activation at low power levels can be minimized and early conduction can be reduced to improve the efficiency. As hard-limiting threshold can cause severe degradation in linearity, an exponentially decaying function (Figure 5-3) with programmable time constant is used to allow for the softer thresholding.

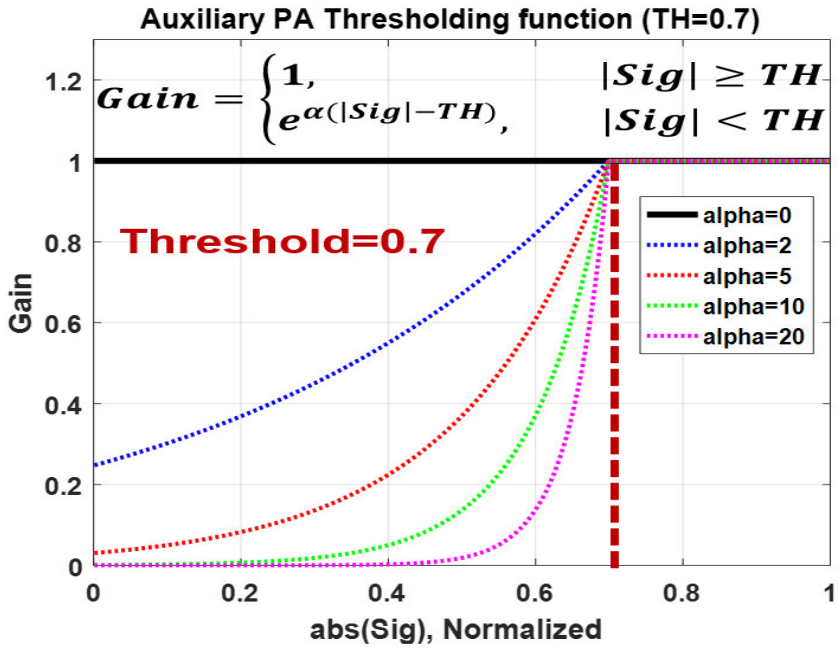

Figure 5-3 – Digital soft thresholding scheme (Example: Threshold= 0.7)

The configurability of the digital threshold limit and the time constant facilitates the tuning for the best optimized linearity-efficiency tradeoff for the Main and the Auxiliary PAs in a practical DPD system.

5.2 Linearization using segmented DPD scheme

Conventional use of a single-segment DPD architecture for the entire operating range of a Doherty PA requires a complex architecture that is unnecessary the lower end of the PA power range. As a result, adaptation of DPD coefficients can be inadequate and too slow to allow for wideband operation. To improve upon this limitation, the operation of the Doherty PA can be subdivided into two regions: *(i)* A lower power region where only the Main PA is operating, and *(ii)* a higher power region where the Main and the Auxiliary PAs are both operating. In upper range of operation, the PA exhibits more significant

higher order nonlinearities and stronger memory effects. The digitally assisted Doherty PA architecture is ideally suited for a segmented DPD approach [45] where first segment of DPD of a simpler nature is used to model the lower range and the second segment of the DPD with more complexity is employed to model the upper range of the Doherty PA operation.

In this work, the segmented DPD is based on the generalized memory polynomial (GMP) scheme [28, 18]. For simplicity, only two segments are used for the segmented-DPD scheme here (with ~130 total number of DPD coefficients). For comparison, a conventional DPD scheme is also based on the GMP scheme. Complexity comparison of the two schemes is shown in Table I.

Table 2 – Complexity comparison (Conventional Vs. Segmented DPD)

DPD Scheme	ALGO	Segment No.	No. of Coeff.	Max. Poly. Order	Max. No. of NL functions
Conventional	GMP	N/A	130	11	20
Segmented	GMP	1	46	5	8
		2	86	7	12

5.2.1 Mathematical description of the segmented DPD scheme for a digitally-assisted Doherty PA architecture

For the digitally-assisted Doherty PA architecture, the output of a generalized memory polynomial (GMP) based segmented DPD actuator can be shown as in equation (6.1). For the simplicity of expression, an unpruned GMP model is given in equation (6.1).

$$z(n) = \begin{cases} \sum_{r=0}^{R}\sum_{q=0}^{Q}\sum_{p=0}^{P} a_{p,q,r}|x_1(n-q)|^p.x_1(n-r), & x_1 \in x, |x| < V_{PD} \\ \sum_{r=0}^{R}\sum_{q=0}^{Q}\sum_{p=0}^{P} a_{p,q,r}|x_2(n-q)|^p.x_2(n-r), & x_2 \in x, |x| \geq V_{PD} \end{cases} \quad (6.1)$$

Where, the number of segments are 2. x(n) and z(n) are the input and output of the DPD actuator, respectively. The order of polynomial is given by P, and the number of taps are denoted by M and R. For simplicity, the GMP model expression shown in equation 6.1 is unpruned. The threshold of the DPD actuator is denoted by V_{PD}. The DPD coefficients are represented by $a_{p,q,r}$. In vector notation, the non-linear functions in equation (6.1) can be represented as a linear combination of kernel functions (shown as $\mathbf{U_1}$ and $\mathbf{U_2}$) based on the selected GMP models for each segment.

$$\mathbf{z} = \begin{cases} \mathbf{U_1 a_1}, & \mathbf{U_1} = \boldsymbol{f}(\mathbf{x_1}) \\ \mathbf{U_2 a_2}, & \mathbf{U_2} = \boldsymbol{f}(\mathbf{x_2}) \end{cases} \quad (6.2)$$

Where, f(.) represents the non-linear function. The DPD coefficients of first and second segments are denoted as $\mathbf{a_1}$ and $\mathbf{a_2}$, respectively. The digital outputs to the main ($\mathbf{s_{Main}}$) and auxiliary PA ($\mathbf{s_{Auxiliary}}$) cells are given in equations (6.3) and (6.4).

$$\mathbf{s_{Main}} = \mathbf{z} \tag{6.3}$$

$$\mathbf{s_{Auxiliary}} = \begin{cases} \boldsymbol{z}.\boldsymbol{e}^{\propto(|\boldsymbol{z}|<\boldsymbol{V_{DH}})}, & |\boldsymbol{z}| < V_{DH} \\ \boldsymbol{z}, & |\boldsymbol{z}| \geq V_{DH} \end{cases} \tag{6.4}$$

Where, $\boldsymbol{V_{DH}}$ is the threshold for splitting the power between the main and the auxiliary PA paths. The starting value of $\boldsymbol{V_{PD}}$ should be identical to $\boldsymbol{V_{DH}}$, but afterwards it may be tweaked (for best linearity performance) to compensate for the expansion of the PAPR of the signal **z**, at the output of the predistorter. Using an indirect learning scheme (as shown in Figure 5-4), identical GMP models are used for the pre-distorter and the post-distorter. The matrices $\mathbf{W_1}$ and $\mathbf{W_2}$ represent the non-linear functions f(.), which are linear combination of kernel functions based on the GMP models used for the time-aligned feedback components $\mathbf{y_1}$ and $\mathbf{y_2}$ (for the corresponding inputs $\mathbf{x_1}$ and $\mathbf{x_2}$). The estimated pre-distorter output ($\hat{z}$) after adaptation is shown in equation (6.5).

$$\hat{\boldsymbol{z}} = \begin{cases} \hat{\boldsymbol{z}}_1 = \mathbf{W_1}\mathbf{a_1}, & \mathbf{W_1} = \boldsymbol{f}(\mathbf{y_1}), & \mathbf{y_1} \triangleq \mathbf{x_1} \\ \hat{\boldsymbol{z}}_2 = \mathbf{W_2}\mathbf{a_2}, & \mathbf{W_2} = \boldsymbol{f}(\mathbf{y_2}), & \mathbf{y_2} \triangleq \mathbf{x_2} \end{cases} \tag{6.5}$$

Using the QR decomposition ($\mathbf{W_1} = \mathbf{Q_1}\mathbf{R_1}, \mathbf{W_2} = \mathbf{Q_2}\mathbf{R_2}$), the least-square solution of equation (6.5) is provided in the equations (6.6) and (6.7). The calculated DPD coefficients of the first and second segments are denoted by $\hat{\boldsymbol{a}}_2$ and $\hat{\boldsymbol{a}}_2$, respectively.

$$\boldsymbol{a_1} = \hat{\boldsymbol{a}}_1 = \boldsymbol{R_1^{-1}}\boldsymbol{Q_1^H}\,\hat{\boldsymbol{z}}_1 \tag{6.6}$$

$$\boldsymbol{a_2} = \hat{\boldsymbol{a}}_2 = \boldsymbol{R_2^{-1}}\boldsymbol{Q_2^H}\,\hat{\boldsymbol{z}}_2 \tag{6.7}$$

Where, $(.)^H$ represents a complex conjugate transpose and $(.)^{-1}$ represents an inverse of a matrix.

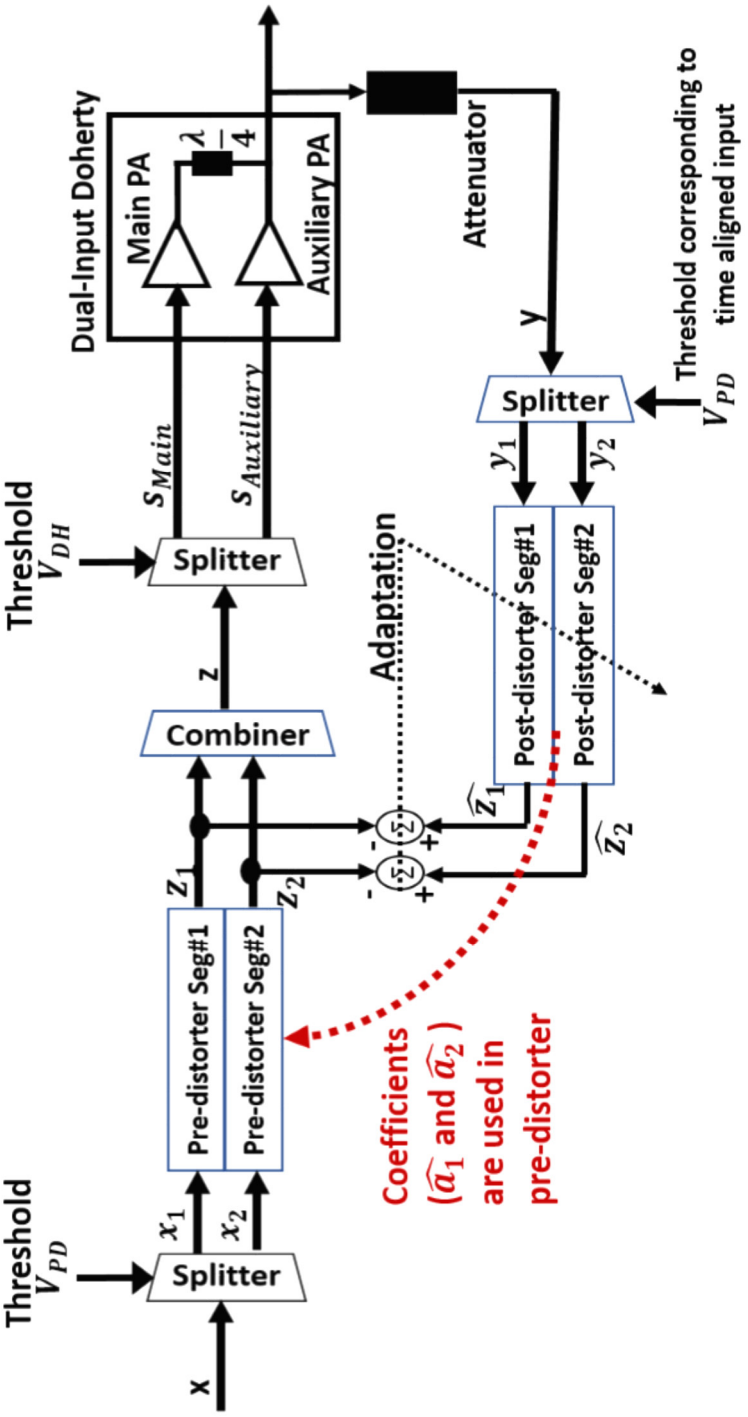

Figure 5-4 – The Segmented DPD scheme based on indirect learning architecture

5.3 Hardware Validation

For hardware validation, a symmetric LDMOS Doherty PA (based on two matched NXP AFT18S230 devices, shown Figure 5-5 The dual-path Doherty lineup (Driver: MW7IC2020N, Final Stage: AFT18S230). with P3dB=~57dBm (500W), operating at center frequency=1845MHz is used. The video bandwidth of the PA is ~120MHz, which is quite suitable for the signal bandwidths up to ~40MHz. The intermodulation distortion products of the device are shown in Figure 5-6. For the DPD characterizations, two split 10MHz LTE carriers of instantaneous bandwidth of 40MHz and PAPR of 6.7dB are used. The CCDF plot of test waveform is shown in Figure 5-7.

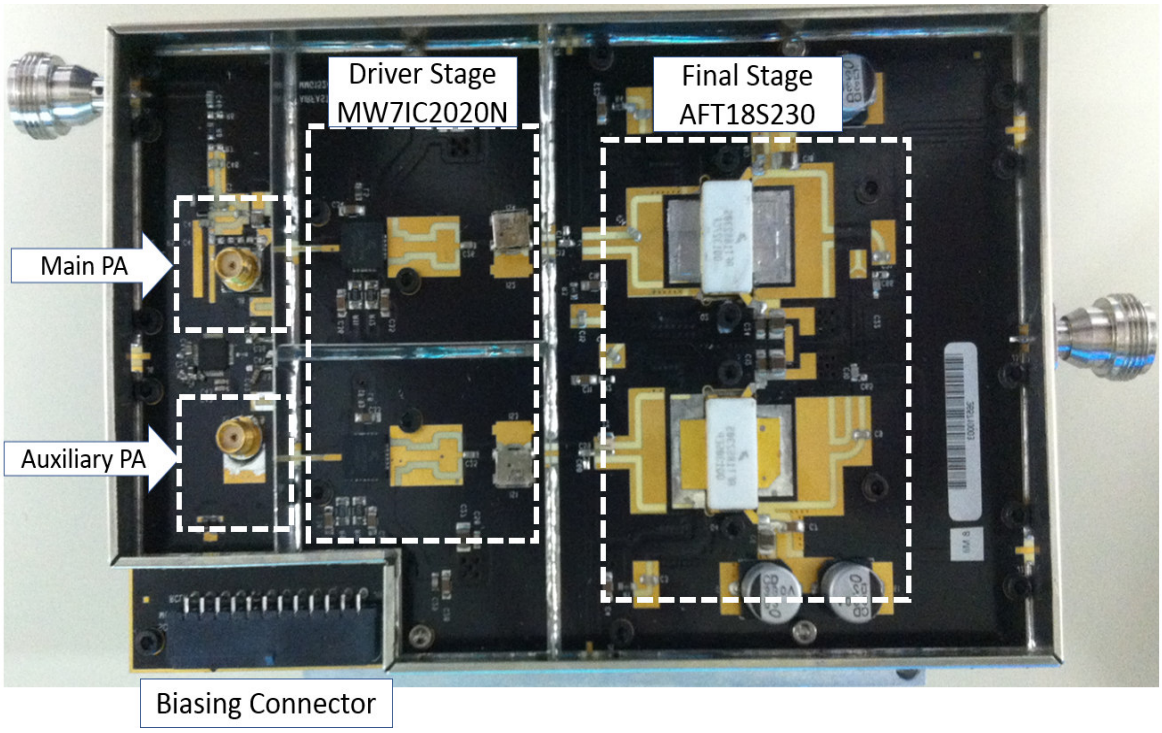

Figure 5-5 The dual-path Doherty lineup (Driver: MW7IC2020N, Final Stage: AFT18S230).

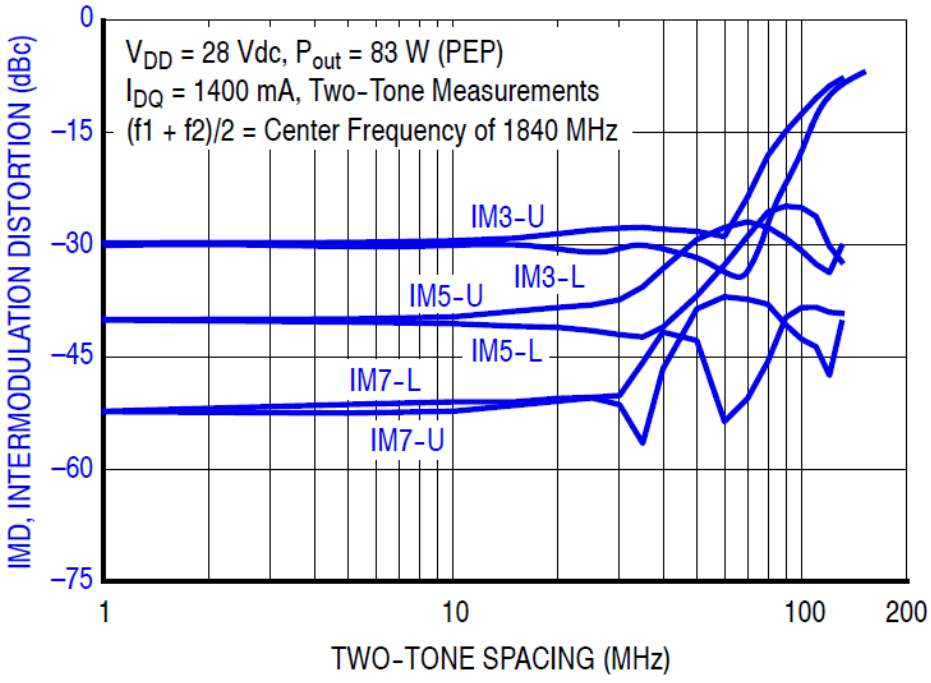

Figure 5-6 – Intermodulation distortion products vs. two-tone spacing (Source: Product datasheet AFT18S230, www.nxp.com)

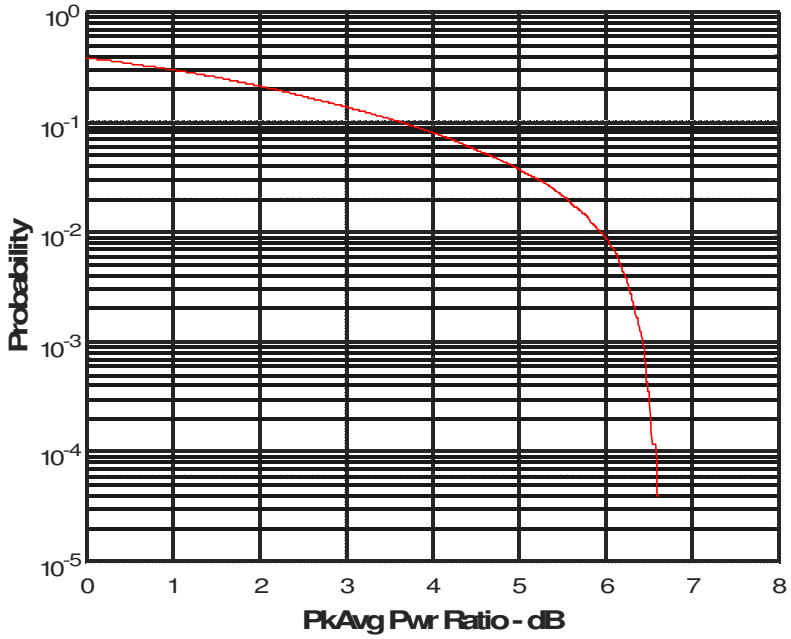

Figure 5-7 – CCDF plot of 2xLTE10MHz waveform with IBW=40MHz.

In the conventional Doherty Mode, when the phase adjustment and the Auxiliary PA thresholding are kept off, the linearization performance is quite good with both the conventional DPD scheme as well as the segmented DPD scheme (Figure 5-8), but the lineup efficiency (combined drain efficiency of driver and final stages) of the operation is low (Eff= 38.4% at Pout= 49.61dBm).

In the high efficiency mode, when the phase adjustment of 20°~40° offset is applied, along with the Auxiliary PA thresholding (using Threshold= 0.8, alpha= 3), the lineup efficiency of 42.36% is achieved at the output power of 49.64dBm. In this experiment, the phase adjustment contributed ~1.9% improvement in efficiency, and Auxiliary PA thresholding resulted in ~2.1% efficiency improvement (over all: 3.96% points). This is summarized in Table 3. These optimizations for efficiency result in degradation of the conventional DPD performance.

Table 3 - Efficiency enhancement summary at ~49.6 dBm Output Power.

Mode	Lineup Efficiency
Phase adjustment OFF Auxiliary thresholding OFF	**38.4**
Phase adjustment ON Auxiliary thresholding OFF	**40.24**
Phase adjustment ON Auxiliary thresholding ON	**42.36**

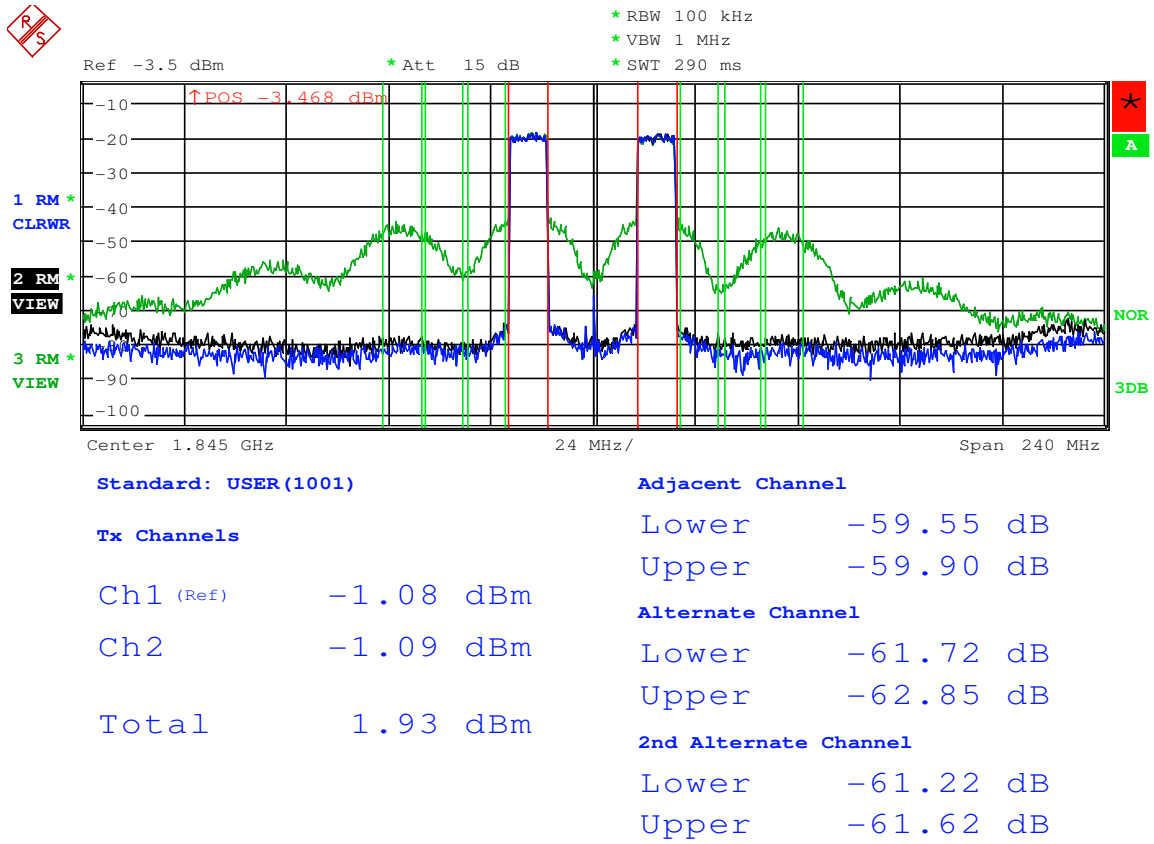

Figure 5-8 – The Phase Adjustment and Auxiliary PA thresholding are OFF, Pout=49.61dBm, Efficiency=38.4%. (Measured ACP, ADJ(L)/ADJ(H):: Green-Raw Linearity -29.3/-30.5 dBc, Black- Conventional DPD -58.5/-58 dBc, Blue- Segmented DPD -59.6/-59.9 dBc)

In high efficiency mode of the Doherty PA, the AM-AM/PM scatter plots in Figure 5-9 show that the DPD coefficients are not optimally converged for the conventional DPD architecture. In Figure 5-11, the black trace (showing the conventional DPD performance) has an adjacent channel power (ACP) level of -44dBc.

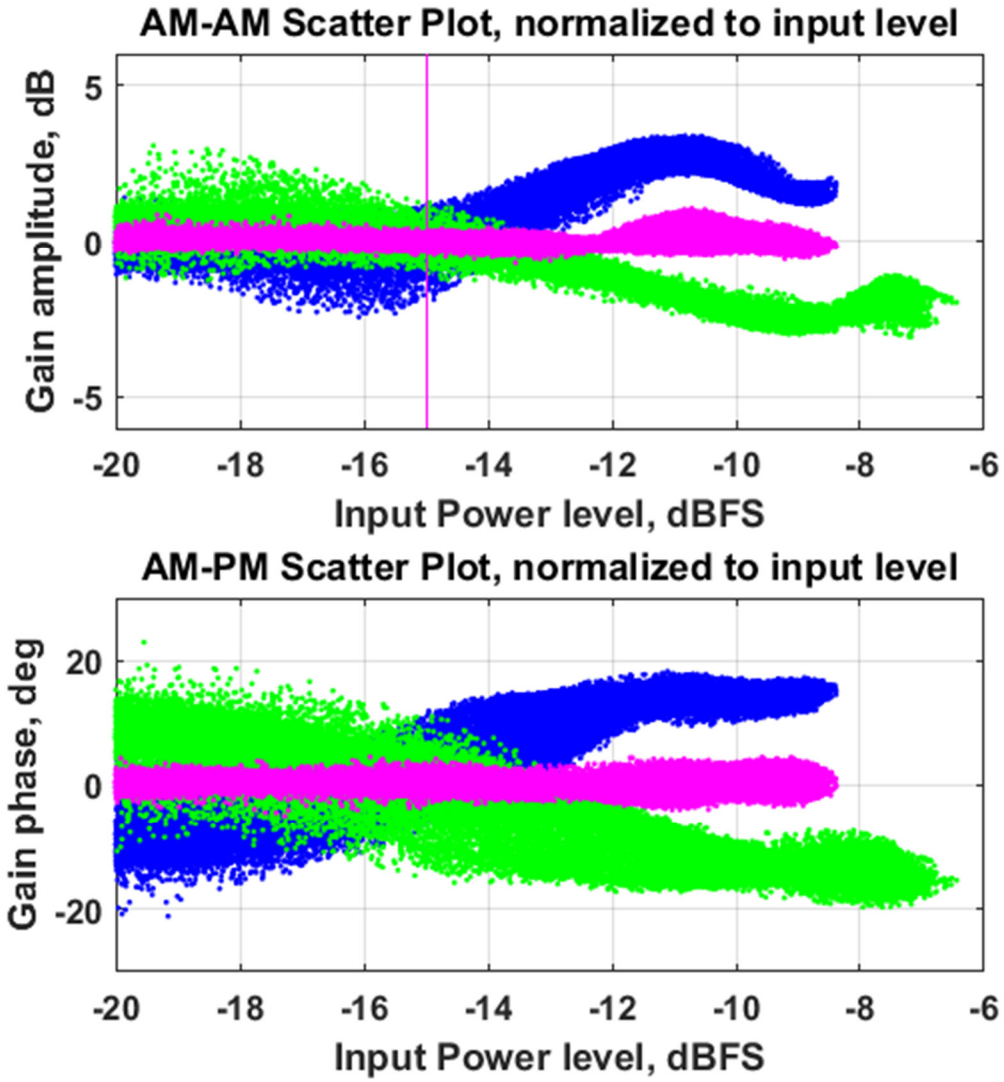

Figure 5-9 - The Measured AM-AM/PM Response (normalized to Input Power level, dBFS) of the Conventional DPD, Efficiency Enhancements are ON. (Blue- Predistorter, Green- PA, Magenta- Combined Response)

With the segmented DPD scheme, the AM-AM/PM scatter plots in Figure 5-10 show improved convergence. In Figure 5-11, the blue trace has ACP performance of better than -55 dBc, which is ~11 dB better than the performance achieved by using the conventional DPD scheme.

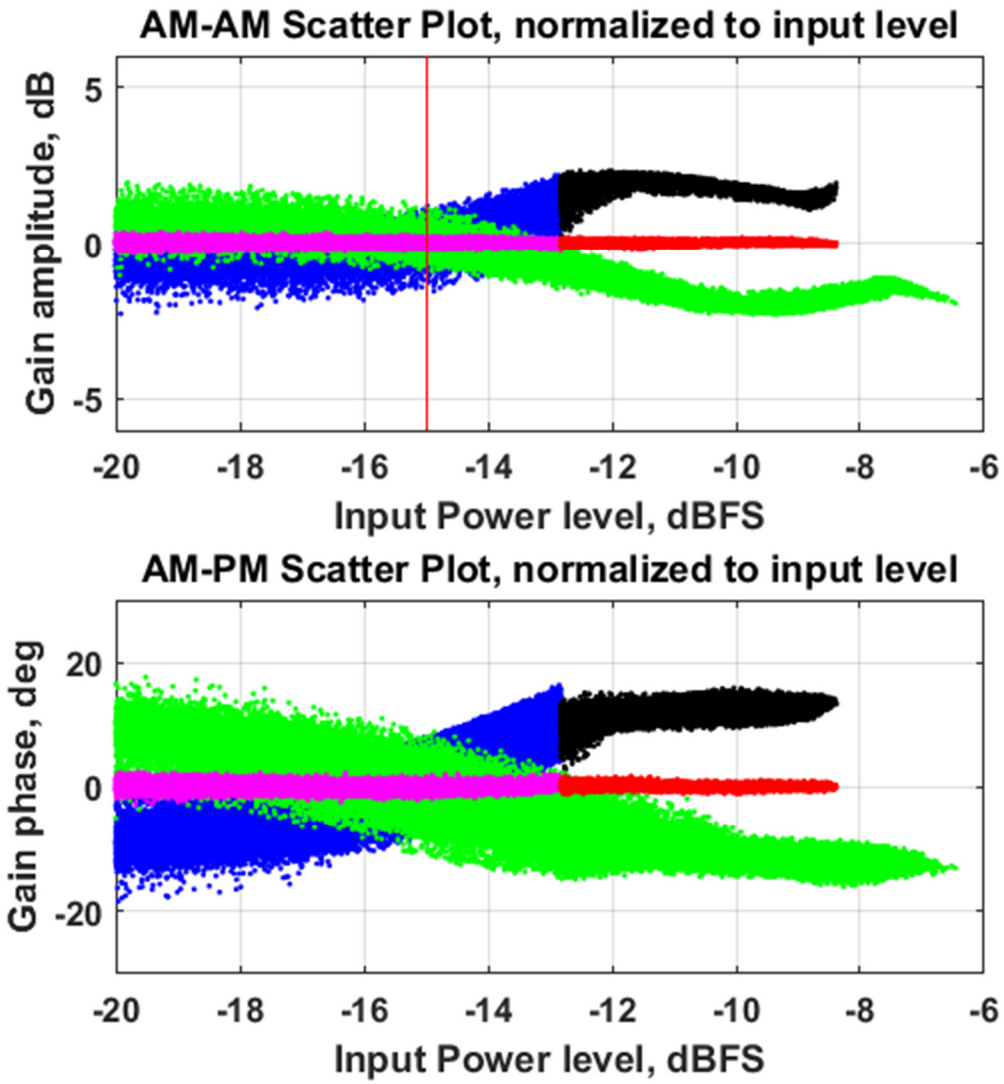

Figure 5-10 The Measured AM-AM/PM Response (normalized to Input Power level, dBFS) of the Segmented DPD, Efficiency Enhancements are ON. (Blue- Predistorter Seg#1, Black- Predistorter Seg#2, Green- PA, Magenta- Combined Seg#1, Red- Combined Seg#2).

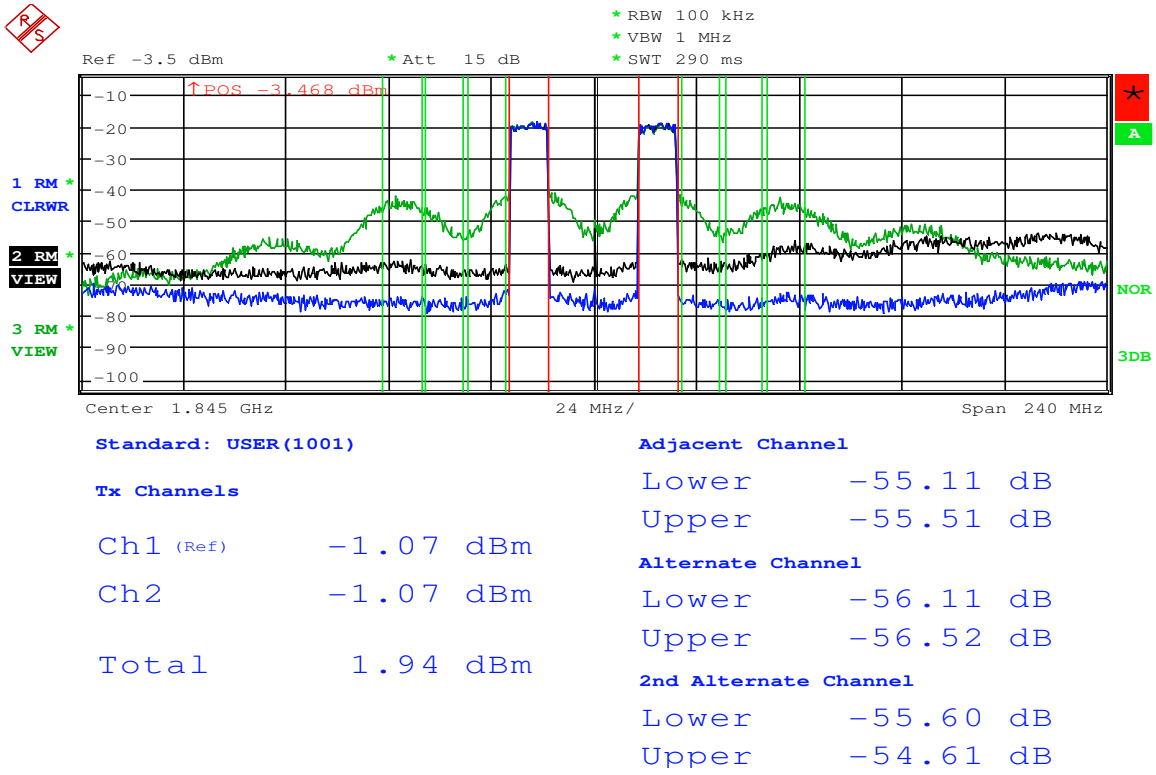

Figure 5-11 – The Phase Adjustment and Auxiliary PA thresholding are ON. Pout=49.64dBm, Efficiency=42.36%. (Measured ACP, ADJ(L)/ADJ(H):: Green- Raw Linearity -26.5/-27 dBc, Black- Conventional DPD -46/-44 dBc, Blue- Segmented DPD -55/-55.5 dBc)

The linearity performance of the conventional and segmented DPD schemes is summarized in Table 4.

Table 4 - Linearity performance summary.

Mode	DPD Off (dBc)		Conventional DPD (dBc)		Segmented DPD (dBc)	
	ADJ(L)	ADJ(H)	ADJ(L)	ADJ(H)	ADJ(L)	ADJ(H)
Phase adjustment OFF Auxiliary thresholding OFF	-29.3	-30.5	-58.5	-58	-59.6	-59.9
Phase adjustment ON Auxiliary thresholding ON	-26.5	-27	**-46**	**-44**	**-55.1**	**-55.5**

5.4 Summary

Using ~57dBm (500W) peak power Doherty PA, an overall lineup efficiency improvement of ~3.96% is demonstrated with the improved phase adjustment and the Auxiliary PA thresholding for the linearization of 2xLTE10MHz with 40MHz IBW. The segmented DPD approach is used to improve the linearity to -55dBc benchmark, which is ~11dB better than the linearity performance achieved using a conventional DPD scheme of similar complexity. According to best of author's information, such efficiency enhancement comparison for the dual-input Doherty architecture does not exist in literature, where similar quality of linearity of the PA is demonstrated with similar signal bandwidths at these higher power levels (500W Peak Power).

CHAPTER 6. CONCLUSIONS, CONTRIBUTIONS AND FUTURE WORK

The digitally-assisted RF circuits are constantly growing in demand. Use of the latest signal processing techniques have a potential of pushing the envelope in improving the performance metrics of the RF circuits. This thesis is a step towards this direction. The primary objective of this research is to use the signal processing techniques in the development of new efficiency enhanced, linearized power amplifier (PA) architectures. This efficiency improvement results in extended battery life in the handset applications and savings in energy costs for the infrastructure applications.

The efficiency enhancement technique for a dual-input Doherty PA is one of the main contributions of this work. This efficiency enhancement is achieved by two methods; first is by improvement of phase adjustments at the inputs of the Main and Auxiliary PA cells and second is by signal conditioning of the waveform being fed to the Auxiliary PA cell. The obvious trade-off of efficiency enhancement of the PA is the degradation of the linearity performance. The development of novel segmented-DPD architecture is the second major contribution of this work which is used to linearize the digitally-assisted Doherty PA in its high efficiency mode.

Using a 500W peak power Doherty PA, operating at center frequency of 1845MHz, overall efficiency improvement of ~4% is demonstrated with improved phase adjustment and soft thresholding of Auxiliary PA waveform. For linearization of 2-carrier LTE10MHz with instantaneous bandwidth of 40MHz, the proposed segmented DPD approach is used

to improve the linearity to -55dBc benchmark, which is ~11 dB better than linearity achieved using a conventional DPD scheme of comparable complexity.

The accurate behavioral modeling of the PA is important in the development of optimum predistorter function for the DPD system. For modeling handset PAs, a novel behavioral modeling technique is developed, which used polynomials along with infinite impulse response (IIR) basis functions. The IIR basis functions proved useful in modeling the short-term as well as long term memory effects with very few parameters. Later, same work is extended to develop a three-port PA, which included the modeling of the bias port of the PA along with the input and output ports. These three-port PA models are useful in the system simulations for the development of the envelope tracking (ET) based PA architectures.

Infrastructure PAs pose a significant challenge to the behavioral modeling due to the presence of higher order non-linearities and strong memory effects. For such high-power PAs, a new technique is developed which combines the pruned Volterra based PA model with IIR basis functions (IIR-PV). For validation, characterization of an 80W class-AB PA, and a 240W asymmetric Doherty PA showed that the IIR-PV offers significant reduction in normalized mean-square error (NMSE) over the modeling performance achieved using the conventional memory polynomial (MP) and the Pruned Volterra (PV) schemes of similar complexities.

In another aspect of this research, it is shown that although the conventional MP scheme may be adequate to model the PAs operating in class-AB mode, but additional cross-term Volterra kernels are needed to model the PAs operating in class-C mode. As the

Doherty PA has an Auxiliary PA cell as one of its component, it also needs a behavioral model which includes the selected cross-terms. This knowledge proved useful in the simplification of the two-segmented DPD architecture for the dual-input Doherty PA, as in first segment when only the Carrier PA is operating (biased in class-AB mode), cross-terms may have a limited advantage.

6.1 Future Work

Based on the research presented in this thesis, several potential aspects of a digitally-assisted Doherty PA can be further explored.

- Improvements in phase adjustments scheme: In this thesis, a simpler phase adjustment approach is used which is static in nature. Development of more complex scheme can be a topic of future research, which adds the additional dimensions of dynamic-range based tuning and frequency dependent tuning into consideration.
- Digitally-assisted multi-band Doherty PAs: The non-idealities in the impedance terminations at the baseband and difference frequencies make the extraction of the baseband model, quite a challenging task. For these wideband scenarios, the phase adjustment and the thresholding Gain function of the waveform to the Auxiliary PA, needs a deeper understanding.
- GaN transistor based digitally-assisted Doherty PA for multi-band applications: The long-term memory effects due to trapping effects, exhibited by the GaN transistors present a unique challenge. Over a wide bandwidth of the PA operation,

the optimum phase adjustment scheme and Auxiliary PA thresholding function needs to be reconfigured.

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