MONO-LAYER C-FACE EPITAXIAL GRAPHENE FOR HIGH FREQUENCY ELECTRONICS

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MONO-LAYER C-FACE EPITAXIAL GRAPHENE FOR HIGH FREQUENCY ELECTRONICS

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To my parents,

Li Zhao and Fengzhu Guo

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SUMMARY

As the thinnest material ever with high carrier mobility and saturation velocity, graphene is considered as a candidate for future high speed electronics. After pioneering research on graphene-based electronics at Georgia Tech, epitaxial graphene on SiC, along with other synthesized graphene, has been extensively investigated for possible applications in high frequency analog circuits. With a combined effort from academic and industrial research institutions, the best cut-off frequency of graphene radio-frequency (RF) transistors is already comparable to the best result of III-V material-based devices. However, the power gain performance of graphene transistors remained low, and the absence of a band gap inhibits the possibility of graphene in digital electronics. Aiming at solving these problems, this thesis will demonstrate the effort toward better high frequency power gain performance based on mono-layer epitaxial graphene on C-face SiC. Besides, a graphene/Si integration scheme will be proposed that utilizes the high speed potential of graphene electronics and logic functionality and maturity of Si-CMOS platform at the same time.

CHAPTER I

INTRODUCTION

1.1 History

Graphene, a two dimensional sheet of carbon atoms in hexagonal lattice, has been drawing attention from academic and industrial researchers for the past decade. Usually referred to as "single layer of graphite" and "flat form of carbon nano-tubes and fullerene", this atomically thin material is considered as the basis of carbon-based materials. Mono-layer graphite material was first investigated by H. Boehm et al in 1962 [8], and then the same material prepared on silicon carbide (SiC) was first reported by A. van Bommel et al in 1975 [89]. The first reports on electrical measurements of this material were published in 2004 by two separate groups. K. S. Novoselov et al from University of Manchester performed measurements on few layer graphite Hall bars obtained by mechanical exfoliation of graphite onto SiO_2/Si substrate, and observed a low temperature Hall mobility around 25,000 cm^2/Vs [71]. C. Berger et al from Georgia Institute of Technology [5], on the other side, prepared the few layer graphite sample by thermally annealing the 6H-SiC(0001) face (Si-face) at high temperatures, performed low-energy-electron-diffraction (LEED) measurement, scanning tunneling microscopy (STM) characterization, and electrical measurement on the samples, and proposed that the material is potentially suitable for future large scale electronic applications.

The field of research was significantly boosted by the first observations of quantum Hall effect (QHE) in mono-layer graphene samples in 2005 by K. S. Novoselov et al [73] and Y. B. Zhang et al [105]. Transport properties of mono-layer graphene

is similar to those of few layer graphite mentioned above, e.g., in terms of resistivity and gate response, whereas quantum Hall resistance quantization behavior is one of the few criterions to separate mono-layer graphene from multi-layers. Due to the existence of Berry's phase π for carriers in mono-layer graphene, Hall resistance quantization only happens at Landau filling factors $\nu = 4n + 2$. In comparison, for AB stacked bilayer graphene, Hall resistance quantization occurs at $\nu = 4n$ with a Berry's phase of 2π [72]. Although the results were obtained from exfoliated graphene that is not suitable for large scale production, these work still put graphene in the list of high mobility electronic materials along with GaAs and other III-V materials. Graphene started to be considered for industrial applications only after large scale production of the material was proven possible with equally good electronic performance. C. Berger et al proved that epitaxial graphene on SiC$(000\bar{1})$ face (C-face) shows carrier mobility exceeding 25,000 cm^2/Vs in 2006 [6], and X. Li et al proposed chemical vapor deposition (CVD) of mono-layer graphene on Cu in 2009 [54]. With such high carrier mobilities, graphene devices were considered to supplement silicon complementary metal-oxide-semiconductor (CMOS) field effect transistors (FET) in future generations of electronics beyond Moore's law.

1.2 Electronic Properties of Graphene

The honeycomb lattice structure of graphene is shown in Fig. 1.1. There are two carbon atoms in each unit cell of the lattice, and are called A and B sites. Resembling the spin-up and spin-down states of electrons, the electronic states orbiting around the A and B sites are often referred to as pseudo-spin. Three out of four 2s and 2p electrons of each carbon atom form σ bonds with electrons of neighboring atoms via sp^2 orbital hybridization, while the left electron of each atom forms π orbital perpendicular to the carbon plane. The σ bond is one of the strongest chemical bonds in materials, making graphene one of the strongest material in nature, comparable

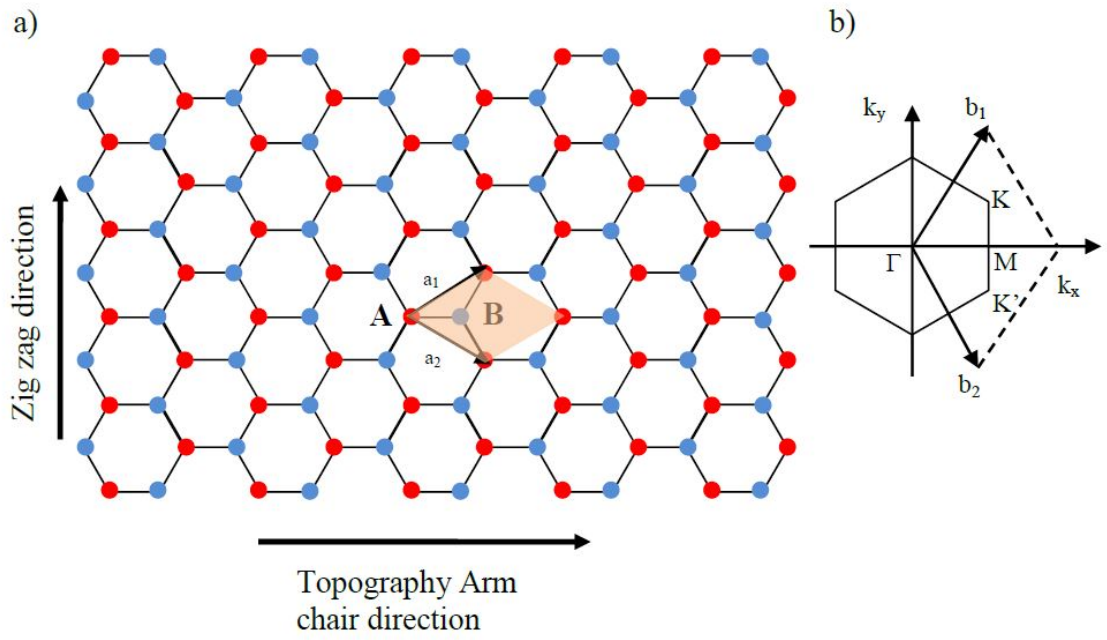

Figure 1.1: (a) Honeycomb lattice structure of graphene, the A and B sublattices are marked by different colors. (b) Momentum space of graphene lattice with base vectors, first Brillouin zone and K points.

with diamond (at least in plane). The electrons on the π orbitals at each atomic site are not localized. Instead, they can hop from one site to its neighbors, thus determining the electronic properties of graphene.

The band-structure of mono-layer graphene is shown in Fig. 1.2. Derived from tight binding calculation, the dispersion relation of graphene is

$$E(\mathbf{k}) = \pm t\sqrt{1 + 4\cos^2(\frac{k_y a}{2}) + 4\cos(\frac{k_y a}{2})\cos(\frac{\sqrt{3}k_x a}{2})} \tag{1.1}$$

when only the nearest-neighbor hopping of electrons is accounted for ($t \approx 2.7eV$, $a \approx 1.42\mathring{A}$ is the distance between nearest-neighbor carbon atoms) [92]. From the equation, the conduction and valence bands meet at the six corners of hexagonal first Brillouin zone (Dirac points). When the band structure is all folded to the first Brillouin zone, there are equivalently two full cones for the band structure near the charge neutral point of graphene, whose centers are often referred to as K and K' points. The energy dispersion of graphene is linear near the Dirac points, and could

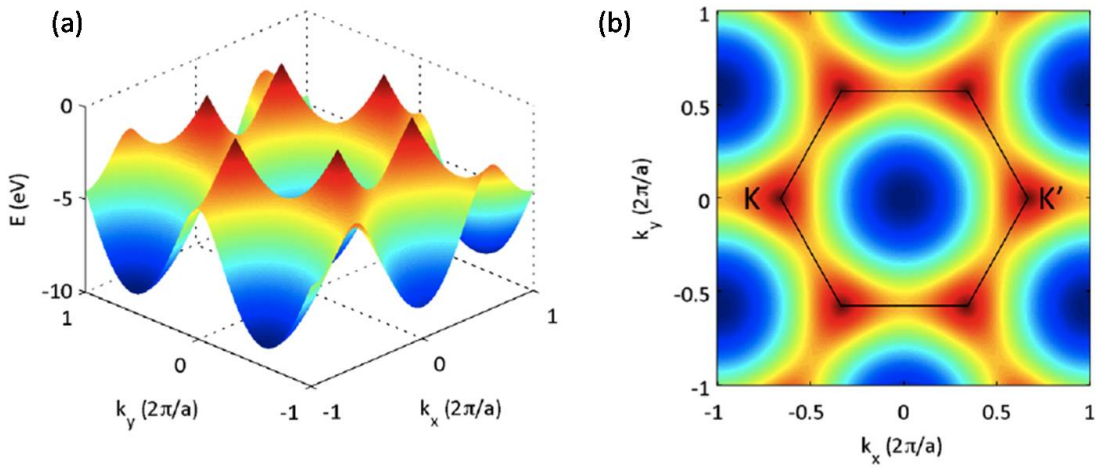

Figure 1.2: Band structure for mono-layer graphene. (a) Valence band of graphene. The six points at zero energy are the Dirac points. (b) 2D view of the band structure in (a) The marked hexagon is the first Brillouin zone.

be approximated as

$$E(\mathbf{k}) \approx \pm\hbar v_f |\mathbf{k} - \mathbf{K}(\mathbf{K}')|, \tag{1.2}$$

where $v_f \simeq 1 \times 10^6 m/s$ is the Fermi velocity, about 1/300 the speed of light, and

$$\mathbf{K} = (\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}), \mathbf{K}' = (\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}). \tag{1.3}$$

Unlike most semiconductors that have approximately parabolic dispersion relation at the edges of conduction and valence bands, graphene has a linear dispersion relation near charge neutral point, similar to that of light. This is why carriers in graphene are often referred to as massless fermions.

The wave function of the electronic states in momentum space around the Dirac points can be expressed in a vector form as long as the occupation on the sublattice sites A and B are treated as pseudo-spins

$$\psi_{\pm,\mathbf{K}}(\mathbf{k}) = \frac{1}{\sqrt{2}} \begin{pmatrix} e^{-i\theta_\mathbf{k}/2} \\ \pm e^{i\theta_\mathbf{k}/2} \end{pmatrix}, \psi_{\pm,\mathbf{K}'}(\mathbf{k}) = \frac{1}{\sqrt{2}} \begin{pmatrix} e^{i\theta_\mathbf{k}/2} \\ \pm e^{-i\theta_\mathbf{k}/2} \end{pmatrix} \tag{1.4}$$

, where $\theta_\mathbf{k} = \arctan(k_y/k_x)$ is the angle of the vector in momentum space. When the electrons are scattered within the same Dirac cone, the pseudo-spin states are changed

along with the momentum, reducing back-scattering in the material, especially for long-range scattering mechanisms such as Coulomb scattering. Scattering between the two Dirac cones would require large momentum transfer $\mathbf{K} - \mathbf{K}'$, thus is also absent for long-range scattering.

To sum up, due to the high Fermi velocity, massless nature, as well as the existence of pseudo-spin for the carriers near charge neutrality to suppress back-scattering, the carrier mobility of pristine graphene is much higher than semiconductors with larger effective electron and hole masses and no back-scattering suppression mechanism. The high carrier mobility makes graphene a strong candidate of high speed electronics for the semiconductor industry. For the academic research, the linear dispersion and pseudo-spin of graphene resembles that of high energy electrons or neutrinos, in which relativistic effects need to be considered. Especially, the linear dispersion exists in a relatively wide range of carrier energy $|E|$ <1eV, and the carrier speed is 1/300 of the speed of light. As a result, carriers in graphene are sometimes considered as "relativistic particles at benchtop", drawing attention from not only condensed matter physicists, but also researchers in high energy physics.

1.3 Graphene in Reality — Effect of Substrates

In the above analysis, graphene is supposed to stand by itself (free-standing), and does not interact with anything else. In reality, most graphene samples are placed or grown on substrates that inevitably interact with them, thus the properties of these graphene samples are not always the same as described in theories. For best understanding of the observations on these samples, effects of substrates on the properties of graphene need to be investigated.

1.3.1 Exfoliated Graphene on SiO_2

SiO_2/Si is a convenient substrate for exfoliated graphene, due to not only its easy accessibility, but also the insulating property of SiO_2 and conductive Si that could

serve as a back gate. Besides, with certain thicknesses of SiO_2, mono-layer graphene could be identified from multi-layer regions simply by an optical microscope, which is really useful for various purposes. Moreover, there is not much charge transfer between graphene and SiO_2, and the doping level of graphene is low after transfer, adding to the benefits of this substrate. However, several limitations of SiO_2 prevent it from being the best substrate for pursuit of "ideal graphene", and are listed as follows.

First, thermally grown SiO_2 does not have an atomically flat surface. STM study on exfoliated graphene on SiO_2 [43] showed that the surface roughness and peak-to-peak distance are both around a few nanometers (see Fig. 1.3 (a)). Such surface corrugation of graphene is in part due to the surface roughness of SiO_2, which is on the order of nm. It may induce inhomogeneous strain inside the graphene lattice, and subsequently causes extra scattering for electrons and holes in graphene due to the non-periodic atomic potential of the lattice.

Besides, the non-ideal interface between graphene and SiO_2 may allow vacancies and dangling chemical bonds [104]. They are the main source of charge puddles at the interface that could not only induce charge inhomogeneity in graphene, but also serve as Coulomb scattering centers that lowers the carrier mobility of graphene. Typical charge inhomogeneity of exfoliated graphene on SiO_2 is around a few $10^{11}/cm^2$, and carrier mobility is around $10^4 cm^2/Vs$, due to the combined effects from the substrate at the bottom and organic resist residue on top.

Due to the above reasons, the carrier mobility of graphene on SiO_2 is limited, and exotic phenomena for ultra-high mobility materials (i.e., GaAs) such as fractional quantum Hall effect and μm scale ballistic transport are absent. Besides, substrate inhomogeneity may induce large performance variation as nano-scale devices are considered. As a result, SiO_2 is not a suitable substrate for future graphene nano-electronics.

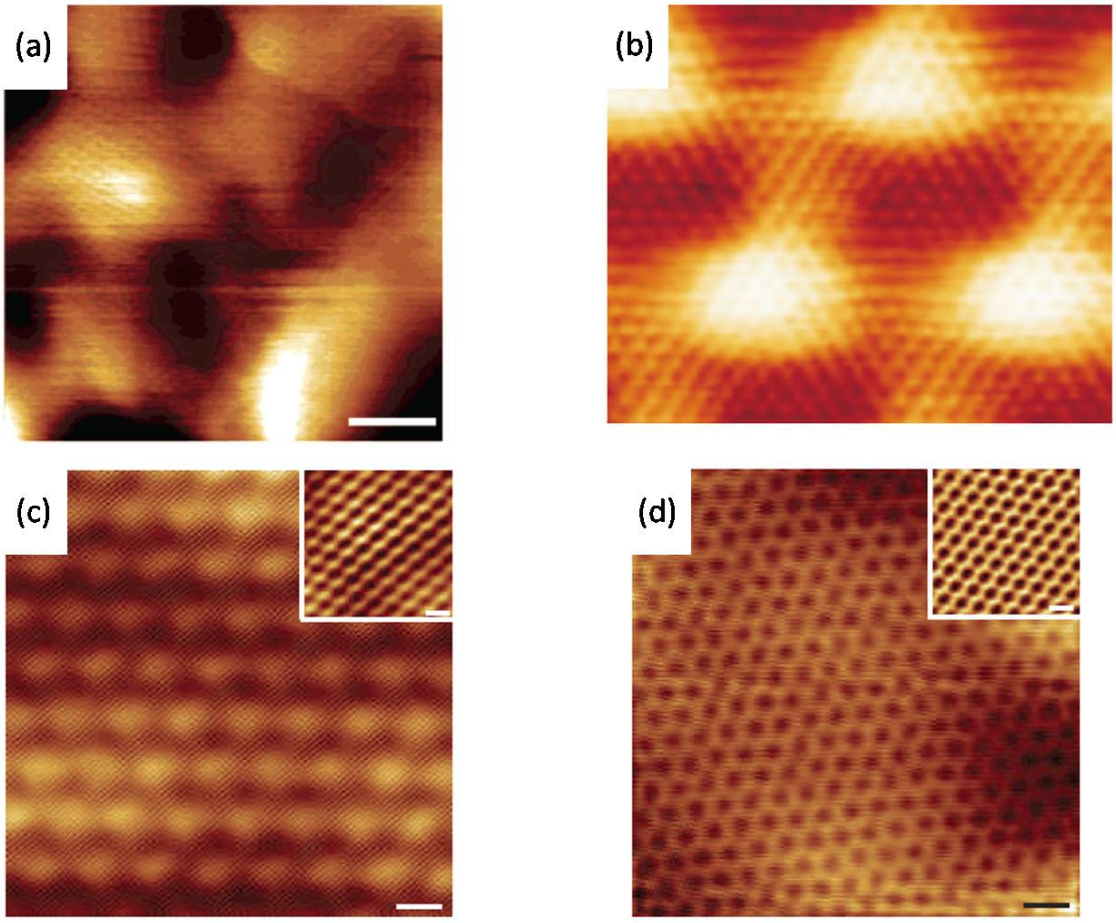

Figure 1.3: STM images of graphene on different substrates. (a)Graphene on SiO_2 from [43]. The scale bar is 2nm. (b) Graphene on Ru from [62]. The image size is $50\mathring{A} \times 40\mathring{A}$. (c-d) Graphene on hBN at different regions from [103]. Scale bars for both images are 2nm.

1.3.2 Graphene on Metals

Due to the success in growing few layer graphene on the surface of various metals, there was strong research effort on the metal-graphene interactions. However, metals are not suitable substrates for graphene electronics, due to the absence of electrical isolation in between. Nevertheless, they could still serve as interesting platforms for research on the interaction between graphene and substrates.

In presence of lattice mismatch between graphene and the metal surface, graphene usually displays an extra periodicity much larger than its own unit cell, and is referred to as a "Moire pattern". Such effect is observable in LEED patterns as satellite spots [32], and in STM images at a periodicity of a few nanometers [62] (see Fig. 1.3 (b)). Note that for STM measurements, the metals are usually annealed prior to the graphene formation so that atomically flat terraces are present at the surface.

As for modifications to the electronic properties induced by graphene-metal interaction, there are two major effects, namely charge transfer and change in band structure. First-principles study on interaction between graphene and metals [47] shows that doping of graphene induced by the metals depends not only on the work function of the metal surface, but also on the interface dipole arising from direct short-range interaction. Graphene is electron-doped by the metal substrates of Cu, Al and Ag, while hole-doped for Au or Pt substrates. In the case of large binding energy between graphene and metals such as Co, Ni, Pd or Ti, the graphene band structure would be strongly perturbed, and its signature linear dispersion may be absent (see Fig. 1.4) due to the hybridization of the π orbital of graphene and d orbital of the metals.

1.3.3 Graphene on Boron Nitride

From the above discussion, interaction with the substrates usually changes the electrical properties of graphene. To approach the ideal 'free-standing' graphene, a straight

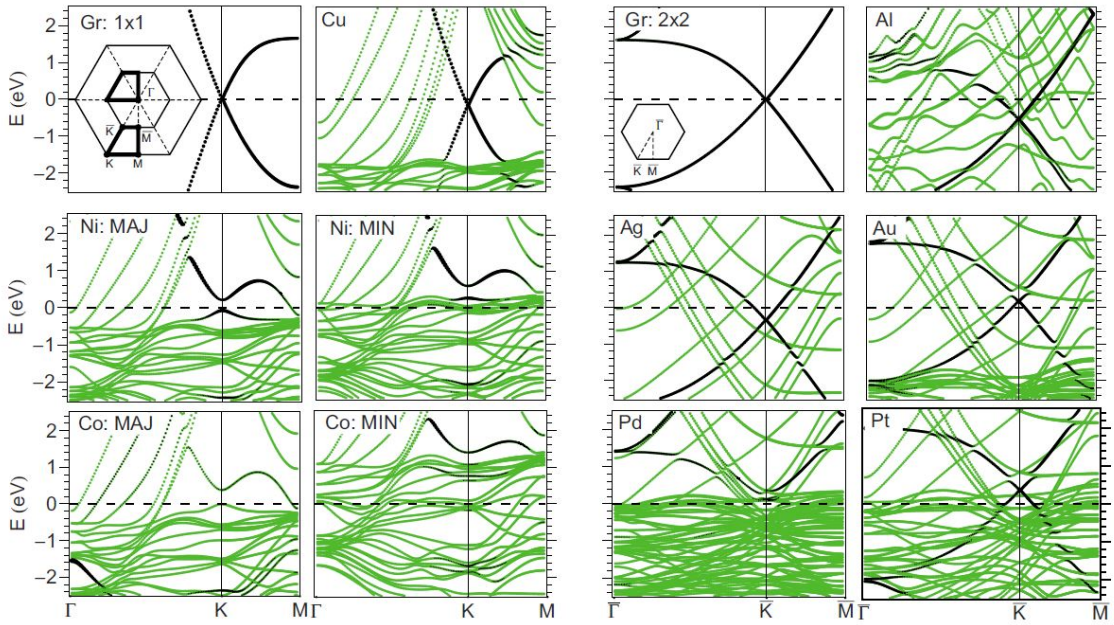

Figure 1.4: Band structure of graphene adsorbed on various metal substrates from first principle calculations in [47]. Gap-like feature is present in the band structure for graphene on Ni, Co, and Pd, while linear dispersion still remains when graphene is on Cu, Al, Ag, Au and Pd.

forward way is to remove the substrates. Fractional quantum Hall effect of graphene was first observed by etching away the underneath SiO_2, thus suspending the exfoliated graphene (suspended graphene) [24, 9]. However, due to the absence of a supporting substrate, the graphene devices are fragile, and the yield is extremely low. Besides, stress is induced to the graphene film as electric field is applied to change the carrier density in graphene, and too strong an electric field may cause the graphene to collapse onto the back gate. In consequence, suspended graphene is not suitable for scalable device fabrication. For ultra-high quality charge neutral graphene devices, a crystalline substrate is required, which has atomically flat surface free from dangling bonds, lattice constant matching well with graphene, and little induced doping or scattering to graphene.

Fortunately, hexagonal boron nitride (hBN) meets every of the above requirements, and fractional quantum Hall effect was observed on exfoliated graphene on

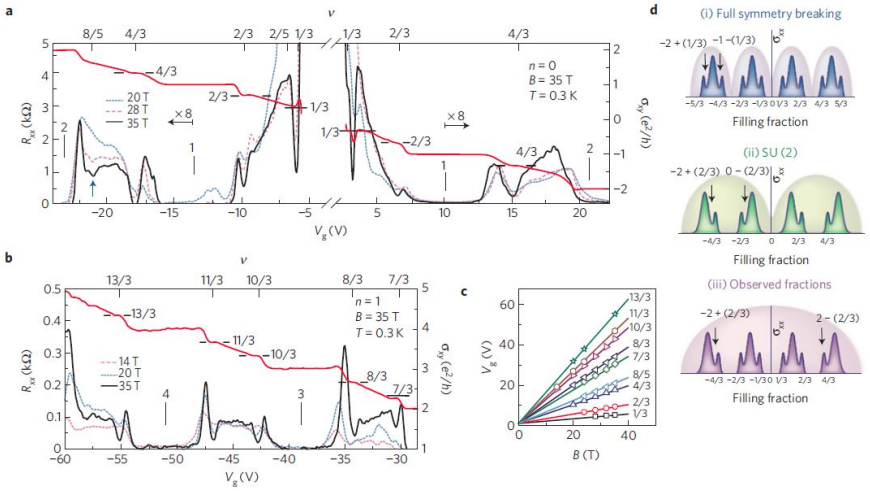

Figure 1.5: Observation of fractional quantum Hall effect in graphene on hBN in [21]. (a-b) Hall resistance quantization and resistivity minima for filling factors at multiples of 1/3 in the n=0 and n=1 Landau levels. (c) Fan diagram showing gate voltages with resistivity minima for different magnetic fields, and linear relation is observed for different fractional filling factors. (d) Schematic of the symmetry breaking mechanisms for observation of certain filling factors.

exfoliated hBN in 2011 [21]. In the resistivity and Hall resistance versus gate voltage measurements at a high magnetic field of 35T (see Fig. 1.5), resistivity minima and Hall resistance quantization are observed at fractional filling factors of $\nu = 1/3$, $2/3$ and $4/3$ in the n=0 Landau level (LL), and $\nu = 7/3$, $8/3$ and $10/3$ in the n=1 LL. This result is comparable with the observation of fractional quantum Hall effect in III-V materials, and the low temperature carrier mobility exceeding 100,000 cm^2/Vs at $10^{10}/cm^2$ charge inhomogeneity together indicate that hBN is a suitable substrate for ultra-high quality graphene electronic devices. In a further study, by placing monolayer exfoliated graphene between hBN layers and contacting graphene with metal only at the edges, low temperature ballistic transport was observed over distances longer than 15μm [94], and the measured room temperature carrier mobility around 40,000 cm^2/Vs was comparable to the theoretical limit due to phonon scattering.

STM study for graphene on hBN demonstrated the existence of Moire patterns due to the lattice mismatch [103]. The Moire patterns (several nanometers in size) result

from both 1.8% lattice constant mismatch and rotational stacking between graphene and hBN (see Fig. 1.3 (c-d)). Spatial maps of the density of states for the sample shows that the charge fluctuation in graphene on hBN is on the order of $10^9/cm^2$, two orders of magnitude lower than that of exfoliated graphene on SiO_2. However, in contrast to some theoretical predictions, the interaction between graphene and hBN does not cause band gap opening [30, 81]. Instead, when graphene and hBN are aligned to the same crystal direction, the Moire pattern size can reach up to $\sim$ 13nm, and the Hofstadter butterfly effect would be observable at accessible magnetic field intensities and charge densities [20, 76, 42].

The Hofstadter butterfly effect on graphene is, in principle, duplicated Dirac cones at non-zero charge densities ($\sim 3 \times 10^{12}/cm^2$ in this case), which can be seen in resistivity and Hall resistance versus carrier density plots (secondary resistivity maximum and sign flipping in Hall resistance, see Fig. 1.6 (a-b)). The name "butterfly" comes from the energy dispersion relation under different magnetic fields, in which the Landau fan diagrams of the original and duplicated Dirac cones intercept, and fractal patterns appear that resembles the shape and pattern of butterfly wings. The effect was first predicted to exist on graphene only at extremely high magnetic fields (exceeding thousands of Tesla) which allows a fraction or integer multiple of magnetic flux quantum $\phi_0 = h/2e$ to penetrate each graphene unit cell a few $\mathring{A}$ in size [39]. In the case of lattice-matched graphene on hBN, the effective unit cell is now that of the Moire pattern due to the weak graphene-hBN interaction, and its size is $\sim$ 13nm. As a result, the required magnetic field and charge density for observation of the Hofstadter butterfly effect are greatly reduced, and the effect is observable in accessible experimental conditions (tens of Tesla magnetic field, a few $10^{12}/cm^2$ carrier density, see Fig. 1.6 (c-d)).

The observation of Hofstadter butterfly effect in graphene on hBN is a very good example of weak graphene-substrate interaction affecting the electronic properties of

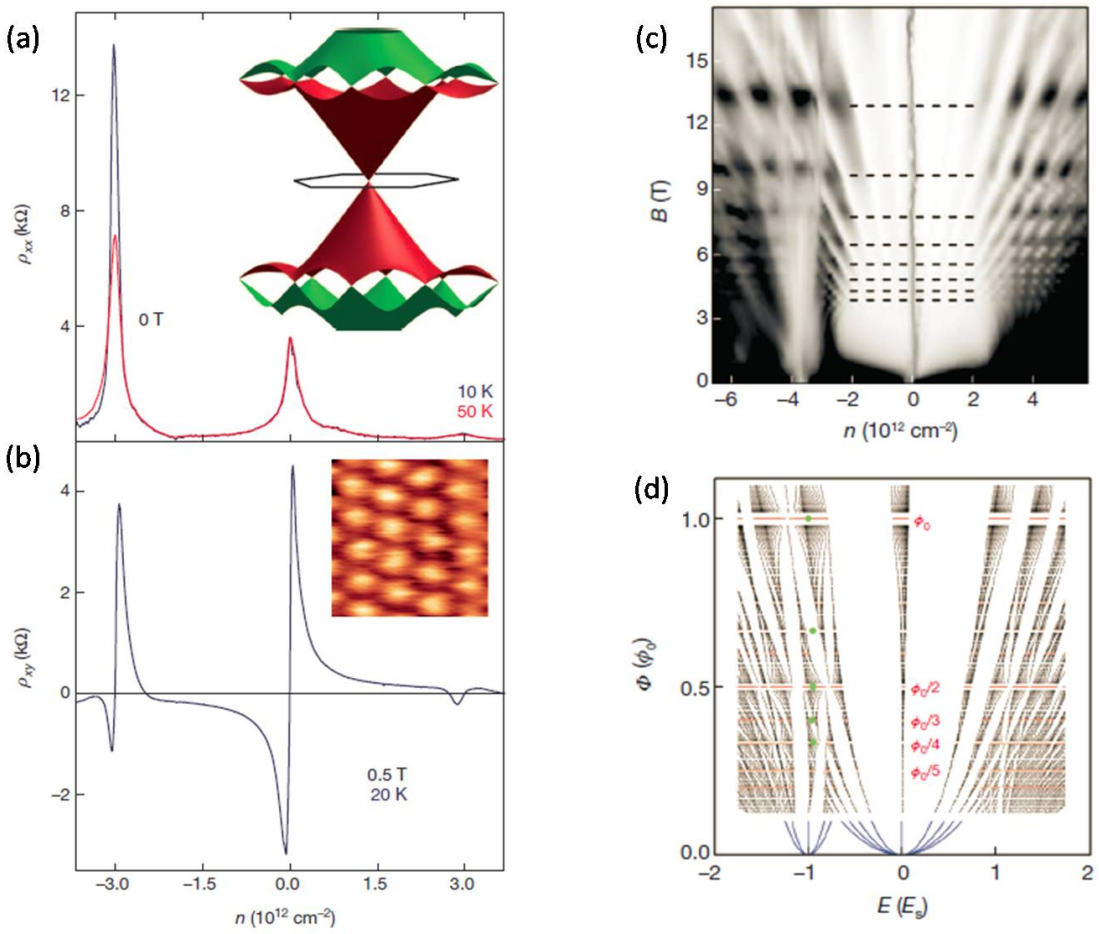

Figure 1.6: Observation of Hofstadter butterfly in graphene on hBN in [76]. (a-b) Resistivity and Hall resistance versus carrier density without magnetic field. Inset of (a): generation of duplicates of Dirac points at non-zero doping due to superlattice effects. Inset of (b): Superlattice structure observed in STM image of graphene on hBN, center-to-center distance of the bright spots being $\sim$ 11nm. (c-d) Experimental result on intersection of Landau fan diagrams from the original and duplicated Dirac points, and corresponding simulation results.

graphene in a non-trivial way. It shows the importance of substrates in graphene electronics, and the possibility of other interesting phenomena related to graphene-substrate interactions.

1.3.4 Epitaxial Graphene on SiC

The above graphene on hBN research relies on mechanical exfoliation of hBN to the substrates, which is not a scalable process due to the maximum size of exfoliated graphene and hBN flakes at tens of μm. Thus for large scale production of graphene on crystalline substrates, another suitable substrate is required. Epitaxial graphene on SiC, electrical transport properties of which was first investigated by C. Berger et al in 2004 [5], is another example of graphene on a crystalline substrate. Unlike graphene on hBN with only 1.8% lattice mismatch, the lattice constants for graphene and SiC are 3.073 $\mathring{A}$ and 2.456 $\mathring{A}$, respectively. Thus the stacking of graphene on SiC is different from that on hBN. Moreover, graphene-SiC interface structure, as well as the stacking order in multi-layer graphene, depends on the polar face of SiC, namely the Si-face and C-face for hexagonal SiC.

For graphene growth on the Si-face of SiC, carbon-rich $6\sqrt{3} \times 6\sqrt{3}$ surface reconstruction occurs prior to the graphene formation, and was confirmed by LEED and STM measurements [5] (see Fig. 1.7). LEED also confirmed that graphene sheets register epitaxially with the underlying SiC lattice. Note that the carbon-rich layer formed before graphene growth shares the same lattice structure with graphene, but is covalently bonded to SiC and partially sp^3-hybridized [31] . Thus its band structure, lack of energy states within $\pm$0.5eV around the Fermi level, deviates from that of graphene, and it is usually referred to as the "buffer layer". Researchers have succeeded in passivating the bonds between SiC and buffer layer by hydrogen intercalation above 600 °C, and obtained "quasi-free-standing" epitaxial graphene on SiC [77]. Unlike the usual Si-face few-layer graphene that is usually strongly

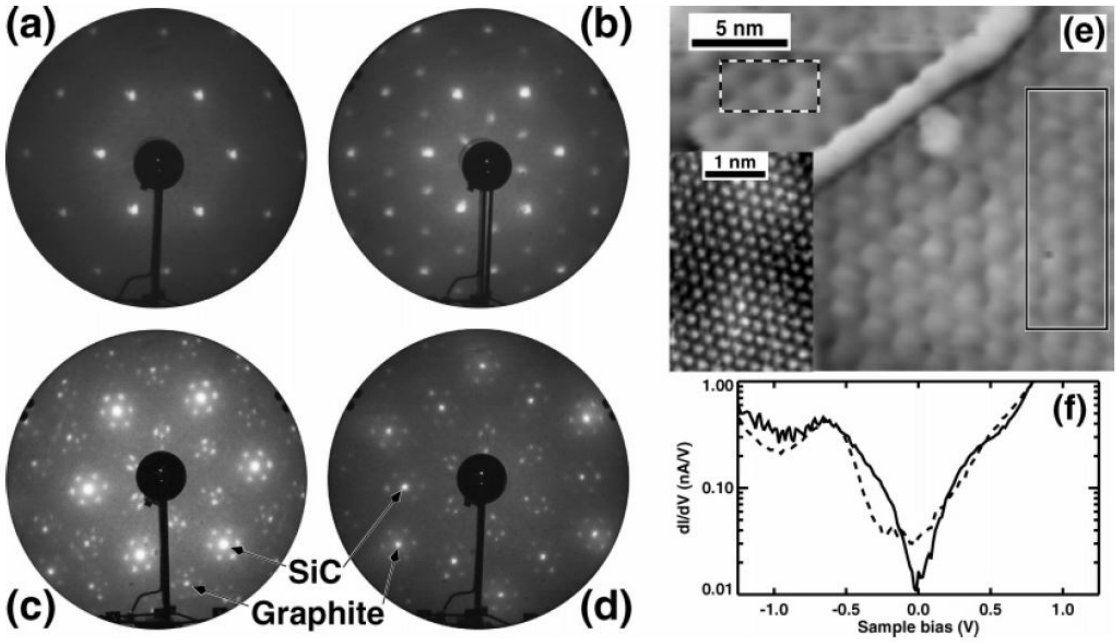

Figure 1.7: (a-d) LEED patterns of graphene/SiC at different stages of growth in [5]. (e) STM image of the sample, showing the superlattice structure. Inset: atomically resolved zoom-in scan for graphene lattice. (f) dI/dV spectra for the region in (e) marked by dashed line.

electron-doped due to charge transfer from the buffer layer, this quasi-free-standing graphene turned out to be nearly neutral (see Fig. 1.8), agreeing well with the name "free-standing". Besides, due to the strong interaction between epitaxial graphene and SiC, multi-layer graphene sheets on the Si-face are AB stacked, and mono-layer graphene usually shows carrier mobilities around 1000 cm^2/Vs [5, 40].

As for epitaxial graphene on C-face SiC, the effects of the substrate are quite different. For multi-layer graphene on C-face, LEED and STM measurements indicate the existence of stacking faults between the layers [38] (see Fig. 1.9 (a-c)). As a result, the top layer behaves just like mono-layer graphene, displaying discrete Landau levels under magnetic fields [65] (see Fig. 1.9 (d)). Mono-layer graphene on the C-face does not seem to have as significant charge transfer from SiC, unlike the case of Si-face graphene. Instead, pristine C-face graphene is close to charge neutral, and the measured carrier mobility is as high as that of exfoliated graphene on SiO_2, allowing

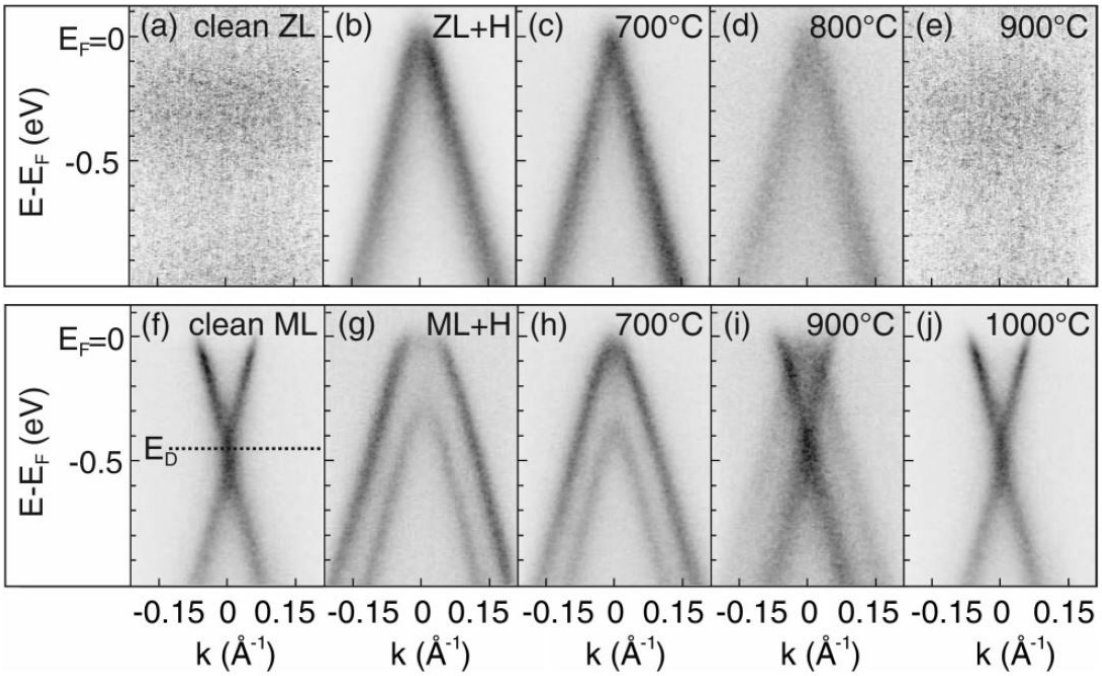

Figure 1.8: ARPES spectra showing the dispersion of π bands of as-grown zero layer (upper row) and mono-layer (lower row) graphene during different stages of hydrogenation in [77].

the observation of quantum Hall effect [98]. There is no definitive conclusion about the nature of graphene/C-face SiC interface yet. But the difference in transport properties between epitaxial graphene on Si-face and C-face SiC indicate that the graphene/SiC interface on the C-face is different from that on the Si-face.

Another interesting system is epitaxial graphene nano-ribbons on the sidewall facets of Si-face SiC [82]. As an etched vertical step on Si-face SiC is annealed at high temperatures, it recrystallizes into a $(1\bar{1}0n)$ facet 27$\sim$28° to the Si-face plane. When the graphitization temperature is properly controlled, graphene is grown only on the sidewall facet, as shown in Fig. 1.10 (c). Unlike C-face or Si-face graphene where graphene and SiC primarily interact at the bulk, sidewall epitaxial graphene nano-ribbons also interact with the SiC substrate at the edges. In fact, there is indication that the edges of sidewall graphene nano-ribbons may be strongly bonded to the SiC [70], providing atomically sharp edges that are key to high quality graphene

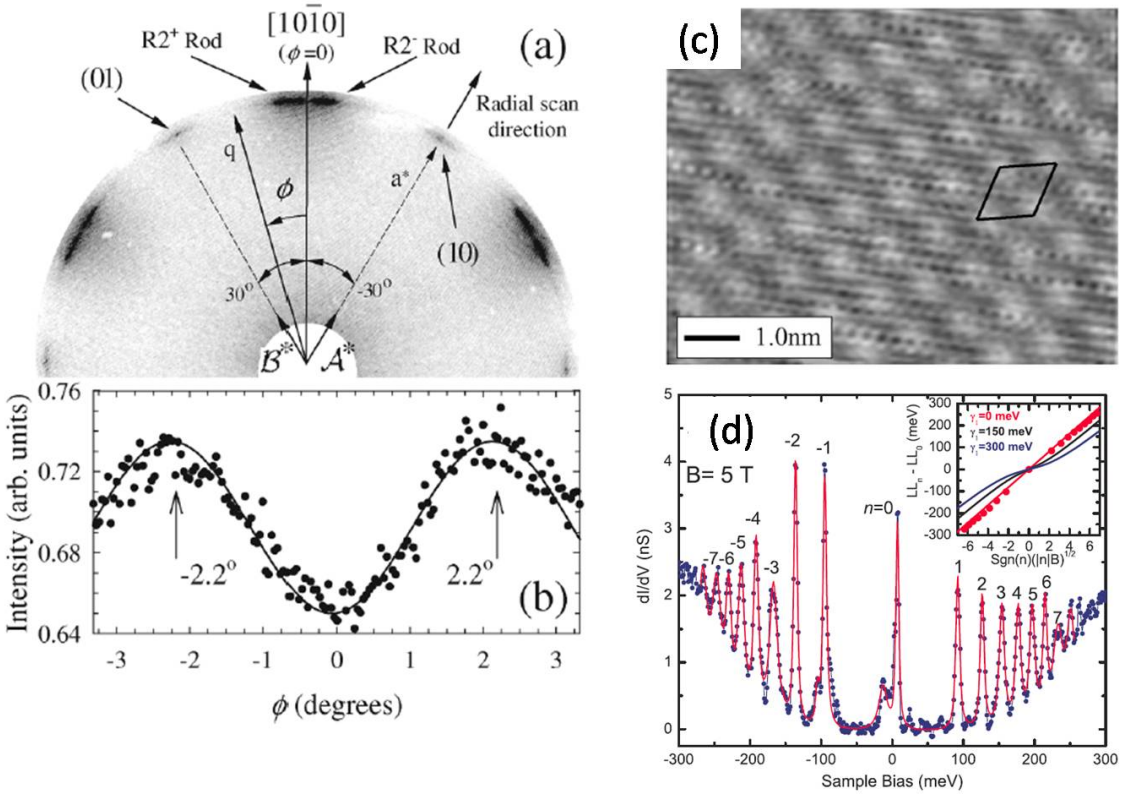

Figure 1.9: (a-b) LEED pattern of multi-layer epitaxial graphene on C-face SiC showing a range of distribution (arc) for the graphene lattice peaking at $\sim 2.2°$. (c) STM image of multi-layer C-face graphene showing superlattice structure with a $\sqrt{13} \times \sqrt{13}$ cell. (d) Direct measurement of Landau quantization in multi-layer C-face epitaxial graphene via scanning tunneling spectroscopy (STS) measurement. (a-c) from [38], and (d) from [65].

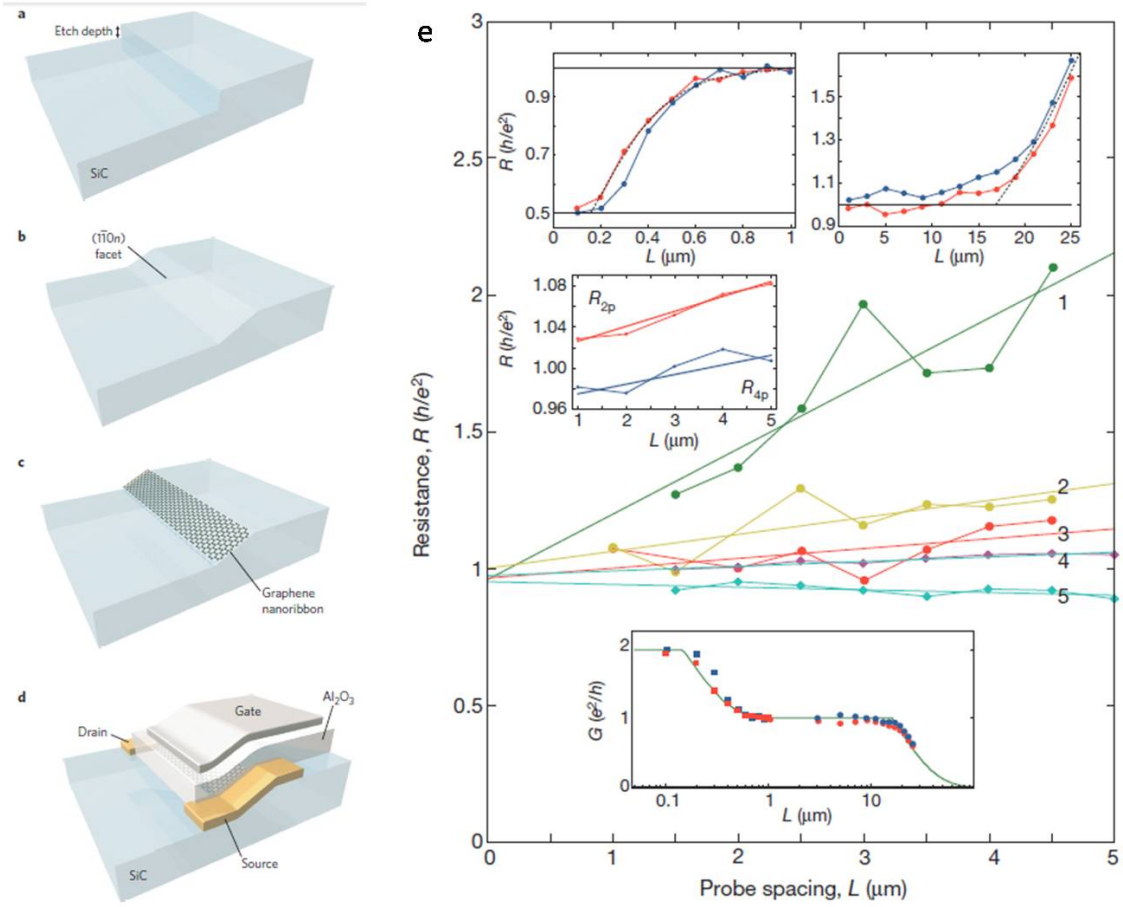

Figure 1.10: (a-d) Fabrication process for sidewall graphene nano-ribbon transistors on Si-face SiC. (e) Length-dependant resistance measurement showing ballistic transport on sidewall graphene nano-ribbons. (a-d) from [82], and (d) from [3].

nano-ribbons. Although the exact mechanism remains uncertain, the combined substrate effects at the bulk and edges of sidewall graphene nano-ribbons make them exceptional ballistic conductors at room temperature [3]. From the multi-probe resistance measurement shown in Fig. 1.10 (e), the resistance of the sidewall graphene nano-ribbon stays at the quantum resistance ($R = h/e^2 \approx 25.8k\Omega$) over 10 μm distance, and is approximately invariant against changing temperature. This is the first time ballistic transport was observed at room temperature at such length scale in ribbons, and again proves the importance of choosing the right substrate to determining the electronic properties of graphene structures.

1.4 Efforts to Open a Band Gap

The major difference between graphene and most semiconductor materials is the absence of band gap in graphene. As a result, there is no "off" state for graphene transistors, limiting its applications in digital electronics. Besides, graphene also lacks current saturation induced by "pinch-off" effect that requires a band gap, and the voltage gain of graphene devices is low, which also limits its potential in analog electronics. Due to the above reasons, there has been experimental efforts to open a band gap in graphene. Several major directions of these efforts are discussed as follows.

1.4.1 Graphene Nano-Ribbons

A most focused-on method to open a band gap in graphene is fabricating graphene nano-ribbons (GNR). Due to quantum confinement, only discrete modes are allowed perpendicular to the GNR, and band gap exists for armchair ribbons of certain widths, similar to that of carbon nanotubes (CNT). From theoretical calculations, the relation $E_g(eV) \approx 1/W(nm)$ is satisfied, where E_g is the band gap, and W is the width of the GNR. Thus for a minimum gap size of 0.5eV for digital electronics, the maximum

allowed ribbon width is 2nm, beyond the ability of current lithography methods. Despite such difficulties, the possibility of band gap engineering by fabricating GNRs of different widths and monolithically obtaining the semiconducting devices with metallic connections still attracts a lot of research efforts into this direction.

One way to fabricate GNR is through electron-beam lithography. M. Y. Han et al reported the observation of energy gap in low temperature transport measurements of exfoliate graphene nano-ribbons defined by e-beam lithography to $\sim$ 20nm wide [36]. In Fig. 1.11, the on-off ratio of the GNR transistors greatly increases with decreasing temperature, which is a signature of the existence of energy gap. Besides, the on-off ratio is smaller for wider ribbons, also in accordance with theoretical predictions. The extrapolated energy gaps for GNR of different widths approximately follow the $1/W$ trend, and $\sim$ 200meV band gap was observed for $W \sim 15nm$. However, later reports showed that the transport in e-beam lithography defined GNR is dominated by variable range hopping (VRH) and Coulomb blockade at low temperatures, due to the rough edges of the ribbons, and the carrier mobilities of these GNR are much lower than that of bulk graphene [35]. Thus this method is not suitable for high speed electronic devices, despite its compatibility with the current semiconductor technology.

Another way to produce sub-10nm wide GNR is through chemical treatment of graphite or CNT [53, 45]. An on-off ratio of $\sim 10^6$ was observed on 5nm wide GNR obtained from expanded graphite, while for unzipped CNT the on-off ratio was around 10 at room temperature. The lower on-off ratio for GNR from unzipping CNT was attributed to smoother edges, which, in principle, should induce less edge scattering for electrons and holes, and enable higher carrier mobilities. Unlike the e-beam lithography approach, this method has not been proven to be scalable, due to the randomly dispersed GNRs on the wafers. Thus it is not yet a viable option for large scale digital electronics.

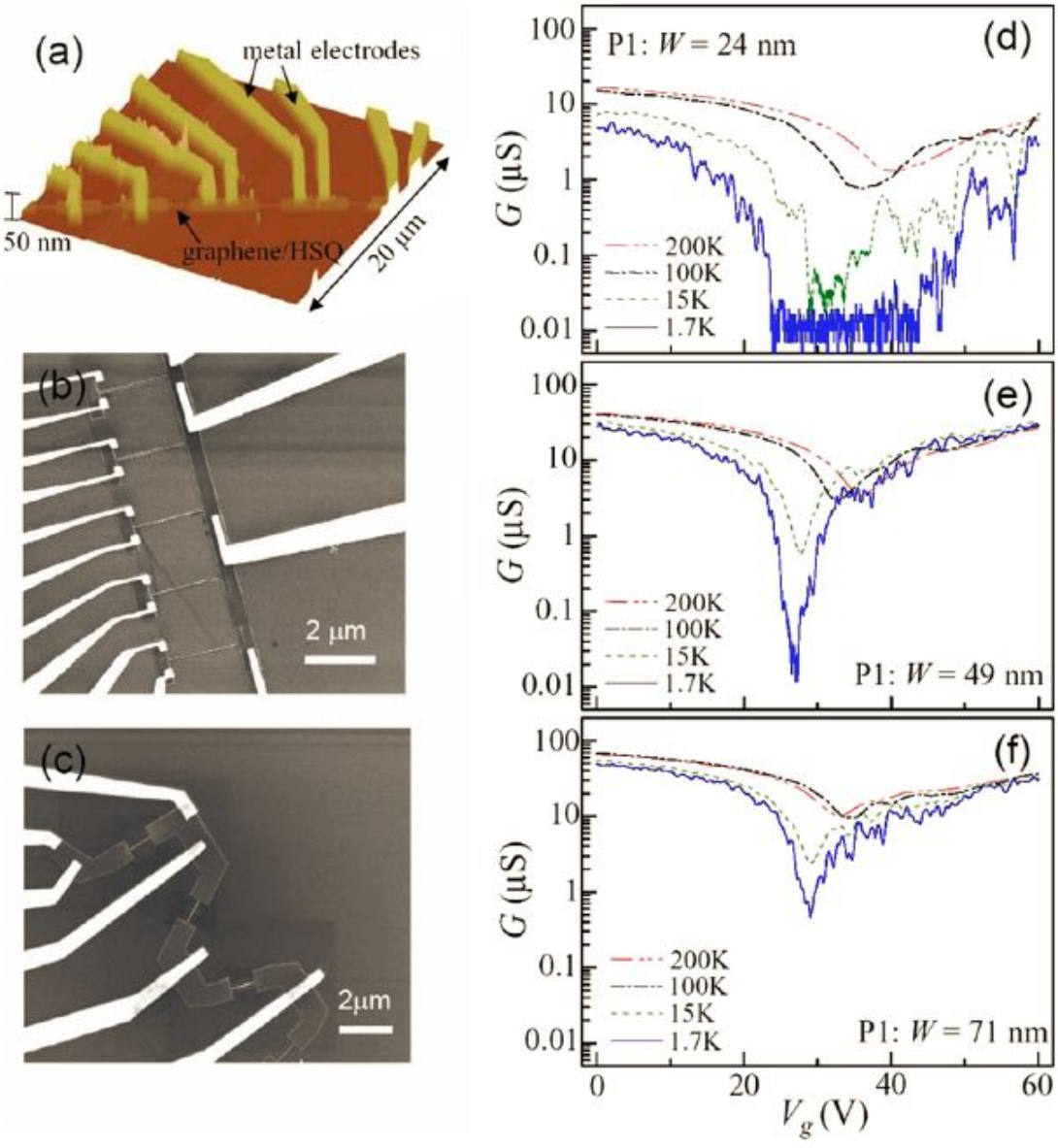

Figure 1.11: (a-c) AFM topography and SEM images of e-beam lithography defined graphene nano-ribbon devices with metallic leads. (d-f) Conductance versus gate voltage curves for nano-ribbons of different widths at different temperatures in [36].

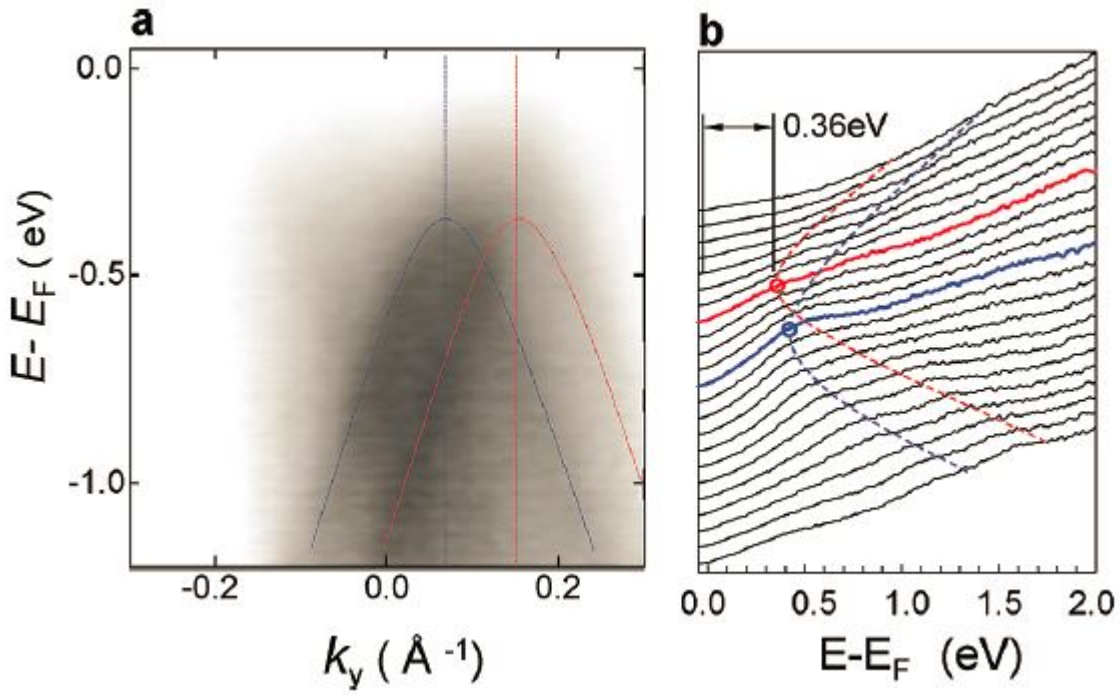

Figure 1.12: Band gap in nitrophenyl-functionalized epitaxial graphene from ARPES measurements.

1.4.2 Functionalized Graphene

Another way to open a band gap in graphene is by chemically bonding functional groups to the graphene lattice. With this treatment, the C-C bonds of graphene turn from pure sp^2 to partially sp^3, and local electron potential is added to some lattice sites. A band gap might be created in this way if the functionalization is designed properly. It does not require atomically accurate lithography methods as in the case of e-beam defined GNR, and is in principle compatible with large scale production. The key of this method is the right choice of functional groups, and how to bond them to graphene in a controlled way. Some results on this approach are discussed below.

An example of functional groups are the aryl-groups [4, 69]. They are introduced to graphene by spontaneous reaction of diazonium salt with C-face epitaxial graphene on SiC. The change in C-C bonds was confirmed by X-ray photoelectron spectroscopy

(XPS) and Raman spectroscopy measurements. Moreover, a 0.36eV band gap was observed by angle resolved photoemission spectroscopy (ARPES) measurements (see Fig. 1.12). The difficulty to achieve a high carrier mobility for functionalized graphene in this case is the randomness of the distribution of functional groups on graphene, and reports are still absent for high quality functionalized graphene transport characteristics.

Another example of functional group would be a single hydrogen atom, and the hydrogenated graphene was referred to as "graphane" [25]. In this study, the exfoliated graphene samples were bombarded with H_2/Ar plasma for 2 hours to reach saturated reaction. A disadvantage of this method is the extremely low carrier mobilities of about 10 cm^2/Vs for the end product, which is an order of magnitude lower than that of silicon. Signatures of VRH were observed in the low temperature transport measurements, indicating a high density of defects in the sample after treatment. Such results do not meet the requirements for high speed electronics, limiting the potential of this approach.

1.4.3 Dual-Gated Bilayer Graphene

AB stacked bilayer graphene is gapless with parabolic dispersion relation near charge neutral. However, as a strong electric field is applied perpendicular to its plane, the symmetry between the two layers is broken, and a band gap is created. Y. B. Zhang et al reported their direct observation of tunable band gap at room temperature in bilayer graphene in 2009 [106]. The device was fabricated by adding Pt/Al_2O_3 gate/dielectric stack on top of exfoliated bilayer graphene on SiO_2, and the bottom doped Si could be used as the back gate. In Fig. 1.13 (a-b), the largest on-off ratio of the device was observed with a large negative voltage bias at the back gate. The extrapolated band gap size increases with increasing inter-layer electric field, and a maximum gap of $\sim$ 250meV was achieved.

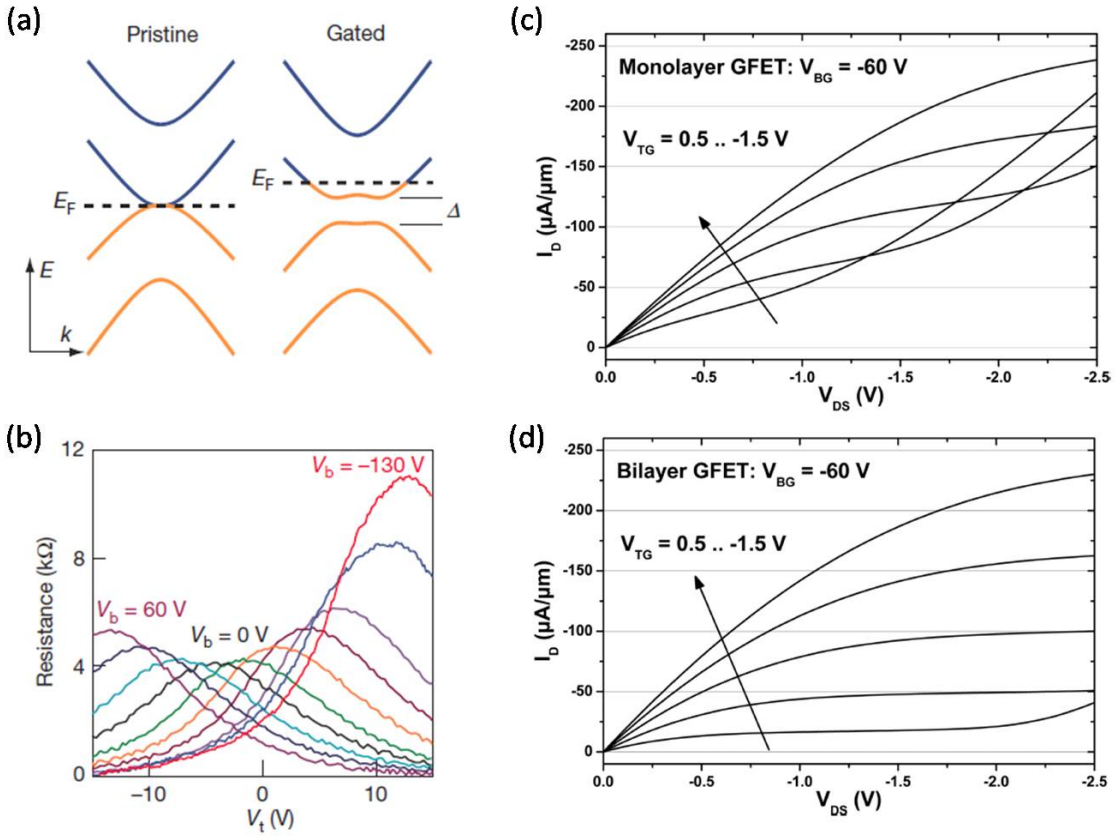

Figure 1.13: Band gap opening for dual-gated bilayer graphene. (a-b) Schematic of band gap opening in bilayer graphene and resistance versus top gate voltage curves at different back gate voltages, showing largest on-off ratio with largest negative back gate voltage [106]. (c-d) Family of drain/source current-voltage curves at different top gate voltages with large negative back gate voltage [83]. Current saturation is observed in bilayer graphene.

Moreover, channel pinch-off induced current saturation was observed on dual-gated bilayer graphene in a later study [83]. Here 90nm thick SiO_2 is used as back gate dielectric for better electrostatic control of the graphene channel, and the top gate dielectric is Al_2O_3. The measured field effect mobility of the device is 2000 cm^2/Vs, which is typical for bilayer exfoliated graphene on SiO_2. In Fig. 1.13 (c-d), the drain-source current-voltage curves at different gate voltages are plotted for mono-layer and bilayer graphene FETs. Unlike mono-layer graphene that displays no obvious current saturation, bi-layer graphene FET shows clear Si-MOSFET-like current saturation at large drain bias and different top gate biases, as long as a large negative back gate voltage is present. The maximum voltage gain of the bi-layer device is around 30 at room temperature, similar to that of Si-MOSFETs with short channels. Such high voltage gain enables the application of bilayer graphene in various digital and analog circuits. Combined with FET mobility an order of magnitude higher than Si-CMOS, it shows a great potential for radio frequency (RF) circuits that are becoming increasingly important with the thriving wireless communication industry.

The dual-gating of AB stacked bilayer graphene is not limited by lithography process or chemical treatment, unlike the case of graphene nano-ribbons and functionalization. However, other restrictions of this method prohibit its immediate application at large scale. First, previous reports on dual-gated bilayer graphene with a band gap are mostly, if not all, based on exfoliated graphene, which, in principle, cannot be used in large scale production. Thus band gap opening of synthesized AB stacked bilayer graphene is still needed to prove its mass production compatibility. Another limit of dual-gating bilayer graphene is the strong electric field required to open a band gap large enough for room temperature operation. For a 300meV gap, the required electric field is close to the breakdown limit of most dielectric materials, while such a gap size is yet too small for a decent device on-off ratio for digital applications. Though challenging, these problems still deserve significant research efforts,

regarding the great benefits tunable band gap and large carrier mobility may bring to the semiconductor industry.

1.5 Motivation

The fast growing industry of wireless communication requires RF devices that can be operated at higher frequencies and consume less power. III-V materials and strained Si (SiGe) are two of the strongest candidates for this purpose, with record high operation frequencies for InP-based high electron mobility transistors (HEMT) [19], and great compatibility with Si-CMOS fabrication for SiGe technology [14].

Graphene was considered as a candidate for this purpose by the Defense Advanced Research Projects Agency (DARPA) in its Carbon Electronics for RF Applications (CERA) Program that started in 2007. A lot of progress on better performance for graphene RF transistors has been made by collective efforts from academic and industrial research institutes. Despite the reported high current gain performance of graphene RF transistors, power gain performance of these devices, which is more relevant for application in practical circuits, remained low. This discrepancy in current and power gain performance for graphene devices was attributed to the lack of band gap and current saturation, relatively low carrier mobility for synthesized graphene (CVD graphene and Si-face epitaxial graphene), large contact resistance between graphene and metals, and poorly designed device structures [79].

Regarding the absence of a clear path in opening a band gap in graphene, I focus my work on improving the power gain performance of graphene transistors in the latter aspects mentioned above. For higher carrier mobility in synthesized graphene, mono-layer C-face epitaxial graphene is better than Si-face graphene and CVD graphene, thus in principal should be a better channel material for RF transistors. Then the major difficulties are controlling the growth of mono-layer graphene,

and techniques to deposit top gate dielectric without significantly affecting the carrier mobility. For lower contact resistance between graphene and metals, the key is the right choice of metal for proper doping of graphene and efficient carrier tunneling in between, which also relies on the interface quality. To this end, palladium is chosen for its large work function to strongly p-dope underneath graphene, and its good adhesion to graphene compared with other metals with large work function (i.e., platinum). Annealing graphene at high temperatures removes the resist residue on graphene, and further helps the adhesion between graphene and metal contacts. For the device design, T-gate structure is used for smaller gate resistance at short channel lengths, which also helps improving the power gain performance.

1.6 Thesis Outline

Growth and characterization of mono-layer epitaxial graphene on C-face SiC will be first introduced in Chapter 2, including growth system and conditions, surface topography and Raman characterization, as well as transport measurements at different temperatures. Methods for dielectric deposition on graphene will be discussed in Chapter 3, leading to the final choice of dielectric layer for C-face graphene RF transistors in Chapter 4. Besides, the fabrication process for T-gate self-aligned RF transistors, along with the DC and RF characteristics of as-made devices, will also be covered in Chapter 4. Attempts on integrating epitaxial graphene on SiC with Si wafers will be mentioned in Chapter 5, and a wafer bonding solution for the integration is proposed and realized. The conclusion of the thesis will be in the last chapter (Chapter 6).

CHAPTER II

MONO-LAYER C-FACE EPITAXIAL GRAPHENE ON SIC — GROWTH, CHARACTERIZATION AND TRANSPORT

2.1 Introduction

2.1.1 Difficulty in C-face Epitaxial Graphene Growth Control

When hexagonal SiC is heated up to high enough temperature in vacuum, graphene layers form on both polar faces, i.e., Si-face and C-face of SiC. From previous reports [18], it is much harder to control the growth of graphene on C-face compared with Si-face of SiC. First, the growth rate of graphene on C-face is much larger than that on Si-face at the same condition, thus allowing a smaller temperature and time window for the growth of few layer graphene (more so for mono-layer graphene) on the C-face. Second, the growth of graphene on the Si-face of SiC starts from SiC step edges [70], whereas on C-face graphene starts to grow also from defects. For example, multi-layer graphene forms locally around a screw dislocation on C-face SiC while no graphene is grown in the nearby regions [41]. Moreover, defects of different types are usually randomly distributed on SiC, and so would the graphene grown from them.

Due to the above reasons, it is hard to control the growth of few layer graphene, not to mention mono-layer graphene, on C-face SiC. Besides, due to its rotational stacking order [38], multi-layer graphene on C-face SiC usually has a single Lorentzian 2D peak in its Raman spectrum, similar to that for mono-layer graphene. It makes it difficult to identify mono-layer graphene on C-face SiC, unlike the case of Si-face graphene or exfoliated graphene on SiO_2, where multi-layer graphene is AB-stacked and displays broadened 2D peaks in Raman spectroscopy. Despite such difficulty, a large amount of research effort is still aimed towards successful control of C-face

graphene growth, due to the advantages of this material as discussed below.

2.1.2 Advantages of C-face Epitaxial Graphene for Electronics

C-face epitaxial graphene on SiC has been investigated for potential electronics applications since 2006 [6]. It has several advantages over Si-face graphene on SiC. First, its mono-layer property is continuous over steps that are 1nm high or less, confirmed by transport measurements on Hall bars [98]. As for Si-face graphene obtained from the reported growth methods, the SiC step edges are generally covered with more than one layer of graphene when graphene on the terraces is mostly mono-layer. Such uniformity in mono-layer C-face epitaxial graphene ensures reproducible electronic properties for devices over step edges. Moreover, the interaction between C-face epitaxial graphene and the substrate is much weaker than that for Si-face graphene, primarily because of the absence of a buffer layer similar to that on Si-face in between. Due to the presence of buffer layer, pristine mono-layer Si-face graphene is often n-doped, with carrier density close to $1 \times 10^{13}/cm^2$. For mono-layer C-face graphene devices, when fabricated with proper methods, the carrier density is usually much lower compared with that for Si-face graphene, on the order of $1 \times 10^{12}/cm^2$. As electronic transport properties are concerned, reported carrier mobility for mono-layer C-face graphene on SiC is usually around 10,000 cm^2/Vs at room temperature [98], and mobility up to 40,000 cm^2/Vs at 4.2 K has been observed [41]. In comparison, Si-face mono-layer graphene on SiC has carrier mobilities of around 2000 cm^2/Vs and 1000 cm^2/Vs with and without hydrogen passivation [78]. With such high mobility, C-face graphene is more favorable for observation of interesting physical phenomena, and possible applications in high speed electronic devices.

Half integer quantum Hall effect was observed on mono-layer C-face epitaxial graphene in 2009 [98]. And it was among the first observations of quantum Hall effect on synthesized graphene [80, 88]. In this work, Hall mobility up to 20,000 cm^2/Vs was

measured at 1.4K on the C-face graphene Hall bar at a carrier density (hole type)of $1.27 \times 10^{12}/cm^2$, and Hall resistivity quantization at $\rho_{xy} = h/2e^2$ with $\rho_{xx} = 0\Omega$ was observed at around 18 Tesla in perpendicular magnetic field. Such high mobility is comparable to that of the best exfoliated graphene on SiO_2. The observation of Hall resistivity quantization at higher Landau levels and lower magnetic fields further indicates the high quality of the sample, i.e., mono-layer epitaxial graphene on C-face SiC.

2.1.3 Parallel Work on C-face Mono-layer Graphene Growth

The confinement-controlled-sublimation (CCS) method [18] is the growth method I used to control the growth of mono-layer C-face graphene, and is to be extensively discussed about in this chapter. Other growth methods for mono-layer graphene on C-face SiC were also investigated by other research groups, and are mentioned here as a reference. By using a graphite cap to cover the SiC sample, N. Camara et al successfully grew long isolated graphene ribbons (several μm wide, hundreds of μm long) on the C-face of on-axis 6H-SiC in 2009 [11]. Here the graphite cap lowers the sublimation rate of Si during the annealing process, thus growth of graphene on the C-face is controlled to a certain extent. As they applied a similar growth process to an 8° off-axis 4H-SiC sample [12], the result was much larger mono-layer graphene islands (tens of μm wide, hundreds of μm long). Hall measurements on these samples showed Hall mobility of $\mu > 5000 cm^2/Vs$, and quantum Hall effect was observed at high magnetic fields and low temperatures. This work not only confirmed the importance of limiting Si sublimation rate in mono-layer C-face graphene growth, but also demonstrated the high quality of C-face mono-layer epitaxial graphene.

2.1.4 Content of the Chapter

This chapter is organized as follows. First, I will introduce the concept and details of CCS method for mono-layer C-face graphene growth. Then various post-growth

characterization techniques and results will be covered, including atomic force microscopy (AFM) and Raman spectroscopy. Following the surface characterization section is the electrical characterization of C-face mono-layer graphene. There I will present graphene Hall bar fabrication process and measurement results, at both room temperature and low temperatures. Observation of quantum Hall effect at relatively low carrier density and low magnetic field will also be mentioned.

2.2 Confinement Controlled Sublimation Method for Mono-layer C-face Graphene

2.2.1 Preparation of SiC Before Growth

Various crystalline forms of SiC exist in nature. According to the layer stacking order, the most commonly seen SiC polytypes are α type (hexagonal stacking) and β type (zincblende stacking). Examples of α type SiC include 2H-SiC, 4H-SiC and 6H-SiC, and for β types SiC, 3C-SiC. The SiC used in this study is 4H-SiC, whose lattice structure is shown in Fig. 2.1. Here the stacking order is written as "ABCBA", and the unit cell in the stack contains 4 SiC bi-layers. The top layer shown in the figure are carbon atoms, and this SiC polar face is referred to as SiC $(000\bar{1})$ (C-face), while the bottom layer contains exclusively Si atoms, and is called SiC (0001) (Si-face).

The SiC material used in this work are research or production grade 3-inch mono-crystalline on-axis semi-insulating 4H-SiC wafers from Cree, Inc. (miscut angle $< 0.3°$). For C-face graphene growth, this polar face is epi-ready and chemical mechanical polished (CMP) with a surface roughness $<$ 1nm. The wafer is then diced into 3.5mm $\times$ 4.5mm dies (samples). To remove the dust particles and organic residue on the surface of SiC induced by the dicing process, the SiC samples are cleaned with an ultra-sonicator in acetone and isopropyl alcohol (IPA) prior to the annealing step. An optimized cleaning recipe is chosen for a resulting dust-free surface, which includes two steps of sonication in acetone for 20 minutes each and change of solvent in between, and a similar two step sonication in IPA for 20 minutes each.

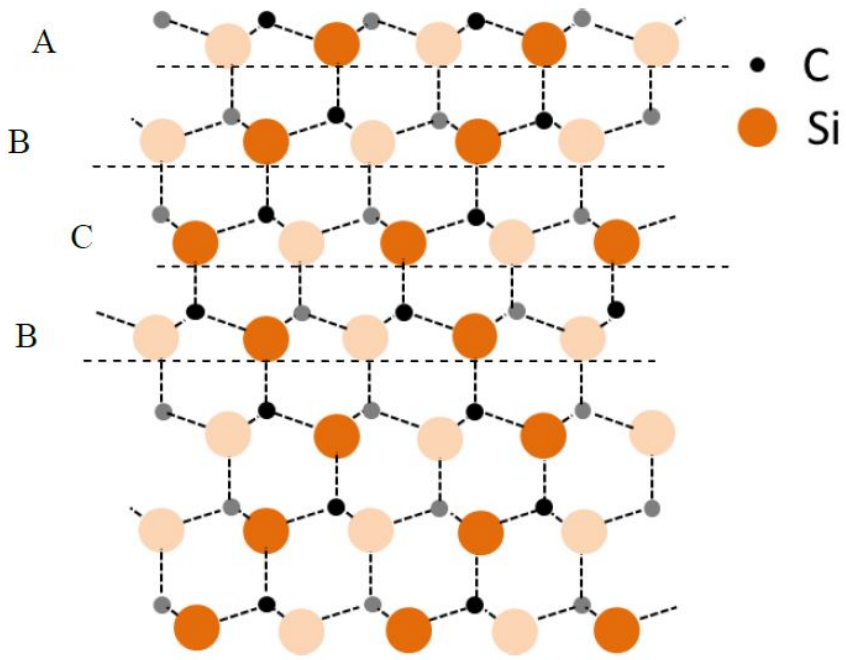

Figure 2.1: Lattice structure of 4H-SiC(000$\bar{1}$) face. Each unit cell contains 4 SiC bilayers, and is 1.0 nm high.

2.2.2 Annealing of SiC for graphene formation

After the above cleaning step, the sample is inserted into a graphite crucible in a home-made high-vacuum induction furnace for the follow annealing process. Schematic of a SiC sample in the graphite crucible is shown in Fig. 2.2 (b). The almost enclosed geometry of the crucible significantly limits the sublimation rate of Si at the surface of SiC during the annealing process, while the aperture on the top cap of the crucible offers a controlled escape for the Si vapor. The Si sublimation rate depends on the size of the aperture, which offers an extra variable besides annealing temperature and time in the growth process design to control the growth rate of graphene. Note that the graphene growth rate is proportional to the Si sublimation rate, due to a much lower vapor pressure of carbon compared with Si at the same high temperature. For example, Si vapor pressure $P_{Si}(1500K) = 1.6 \times 10^{-6}$ Torr, and $P_{Si}(2000K) = 1.1 \times 10^{-2}$ Torr, while the vapor pressure for carbon at these temperatures is in

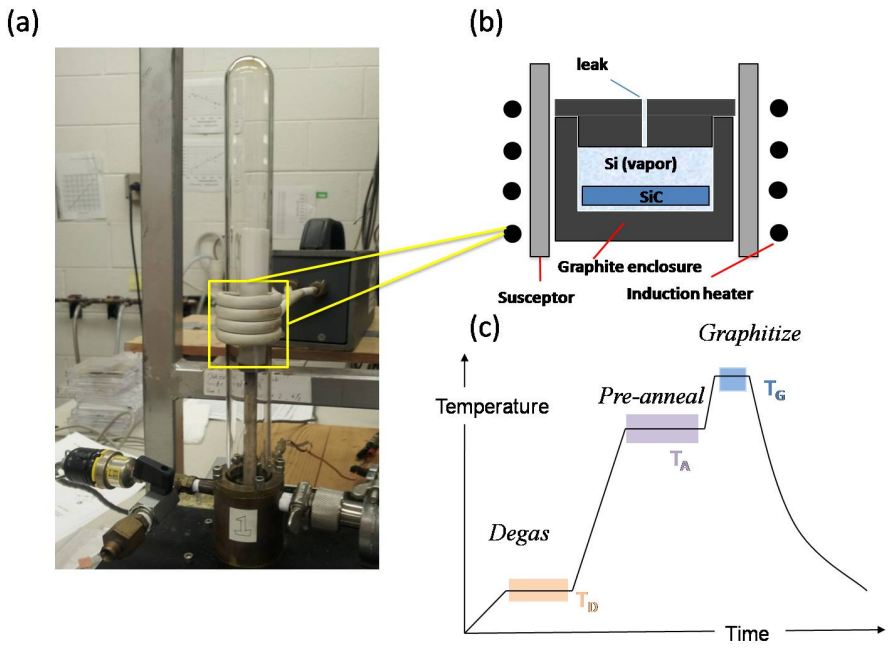

Figure 2.2: (a) Photo of the induction furnace system used in this study. (b) Schematic of a SiC sample in the graphite crucible with a leak, surrounded by susceptor and RF induction coil. (c) Typical annealing process for graphene growth containing three stages: degas, pre-anneal and graphitization.

the 10^{-10} Torr range. Since there is adsorption of Si in the graphite crucible after several annealing cycles of SiC, the sublimation rate of Si from the crucible should be accounted for as the exact graphene growth rate is concerned. On the other side, each sublimated atomic layer of Si would leave an atomic layer of carbon behind for graphene formation. According to the carbon atom density in SiC and graphene, there are approximately enough carbon atoms in 3 SiC bi-layers to form a mono-layer of graphene.

The graphite crucible is inside a quartz tube, and is surrounded by a molybdenum cap as the susceptor and a ceramic tube for heat insulation, as shown in Fig. 2.2 (a). The system is pumped down by a turbo pump with a mechanical backing pump, and is usually pumped to $1 \sim 2 \times 10^{-6}$ Torr before starting the annealing process. The temperature of the sample is monitored by a thermocouple touching the crucible. A typical heating sequence is shown in Fig. 2.2 (c). There are 3 annealing stages in

this process. The first stage is the degas stage at about 200 °C for 20 minutes until outgassing of the system is completed . The second stage at around 1200 °C for 20 minutes is chosen so that the native oxide on SiC surface is removed, the surface material starts to flow for initial atomic step formation without sublimation of Si and graphene formation. And in the final stage at about 1500 °C for 5 $\sim$ 30 minutes, surface Si atoms on SiC start to escape from the sample, and graphene forms. After that, the system is naturally cooled down in high vacuum to prevent post-growth contamination to the graphene.

2.3 Characterization of C-face Mono-layer Graphene After Growth

2.3.1 Introduction to the Characterization Methods

2.3.1.1 Atomic Force Microscopy

Atomic force microscopy (AFM) belongs to a larger category of surface characterization method, namely scanning probe microscopy (SPM). It utilizes a cantilever with a sharp tip at its end to detect the surface topography. The tip interacts with the sample surface through Van de Waals (VDW) force during the measurement, thus could pick up the information of surface topography change during the scan to generate images. There are two major operation modes for standard AFM, contact mode and non-contact mode. In contact mode, the tip is pressed against the sample surface at a fixed force (typically a few nN), and the cantilever is deformed to maintain the force as the tip scans over the sample surface. Such deformation of the cantilever is measured by a photo detector recording the deflection of a laser beam aligned to the end of the cantilever. The signal is then converted to the height profile of the sample surface. In non-contact mode, the tip is a few nm away from the sample surface, and is set to oscillate slight above its resonance frequency, which depends not only on the mechanical property of the cantilever and the tip, but also on the VDW force between the tip and the sample surface. As the distance changes between the tip and

the sample surface as the tip is scanning over the surface, so does the VDW force as well as the oscillation amplitude of the cantilever. Such change is detected by a similar laser beam/photo detector system as in the contact mode. It would be fed back to the piezoelectric system that modifies the height of the tip to keep constant tip-sample distance, while monitoring the height of the tip at the same time. 2D plots of the height profile of the sample surface are thus obtained.

Both of the above methods have advantages and disadvantages. Contact mode is easier to understand in equipment design and data analysis. But it may cause damage to the sample surface during the measurement, due to the direct contact of the tip to the sample. In contrast, non-contact mode does not harm the sample surface, since the tip does not have to touch the surface. Instead, it is harder to realize, especially on soft surfaces or in liquid. Both methods are widely used due to their high resolution, and less technical difficulty compared with scanning tunneling microscopy (STM). The AFM instrument used in this work is Park System XE70, with non-contact tip PPP-NCHR having a typical tip size of 10nm from NANOSENSORS^{TM}. The lateral resolution of the system is limited by the tip size to $\sim$ 10nm, and the height resolution is 0.1 $\mathring{A}$ as the system is in air and at room temperature.

2.3.1.2 Raman Spectroscopy

Raman spectroscopy is primarily used to characterize phonon modes (interacting with electrons) of materials. It measures the photo intensity of the laser reflected from the sample at different wavelengths from the incident laser beam. This is generated due to phonon-induced relaxation of electrons excited by the incident mono-chromatic laser. Certain selection rules have to be satisfied for the electron-phonon scattering to occur, thus Raman spectra reflects both the electronic and phonon band structures of the material.

A graphene Raman spectrum has three signature peaks in the window 1200$\sim$3400

cm^{-1}, namely D peak ($\sim$ 1350 cm^{-1}), G peak ($\sim$ 1580 cm^{-1}), and 2D peak ($\sim$ 2680 cm^{-1}) (with 532nm laser). The relating electron-phonon interaction for these peaks are demonstrated in Fig. 2.3. An electron-hole pair is excited by an incident photon in the same Dirac cone for all three cases. For the G peak, the electron undergoes inelastic scattering with the zone-center E_{2g} optical phonon, and then the electron-hole recombination creates a photon with slightly lower energy than the incident photon. For D and 2D peaks, the excited electron interacts with an A_{1g} phonon, and is scattered to the opposite Dirac cone. In the case of D peak, the electron is then elastically scattered by a defect or zone boundary in graphene back to the conduction band of the original cone, and recombines with the hole to emit a photon with lower energy. Thus the intensity of D peak reflects the density of defects in the graphene sample. As for the 2D peak, the electron is scattered back to the original Dirac cone by another A_{1g} phonon before the recombination, thus the photon energy (wave number) shift from the incident photon is twice that of the D peak, the reason why it is called "2D" peak.

From the Raman spectra of graphene samples, a few electronics properties of the material could be investigated [17]. First, since the D peak is primarily defect-driven while G peak is not, the ratio between the intensity of the two, i.e., I(D)/I(G) is often used to indicate the defect density of large graphene samples. For graphene sheets with low defect density, this ratio is close to zero. Besides, mono-layer and multi-layer graphene (AB stacking) have different 2D peak profiles. For mono-layer graphene, the 2D peak is typically single Lorentzian because of the finite lifetime of phonons. Combination of multiple single Lorentzian peaks for the 2D peak is observed on multi-layer graphene, due to different energies of phonons involved in the scattering at different electronic bands in multi-layer graphene. For example, the 2D peak of AB stacked bi-layer graphene is a combination of four Lorentzian peaks. This character in 2D peaks of graphene is usually used to identify mono-layer graphene.

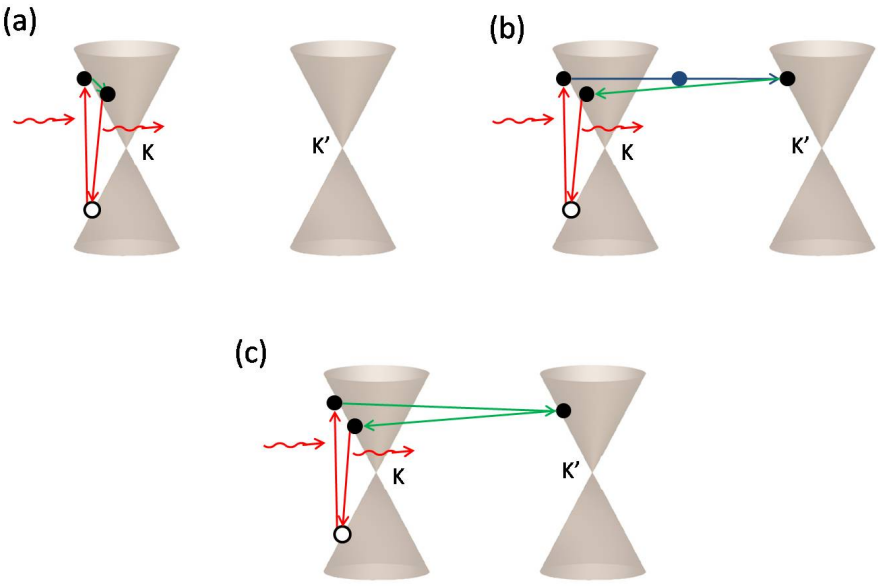

Figure 2.3: Electron-phonon (e-ph) scattering for graphene Raman peaks. (a) G peak involves one e-ph scattering within the same Dirac cone. (b) D peak involves one e-ph scattering to different cones, and another elastic scattering for the electron with a defect or zone boundary. (c) 2D peak involves two inter-cone e-ph scattering.

Third, the shift in wave numbers for G and 2D peaks is also indication of the doping level and strain of the graphene sample. Increase in both electron and hole doping rises the energy of E_{2g} phonon, thus higher shift in G peak. For 2D peak, the energy of A_{1g} phonon increases when graphene changes from electron to hole doped, so the 2D peak shifts monotonously with change of graphene doping.

2.3.2 AFM Topography of C-face Epitaxial Graphene on SiC

Fig. 2.4 (b) is an AFM image of C-face multi-layer graphene at screw dislocations in SiC. SiC steps around the screw dislocation are obvious in the image, while > 10 nm high pleats cover the scanned graphene region (white stripes in the AFM images). They originate from different thermal expansion coefficients of graphene and SiC during the cool down step in the growth process. The large Si sublimation rate around the screw dislocation result in uncontrollable growth rate for graphene, thus the end product is multi-layer graphene. Note that not all multi-layer graphene grows

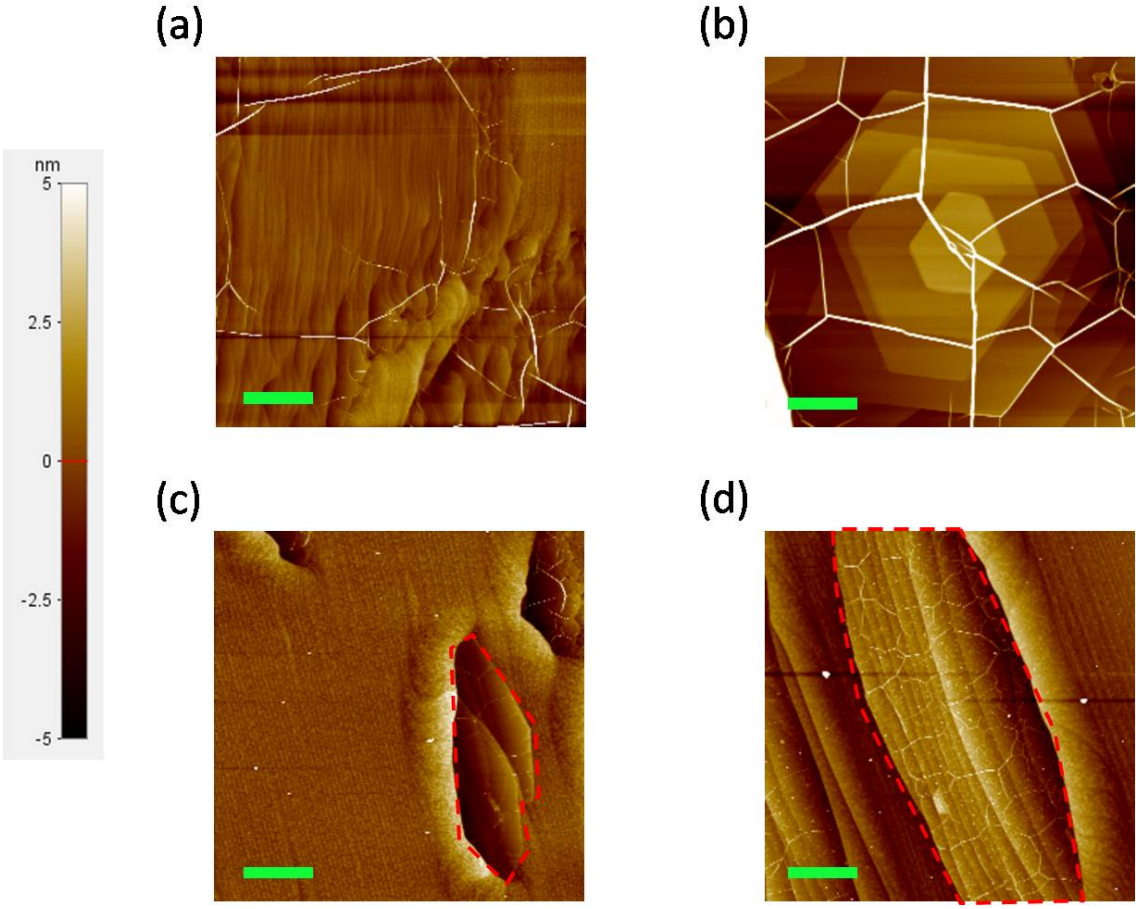

Figure 2.4: AFM images of multi-layer and mono-layer C-face graphene. (a) Typical topography of multilayer graphene with pleats. Scale bar is 4 μm. (b) Multi-layer graphene on top of screw dislocation of underlying SiC. Scale bar is 1 μm. (c) Pristine mono-layer graphene region (marked by red dashed line) with surrounding bare SiC. Scale bar is 4 μm. (d) A larger region of mono-layer graphene with residue particles on top. Scale bar is 3 μm.

from dislocations, as shown in Fig. 2.4 (a), despite that dislocations usually result in multi-layer graphene growth after annealing.

Example AFM images of mono-layer C-face graphene are shown in Fig. 2.4 (c-d). Compared with the surrounding region not covered by graphene, mono-layer graphene region has a smoother surface on each step terrace, while the step size and height in graphene region are larger than that of bare SiC. There are also pleats on mono-layer graphene, but their height (a few nm) is much smaller compared with that of multi-layer graphene, and there are usually fewer pleats per unit area as well.

Besides, there is no recognizable "seed" or starting point for the growth of mono-layer C-face graphene, which indicates that mono-layer graphene on C-face either starts to grown from seeds undetectable by AFM, or the growth is spontaneously initiated. The size of mono-layer graphene region varies from sample to sample. It not only depends on the growth condition, i.e., annealing temperature and time, temperature ramping pattern (ramping speed, overshoot, etc.), but is also related to properties of the SiC, i.e., the surface quality and miscut angle. For the surface quality, samples with too many defects such as screw dislocations are generally less covered by mono-layer graphene, since multi-layer graphene initiated from these defects already covers most of the surface due to their larger growth rate, and prohibits the growth for mono-layer graphene. The SiC wafer miscut angle is defined as follows. 4H-SiC used here are supposed to be diced exactly on the SiC(0001) plane, while in the actual wafer dicing there is an error in the dicing direction. On-axis wafers from CREE Inc. guarantee miscut angles $< 0.3°$, and the miscut angle of each wafer is measured after dicing. The SiC wafers used in this study usually have miscut angles from $0°$ to $0.2°$, and typically mono-layer graphene of larger size is obtained with smaller miscut angles.

To identify mono-layer graphene regions on C-face SiC, a few differences in surface topography between multi-layer and mono-layer graphene could be utilized, according to the above description of AFM images. First, mono-layer C-face graphene grown at moderate annealing temperatures does not have recognizable defects in underneath SiC as the initiation, while multi-layer graphene usually starts to grow on defects such as screw dislocations. Second, the height of pleats in mono-layer graphene is usually a few nm (up to 5nm), while multi-layer graphene often has $>$ 10nm high pleats. However, the graphene regions that meet the above criteria are not always mono-layer graphene, and cross-reference of Raman spectra of the regions are used to double confirm the mono-layer property.

2.3.3 Raman Spectroscopy of C-face Epitaxial Graphene on SiC

Raman spectra of multi-layer and mono-layer epitaxial graphene on C-face SiC are shown in Fig. 2.5. The main differences in Raman spectra between multi-layer and mono-layer graphene are G peak and 2D peak profiles. For G peak in general, the intensity is larger when there are more layers of graphene. For mono-layer graphene, its G peak is much smaller compared with the largest peak of SiC background at $\sim$ 1500 cm^{-1}, and its full width at half maximum (FWHM) is usually below 10 cm^{-1}. As for the 2D peak, the analysis is more complicated. For mono-layer graphene, its 2D peak is single Lorentzian, the same as the case of mono-layer exfoliated graphene, and its FWHM is below 30 cm^{-1}. The profile of 2D peak of multi-layer C-face graphene highly depend on the stacking order of the layers. In the case of rotational stacking [38], the 2D peak is still single Lorentzian, since each layer in the stack acts as an electronically independent graphene mono-layer in this case. Its intensity would be higher than that of mono-layer graphene, though, since more than one layer of graphene are contributing to it. In the other case, when AB stacking is present in the graphene layers, the 2D peak would be an overlap of multiple single Lorentzian peaks centered at different Raman shifts, similar to AB stacked bi-layer and multi-layer exfoliated graphene.

As far as identification of mono-layer graphene on C-face SiC via Raman spectra is concerned, both the G peak and 2D peak need to be concerned. As discussed above, the relative G peak intensity to the background SiC spectra (for monolayer, height of the G peak is smaller than half of SiC background peak at 1500 cm^{-1}) is used to roughly exclude most of the multi-layer graphene. Further confirmation comes from the analysis of 2D peaks, and regions where single Lorentzian peaks with proper intensity (i.e., that in Fig. 2.5 (d), which is lower than the highest SiC peak in the window) and FWHM (below 30cm^{-1}) are finally selected to be candidates of mono-layer graphene. At the same time, the intensity of D peak in the spectra needs

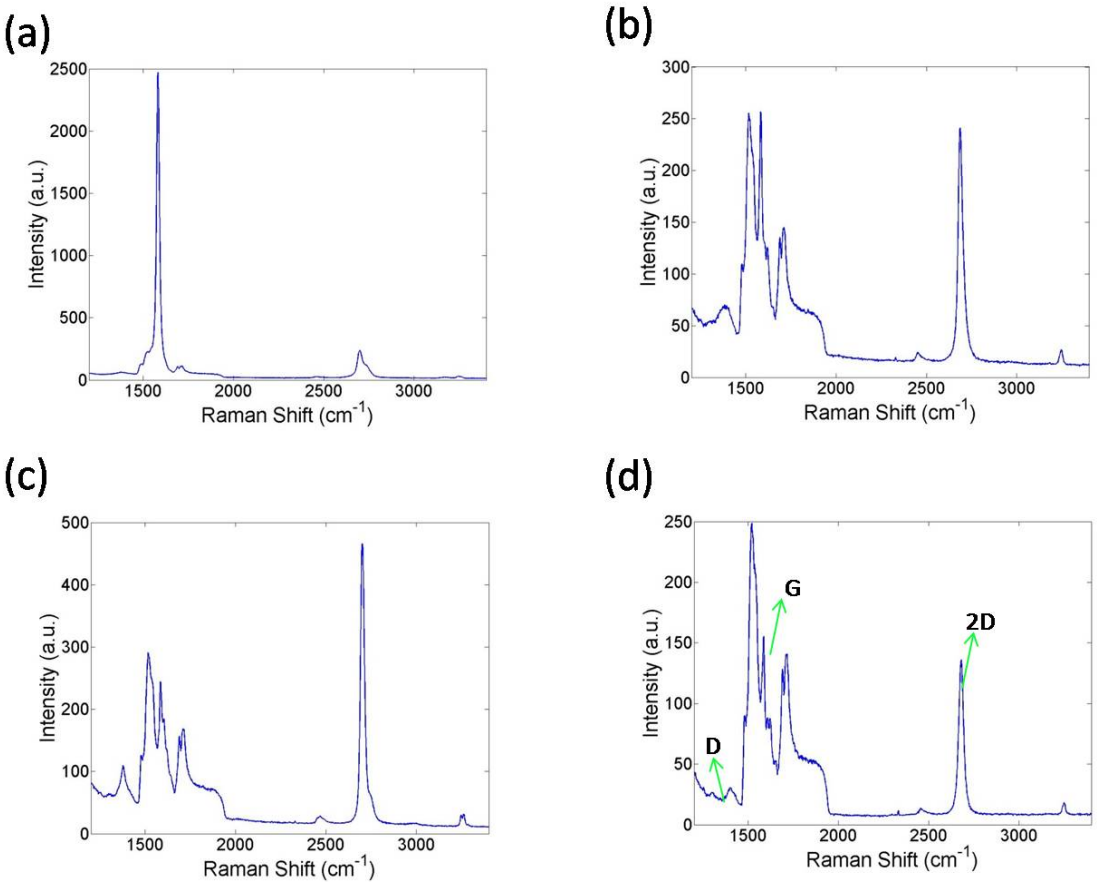

Figure 2.5: Raman spectra of multi-layer and mono-layer C-face graphene on SiC. (a) >10 layer graphene with strong G peak and 2D peak that is not single Lorentzian. (b) Few-layer graphene with single Lorentzian 2D peak, indicating rotational stacking. (c) Few-layer graphene with 2D peak that is not single Lorentzian. (d) Mono-layer graphene Raman spectrum with single Lorentzian 2D peak, G peak with moderate intensity, and absence of D peak, indicating low defect density. Note that the spectra "background" besides the three graphene peaks in (a-d) are the SiC Raman spectra.

to be considered for the defect density in the mono-layer graphene. For a properly grown sample, the Raman spectra of its mono-layer graphene should be free from recognizable D peaks. In the Raman spectroscope used here, it should be smaller than the background noise ($\sim$ 30 in arbitrary unit (a.u.) while the intensity of mono-layer graphene G peak is 500$\sim$1000 in the same unit), thus the D/G ratio is smaller than 5%, which is similar to that of the best exfoliated graphene samples.

Combined with signatures in AFM topography, the above characterization method for C-face epitaxial graphene in Raman spectra could identify mono-layers with a high chance, as confirmed by further electrical characterization (Hall resistance versus magnetic field, QHE, etc). Such identification approach is used for Hall bar fabrication on mono-layer C-face epitaxial graphene, as well as further top-gated graphene transistors and RF transistors, which will be covered in the following chapters.

2.4 Electrical Characterization of Mono-layer C-face Graphene Hall Bars

2.4.1 Fabrication Equipments

2.4.1.1 Electron Beam Lithography

E-beam lithography (EBL) is usually used to pattern structures with small features, sometimes down to 10nm, by exposing the e-beam resist at designated regions on the samples with focused electron beam. Due to the smaller wavelength of electrons than photons, EBL can reach a smaller feature size than that of photo-lithography. However, with pixel-by-pixel exposure mechanism and absence of electron source with high enough intensity, EBL is far less efficient compared with photo-lithography, thus is rarely used in the semiconductor industry except for the gate structures in III-V high-electron-mobility-transistors (HEMT). For a EBL process, a sample (wafer) is first coated with e-beam resist, then inserted in the EBL system for exposing designated regions to the electron beam. After that, the sample undergoes a developing step, in which it is immersed in developer solution that dissolves the e-beam resist

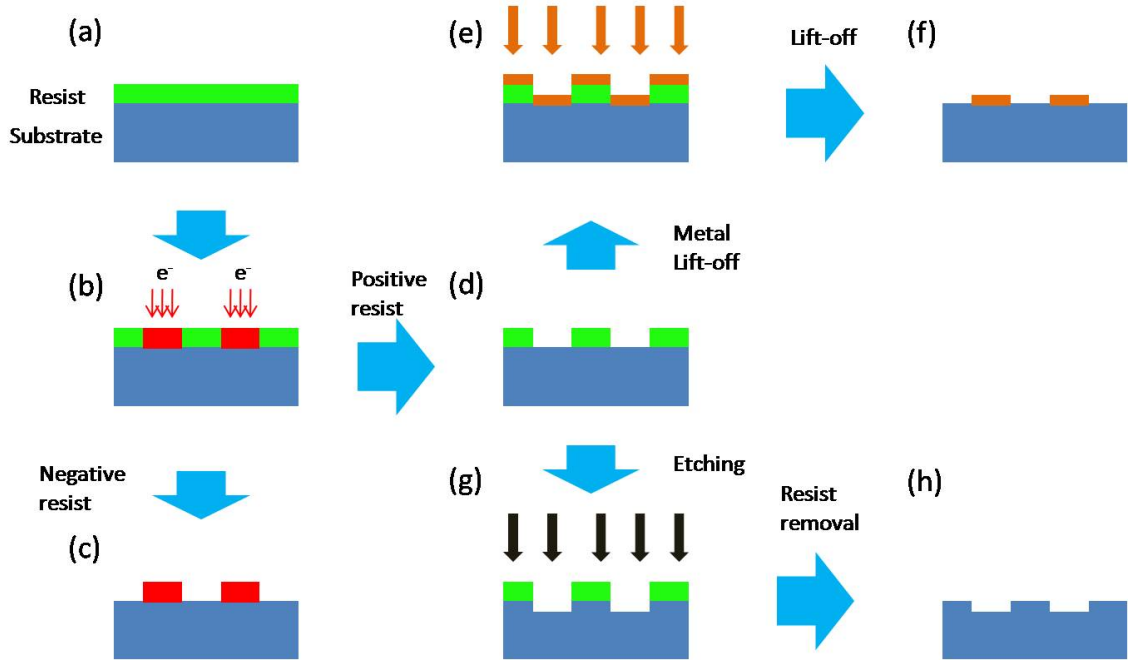

Figure 2.6: Schematic diagram of e-beam lithography process with positive and negative resist, for metal lift-off and material etching, respectively. (a) Spin coat e-beam resist on the substrate. (b) Expose designated regions to the e-beam. (c-d) Develop the pattern in proper developers, and for negative resist, unexposed resist is removed, while for positive resist, exposed resist is removed. (e-f) Metal is deposited on the substrate, then lift-off step removes the resist with metal on top, and only the metal in the exposed regions remain. (g-h) The substrate is etched to a certain depth, while the resist protects underlying substrate from the etching, thus only the exposed regions are etched.

of exposed (for positive resist) or unexposed regions (for negative resist). The end product is a sample with e-beam resist in desired regions to prevent such regions from being etched or covered by deposited material (lift-off) in further processes. A schematic of the process is shown in Fig. 2.6. Different steps of this process for this study are discussed about as follows.

First, the most used e-beam resist in this study is positive tone poly-methyl methacrylate (PMMA) 950k (molecular mass), accompanied by methyl methacrylate (MMA) when lifting-off of thick layers of metals. PMMA is dissolved in anisole at certain concentrations for different film thicknesses. The thickness also depends on the speed and time of the spin-coating. For example, with PMMA 950k A6 (6%

in anisole) at a spinning speed of 5000 rpm (round per minute), the end product is 600nm thick PMMA layer on 3.5mm $\times$ 4.5mm samples, and this recipe is used in this study for general graphene etching mask, and $<$ 60nm thick metal lift-off. Another recipe used in RF transistor T-gate fabrication is PMMA 950k A2 (2% in anisole) at 7000 rpm, resulting in 70nm thick PMMA layer. Note that 50nm wide features have be obtained with the latter recipe. After the spin-coating, the PMMA layer requires a baking process to get rid of the extra solvent and promote the cross-linking of the polymer. Here this baking step is performed on a hot plate at 180 °C for 90 seconds.

In the following e-beam exposure, two different EBL systems are used in this study. For Hall bar fabrication, a EBL system built from JEOL JSM-5910 SEM (at the School of Physics, Georgia Tech) is used. This system uses 30kV e-beam acceleration voltage, and has a spacial resolution of 100nm and aligning accuracy of 200nm. For RF transistor fabrication that requires sub-50nm features and ultra-smooth metal edges to prevent un-necessary microwave dispersion, a JEOL EBX-9300 EBL system (in the Georgia Tech cleanroom) is used with acceleration voltage at 100kV. It has a spacial resolution of 10nm, and alignment accuracy of 20nm. The pattern for exposure is designed in AutoCAD^{TM}, and converted to an pixel-by-pixel exposure map for the EBL system. The dose for exposure, which is the amount of incident electron charge to the sample (in $\mu C/cm^2$), is also defined in the file, which is set to be 400 $\mu C/cm^2$ at 30kV, and 1200 $\mu C/cm^2$ at 100kV acceleration voltage. It is then translated into exposure time per pixel at a fixed e-beam current. When multiple EBL steps are required in a process, the patterns of different steps need to be aligned with each other. This is realized by metallic (often gold) marks on the sample as a reference that have strong contrast to the substrate (SiC) under e-beam. Prior to each step of e-beam exposure, these marks are inspected and their positions are recorded relative to the center of field of view (FOV). Then a transfer matrix (including translation and rotation) is calculated automatically, and the pattern file is converted to the real

exposure profile according to the matrix. For the EBL system built from JEOL JSM-5910 SEM, the inspection of the alignment marks is performed manually by looking at the whole marks in the SEM. As for the state-of-the-art JEOL EBX-9300 EBL system, the alignment marks (crosses) are detected by line scans across the vertical and horizontal bars of the cross, and the edges are determined automatically from the scans, which provides a higher alignment accuracy.

As for the developing of the exposed PMMA, a mixture of methyl isobutyl ketone (MIBK) and IPA at a volume ratio of 1:2 or 1:3 is used at room temperature. The sample is soaked in the solvent for 15 seconds (for the home-built EBL) to 1 minute (for JEOL EBX-9300) before getting rinsed with flowing IPA for another 30 seconds to remove any residue developer. A longer developing time may result in a more thorough removal of unwanted resist residue, but could cause over-developing that may result in oversized developed regions. Over-developing should be avoided for MMA/PMMA bi-layer resist where MMA gets more developed than PMMA to provide an undercut in the resist for easier lift-off, since excessive undercut may cause the upper PMMA layer to collapse, and subsequent lift-off failure.

2.4.1.2 Reactive Ion Etching

Reactive ion etching (RIE) is a useful dry etching method for materials, which are graphene and SiC (for alignment marks and sidewall nano-ribbons) in this study. The plasma, generated by a high frequency electric field in the system, ionizes the reactants, and reduces chemical reaction barriers. When the energized ions strike on the sample surface, both physical sputtering and chemical reaction occur, among which sputtering is directional (anisotropic) while the chemical reaction is usually not (isotropic). To etch only the desired regions, a mask is used to protect the regions not to be etched. The mask can be soft mask such as patterned resist (PMMA) or hard mask such as metals (Ni) and oxides (Al_2O_3), depending on the target material

and depth for the etching process. For few layer graphene removal, PMMA is usually used as the mask, while for deep etching of SiC for alignment marks (600nm deep), 100nm thick Ni is used due to its good selectivity in the etching process. A typical graphene etching recipe includes O_2 plasma exposure at a power of 16W in an 8-inch chamber for 30 seconds to remove up to 10 layers of graphene or $\sim$ 100nm thick PMMA 950k. Due to the bad selectivity of PMMA against O_2 plasma, thick enough PMMA is required for the etching, and the minimum feature size of the patterned structures is limited considering the required robustness of the PMMA structures to withstand the etching process.

Another application of RIE in this study is de-scumming before metal deposition. When the graphene regions of devices are not exposed to the e-beam, after developing of the resist, the sample is subject to O_2 RIE for 20$\sim$30 seconds at the same condition mentioned above to remove any resist residue from the developing step, while still leaving thick enough resist layer in the protected regions for future lift-off. As the residue is removed, the deposited metal layer has a smoother surface, and its adhesion to the substrate is improved.

2.4.1.3 Electron Beam Evaporation

Most metal deposition processes in this study (contacts, gates, etc) are performed using e-beam evaporators. The system is in vacuum, and consists of metal sources, a e-beam source, a thickness monitor and a sample stage. The electron beam is focused on the metal source (beam spot diameter $<$ 1cm) to locally heat it up to above its melting point. As a result, a small portion of the source vaporizes and metal atoms move towards the faced-down samples 50$\sim$100 cm above the source for directional deposition. A shutter located above the metal source can be opened and closed to start and stop the deposition at any time, while the thickness monitor records the metal deposition rate (in $\mathring{A}$/sec) and total thickness. Different metal sources are

stored in the system, so that multiple types of metal can be deposited subsequently on the sample without bringing the sample to air. The system pressure prior to and during the metal deposition is usually kept at 1×10^{-5} to 1×10^{-6} Torr for directional deposition, and to avoid possible reaction between the metal source and residue gas in the system, such as aluminum with oxygen (there are exceptions). The deposition rate for the metals ranges from 0.1 to 3 $\mathring{A}$/sec. Generally, a lower deposition rate results in a more uniform deposited film, while consuming more process time. For example, for metal contacts to graphene, palladium/gold (Pd/Au) stack is used, and the deposition rates of both metals are set to 0.7 $\mathring{A}$/sec for a relatively smooth surface (surface roughness on the order of nm) at a relative short period of process time.

Special attention is required for evaporation of metals with high melting points, such as platinum (Pt). In this case, the temperature of the sample increases as the source is heated up by e-beam, primarily due to radiation. With overheating of the sample, the patterned PMMA resist covering the sample may partially deform, and can cause failure in structure definition and lift-off. Thus the sample should be far away from the metal source (which causes lower deposition rate at the same e-beam input power instead), and the total metal thickness is limited (maximum 30nm thick Pt at 1.0 $\mathring{A}$/sec for the system used in this study).

2.4.2 Fabrication Process Flow

The fabrication process flow for mono-layer C-face graphene Hall bars is shown in Fig. 2.7. First, EBL and e-beam evaporation of Ti/Au define alignment marks on the C-face of the sample to assist identification of mono-layer graphene and aligning for further EBL steps. After a metal lift-off process in warm acetone to remove the resist residue as much as possible, regions around the alignment marks are inspected with optical microscope and Raman spectroscopy to identify mono-layer graphene. Then the areas of interest are scanned with AFM (along with the alignment marks) to

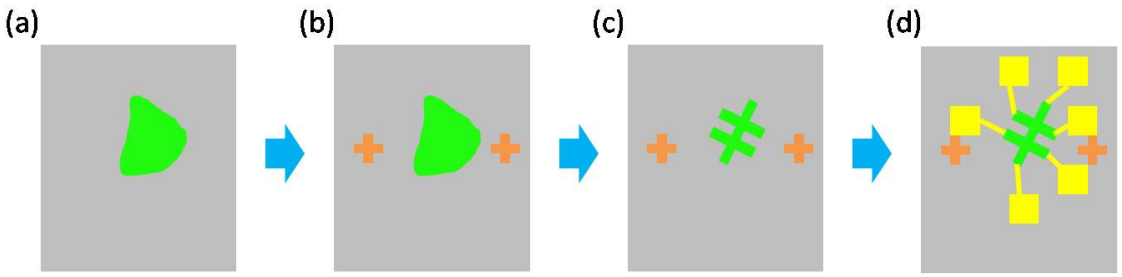

Figure 2.7: Process flow for mono-layer C-face graphene Hall bar fabrication. (a) As grown mono-layer C-face graphene (green region) on SiC. (b) Alignment marks are deposited on the sample near the mono-layer graphene. (c) EBL and RIE to remove extra graphene and define the Hall bar. (d) EBL and Pd/Au deposition to fabricate metal contacts and probing pads for the devices. Note that the graphene region, Hall bar, metal pads and SiC sample are not plotted in actual scale.

obtain the positions of the mono-layer graphene relative to the marks, which will be used in EBL pattern files. EBL is used to define the graphene Hall bar protected by PMMA layer, while excessive graphene is removed by O_2 RIE. Finally, metal contacts to the graphene Hall bars are defined by another EBL step and metal deposition of Ti/Pd/Au, and the sample is ready for electrical measurement after the metal lift-off. A few key steps are discussed about in detail as follows.

First, Ti/Pd/Au tri-layer of 0.5nm/20nm/40nm is selected as the contact metal stack to graphene Hall bars. This recipe does not provide the lowest contact resistance between graphene and metal, due to the presence of the low work function Ti as the bottom layer. Nor does this recipe provide the most robust contacts, since there is only 0.5nm thick Ti, while Pd and Au are not metals with good stiffness and adhesion to the substrate. However, this combination of metal stack provides a good balance between low contact resistance and robustness, which facilitates room temperature probe station measurements that require relatively mechanically robust probing pads, and low temperature low noise measurements that take advantage of the relatively small contact resistance enabling stable 4-point and Hall resistance measurements. Besides, the metal stack is fabricated in a single e-beam evaporation

step, preventing surface oxidization of the Ti and Pd layers. Note that in RF transistor fabrication (in Chapter 4), two separate steps are taken for fabrication of metal contact to graphene and probing pads, respectively, in order to reach the smallest possible contact resistance.

A more tricky step is the surface treatment of graphene Hall bars after contact fabrication. Since oxygen and/or water in air may cause p-doping to C-face graphene, as-made C-face mono-layer graphene Hall bars are usually found to be hole-doped from Hall measurements. However, for the observation of the quantum Hall effect at reasonable magnetic fields, the graphene sample needs to be doped at relatively low levels (either n or p). For example, to observe the $\nu = 2$ plateau at a magnetic field of 18 Tesla (T), a carrier density of $\sim 1.3\times10^{12}/cm^2$ is required, which is lower than that of graphene samples completely exposed to air. Even though the sample chamber is in vacuum as the measurement is performed at low temperatures, the adsorbents at graphene surface still remain after the pump down. The method I use to solve this problem is to cover the sample with a thin layer of PMMA residue ($\sim$ 10nm) simply through a step of spin-coating followed by room temperature acetone removal in a relatively short period of time (5 minutes). Then the sample is "annealed" in hot water ($> 80°$C) for 30 minutes. As counterintuitive as this step might seem, though, the result is low-level doped (n or p) graphene Hall bar (from Hall measurement). An AFM image of the Hall bar after the above process is shown in Fig. 2.8, along with a schematic diagram of electrical connections for measurements.

2.4.3 Room Temperature Electrical Characterization

As-fabricated graphene Hall bars are first characterized on a room temperature probe station. During each measurement, two probes provide constant current to the Hall bar, and another two probes measure the voltage drop between two contacts on the same side (4-point resistance) or opposite sides (Hall resistance) of the bar with or

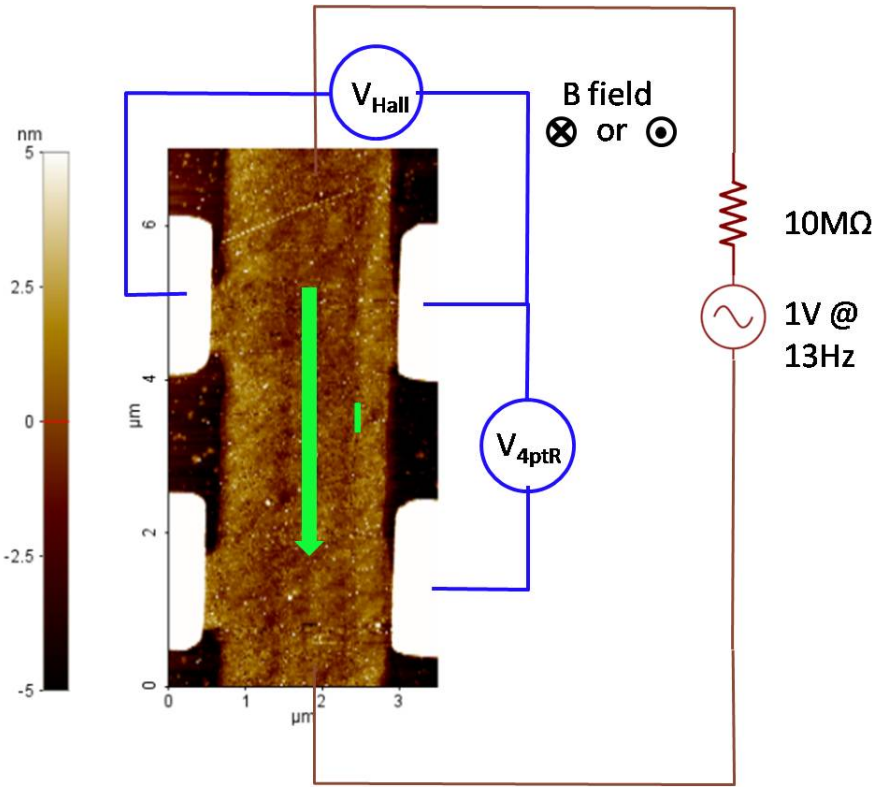

Figure 2.8: AFM image of as-fabricated C-face mono-layer graphene Hall bar with PMMA resist residue, and schematic of electrical connections for resistivity and Hall resistance measurement.

without a small magnet under the sample that provides $\sim$ 0.15T magnetic field on either direction penetrating the Hall bars, as shown in Fig. 2.8. The current and voltage are provided and measured with SR830 lock-in amplifiers at 13 Hz, and the input current is maintained constant by applying a constant voltage (1V to 5V) to the devices through a series resistance (1 MΩ to 1 GΩ) much larger than the two point resistance of the Hall bar (usually below 30 kΩ). The magnetic field is reversed during the Hall resistance measurement, and the results with different magnetic field directions are recorded and subtracted to obtain the Hall resistance R_H in Ω/T. The carrier density of the Hall bar is extracted as $n = 1/(eR_H)$ in m^{-2}. The resistivity of the Hall bar is extracted from 4-point resistances R_{4pt} and the dimensions (length L and width W) of the Hall bar as $R_{sq} = R_{4pt}/L \times W$. In this study, $W = 1 \sim 3\mu m$, and $L = 4 \sim 6\mu m$. Hall mobilities of the measured devices are extrapolated as $\mu_{Hall} = R_H/R_{sq}$.

Table 2.1: Room Temperature Hall Mobility of C-face Mono-layer Graphene

Sample #	Resistivity R(Ω/sq)	Hall Resistance (Ω/T)	Carrier Density p-type ($10^{12}/cm^2$)	Hall Mobility (cm^2/Vs)
#1	600$\sim$620	680$\sim$760	0.82$\sim$0.92	11,000$\sim$13,000
#2	620$\sim$930	830$\sim$1000	0.63$\sim$0.75	10,000$\sim$13,000
#3	560$\sim$680	910$\sim$970	0.64$\sim$0.69	13,000$\sim$17,000
#4	580$\sim$610	830$\sim$850	0.74$\sim$0.75	$\sim$14,000
#5	650$\sim$820	890$\sim$990	0.63$\sim$0.70	12,000$\sim$14,000

Table. 2.1 shows the room temperature measurement result of five Hall bars on the same sample with 8 probes on each Hall bar. Thus four 4-point resistances (converted to two average resistivity results on each device) and three Hall resistances are measured on each device, and a range of extrapolated Hall mobilities are provided. From the data, the mobilities for the measured devices are all between 10,000 and 20,000 cm^2/Vs, indicating the high quality of C-face mono-layer graphene, and reproducibility of the electronic properties at room temperature.

2.4.4 Low Temperature Electrical Characterization

Low temperature electrical measurement of C-face mono-layer graphene Hall bars is performed in a liquid helium cryogenic station (cryostat) with a superconducting magnet up to 9 Tesla. 4-point resistance and Hall resistance are measured with lock-in amplifiers in magnetic field sweeps from -9T to 9T at 4.2 Kelvin (K). Examples of magneto-resistance and Hall resistance versus magnetic field data plots are shown in Fig. 2.9. Shubnikov-de Haas oscillation can be observed in the magneto-resistance curves, and Hall resistance quantization at different Landau filling factors corresponds well with the minima of the magneto-resistance. Such result confirms that with the above fabrication method for Hall bar devices, high quality C-face mono-layer graphene demonstrates transport properties similar to that of mono-layer exfoliated graphene on SiO_2 [105, 73]. The result is reproducible not only over different devices of the same sample, but also over different samples. Thus high carrier mobility is an innate property of C-face mono-layer epitaxial graphene on SiC.

On a Hall bar device with carrier density much lower than regularly observed ($1.9 \times 10^{11}/cm^2$), an even higher Hall mobility of $\mu = 39,800 cm^2/Vs$ is measured at 4.2K [41]. Magneto- and Hall resistances of this device are plotted in Fig. 2.10. Due to the low carrier density and high mobility, the $\nu = 2$ Landau level quantization occurs at $\sim$ 3.5T magnetic field, with the Hall resistance quantized at exactly $h/2e^2$ and magneto-resistance approaching zero, typical evidence of the quantum Hall effect. Here, due to the emerging cyclotron states in the Hall bar, carriers are localized in the bulk of the device and do not contribute to the transport, while electrons and holes propagate ballistically only on protected edge states of the device, causing observation of zero resistance in 4-point measurements. As the magnetic field is raised above 5T, the magneto-resistance starts to increase, while the Hall resistance starts to increase at $\sim$ 7T, indicating that the spin symmetry for carriers in mono-layer graphene is broken. This is the first time quantum Hall effect is observed on synthesized graphene

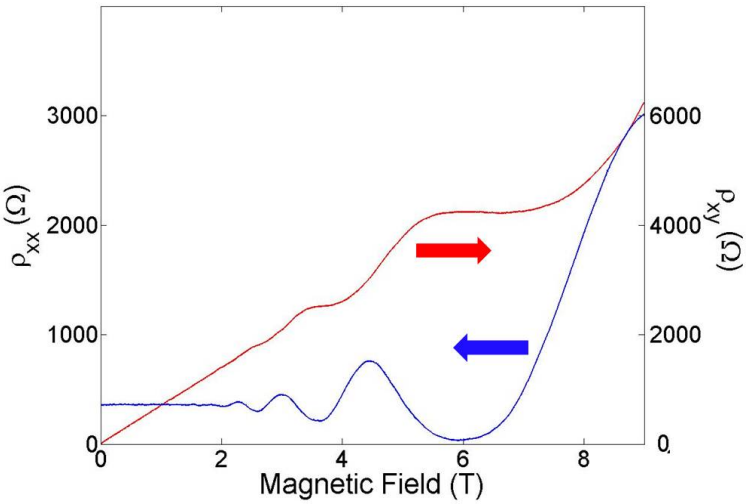

Figure 2.9: Magneto-resistance and Hall resistance of a mono-layer C-face graphene Hall bar measured at 4.2K under magnetic field up to 9T. Shubnikov-de Haas oscillation can be observed in the magneto-resistance, and corresponding Hall resistance quantization are visable up to $\rho_{xy} = h/6e^2$. The extrapolated carrier density of the device from Hall resistance is $n = 9 \times 10^{11}/cm^2$, and the Hall mobility is $\mu_{Hall} = 19300 cm^2/Vs$ under this condition.

(CVD graphene, epitaxial graphene on SiC) at such low magnetic field.

The observation of Hall resistance plateaus at filling factors $\nu = 4n + 2$ is a clear evidence of mono-layer graphene, due to the Berry's phase π of its carriers. In comparison, for AB stacked bilayer graphene, quantum Hall plateaus are present at filling factors $\nu = 4n$ with a Berry's phase of 2π [72]. In this study, the quantum Hall resistance plateaus are used as an unambiguous criterion of the mono-layer nature of the graphene samples. The validity of the identification methods for mono-layer graphene through AFM images and Raman spectra, as described above, is confirmed by the observation of quantum Hall effect with corresponding filling factors on the same devices.

2.5 Summary

In this chapter, I introduced the growth and characterization equipments and methods for mono-layer epitaxial graphene on C-face SiC. The fabrication method of Hall

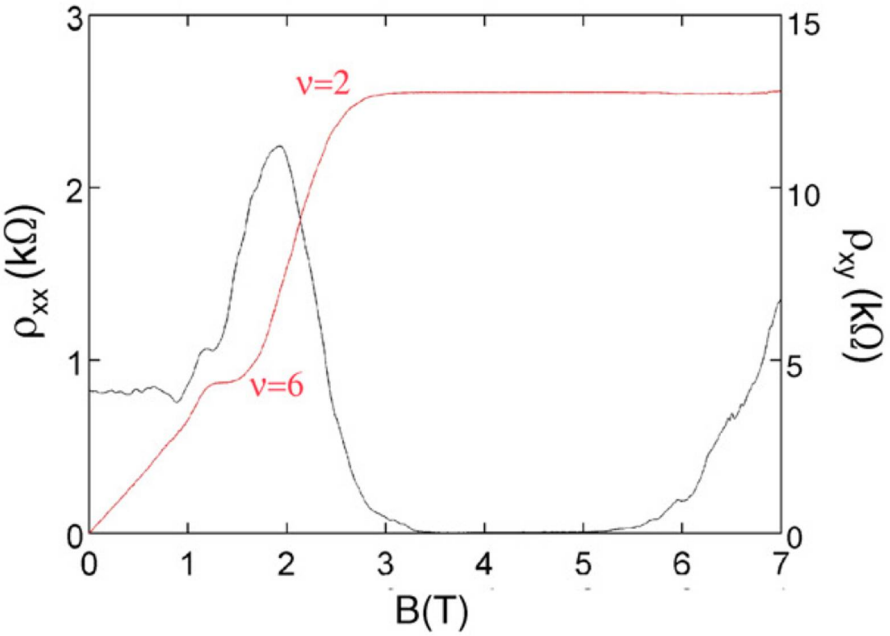

Figure 2.10: Magneto-resistance and Hall resistance versus magnetic field up to 7T at 4.2K from [41]. $\upsilon = 2$ quantum Hall plateau in Hall resistance appears at $\sim 3T$, and magneto-resistance becomes zero at $\sim 3.5T$. The Hall mobility of this device is $\mu = 39,800 cm^2/Vs$, which is one of the highest measured on synthesized graphene.

bar devices aiming for observation of quantum Hall effect at low temperatures is also discussed about in details, followed by the electrical measurement results at both room temperature and low temperature (4.2K), where quantum Hall effect is indeed demonstrated. The measured room temperature and low temperature carrier mobilities rival the best exfoliated graphene on SiO_2, but are still not as good as that of exfoliated graphene on boron nitride (BN). This could be attributed to the presence of PMMA on top of C-face graphene that may induce electron scattering, and the SiC substrate may not necessarily be part of the reason. Such results show that mono-layer epitaxial graphene on SiC has transport properties suitable for future high speed electronic devices.

In order to realize such electronic devices, top gates are required to modify the carrier density in graphene, similar to the principle of a MOSFET. To this end, a reliable method to deposit dielectric layers on graphene is required. Beside all the

ordinary requirements for dielectric materials in MOSFETs, dielectric layer in this case should also maintain the transport performance of graphene. The investigation on this topic will be discussed in detail in the next chapter.

CHAPTER III

DIELECTRIC LAYER ON C-FACE EPITAXIAL GRAPHENE ON SIC

3.1 Introduction

3.1.1 Summary of Previous Work

Access to carrier density modification is crucial to research and application of any material for electronics. A mostly used method to tune the carrier density is electrical gating, which includes top and back gating. For graphene, a most widely used gating method is back gating, since exfoliated graphene and CVD graphene are usually transferred onto SiO_2/Si substrate where doped Si could serve as the gate, while SiO_2 is the gate dielectric. This is a good choice to gate graphene for material characterization, but not suitable for more complicated device concepts or circuit level device operation. However, for epitaxial graphene on SiC, the SiC substrate cannot serve as the back gate in most cases, due to the absence of a dielectric layer (doped SiC as the back gate is used by a few research groups [90]). Besides, in most cases, a back gate universally modifies the carrier density of all the devices on the same wafer die, while circuit level applications usually requires separate gate voltage tuning down to each device. Since epitaxial graphene is usually considered as a scalable platform for graphene electronics with possible industrial applications, top gating methods on this material is necessary for the technology development. To this end, a lot of research effort from academic and industrial institutions has been paid, and several gate dielectric deposition methods have been proposed and investigated. Some of these methods are introduced below.

One of the first proposed dielectric deposition methods for graphene is the NO_2-trimethylaluminum (TMA) functionalization method to serve as the seed for further atomic layer deposition (ALD) of Al_2O_3 with TMA and H_2O [96]. In this study, 50 cycles of NO_2/TMA ALD process were performed to form a seed layer on exfoliated graphene prior to the ordinary H_2O/TMA cycles for Al_2O_3 deposition. This method chemically modifies the surface properties of graphene, so that Al_2O_3 could be uniformly deposited on top via ALD, which cannot be achieved on pristine graphene due to its chemical inertness [95]. Though p-n junction behavior of graphene was demonstrated in this work, the carrier mobility was decreased by this functionalization method due to the chemical reaction between NO_2 and graphene surface. A later report on graphene RF transistors used this dielectric deposition method, and successfully fabricated graphene FETs that could operate at gigahertz frequencies [58].

Another method mentioned in a few reports is direct physical vapor deposition (PVD) of oxide layers on graphene. In 2007, M. C. Lemme et al used 20nm thick PVD SiO_2 as the top gate dielectric layer for graphene field effect devices [52], and serious mobility degradation was observed. Thermal evaporation of HfO_2 was used as the dielectric layer for epitaxial graphene on SiC in another report [46], and FET mobility as high as 5000 cm^2/Vs was measured on C-face multi-layer graphene. This method was not widely used in later studies on top-gated graphene devices despite its straightforward nature, due to the relatively low observed carrier mobility in gated graphene.

A first dielectric deposition method that does not significantly reduce the mobility of graphene was proposed in 2009 by S. Kim et al [49]. Here a 1$\sim$2 nm thick aluminum layer is deposited onto graphene by e-beam evaporation prior to ALD process for Al_2O_3 deposition. This thin Al layer is naturally oxidized in air during the transfer of the sample from the evaporator to the ALD chamber. It served as the seed layer for the ALD process, while not degrading the mobility of graphene as much as does the

NO_2 functionalization method. Field effect mobility above 8000 cm^2/Vs was observed on top-gated mono-layer exfoliated graphene on SiO_2/Si in this work, which is very promising for high speed FETs and non-conventional device designs.

Modification to the above seed layer + ALD method was reported by D. B. Farmer et al in 2009 [26]. Instead of thin evaporated Al layer, a 10nm thick polymer layer was used as the buffer layer for further HfO_2 ALD process. The polymer is NFC 1400-3CP from JSR Micro, Inc., and is diluted in propylene glycol monomethyl ether acetate (PGMEA) for spin-coating on graphene samples. The mobility degradation of mono-layer exfoliated graphene on SiO_2/Si is minimized due to the application of this buffer layer. With this dielectric deposition method, Y.-M. Lin et al were able to achieve a cut-off frequency of 100 GHz on 240nm channel epitaxial graphene RF transistor on Si-face SiC [57]. This method will be discussed about in details later in this chapter.

The above dielectric deposition methods are all compatible with wafer-scale fabrication of top-gated devices. However, none of them could support self-aligned contacts in the process flow, whereas self-alignment is widely used in Si-CMOS devices for minimization of access resistance of devices with limited lithography alignment accuracy. In Si-CMOS fabrication process, the dielectric layer is usually deposited or thermally grown homogeneously on the surface before application of the gate stack and the subsequent etching away of dielectric layer using the gate itself as the mask. Such procedure is not compatible with graphene, since graphene would be damaged in the etching step that involves O_2 plasma. To have a dielectric deposition technique compatible with self-alignment, R. Cheng et al proposed a process including a transfer step for the gate/dielectric stack fabricated on a separate wafer to graphene [15], so that the dielectric material resides only under the gate metal, and no etching step is required. With this method, a record-high cut-off frequency of 427 GHz was achieved on exfoliated graphene with 67nm gate length.

3.1.2 Content of the Chapter

Thanks to the above efforts in finding suitable dielectric deposition methods for graphene, numerous choices are provided regarding the application of dielectric layer on C-face epitaxial graphene on SiC. Several approaches have been experimented on C-face graphene, and they will be discussed in this chapter. This chapter is organized as follows. First, principles of ALD will be briefly introduced, followed by the demonstration of the dielectric deposition methods I used on C-face graphene, including the polymer buffer layer/ALD Al_2O_3, slow deposition of Al, and the Al seed layer. The resulting samples for each of the above methods are characterized for their surface quality and electrical properties, such as hysteresis, leakage, and graphene mobility.

3.2 Introduction to Atomic Layer Deposition Method

ALD is an important technique for thin film deposition in various applications [29]. It is the deposition method of choice for most of the state-of-the-art Si-CMOS fabrication processes featuring high-k dielectric and metal gate (HKMG), and is used by major semiconductor companies such as Intel and TSMC. It has atomic-level control for the thickness of the deposited materials, and possesses unique advantage in conformal coverage for high aspect-ratio features.

An ALD process is similar to CVD processes that use binary reactions. However, unlike CVD process in which two precursors are present simutaneously and the end product is deposited continuously over time, in an ALD process the substrate is exposed to each vaporized precursor alternatively and step-like reaction takes place. A schematic diagram showing the mechanism behind an ALD process is shown in Fig. 3.1 [28]. The substrate is alternately exposed to the two precursors, and each precursor reacts with the substrate surface in a self-limited fashion. Thus at each cycle of the binary reaction, one extra mono-layer of the final product material is formed on the surface. Enough time is provided for the exposure of the surface to

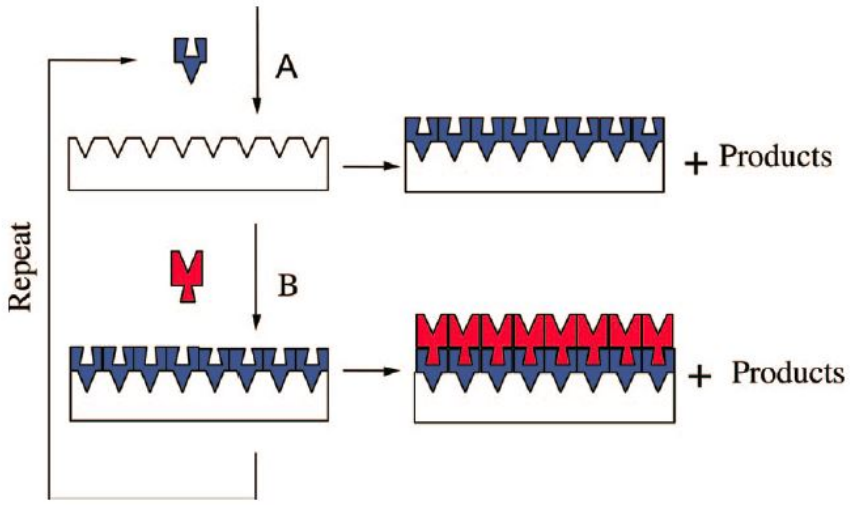

Figure 3.1: Schematic representation of surface self-limiting chemistry of ALD process from [29].

each precursor so that all possible surface sites can react with the precursor. Each exposure is followed by enough pumping time, so that most of the extra precursor is evacuated from the reaction chamber to prevent excessive CVD-like reaction. As a result, very conformal coverage is achieved, especially beneficial for pinhole-free dielectric deposition.

There are two types of ALD techniques, thermal ALD and plasma-enhanced ALD (PEALD). For thermal ALD, the system is usually heated up to certain temperatures (150 °C to 600 °C) for better reaction and easier evacuation of excessive precursors during pump down. For example, the dielectric material used in this study is Al_2O_3, and the system temperature is usually set to 250 °C, so that excessive precursors, namely TMA and (especially) water, can be easily pumped away in their vapor form. The chemical reaction in this process is $2TMA + 3H_2O \rightarrow Al_2O_3 + 6CH_4$. As for PEALD, plasma is used to lower the reaction barrier for the precursors, so that the reaction temperature can be reduced, and sometimes even room temperature reaction becomes possible. For example, for the same Al_2O_3 deposition in PEALD, TMA and O_2 can be used as the precursors, and the substrate/precursor is exposed to plasma

only at the O_2 cycle, which ionizes the precursor so that it would react with the surface at a lower temperature. Moreover, O_2 is much easier to pump away than water, especially at low temperatures. However, in the case of graphene, PEALD is not a good choice, since plasma may induce defects to graphene and lower the carrier mobility. Thus when a low temperature ALD process is considered for graphene (i.e., when there is polymer on the substrate), thermal ALD is by far the only choice, and the pump down time needs to be elongated so that excessive precursors (especially water) can be removed as much as possible.

One of the disadvantages of the ALD technique is its time consumption. Typical process time for ALD is $10 \sim 60$ seconds per cycle, while the deposition rate is around $1\mathring{A}$/cycle, thus the deposition rate is below $0.1\mathring{A}$/s. This is over an order of magnitude lower than the deposition rate of other methods, and makes ALD process inefficient for thick material deposition, such as the hundreds of nm thick oxide between contact metal layers for electrical isolation. Nevertheless, it is not a big issue for gate dielectric layer deposition in modern Si-CMOS technologies, since the dielectric thickness in this case is usually below 10nm, which is translated to less than 100 cycles, and less than an hour of reaction time for each batch of wafers. Provided the compatibility with high-k dielectrics, angstrom-level thickness control and pinhole-free quality, such time consumption for ALD process is acceptable for gate dielectric deposition in current Si-CMOS technology.

Since ALD with polymer buffer layer is investigated in this study, the mechanism of Al_2O_3 ALD on polymers needs to be mentioned. Schematic of the reaction is shown in Fig. 3.2 [97]. For the first tens of cycles of reaction, the precursors seep into the gaps between polymer chains and adhere on to the surface inside the polymer layer. Uniform growth of material on the surface starts after the growth of oxide inside the polymer coalesce and the gaps are sealed. Thus more cycles of reaction are required for the same material thickness when ALD on polymers is considered.

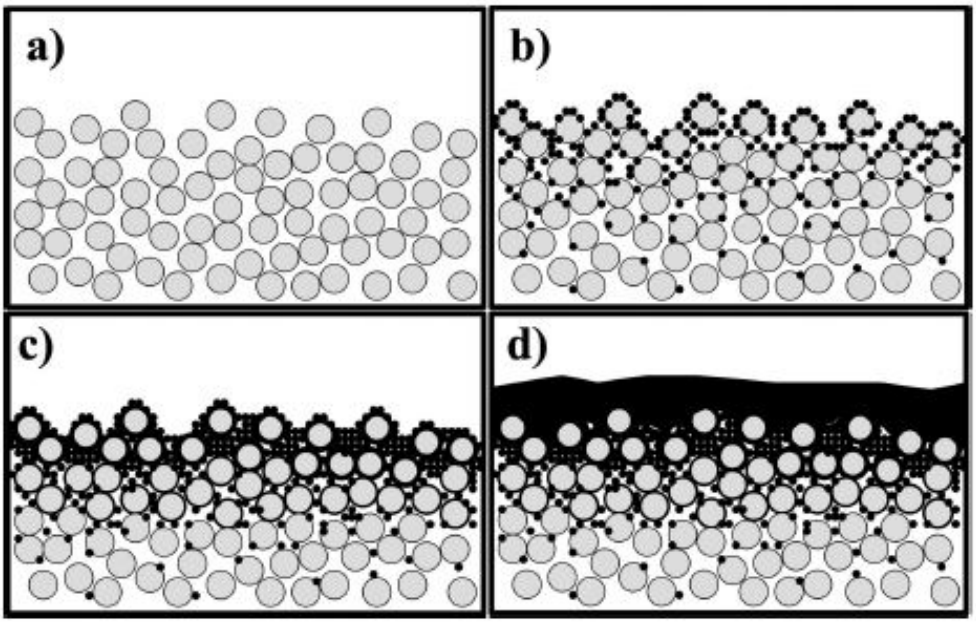

Figure 3.2: Schematic of Al_2O_3 ALD process on polymer films. (a) Cross section of polymer chains prior to the process. (b) After a few cycles, Al_2O_3 clusters nucleate around the polymer chains close to the surface. (c) Coalescence of the clusters to close the buried polymer chains. (d) Al_2O_3 starts to continuously form on the surface. This figure is taken from [29].

3.3 Al_2O_3 ALD on C-face Graphene with Polymer Buffer Layer

The first method I experimented on C-face graphene for dielectric deposition is the polymer buffer layer method of D. B. Farmer et al [26]. In principle this method does not cause damage to graphene, and the result carrier mobility exceeds 7000 cm^2/Vs on exfoliated graphene after dielectric deposition. Some changes I make from the reported method involve using Al_2O_3 instead of HfO_2 as the dielectric material for better dielectric quality, and using C-face epitaxial graphene instead of exfoliated graphene for its potential in scalable production.

3.3.1 Process Flow

After mono-layer graphene Hall bars and transistors (metal source and drain with graphene in between) are fabricated, the sample is annealed in air at 400 °C for 30

minutes to remove the PMMA residue. Then the sample is transferred into a spin-coating system for deposition of the polymer used by D. B. Farmer et al, namely NFC 1400-3CP (referred to as NFC afterwards). After a drop of the polymer in PGMEA is applied, the sample is spun at 4000 rpm for one minute before being baked on a hot plate at 180 °C for 5 minutes to evaporate the extra solvent. $\sim$ 8nm thick NFC is deposited on the sample as a result. The following step is Al_2O_3 ALD at 150 ° for 120 cycles to deposit $\sim$ 15nm thick Al_2O_3 on the polymer. E-beam lithography and e-beam evaporation of Ti/Au are used to define local top gates on the Hall bars and transistors.

3.3.2 Surface Characterization

After NFC polymer is spin-coated on multi-layer C-face epitaxial graphene on SiC, the surface topography of the sample is investigated using AFM, as shown in Fig. 3.3 (a-b). The surface is rougher than the atomically-flat pristine graphene, and the roughness is around 0.3nm after the polymer deposition, while the polymer grain size shown in Fig. 3.3 (b) is small (below 20nm). To determine the suitability of the polymer as the seed for further dielectric deposition, the sample is scanned by AFM after 200 cycle of Al_2O_3 ALD at 150 °C at the edge of a cut made by razor blade to remove part of the Al_2O_3 and NFC, as shown in Fig. 3.3 (c-d). The measured height of the bilayer is in good agreement with the estimated height of NFC and alumina, and the surface roughness of the bilayer is still within acceptable range (0.5nm).

According to the above AFM characterization of the surface, NFC polymer can be uniformed deposited on C-face graphene via spin-coating, and serves as the seed layer for uniform deposition of Al_2O_3 via ALD. The surface of the end product is relatively smooth, and meets the requirement for further top-gating.

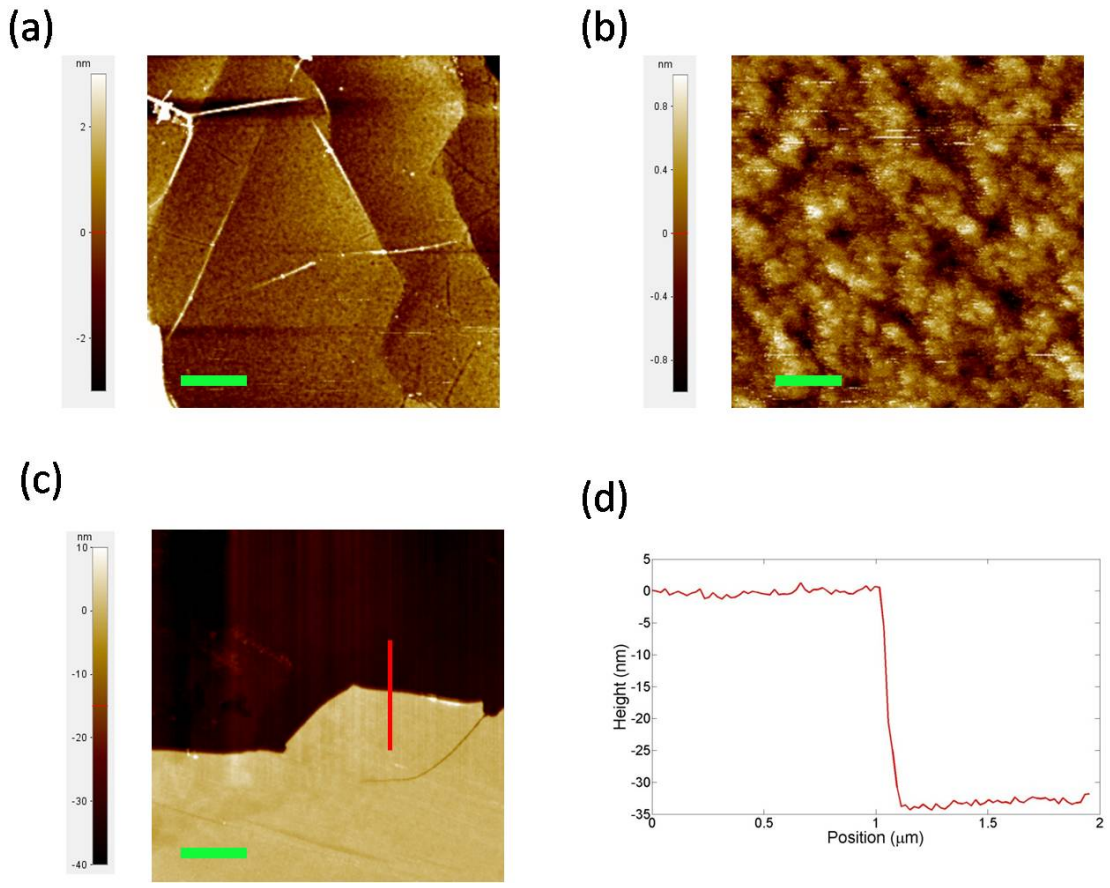

Figure 3.3: AFM images of C-face graphene spin-coated with NFC. (a) Multi-layer graphene coated with $\sim$ 10nm thick NFC, and granular texture is visible on the step terraces. Scale bar is 1μm. (b) Zoom-in scan of the sample sample on a single step terrace.. Surface roughness of the sample is 0.3nm. Scale bar is 100nm. (c) After 200 cycle Al_2O_3 ALD is applied on top of NFC, the sample is scanned at a cut (by razor blade to remove alumina and NFC), and the total height of NFC and alumina is 33nm, in good agreement with $\sim$ 22nm alumina by ALD and 10nm thick NFC. The surface roughness of the higher region is 0.5nm. Scale bar is 1μm. (d) Height profile of the red line in (c).

3.3.3 Electrical Characterization

Hall bars and FETs are fabricated with NFC buffer layer and ALD Al_2O_3 as the gate dielectric, and the gate response of the devices is characterized at room temperature in air. Optical images of as-made devices with top gates are shown in Fig. 3.4 (a-b), and the 8-terminal Hall bar is measured in this study. Two out of the eight contacts failed during the fabrication, and the rest six contacts, shown in the image, are used for the characterization. Constant current is provided to the Hall bar from C1 to B4 by a lock-in amplifier with 1V voltage at 13Hz in series with a 1MΩ resistor. Voltage drops between B1 and B2, A11 and A10 are measured for the resistivity of the Hall bar, and voltage drops between B1 and A11, B2 and A10 are measured with external magnetic fields to obtain the Hall resistance. The corresponding results with different gate voltages are shown in Fig. 3.4 (d-g). The measured carrier density at zero gate voltage is $\sim 2\times10^{12}/cm^2$ p-type from the Hall measurement with resistivity at about 1kΩ/sq, converting to a zero gate voltage Hall mobility of $\sim$ 3000 cm^2/Vs. The hysteresis of the device is 0.6V in a ±3V gate voltage range at room temperature in air. From the data, the maximum electron and hole type Hall mobilities of this device are $\sim$ 3000 and 5000 cm^2/Vs, respectively, similar to those for typical exfoliated graphene devices with top gates [26]. The gate capacitance derived from the gate-dependent Hall measurement is $C_G \sim 1.5mF/m^2$, which agrees with the estimation of the capacitance from 15nm thick Al_2O_3 + 8nm thick NFC polymer.

The gate leakage of the device is shown in Fig. 3.4 (h). The measured leakage does not affect the validity of the above measurement results, but is not negligible. This leakage could partially be attributed to the particles appearing on the surface of the sample after the air annealing at 400 °C, possibly due to migration of gold particles from the contacts on the sample surface at such temperatures (note that this problem is solved in further studies (next chapter) where platinum is deposited on top of gold for the contacts to avoid the migration of gold particles). These

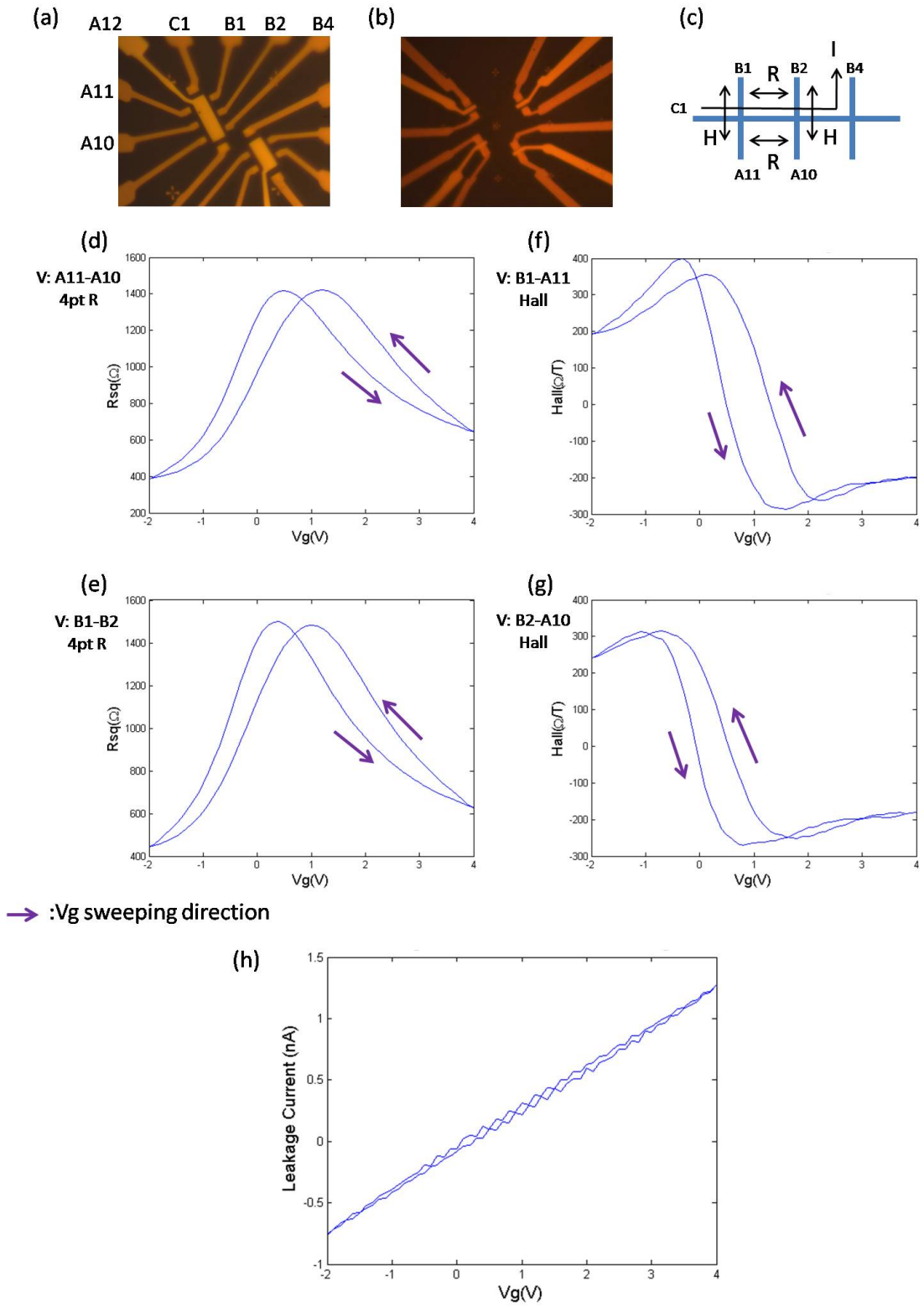

Figure 3.4: (a-b) Optical images of as-made Hall bars and FETs with the polymer buffer layer method. (c) Measurement configuration of the Hall bar. (d-e) 4-point resistivity versus gate voltage. (f-g) Hall resistance versus gate voltage. (h) Leakage current versus gate voltage. All the electrical measurements are performed at room temperature.

particles may cause inhomogeneous spin-coating of NFC polymer and the following ALD Al_2O_3, generating pinholes in the dielectric layer that induce such gate leakage.

Transport properties of 2-terminal transistors (FETs) are also characterized on the same sample. The channel width and gate length are both 3 μm for the two devices, while the source/drain separation for the two FETs are 6 and 3 μm, respectively. The 2-point resistance versus gate curves for the two devices are plotted in Fig. 3.5. FET1 is slightly p-doped, and the on-off ratio of the device is about 2, presumably due to the un-gated graphene leads at the source and drain. As for FET2, the device is heavily p-doped, and the charge neutrality is reached at $\sim$ 8V of gate voltage. The on-off ratio of this device, exceeding 18, is much higher than FET1. This is in part due to the absence of un-gated graphene regions in FET2, indicating the importance of accurate alignment for high quality transistors. But the large difference in carrier density at zero gate voltage for the two devices can not be totally explained by the un-gated region. It could possibly be attributed to (at least in part) the difference in gold particle density on graphene for the two devices, due to different distances from the center of the channel to the gold source/drain contacts.

3.4 Slow Deposition of Al for Alumina on C-face Graphene

The above polymer buffer layer approach for dielectric deposition on graphene is not compatible with self-aligned source and drain contacts, which is key to reducing access resistance of transistors in current Si-CMOS technology and III-V material-based RF devices. To combine the dielectric deposition method with self-aligning technology, the dielectric layer should be deposited after the gate region is exposed by e-beam lithography and developed. A most straight forward way to achieve this is to use high purity oxide materials, such as Al_2O_3 and SiO_2, as the evaporation source for dielectric deposition. But due to the high melting point of these oxides, the sample is heated up during the deposition through thermal radiation, and the patterned e-beam

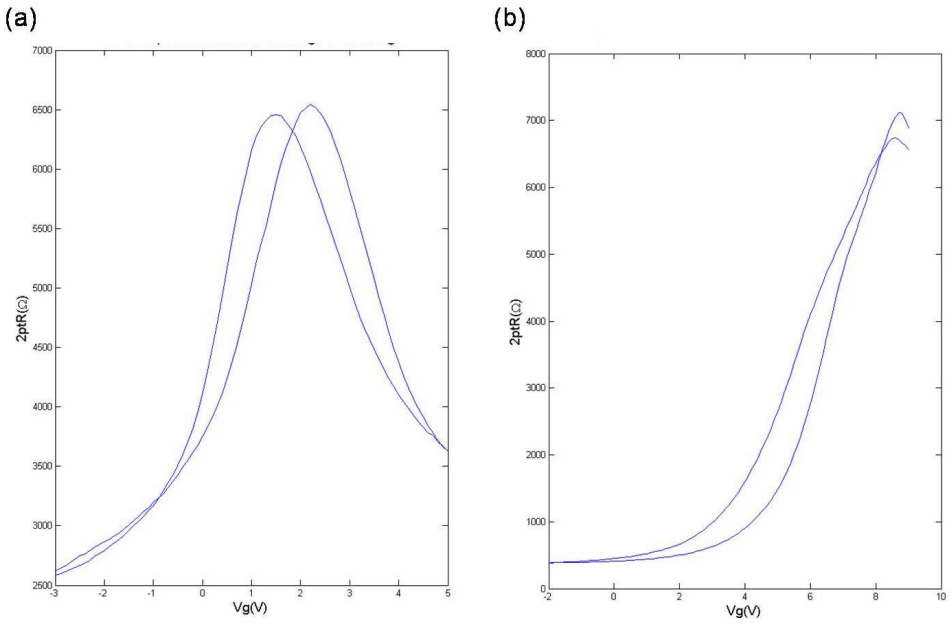

Figure 3.5: 2-point resistance versus gate voltage curves of two FETs ((a) FET1 and (b) FET2) shown in Fig. 3.4 (b). The measurement is performed at room temperature.

resist structures are partially melted. Besides, even when the oxide is deposited on a bare SiC sample, the large surface roughness (up to a few nanometers) makes this option not suitable for high quality dielectric on graphene devices. In comparison, aluminum has a low melting point (660 °C), and can be e-beam evaporated without overheating the sample surface. Moreover, when deposited at a low rate ($< 0.3\mathring{A}$/s) and under low vacuum ($\sim 1\times10^{-5}$ Torr), the end product is still optically transparent within a thickness of 30nm. This indicates that the deposited Al is oxidized during the evaporation, and could possibly serve as the dielectric layer without melting the patterned resist structures. When multi-layer resist is used for T-gate structures (details about T-gate patterning will be introduced in the next chapter), this dielectric deposition approach is compatible with self-aligned contacts.

3.4.1 Process Flow

In order to utilize self-aligned source and drain, a different fabrication process is required than in the case of polymer buffer layer. Instead of defining the gate/dielectric after source/drain contact deposition, here the gate/dielectric stack is fabricated at the beginning of the process. Starting from an as-grown C-face graphene sample with mono-layer regions and alignment marks, e-beam lithography on tri-layer PMMA resist is used to pattern T-gate structures on the mono-layer graphene (see Appendix B for more details about T-gate). After developing the pattern in MIBK/IPA, e-beam evaporation of Al is performed at a pressure of $\sim 1 \times 10^{-5}$ Torr and deposition rate of 0.2 $\mathring{A}/s$ for 20 $\sim$ 30 nm thick aluminum oxide. The relatively low vacuum in the evaporation chamber provides enough oxygen to oxidize the aluminum as it is slowly deposited on the sample surface. Then the Al source is used in the same run for depositing 60nm thick Al at 1.0 $\mathring{A}/s$ as the gate metal. After the lift-off, source/drain regions are pattern across the gate using PMMA, and 5nm/10nm Pd/Au is deposited on the sample as the contact metal. The following step is removing the extra graphene with O_2 RIE using EBL patterning, then patterning and depositing Ti/Au as the metallic probing pads.

3.4.2 Surface Characterization

AFM is used to characterize the surface topography of multi-layer C-face graphene after 2nm Al is slowly deposited on top (0.2$\mathring{A}$/s), as shown in Fig. 3.6. After the deposition, the sample surface is flatter than in the case of NFC polymer (roughness is around 0.2nm), and the grain size is below 20nm. Such surface roughness is better than that of fast-deposited Al (typically 1$\mathring{A}$/s. Uniformly deposited alumina using this method is especially suitable to be used as the top gate dielectric for devices that require uniform gate-induced doping, and the slow deposition reduces the damage to the underlying graphene layers since the Al particles arrive at the sample surface with

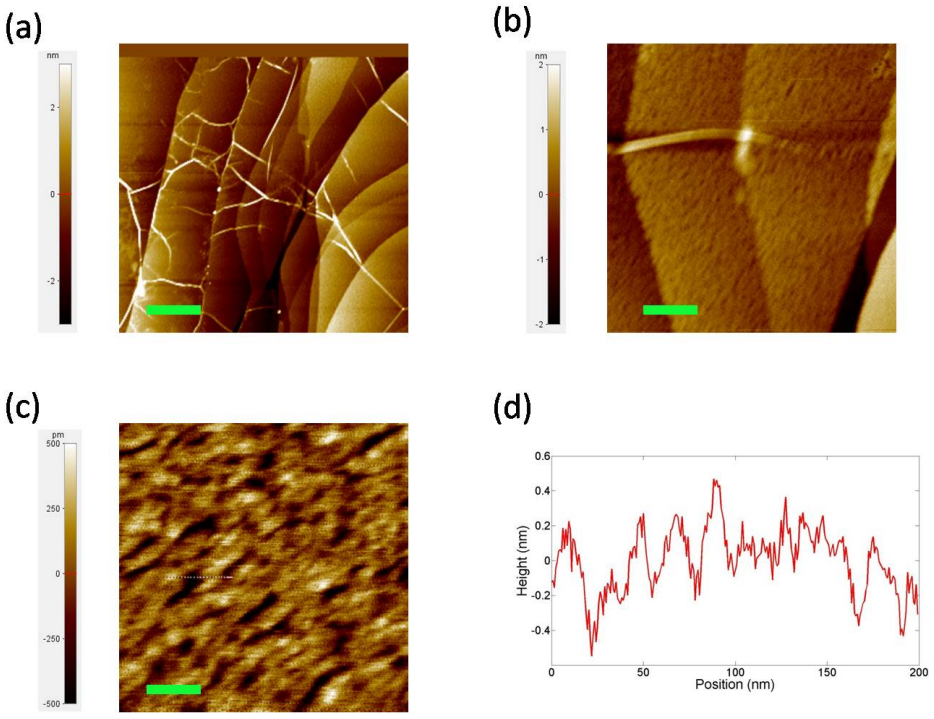

Figure 3.6: AFM images of C-face multi-layer graphene after 2nm thick Al deposition at a slow rate (0.2Å/s). (a) Relatively large area scan with no observable granular feature. Scale bar is 1μm. (b) Zoom-in scan with granular feature appearing on the graphene surface. Scale bar is 200nm. (c) An even smaller scan shows that the surface roughness of the sample after slow Al deposition is 0.2nm, and the grain size is below 20nm. Scale bar is 40nm. (d) Height profile on the sample surface in (c).

very low momentum.

3.4.3 Electrical Characterization

Gate response of top-gated mono-layer C-face graphene Hall bar using slow deposition of Al is shown in Fig. 3.7 (a-c). At zero gate voltage, the device is n-doped ($n = 1.6 \times 10^{12}/cm^2$) with a resistivity of $R_{sq} = 530\Omega/sq$. Thus the measured Hall mobility at zero gate voltage is $\mu_{Hall} = 7500cm^2/Vs$. From the gate voltage sweep, the hysteresis of the device is $\sim$ 0.3V for -2.5V to 1.5V gate voltage range. This voltage range is chosen not to induce dielectric breakdown. The gate capacitance is about $2.9mF/m^2$, in good agreement with the deposited AlO_x thickness of 30nm. The average FET mobility for electrons in this Hall bar extrapolated from conductivity versus gate voltage curve is $\mu_{FET} = 8700cm^2/Vs$, comparable with that of the best top-gated graphene devices (with scalable gate dielectric deposition method) in previous reports. The leakage current of the device does not exceed 30pA in the above gate voltage range, much smaller than that of the polymer buffer layer + ALD Al_2O_3 dielectric layer. The above result shows that with proper top gate dielectric, mono-layer C-face graphene can exhibit very high FET mobility.

To demonstrate the potential of mono-layer C-face graphene with AlO_x dielectric layer in high frequency applications, prototype dual-gate RF transistors with 150nm gate length are fabricated and characterized with a S-parameter network analyzer up to 50 GHz [41] (see Appendix A for more details about S-parameters and high frequency measurement). Typical family of current-voltage (IV) curves under different gate voltages and current gain versus frequency curve are shown in Fig. 3.7 (d-e). From the family of IV curves, the maximum measured current density in the transistor is about 1.5 mA/μm at 1V drain-source bias, and slight current saturation is observed at high drain biases. The device can not be totally turned off, due to the absence of a band gap in graphene. For the high frequency response of the device, the

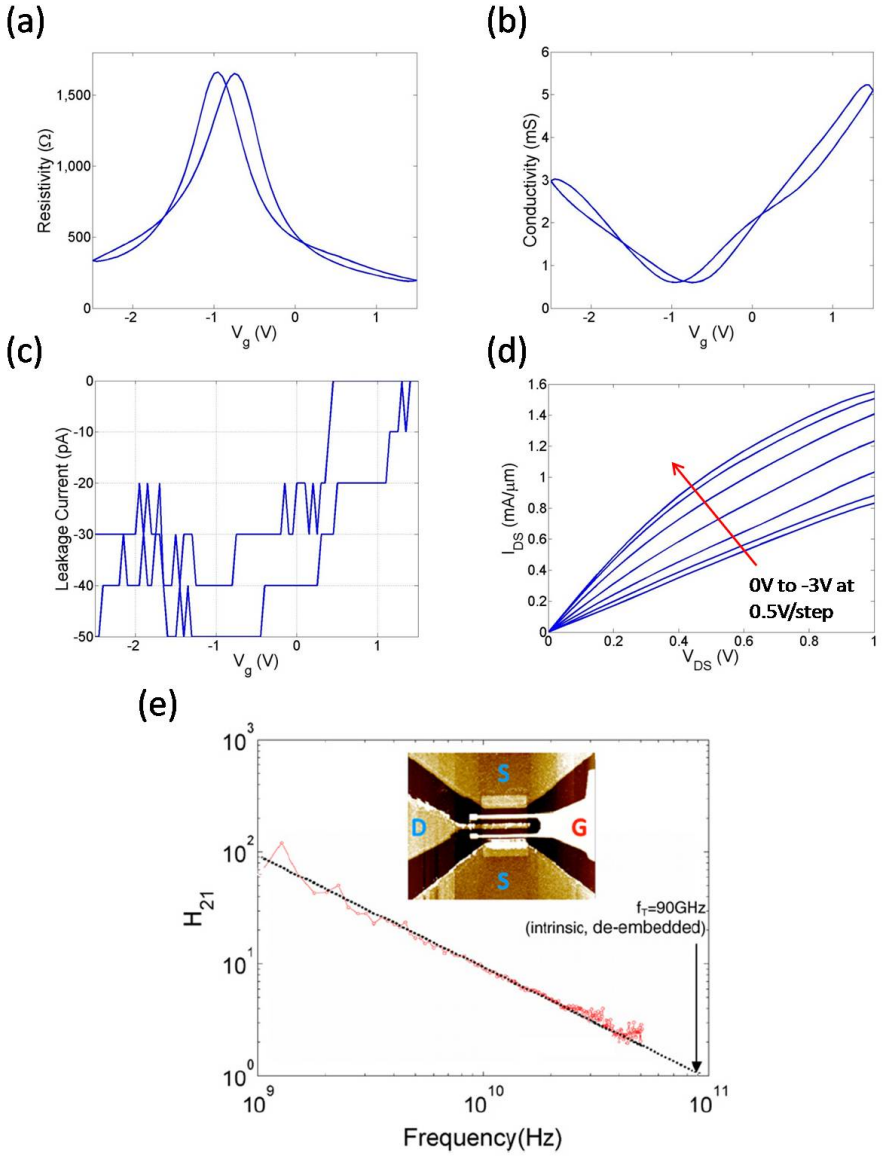

Figure 3.7: Electrical characterization of top-gated mono-layer C-face graphene using slowly deposited Al to form alumina as the dielectric layer. (a-b) Resistivity and conductivity of a Hall bar versus gate voltage. The extrapolated FET mobilities for electrons and holes of this device are $\mu_{FET} = 8700cm^2/Vs$ and $5000cm^2/Vs$, respectively. (c) Gate leakage current versus gate voltage. (d) Family of drain/source current-voltage curves at different gate voltages for an RF transistor fabricated using the same dielectric layer. Maximum on current of this device is above 1.5 mA/μm. (e) Current gain versus frequency for 150nm channel length dual-gate RF transistor shown in the inset. Cut-off frequency of this device is 90 GHz.

current gain versus frequency curve follows the 20dB/dec rule, confirming the validity of the measurement. The extrapolated cut-off frequency of this device is 90 GHz after de-embedding, better than that for Si-CMOS RF transistors at similar gate length.

However, maximum oscillation frequency of this device cannot be extracted from the Mason's unilateral gain versus frequency plot (data not shown), since the curve does not follow 20dB/dec rule. This indicates that the power gain performance of this device is far inferior compared with its current gain performance. Thus changes in the fabrication process need to be made for better high frequency power gain performance in graphene RF transistors.

3.5 Al Seed Layer + ALD on C-face Graphene

A most straightforward change from the above process for better power gain performance of the devices is a thinner dielectric layer. However, the breakdown electric field for the slowly deposited Al (AlO_x) is too small for thinner dielectric layer. To solve this problem, the slow deposition of Al is only used for seed layer, which, as in the case of thicker AlO_x, should not seriously affect the graphene carrier mobility. On top of the seed layer, ALD is used for Al_2O_3 as the bulk part of the dielectric layer for better breakdown behavior at smaller thicknesses. The strategy of depositing the dielectric/gate metal after e-beam lithography for the T-gate structure remains unchanged. In consequence, low temperature ALD process (below 100 °C) is required in order to protect the patterned resist structures

3.6 Summary

In this chapter, I introduced different dielectric deposition methods experimented on top of mono-layer epitaxial graphene on C-face SiC. First, the polymer buffer layer + ALD Al_2O_3 approach similar to that by D. B. Farmer et al was used on as-made C-face graphene samples, and acceptable mobilities were measured on the top-gated devices. To have a dielectric deposition method compatible with self-aligned source

and drain, slow deposition of Al for AlO_x as the dielectric layer was investigated, and high carrier mobility was observed along with high cut-off frequencies on prototype RF transistors. Finally, in order to improve the high frequency power gain performance of the mono-layer C-face graphene devices, a new method was proposed. It incorporates slow deposition of Al for the seed layer and ALD Al_2O_3 on top as the dielectric layer restricted to the gate region, thus it is still compatible with self-aligned source and drain. Details about this new method will be explained in the next chapter about graphene RF transistors.

CHAPTER IV

MONOLAYER C-FACE GRAPHENE RADIO FREQUENCY TRANSISTORS

4.1 Introduction

4.1.1 Summary of Previous Work

The idea of utilizing graphene in ultra-high frequency applications has been proposed since 2008 [46, 64], due to its low dimensionality, high carrier mobility and saturation velocity. The first graphene-based radio frequency (RF) transistors and measurements were demonstrated on exfoliated graphene soon afterwards [58]. For possible large-scale application of graphene RF devices, epitaxial graphene on Si-face SiC was used in RF transistors by J. S. Moon et al, and cutoff frequencies comparable with that of silicon MOSFET at similar gate lengths were achieved [68]. Y.-M. Lin et al from IBM T. J. Watson Center reported their wafer-scale epitaxial graphene RF transistors with a record cutoff frequency of 100 GHz at 240nm gate length, exceeding the performance of Si MOSFETs at similar gate lengths, and approaching the state-of-the-art III-V material-based RF devices [57].

Since then, the field of graphene RF devices has grown rapidly. To achieve higher cut-off frequencies, the major research focus was on top-gating methods for graphene transistors enabling higher carrier mobility, as well as smaller channel lengths, since the cut-off frequency of devices increases with decreasing channel length. On exfoliated graphene, L. Liao et al reported an after-deembedding cutoff frequency of 300 GHz on 140nm-channel graphene RF transistors with a nanowire gate and self-aligned source/drain contacts [56]. And recently, a record high cutoff frequency of 427 GHz was achieved on 70nm-channel exfoliated graphene transistor with transferred gate

stacks [15]. On synthesized graphene (CVD graphene, epitaxial graphene on SiC), Y. Q. Wu et al from IBM T. J. Watson Center reported cutoff frequency of 155 GHz on 40nm-channel CVD graphene transistors with diamond-like carbon as the substrate to minimize charge traps [100]. With an optimized fabrication process, the same research group improved their device performance to a cutoff frequency of 300 GHz and 350 GHz on 40nm-channel RF transistors on CVD graphene and epitaxial graphene, respectively [99]. Such result is already comparable to that of state-of-the-art III-V material RF devices.

Despite the significant current gain performance (cutoff frequency) of graphene RF devices, the power gain performance (maximum oscillation frequency f_{max}, see Appendix A) of such devices remained low compared with similar devices based on silicon and III-V materials. In the first work on epitaxial graphene RF transistors, f_{max} of 10$\sim$15 GHz were measured on 2μm channel devices [68]. In the 100 GHz graphene RF transistors by Y.-M. Lin et al, the highest measured f_{max} was 14 GHz on a 550nm channel device. The performance was improved to f_{max} of 34 and 35 GHz in the work by I. Meric et al [37] and Y. Q. Wu et al [101], respectively. And more recently, a record f_{max} of 44 GHz on CVD graphene RF transistor has been demonstrated [99]. In comparison, f_{max} above 1 THz has already been observed on InP-based high electron mobility transistors (HEMT) [50]. And the power gain performance of graphene transistors is an order of magnitude lower than that of commercially available silicon and III-V devices.

Nevertheless, there has been a lot of research effort towards utilizing graphene transistors in RF applications. In 2010, H. Wang et al demonstrated ambipolar frequency multiplier based on CVD graphene that could operate up to 1.4 GHz [93]. And in 2011, Y.-M. Lin et al succeeded in fabricating wafer-scale graphene integrated circuit (IC) that could operate up to 10 GHz as RF mixer [59]. Recently, E. Guerriero et al reported their CVD graphene-based 3-stage ring oscillator working up to 1.28

GHz, representing graphene devices with applicable voltage and power gain at high frequencies [33]. Whereas in Si-CMOS platform, 3-stage ring oscillators with tunable frequency up to 7.8 GHz, and SiGe-based transmitter and receiver chipset with RF mixers operating at 160GHz have already been demonstrated [60, 75]. In conclusion, for graphene to be comparable with existing RF platforms in practical applications, more emphasis is still required on improving the power gain performance.

4.1.2 Advantages of Monolayer C-face Epitaxial Graphene on SiC for RF Devices

In previous efforts in the literature on scalable fabrication of graphene RF transistors, the starting material was either CVD graphene or epitaxial graphene on Si-face SiC, while little attention was given to C-face epitaxial graphene. Though it is hard to control its growth, especially when it comes to monolayer, C-face epitxial graphene on SiC has several properties suitable for high frequency performance, and they are listed below.

First, the electron and hole mobilities of C-face epitaxial graphene well exceed those of CVD graphene on SiO_2 and Si-face epitaxial graphene. With proper fabrication process, C-face epitaxial graphene demonstrate a Hall mobility over 10000 cm^2/Vs without a top gate, and FET mobility of 8000 cm^2/Vs with a top gate and AlO as dielectric, as shown in the previous chapter. This is much higher than the reported carrier mobility of CVD graphene and Si-face epitaxial graphene.

Besides, SiC as the substrate is more suitable for high frequency nano-electronics than standard substrates for CVD graphene such as SiO_2/Si. Considering the ability to be further scaled down to nanoscale, the future of SiO_2 is limited due to its amorphous nature, whereas SiC still has high potential since it is mono-crystalline. Moreover, the carrier saturation velocity (the velocity of a carrier in semiconductor at which the carrier has high probability to be scattered by optical phonons) of graphene on SiO_2 is limited to $4 \times 10^7 cm/s$ by the 55$\sim$60 meV surface optical phonon energy

of SiO_2, whereas the minimum optical phonon energy of SiC is 115meV. As a result, epitaxial graphene on SiC allows faster carrier transport compared with graphene on SiO_2. For a similar reason, Y. Q. Wu et al used diamond-like-carbon as the interface layer for CVD graphene RF transistors [100].

Third, the use of monolayer graphene in this study deserves some explanation. In the case of rotationally stacked multi-layer graphene on the C-face of SiC, each layer behaves like an independent monolayer graphene except for the inter-layer charge transfer. As a result, when the multi-layer graphene is top-gated, the charge carriers on the upper layers partially screen the electric field penetrating the layers, and the gate tuning effect is weakened for the bottom graphene layers. Since high device performance requires efficient gating capability on the channel material, monolayer graphene, without the screening effect for the gate field, is chosen in this study. Note that in AB stacked multi-layer graphene such as exfoliated graphene, the layers are strongly coupled, and the gate effect is similar to that of monolayer graphene [71].

Due to the above properties, monolayer C-face epitaxial graphene is chosen in this study as the platform for RF devices for the first time [34]. Moreover, a number of fabrication techniques are utilized on this material to further enhance the performance of the devices, which will be explained in detail later.

4.1.3 Content of the Chapter

In this chapter, I will introduce the fabrication process for RF transistors on monolayer C-face epitaxial graphene. Then the DC measurement results for as-fabricated devices will be analyzed, followed by high frequency S-parameter measurement results. Finally, I will discuss the properties of C-face eptaxial graphene and the fabrication techniques leading to improved power gain performance compared with previous work.

4.2 Fabrication Process for Radio Frequency Transistors

Schematic diagram of the fabrication process flow for epitaxial graphene RF transistor is shown in Fig. 4.1. Mono-layer graphene is grown on C-face SiC, followed by spin-coating of trilayer PMMA 950K/MMA(MAA)/PMMA 50K e-beam resist and lithography to define the T-gate. After e-beam evaporation of ∼4nm seed layer alumina, the sample is transferred into the ALD chamber for low temperature deposition of 10nm Al_2O_3 as the gate dielectric. Ti/Au/Pt is e-beam evaporated to form the gate metal, and the T-gate structure with dielectric layer confined to the gate region is obtained after a lift-off step in warm acetone. In order to minimize the access resistance of the devices, Pd/Au is evaporated onto the tilted sample with e-beam lithography-defined source/drain region, thus having self-aligned metal contact under the gate head. Finally, the source/drain/gate contacts are extended to the probing pads via e-beam lithography and evaporation of Ti/Au. A few key steps of the process flow are explained in details as follows.

First, in Fig. 4.1(b), for the definition of T-gate structure, trilayer PMMA resist is used. Among them, the bottom PMMA 950K layer has the lowest sensitivity to e-beam, and the highest dose of ∼900 $\mu C/cm^2$ is required to expose this layer that defines the gate foot (down to 50nm long). The top PMMA 50K layer has a higher sensitivity to e-beam, and a lower dose of 600 $\mu C/cm^2$ is enough to expose this layer. Therefore the size of the gate head can be defined independent of the gate foot. The middle layer of MMA(MAA) has the highest sensitivity among all three layers, and is used to provide an undercut for a better lift-off. For the T-gate resist structure to remain intact throughout the following ALD process, low temperature in the ALD chamber is required to prevent the resist from flowing [7]. Here 70 °C is chosen for both the resist structure integrity and prevention of excessive adhesion between the bottom layer of PMMA and graphene. In the meantime, I use a long purge time of 60s for the H_2O cycle and 35s for the TMA cycle to accommodate the low temperature

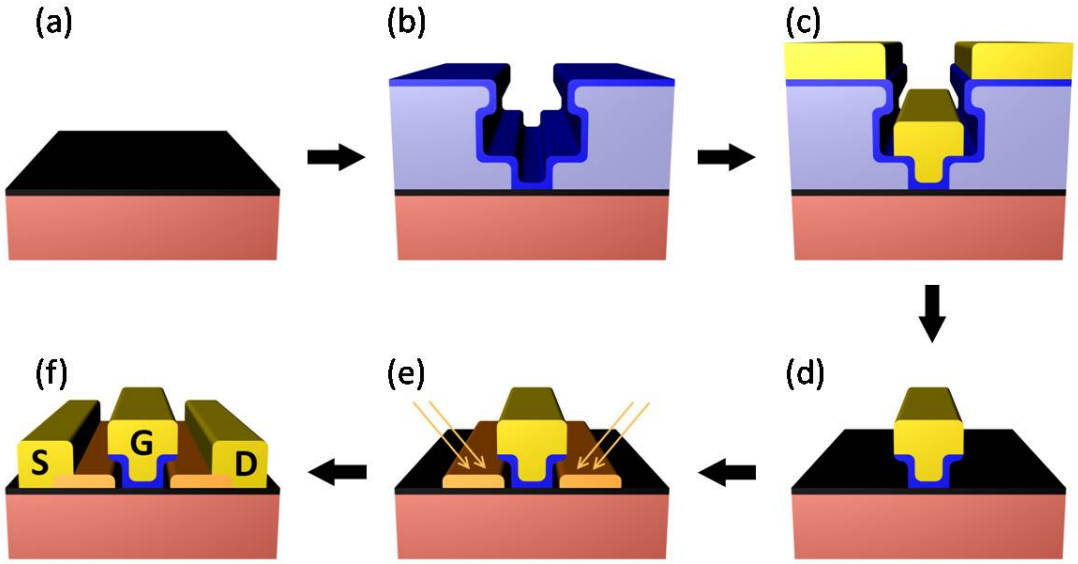

Figure 4.1: Fabrication process flow for C-face epitaxial graphene RF transistors. (a) Monolayer graphene on C-face of SiC. (b) The T-gate is patterned using tri-layer resist and e-beam lithography, followed by aluminum seed layer deposition and ALD of Al_2O_3. (c) Ti/Au/Pt is deposited on top as the gate metal. (d) After lift-off, the T-gate stands on graphene. Note the sides of the T-gate are coated by an insulating layer. (e) Angle deposition of Pd/Au to form self-aligned contacts. (f) Ti/Au source and drain are deposited on top of the self-aligned contacts as probing pads.

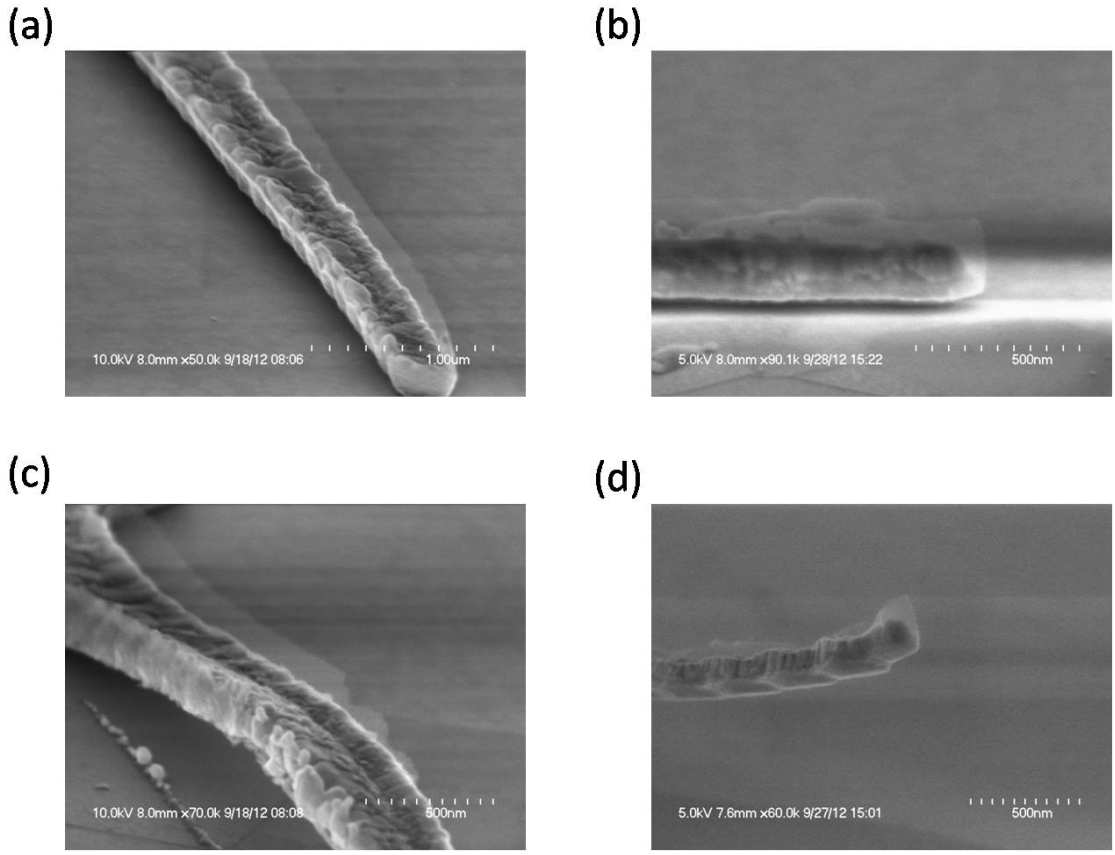

Figure 4.2: SEM images of failed T-gate structures fabricated without the BCl_3 RIE process. (a) T-gate with thin Al_2O_3 attached to the edges. (b) Side view of the attached Al_2O_3 to the gate. (c) T-gate structure is partially detached from the substrate due to the pull by the Al_2O_3 at the edges in the lift-off process. (d) Zoom-in scan of bent gate structure away from the substrate (not shown).

ALD process.

Second, in Fig. 4.1(c), due to the conformal coverage of Al_2O_3 in the ALD process, the oxide layer on sidewalls of top and middle resist layers could pull the gate strutures away from the sample during lift-off, especially for small gate foot with weaker adhesion to graphene. To solve this problem, an extra etching step is required after the deposition of gate metal to remove the Al_2O_3 on the sidewall of the resist layers. Due to the anisotropic nature of the etching, the sample is positioned on a tilted stage in the RIE chamber with BCl_3 as the etchant so that the resist sidewalls are exposed to the plasma. Note that two RIE steps are required to remove the sidewall Al_2O_3 on

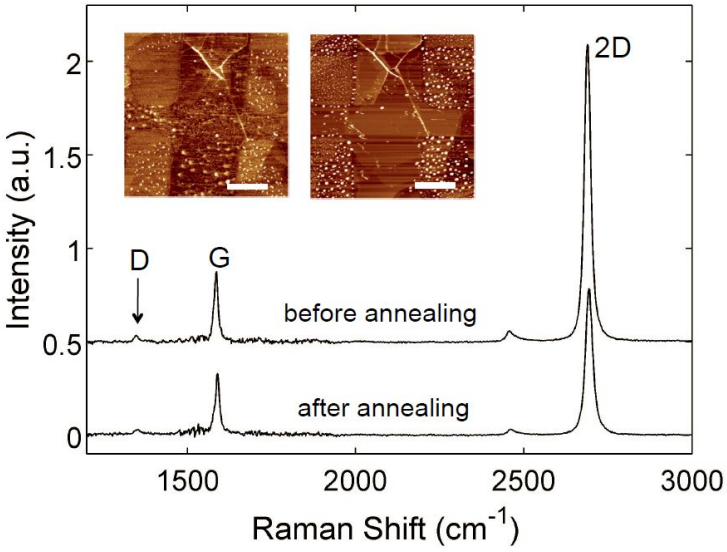

Figure 4.3: Raman spectra of mono-layer C-face graphene before and after air annealing at 400 °C for 30 minutes. Inset: AFM images of a Hall bar cross before (left) and after (right) air annealing. Note that the particles on the cross in the left image are absent in the right image. Scale bar is 1μm.

the two sides of T-gate. The already deposited gate metal protects the underneath dielectric layer. With this extra step, RF transistors with 50nm gate length can be fabricated, whereas all 50nm T-gates (6 out of 6) are detached from the substrate on one sample when the Al_2O_3 on resist sidewalls is not removed. Examples of Al_2O_3 on the T-gate edges and T-gates detached from the substrate are demonstrated in Fig. 4.2.

Another step that deserves more explanation is the angle deposition of the self-aligned source and drain metal contacts. For better metal/graphene contact, it is preferable to deposit metals on graphene with minimal surface contamination. To this end, the sample is annealed in air up to 400 °C after T-gate fabrication to remove the resist residue on graphene. This air annealing step does not induce damage to graphene, especially as the top Pt layer of the gates prevents possible migration of gold particles during the annealing. In Fig. 4.3, it is clear that after the annealing, the D-peak intensity in the Raman spectrum of graphene does not increase, and

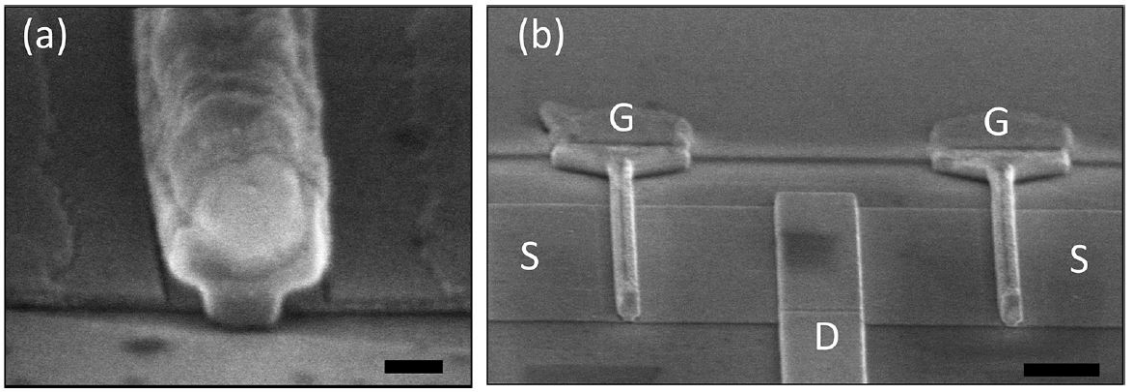

Figure 4.4: SEM images of as-fabricated RF transistors. (a) Zoom-in image of the T-gate with 100nm gate foot and metal source/drain self-aligned to its gate foot . Scale bar is 100nm. (b) The whole dual-gate transistor with its two sources/gates and one common drain noted. Scale bar is 2μm.

residue-induced graphene surface roughness is absent on the AFM image. In the following step for self-aligned source/drain contact deposition, the sample is tilted by 45 ° relative to the deposition direction of the metal sources, and the distance between the contact and the gate foot is determined by the geometry of the gate. Since the gate foot height is about the same as the bottom PMMA 950K resist layer in the T-gate lithography step (70nm), the gate head is designed to be ∼80nm beyond the edge of gate foot on each side, so that there is only ∼10nm exposed graphene under the gate head. For the choice of contact metal, Pd has a high work function $> 5.1eV$ (the work function of charge-neutral graphene is around 4.6eV), and provides good adhesion with graphene. As a result, the graphene under source/drain contacts is strongly p-doped [102], and a low sheet resistance is obtained for a small overall contact resistance per channel width. Note that angle deposition would result in metal on the sidewalls of the resist layer that defines the overall source/drain regions, and causes lift-off failure. To prevent this, the thickness of the self-aligned contacts is limited to 4nm Pd/8nm Au on each side of the gate. When thicker metal contacts are required for lower contact metal resistance, an extra non-tilted deposition step with arbitrary metal thickness can be added prior to angle deposition.

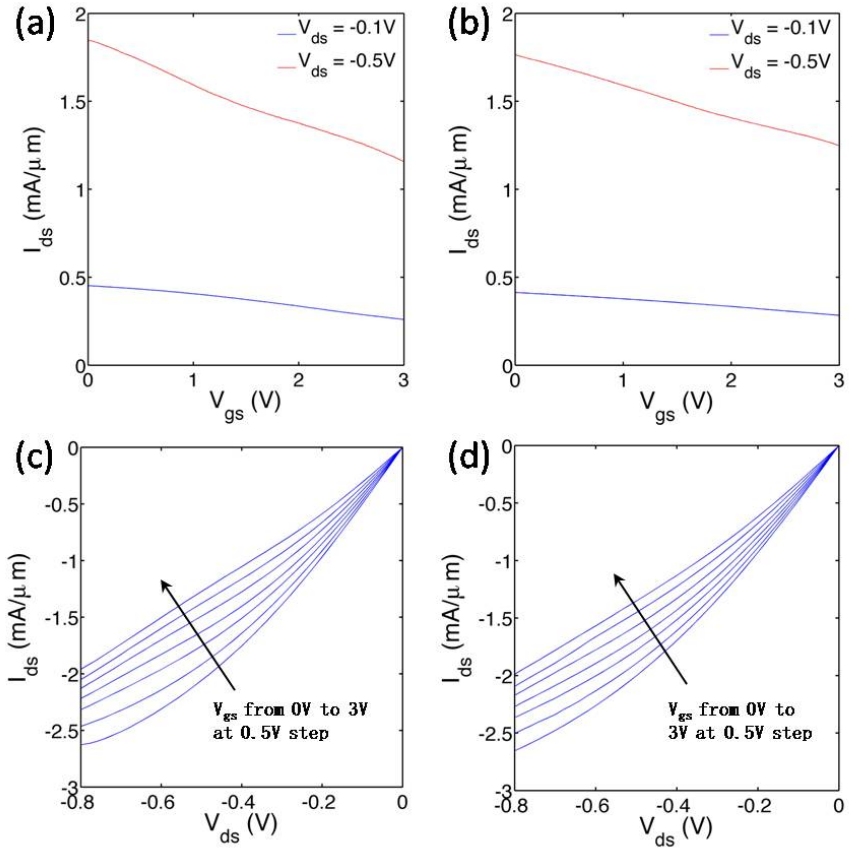

Figure 4.5: DC characteristics of GFETs on C-face graphene with 100 nm and 250 nm gate lengths. (a)-(b) Current density plotted as a function of gate voltage at Vds = -0.1V and -0.5V for gate length (a) 100nm and (b) 250nm. (c)-(d) Drain-source IV characteristics at gate voltage ranging from 0V to 3V at 0.5V step on (c) 100nm and (d) 250nm gate devices. Maximum current density of $\sim$ 2.6mA/μm is observed.

After the fabrication process as described above, RF transistors shown in Fig. 4.4 can be measured on a probe station for DC characteristics and high frequency performance with an S-parameter network analyzer.

4.3 Electrical Characterization of C-face Graphene Transistors

4.3.1 DC Characteristics

DC measurement of graphene RF transistors is performed on a probe station with Keithley 2400 broad purpose sourcemeters for drain/gate voltage supply and drain

current/gate leakage measurement. Drain current versus gate voltage characteristics at different drain biases for two different gate lengths are plotted in Fig. 4.5(a-b). The graphene channel of all the measured devices is strongly p-doped, and positive gate voltage up to 3V cannot tune the channel to charge neutrality. Drain/source IV curves at different gate voltages are shown in Fig. 4.5(c-d). The current density of both 100nm and 250nm devices at -0.8V drain bias changes from $\sim$2.6 mA/μm at zero gate bias to $\sim$2 mA/μm at 3V gate bias, a current density change of 30%. At a drain bias $>$ 0.5V, there is some indication of current saturation, due to either carrier velocity saturation or device self-heating effect. Current saturation similar to that on silicon MOS transistors is absent in graphene transistors without a band-gap, and voltage gain much larger than 1 cannot be observed in measured devices when the channel length is below 300nm.

Nevertheless, high on-current of 2.6 mA/μm and maximum transconductance of 0.25 mS/μm are beneficial for high frequency performance of the devices. Moreover, the minimum 2 point resistance per channel width of the devices is about 200 $\Omega\mu$m, indicating that the contact resistance is below 100 $\Omega\mu$m (2 point resistance is the sum of source and drain access resistance and the channel resistance), and is among the smallest contact resistance ever observed on graphene devices [66]. Smaller contact resistance provides larger transconductance for a given channel property, thus better high frequency current gain performances. More importantly, smaller contact resistance generates less power dissipation on the contacts, and enables better high frequency power gain performances.

4.3.2 RF Characteristics

The RF performance of C-face epitaxial graphene transistors is characterized in an S-parameter network analyzer up to 50GHz in Dr. John D. Cressler's lab at School

of Electrical and Computer Engineering, Georgia Institute of Technology. The measurement is performed at ambient condition using standard ground-signal-ground (GSG) probes with 100 μm pitch. The system is calibrated with the short-open-load-through (SOLT) process on a standard calibration die before measuring the devices under test (DUT), to eliminate the parasitic effects of the wiring and probes. To further remove the parasitic effects of the probing pads and connections to the source, drain and gate of the device for extrapolation of intrinsic high frequency properties of graphene, de-embedding process similar to Ref. [100] is applied. Namely, the "open" and "short" structures have the same layout as the graphene DUT, except that there is no graphene as the channel in the "open" structure, and all the contacts are shorted to each other in the "short" structure.

Here, graphene transistors with two different gate lengths (250nm and 100nm) are characterized, and the high frequency current gain performance ($|H_{21}|$ versus frequency) is demonstrated in Fig. 4.6 (a-b). Before de-embedding, a maximum f_T of 41 GHz is observed on a device with 100nm gate length at V_g = 3.5 V and V_{ds} = -0.5 V. Such cutoff frequency is comparable to the highest non de-embedded cutoff frequency reported to date on graphene RF transistors [55]. On 250nm devices, a cutoff frequency before de-embedding of 32 GHz was measured, showing the reproducibility of the non de-embedded current gain performance of the devices. After de-embedding, cutoff frequencies of 110 GHz and 60 GHz were measured on 100 nm and 250 nm gate length devices, respectively. These measured f_T values agree well with the estimated $f_T = g_m/2\pi C_g \sim$ 80-110 GHz using the measured g_m = 0.25 mS/μm for the 100nm long and 7μm wide dual gate device, and 15nm thick dielectric with dielectric constant $\kappa = 6\sim8$ for ALD Al_2O_3. Further measurements on 50nm gate devices show an after de-embedding cutoff frequency f_T = 205 GHz (see Fig. 4.6 (c)). The above results on devices with different gate lengths approximately follow the law $f_T \propto 1/L_g$ with L_g being the gate length, as shown in Fig. 4.6 (d). They are higher than those

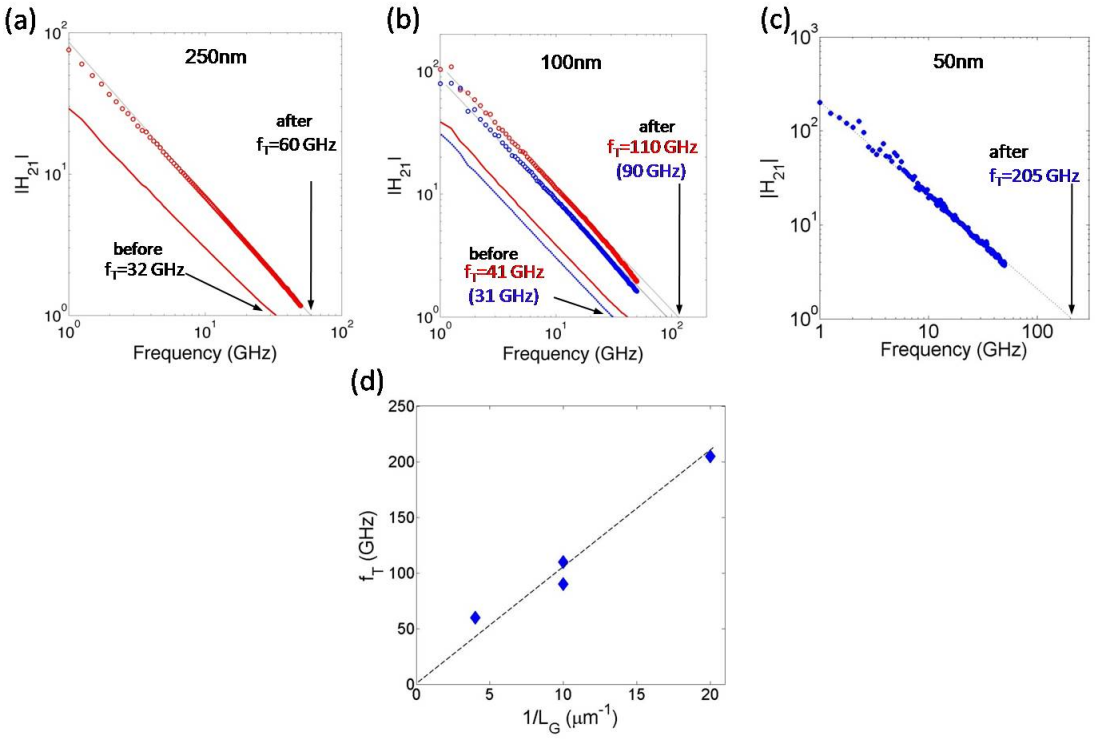

Figure 4.6: High frequency current gain characteristics of GFETs on C-face graphene with different gate lengths. (a) $|H_{21}|$ for a 250nm gate length GFET before (solid line; f_T= 32 GHz) and after (circles, by extrapolation of theoretical slope of 20 dB/decade to$|H_{21}| = 1$, $f_T = 60$ GHz) de-embedding. (b) H_{21} versus frequency on two devices with 100 nm gate length; device 1 (red) before de-embedding (solid red line) and after de-embedding (red circles); device 2 (blue, ibidem). Cutoff frequencies for device 1 and 2 are before de-embedding f_T= 41 GHz (31 GHz), resp, and after de-embedding $f_T = 110$ GHz (90 GHz), resp. (c) $|H_{21}|$ for a 50nm gate length GFET after de-embedding shows a cutoff frequency $f_T = 205$ GHz. (d) Cutoff frequencies of devices plotted versus inverse of gate lengths. The curve approximately follows $f_T \propto 1/L_g$.

for silicon MOSFETs with similar gate lengths, while being half as much as those for the best III-V material based HEMTs with similar gate lengths.

For applications of RF transistors in circuits such as low noise amplifiers (LNA) and power amplifiers (PA), a more relevant figure of merit is the maximum oscillation frequency f_{max}. Mason's unilateral gain (MUG or U in the figure) versus frequency curves for 100nm and 250nm gate devices are plotted in Fig. 4.7, and maximum oscillation frequencies are extrapolated. Before de-embedding, f_{max} = 38 GHz and 33 GHz on two 100nm gate devices, and f_{max} = 36 GHz on a 250nm gate device are observed. Note that the cutoff frequencies and maximum oscillation frequencies are obtained on the same set of devices. After the de-embedding process, these devices show f_{max} = 70 GHz and 58 GHz for the 100nm and 250nm gate devices, respectively, and the 20 dB/dec law for MUG - frequency relation is obeyed. To my best knowledge, the above f_{max} on 100nm gate devices is the highest reported up to date for graphene RF transistors with any graphene production method on any substrates [15, 99]. Furthermore, all of the six measured 100nm devices show f_{max} between 50 and 70 GHz after de-embedding, indicating the reproducibility of power gain performance on the C-face epitaxial graphene RF transistors. Altogether the above results show that C-face SiC is a promising substrate for high frequency graphene devices.

4.4 Discussion on Electrical Characteristics

In prior reports on graphene RF transistors, the measured maximum oscillation frequencies were not only much lower than the cutoff frequencies on the same devices, but also lower than the f_{max} of silicon CMOS with similar gate lengths. Such inferior power gain performance was attributed to large gate resistance, large contact resistance and non-optimized device designs. By contrast, the RF transistors presented here and based on C-face graphene show comparable (high) f_T and f_{max}, which represents an optimal situation for applications in RF circuits. Here, the record high

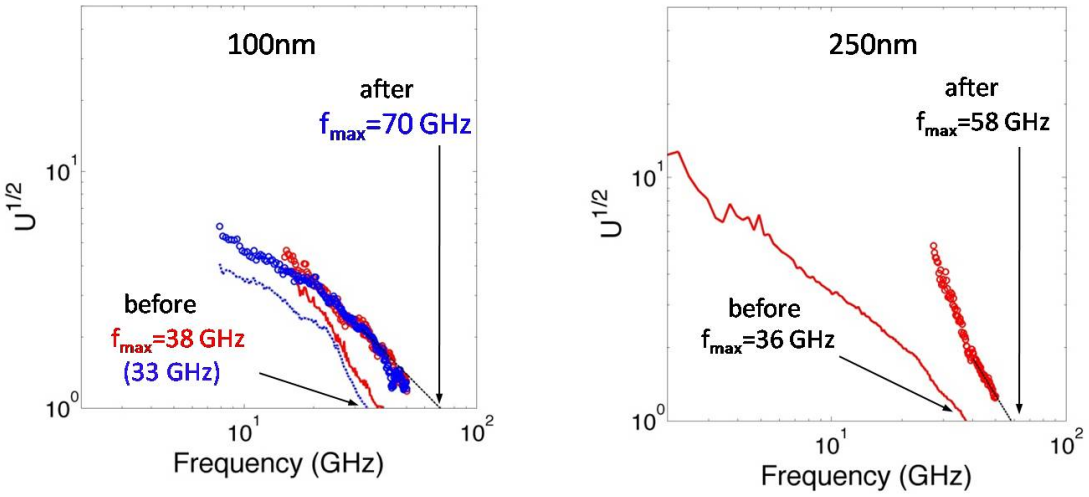

Figure 4.7: Masons unilateral gain versus frequency for the two 100 nm gate GFETs shown in Fig. 4.6. Intercepts $U^{1/2}$ =1 (slope 20 dB/dec) give f_{max} =38 GHz and 33 GHz before and 70 GHz after de-embedding. (d) Same as (c) for the 250nm gate length GFET in (b) fmax=36 GHz and 58 GHz before and after de-embedding.

frequency power gain performance on the graphene transistors should be attributed to not only a proper choice of substrate and channel material, but also application of suitable process flow for the device fabrication. To be specific, the reproducible high f_{max} results from the T-gate design, self-alignment technique, and small contact resistances in the devices. The relation between f_T and f_{max} is [48]

$$f_{max} = \frac{f_T}{2\sqrt{2g_D(R_G + R_{SD}) + 2\pi f_T R_G C_G}}, \tag{4.1}$$

where g_D is the drain-source differential conductance, R_G is the gate resistance, R_{SD} is the sum of drain and source access resistances, and C_G is the gate capacitance. From this equation, it is obvious that to get a larger f_{max} at a given gate length and dielectric thickness, we need a larger cutoff frequency, smaller drain-source differential conductance and lower drain source access resistances. Relating this equation to C-face epitaxial graphene RF transistors, the T-gate design is aiming for lower gate resistance, and the self-alignment technique, along with the small contact resistance, contribute to lower access resistance. These aspects will be discussed in detail below.

T-gates are widely used in high frequency devices such as HEMTs for smaller

gate resistance. In this case, the gate heads of the graphene transistors mentioned above are 160nm larger than the gate foot length and are $\sim$ 150nm thick, resulting in gate resistance of $\sim 1\Omega/\mu m$ per channel width that is approximately independant of channel length. Such low gate resistance is about an order of magnitude lower than that for ordinary metal gates, and over two orders of magnitude lower than highly doped nanowire gates [56].

The superior power gain performance of the devices here can also be attributed in part to the self-alignment technique. Note that self-alignment was applied in previous reports on graphene RF transistors [15, 56, 2], where the gate was used as part of the mask for perpendicular e-beam evaporation of contact metal to isolate the source and drain. With such method, the length of exposed graphene is defined by the difference between the size of the gate head and channel length (gate foot), which is 100 $\sim$ 200 nm in general. In this work, e-beam evaporation of contact metal with tilted samples is chosen to further reduce the exposed graphene region. By careful design of the size of gate head and foot, along with consideration of the sample tilting angle during deposition, the total exposed graphene length on the source and drain sides can be reduced to $\lesssim$ 20nm. This value is mainly limited by the accuracy of e-beam lithography and lift-off process in defining the size of the gate head and edge roughness. Considering that the exposed graphene resistivity should be about a few hundred Ω, this angle deposition of self-aligned source and drain contacts could reduce the access resistance per unit channel width by several tens of $\Omega\mu$m compared with perpendicular deposition. Along with a low contact resistance, the above reduction can be a significant proportion of the total access resistance, and may result in appreciable improvement in the power gain performance, especially at the absence of pinch-off and current saturation (large g_D).

In previous reports, another way to reduce the access resistance of the devices was an accurate alignment of source and drain contacts with respect of the gate or even

overlapping the gate with source and drain [100]. This was achieved at the price of increased parasitic capacitance in the devices due to the partial overlapping of gate and contacts with high-k dielectric in between. In comparison, the angle deposition of contacts with T-gates used here does not significantly add to the parasitic capacitance of the devices. Considering the 70nm high gate foot, 10nm thick contact metal layer, and the air gap between the gate head and the contacts, the angle deposition induces an extra parasitic capacitance no more than 10% of the device gate capacitance, even in 50nm gate devices. Such increase in parasitic capacitance is negligible compared with that in the overlapped source and drain design which is limited by the alignment accuracy, and is tolerable considering the significant reduction of access resistance. With a reasonable yield, the angle deposition technique improves the access resistance of the devices with minimal sacrifice in other aspects, and is one of the key reasons for the record power gain performance demonstrated above.

Contact resistance R_C is another limiting factor for the high frequency performance of the devices. In previous reports on graphene RF transistors, the contact resistance per channel width ranges from 300 $\Omega\mu m$ to several k$\Omega\mu$m [79], which is about an order of magnitude higher than that for the best Si CMOS and III-V HEMTs. While the effect of contact resistance on f_T has been extensively discussed in the context of graphene, its effect on f_{max} was rarely mentioned, even though a large R_C degrades f_{max} more than f_T. With large R_C and small channel resistance, most input RF power to the devices is dissipated by the contacts rather than the channel. Furthermore, the absence of current saturation exacerbates the effect, since without a band gap, there is no mechanism in graphene to make the differential channel resistance to be much larger than the contact resistance. On the contrary for f_T, the presence of large contact resistance can be compensated by increased drain-source bias, and a high transconductance could still be achieved.

The small contact resistance between Pd/Au and C-face epitaxial graphene is the

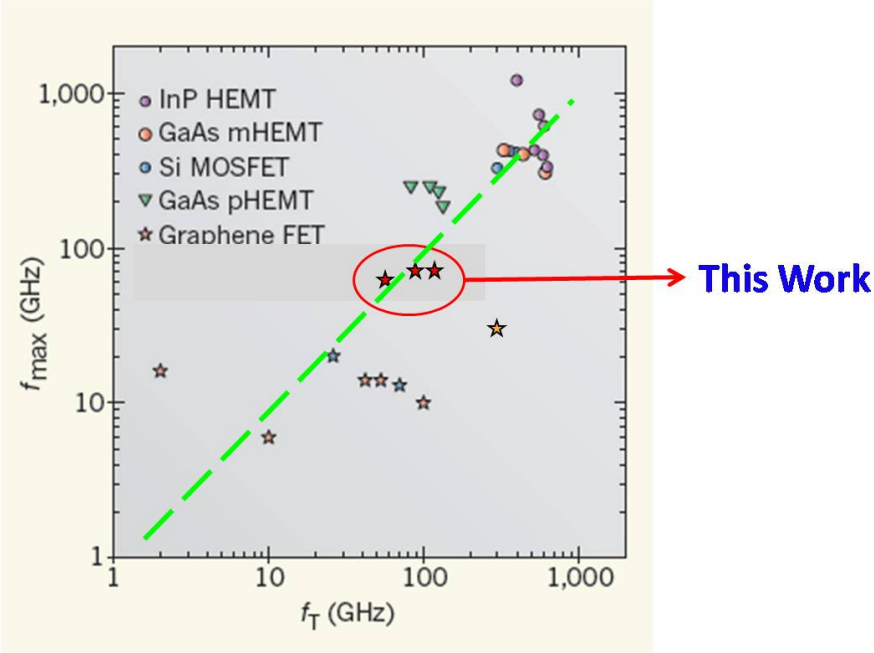

Figure 4.8: Comparison of the f_T and f_{max} of C-face epitaxial graphene RF transistors with previous reports [79].

key to record high f_{max} (with and without de-embedding). Since R_C <100 $\Omega\mu$m, most of the input RF power is amplified in the channel at the optimal operation point of the device. From Equation 4.1, f_{max} of the 100nm device can be estimated from devices parameters obtained from fabrication process and DC measurements. Namely, with the dual gate design, 7μm channel width and 15nm thick Al_2O_3 as the dielectric, the parameters are: channel conductance $g_D \approx 30mS$, source drain access resistance $R_{SD} \approx 15\Omega$ (due to the self-alignment of source and drain contacts, the access resistance of the devices comprises of primarily contact resistance), the gate resistance $R_G \approx 3\Omega$, and the gate capacitance $C_G \approx 5fF$. With the above parameters, the maximum oscillation frequency is estimated to be $f_{max} \approx 74$ GHz for the 100nm device, in good agreement with the measured result $f_{max} = 70$ GHz.

4.5 Summary

In this chapter, I have demonstrated a new fabrication process for graphene RF transistors based on mono-layer epitaxial graphene on C-face SiC. With T-gate design and self-alignment technique to minimize gate and access resistance, high cutoff frequency f_T = 41 and 110 GHz and record maximum oscillation frequency f_{max} = 38 and 70 GHz, before and after de-embedding, are achieved on devices at 100nm gate length. Reproducible results of comparably high f_T and f_{max} are obtained on multiple devices, which are desirable for possible applications in functional circuits. Comparing the above results with corresponding figures of merit in previous reports on RF transistors in graphene and other materials [79], as shown in Fig. 4.8, it is indicated that the improvement made in this study is on the right trend. It opens a pathway toward better power gain performance in graphene RF devices, and shows the potential of C-face epitaxial graphene in future high frequency applications.

CHAPTER V

WAFER BONDING SOLUTION TO EPITAXIAL GRAPHENE SILICON INTEGRATION

5.1 Introduction

5.1.1 Background

With its unique properties such as two dimensionality, high carrier mobility and large carrier saturation velocity, graphene is proposed as a candidate for future high frequency applications, as discussed about in the previous chapter. Furthermore, with its carriers behaving like Dirac particles and exhibiting ballistic transport at room temperature in nanoribbons [3], graphene also has strong potential as a platform for novel device concepts. However, the incompatibility of band gap and high mobility in this material up till now greatly limits its application in digital technology. As a result, a viable approach to combine graphene with existing platforms for logic circuits is required for possible electronic application of graphene in the near future. Since by far the most successful platform for digital electronics is Si-CMOS, the development of graphene electronics relies greatly on the success of integrating graphene devices with Si-CMOS technology.

Starting from the first report about electrical measurements of few layer graphene exfoliated onto SiO_2/Si wafers [71], most efforts towards combining graphene devices with crystalline Si lie upon transferring graphene to Si wafers, and lithographic methods to define the graphene devices. Meanwhile, researchers are faced with numerous obstacles trying to optimize this approach. On the one side, the widely used technique for graphene transfer of scotch tape exfoliation is not scalable or reproducible [79]. As CVD graphene was introduced, a wet transfer method was proposed to remove the

growth substrate (usually copper), and apply the as-grown graphene film to various substrates. Ions and polymer are inevitably involved in this approach, leaving the end product with impurities and charge puddles. On the other side in the lithography process, the edges of the defined structures are not smooth at the nanometer scale, which induces scattering, Coulomb blockade, and Anderson localization to the carriers in graphene. The lithography-induced rough edges in graphene nano-structures prohibit the realization of graphene nano-electronics, and is the primary reason for the incompatibility between sizable band gap and high carrier mobility in graphene nano-ribbons [36]. With these obstacles, there is no clear path towards integrated system of graphene and Si-CMOS that could utilize the key advantages of both platforms via graphene transfer technology.

On the contrary, epitaxial graphene is grown on a SiC, a semi-insulating crystalline substrate ideal for nano-electronics, thus there is no need for a transfer process. Besides, recent progress of selective growth for graphene on the sidewalls of Si-face SiC provides graphene nano-structures having novel properties without post-growth lithography [82, 3]. It provides an ideal platform for novel device concepts, whose potential would be better realized if combined with state-of-the-art Si-CMOS technology. However, the high temperature required for graphene growth ($> 1400°C$) is not compatible with Si-CMOS processes. As a result, a post-graphene-growth integration solution is required for epitaxial graphene/SiC and Si-CMOS platforms.

Here, I show in principle that by using the Silicon-on-Insulator (SOI) technology [51, 63, 10], a thin mono-crystalline silicon layer ready for CMOS fabrication can be applied on top of epitaxial graphene on SiC. This approach provides a new graphene-to-Si integration strategy, in which the two platforms are bonded together into a double layer structure and interconnected by metal vias. This method, inspired by the industrial development of 3-D hyper-integration stacking thin-film electronic devices [87, 61], preserves the properties of epitaxial graphene and enables the full

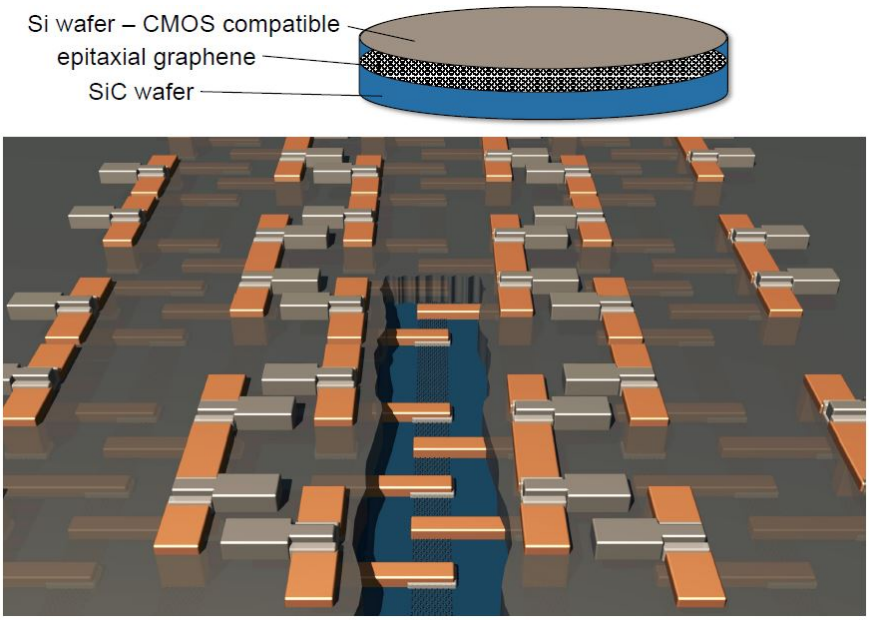

Figure 5.1: Schematic structure of EG on SiC/Si-CMOS hybrid system. The top layer is the thin crystalline Si transferred onto graphene/SiC based on which MOSFETs are fabricated. And the bottom layer is the EG/SiC platform with graphene devices. The two platforms are electrically interconnected by metal vias.

spectrum of CMOS processing.

5.1.2 Advantages of EG/Si system

Schematic of the integrated hybrid system is shown in Fig. 5.1 [23]. Si-CMOS transistors are on the top layer, and graphene devices with metal leads are underneath. The two platforms are isolated by oxide layers in between, and are electrically connected by metal vias through the Si/oxide layers. Such EG/Si system has several advantages compared with most graphene/Si integration schemes in previous literatures [27, 1, 67]. First, in most reported graphene/Si integration methods, graphene and Si devices are implicitly designed side by side, while in the EG/Si system, devices on the Si platform can be positioned on top of graphene devices (thanks to the inter-platform isolation layers), thus a similar functional die consumes a less portion of a wafer. Second, the implementation of mono-crystalline Si layer onto EG/SiC could, in principle, be performed at wafer scale, whereas large scale ion-free transfer

of graphene onto Si wafer is not yet available, and other methods to grow Si on top of graphene, such as chemical vapor deposition or molecular beam epitaxy (MBE), can not provide a Si layer with equally high quality. Third, thanks to the adoption of ALD Al_2O_3 on EG/SiC, the as-grown graphene nano-structures are kept intact during the transfer process, thus their unique properties could be maintained. And finally, the whole transfer process stems from the well developed SOI technology, process transfer from which would facilitate future optimization and yield improvement

.

There has been concerns about epitaxial graphene on SiC that the price of SiC would hinder the commercialization of the technology. However, as high-end electronics is the target for EG/Si system, the \$20/cm^2 cost for SiC takes only a few percent of the price for the end product, which is in the acceptable range especially when electronics under extreme conditions is under consideration.

5.1.3 Content of the Chapter

In this chapter, I will first explain the fabrication process for EG/Si integration. Then characterization of the end product will be covered, and efforts on integrating sidewall graphene nano-structures with Si will be introduced. Electrical characterization of graphene devices after the integration process will be discussed afterwards, followed by discussions on future prospectives of the technology.

5.2 Fabrication Process for Epitaxial Graphene-Si Integration

5.2.1 Process Flow

The whole fabrication process flow is demonstrated in Fig. 5.2. The starting materials are p-doped Si ($10^{15}/cm^3$) and semi-insulating 4H-SiC samples (both are 3.5mm $\times$ 4.5mm dies). On Si, 100$\sim$300nm thick SiO_2 is formed on the surface through thermal oxidization, followed by hydrogen ion implantation (140 keV, $8.5\times10^{16}/cm^2$) into the

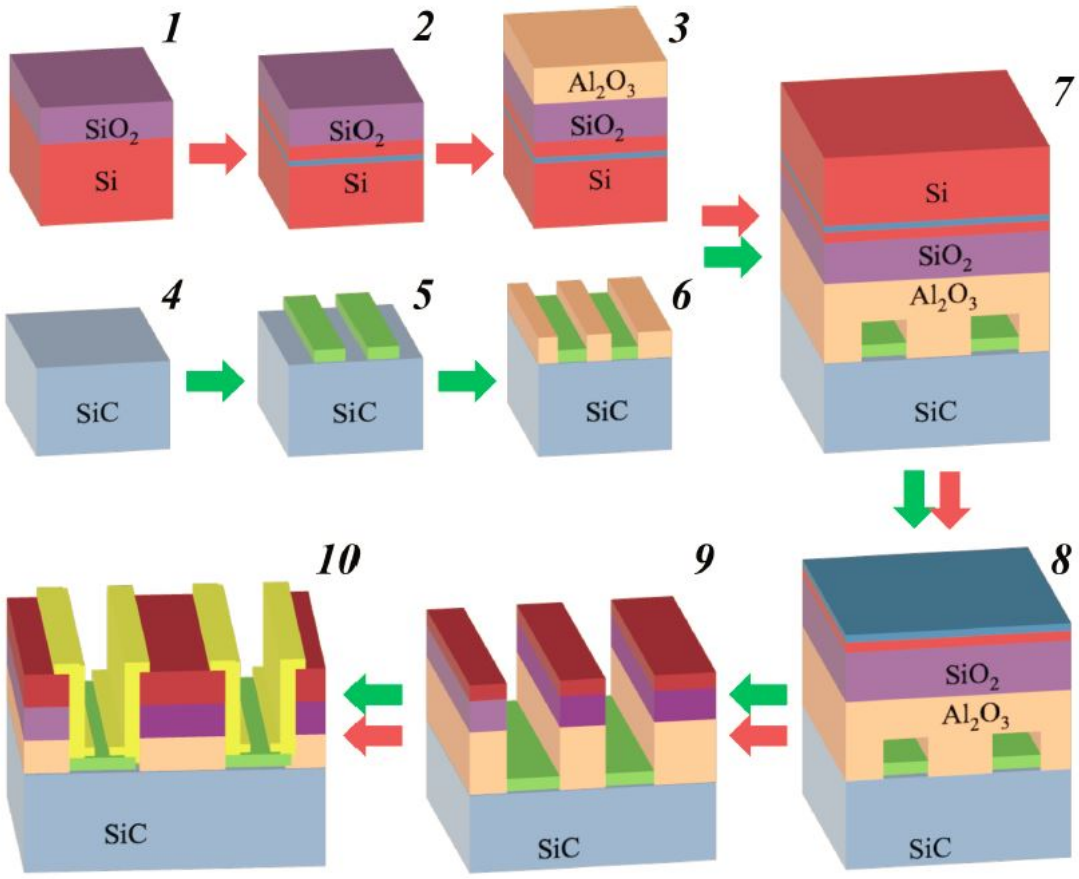

Figure 5.2: Schematic diagram of process flow for EG/Si to SiO_2/Si integration. (1-3) H ion implantation and Al_2O_3 deposition on SiO_2/Si. (4-6) Epitaxial graphene growth and selective Al_2O_3 deposition on SiC. (7-8) Wafer bonding and smart-cut for two platforms. (9-10) Etching through Si layer for via fabrication.

wafer at a depth of 900nm according to the implantation simulation. The temperature of the wafer is maintained at 15 $^{\circ}C$ during the implantation to avoid surface blistering. Note that the above steps are performed before the Si wafer is diced. For the SiC sample, two ways of graphene production are used. On the C-face, sub-monolayer graphene is grown at $\sim$1500 $^{\circ}C$ using the CCS method described in Chapter 2. On the Si-face, graphene nanoribbons are grown on the sidewalls defined by prior EBL and SF_6/O_2 RIE using patterned PMMA as the mask [3]. Then 30nm thick Al_2O_3 is grown on both SiO_2/Si and EG/SiC samples in an ALD system at 160 $^{\circ}C$ with TMA and H_2O as precursors. After the deposition of Al_2O_3, the samples are stored in de-ionized (DI) water for more than 24 hours to improve their surface hydrophilicity.

The following flip-chip wafer bonding is first performed in DI water to avoid particle contamination from air, then the bonded samples are transferred to a pressure module where $\sim$ 30N force is applied to the center of the samples on the SiC side. The samples in the module are first annealed at 100 $^{\circ}C$ for 1 hour to improve the bonding quality. Then the pressure is removed, and the samples are further annealed in a muffle furnace to 300 $^{\circ}C$ in air for 30 minutes to further increase the bonding strength. The temperature of the muffle furnace is then increased to 400 $^{\circ}C$ at a ramping speed of 5$^{\circ}C$/min, and the resulting activation of the implanted hydrogen layer splits the Si sample at the implantation plane. Due to the large bonding strength, the 900nm Si/SiO_2 layer still adheres to the SiC sample after the splitting, and successful transfer of crystalline Si layer onto EG/SiC samples is achieved. The sample is then slowly cooled down to room temperature to avoid detaching of the Si layer from SiC that could occur with rapid thermal contraction.

For further fabrication of interconnects between the Si layer and EG/SiC, regions of Si/SiO_2 need to be etched away for vias. To this end, 1μm thick photoresist layer (Microposit SC1813) is spin coated on the Si side of the bonded bilayer, and is patterned using photolithography to serve as a mask for Si and SiO_2 dry etching

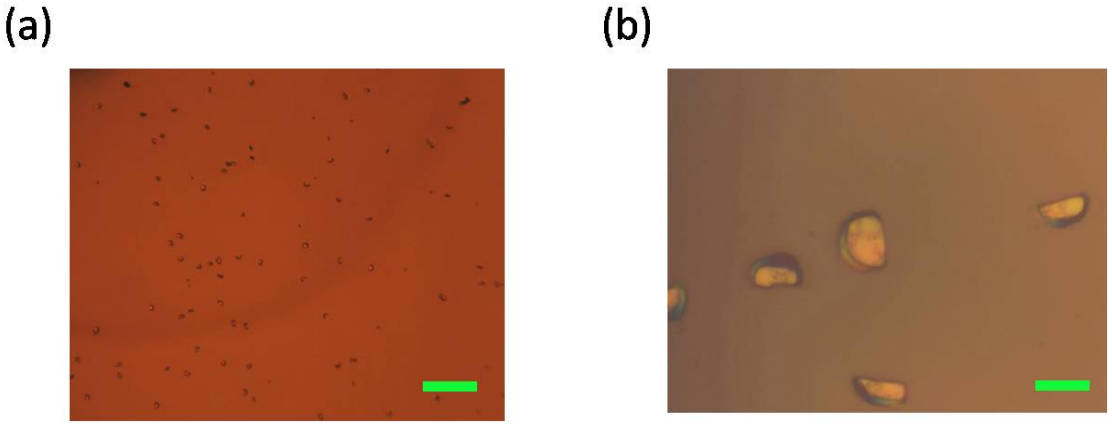

Figure 5.3: Optical images of $\sim$10μm Si "particles" transferred onto SiC due to shallow hydrogen ion implantation in the Si samples. (a) Scale bar is 100μm. (b) Scale bar is 10μm.

using SF_6/O_2 and CHF_3/Ar RIE, respectively. Al_2O_3 right on top of graphene is removed in a solution of H_3PO_4/H_2O (1:3) at 60 $^\circ C$. With the holes in designated regions of $Si/SiO2/Al_2O_3$ as a result of the above process, metal vias between the two platforms can be implemented before or after the Si-CMOS fabrication process.

5.2.2 Key Steps in the Process

In the above fabrication process, several steps are crucial to the success of the whole process. And they will be explained in details as follows.

First, the depth of the implanted hydrogen into Si is designed to be 900nm, which is determined for the integrity of the transferred Si layer. In the experiment, hydrogen implantation depth of 300nm was tested, and the result was bonded Si region with the size of $\sim 10\mu m$, as shown in Fig. 5.3. On the contrary, transferred Si region as large as several mm is achieved with implantation depth of 900nm. The difference could in part be attributed to the inhomogeneity of the implantation depth in the 300nm case, causing too small implantation depth in some regions that induces breaking in the transferred Si layer during the smart-cut. With a more uniform implantation technique, a thinner Si layer can, in principle, be transferred to EG/SiC using the

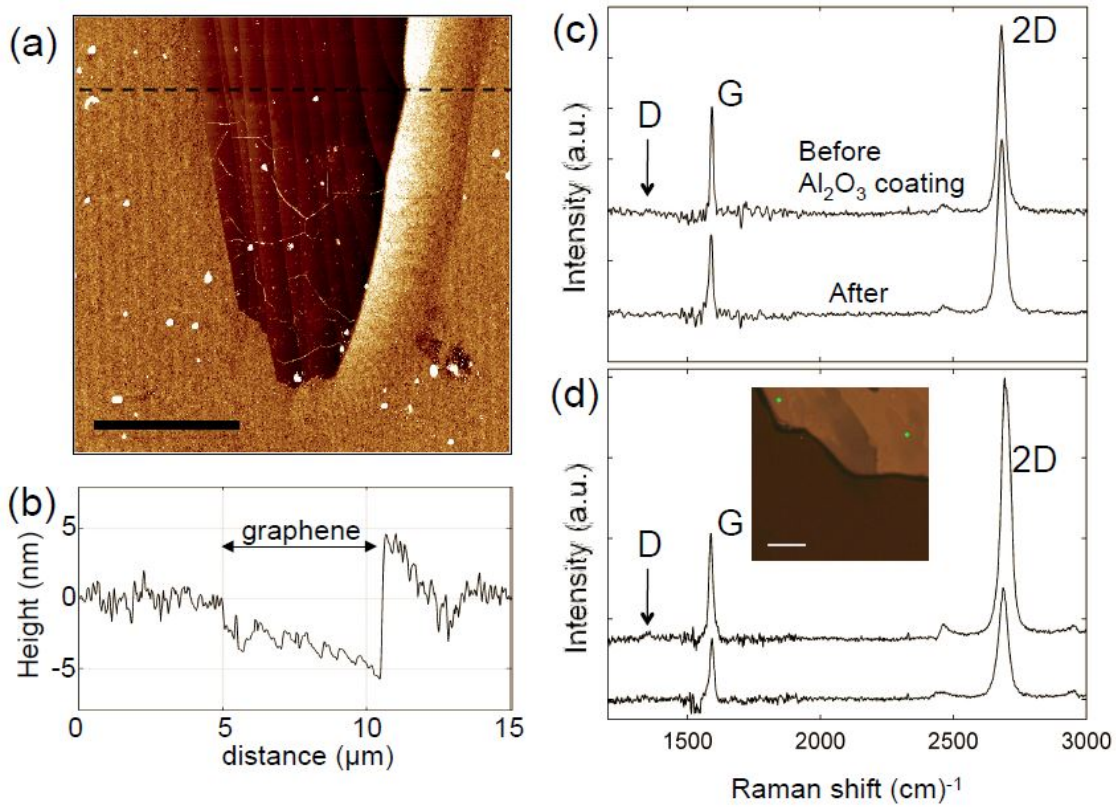

Figure 5.4: Surface characterization of C-face graphene after selective ALD of Al_3O_3. (a) AFM image of a partially graphitized region on C-face SiC after the ALD process. Scale bar is 5 μm. (b) AFM height profile along the dotted line in (a), showing that the graphene region is $\sim$ 2nm lower than the SiC with Al_2O_3. (c) Comparison of Raman spectra of the graphene region before and after the ALD process. Here the SiC background is subtracted, and the ALD process does not induce D peak to graphene. (d) Raman spectra taken at different graphene regions shown as the green dots in the SEM image in the inset.

same process.

Second, the atomic layer deposition of Al_2O_3 on both the Si and EG/SiC samples needs further explanation. In fact, it is one of the most important reasons for the success of the Si to EG/SiC bonding and smart-cut. It has been over two decades since SOI was first used in the industry [13], but only a few reports in literature covered Si to SiC wafer bonding [44, 22, 85, 16], and none of them mentioned Si wafer bonding to SiC with graphene. There are two primary problems in the wafer bonding of Si to SiC. One is the different thermal expansion coefficient inducing de-bonding

as the wafers are annealed to high temperature for increased bonding strength. The other one is lack of high quality thermal oxide on SiC surface which is crucial for the often used hydrophilic bonding. Moreover, as Si wafer bonding with EG/SiC is considered, graphene's hydrophobic nature and fragility under mechanical treatments add further more to the difficulties.

In this study, the solution to all these problems is Al_2O_3 ALD on the graphene-free regions of EG/SiC and Si samples. As Al_2O_3 ALD is performed on EG/SiC without prior seed layer, alumina preferably grows on the SiC region [95], as shown in Fig. 5.4 (a), due to the inertness of graphene surface to the precursors (TMA and water in this case). Besides, the quality of the graphene is not affected by the ALD process, which is indicated in the comparison between Raman spectra of graphene before and after the ALD process, as shown in Fig. 5.4 (c). This layer of Al_2O_3 on both samples serves as the bonding interface, and graphene is protected from direct physical contact to Si. Terminated with -OH after the ALD process, the surface of Al_2O_3 is compatible with the following hydrophilic bonding. And due to the atomic precision in the thickness of Al_2O_3 in the ALD process, the final surface roughness is suitable for wafer bonding, considering that the starting SiO_2/Si and SiC samples have surface roughness at the nm scale. Besides, this Al_2O_3 layer also relaxes the stress from different thermal expansion coefficients of Si and SiC by having the same material at the interface. To sum up, the utilization of ALD Al_2O_3 properly solves the problems of thermal stress and lack of good oxide layer in SiC to Si wafer bonding, and prevents possible damage to graphene in the bonding process.

Third, in the etching process for inter-layer via fabrication, precise etching depth is required for good electrical contact to graphene. Over-etching of the materials above graphene would result in damage to the atomically thin graphene layer, while under-etching would leave insulating materials on top of graphene preventing further electrical contact. Here three steps of etching are performed. The first step is dry

etching of the Si layer with SF_6/O_2 plasma, and the underneath SiO_2 serves as the etch stop layer. The second step is dry etching of the SiO_2 layer with CHF_3/Ar plasma, and the Al_2O_3 below acts as the etch stop layer in this case. The third step is wet etching of Al_2O_3 in warm phosphoric acid solution that does not damage the graphene due to its weak oxidizing ability. Here the Al_2O_3 layer is used again for its etching resistance to CHF_3/Ar plasma, further showing the importance of the ALD step in this whole process.

5.3 Sample Characterization

5.3.1 Characterization at Different Process Steps

The samples are characterized at different steps of the process. Fig. 5.5 shows the results of wafer bonding and smart-cut for C-face epitaxial graphene on SiC with Si. Here the sample size is 3.5mm by 4.5mm, as shown in Fig. 5.5 (a) after bonding. Seen through the transparent SiC wafer, the golden color covering most of the three samples are the successfully bonded regions, while the areas with different colors at the corners are not as well bonded as the center. Note that in wafer scale bonding, it is known that the presence of one 1μm size particle between the wafers would induce unbonded area with the size of $\sim$ 5mm [86], close to the size of the whole sample used here. The optical images of EG/SiC and Si samples after the smart-cut are shown in Fig. 5.5 (b), left and right. On the Si sample, the SiO_2/Si layer above the implanted hydrogen level in the brown region at the center is transferred to the EG/SiC sample, on which the brown region is almost identical to the right one. SEM image at the edge of the transferred SiO_2/Si on the EG/SiC sample (Fig. 5.5 (c)) clearly shows the cross section of different layers involved. The top layer with rough surface is the transferred Si, and the roughness is induced by the smart-cut process. Note that in an industrial SOI process, this surface would undergo additional CMP process for a smoother surface before following steps. The middle layer with

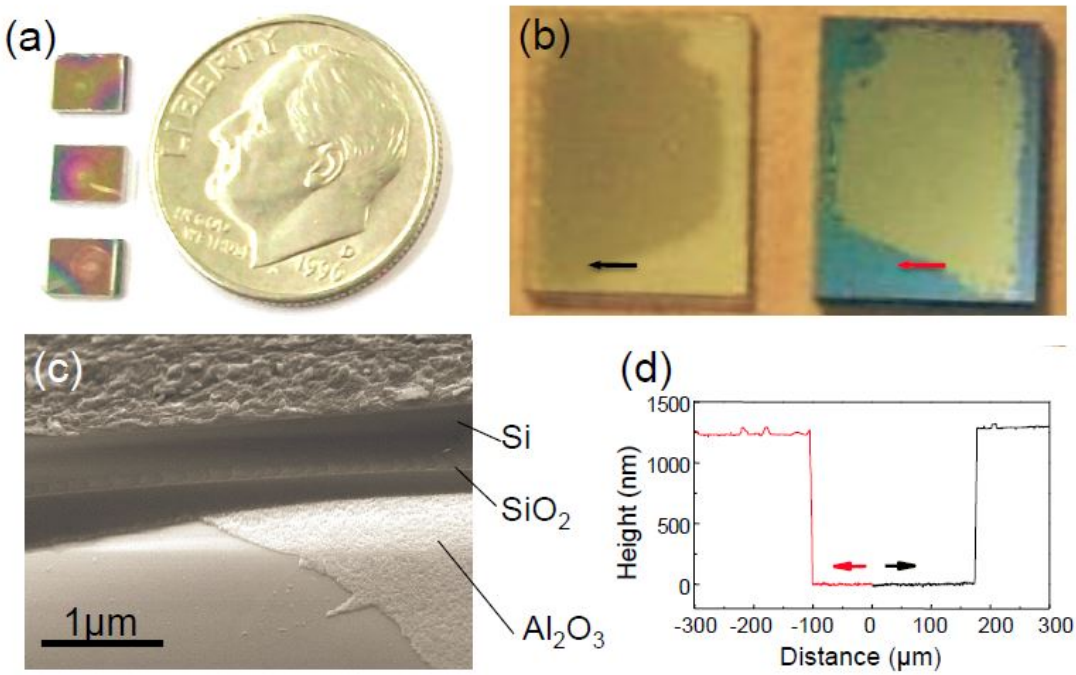

Figure 5.5: Surface characterization of the Si layer bonded with C-face EG/SiC. (a)Optical images of three 3.5mm×4.5mm samples after wafer bonding. Golden/purple regions of the samples are strongly bonded. (b) EG/SiC and Si samples after the smart-cut. The darker brown region on the left SiC sample correspond to the transferred thin Si layer, and on the right sample a symmetric region showing color difference from the rest of the sample indicates removed Si. (c) SEM image of Si-on-EG/SiC sample after smart-cut. The image shows a cross sectional view of the sharp and clean interface between transferred SiO_2/Si and the SiC substrate that is partially covered by Al_2O_3. (d) Height profile on both samples in (b), showing that the transferred Si/SiO2 layer is 1.2 μm thick.

stripes at the cross section is the silicon oxide layer. On the EG/SiC surface without transferred Si, the smooth region on the bottom left corner is graphene, while the rough region to the right is the SiC surface covered with Al_2O_3. The roughness on the Al_2O_3 can be attributed to incomplete transfer of Al_2O_3 from the Si sample to EG/SiC in the unbonded regions. The height profile at the edge of transferred SiO_2/Si on EG/SiC (Fig. 5.5 (d) right) shows a total thickness of 1.2 μm for the transferred material, in agreement with the involved 300nm thick SiO_2 and 900nm thick Si above the implanted hydrogen level. Similar height profile at the edge of transferred region on the Si sample (Fig. 5.5 (d) left) shows a similar depth for the removed material. Together these optical and SEM images of the samples at different steps of the bonding and smart-cut process demonstrate the success for the transfer of Si layer to EG/SiC.

Fig. 5.6 shows the results for wafer bonding of Si and the Si-face of SiC with structured sidewall graphene nano-ribbons. With the same wafer bonding process described above, most area of the samples is well bonded, as indicated by the uniform color except the top corners in the optical image in Fig. 5.6 (a). In the magnified optical image in Fig. 5.6 (b) through the transparent SiC sample, the sidewall structures are clearly visible. To demonstrate that there is graphene on the sidewalls of Si-face SiC, AFM and EFM images are shown in Fig. 5.6 (c) and (d). The lines with bright contrast in the EFM image indicate the signature of graphene right at the patterned sidewalls. To obtain these sidewall graphene nano-ribbons, 50nm deep trenches are etched into Si-face of SiC with SF_6/O_2 plasma, and the sample is heated to $\sim 1500\ ^\circ C$ for 2 minutes. The result is 100nm wide graphene nano-ribbons on the sidewalls of the trenches, similar to that in [82].

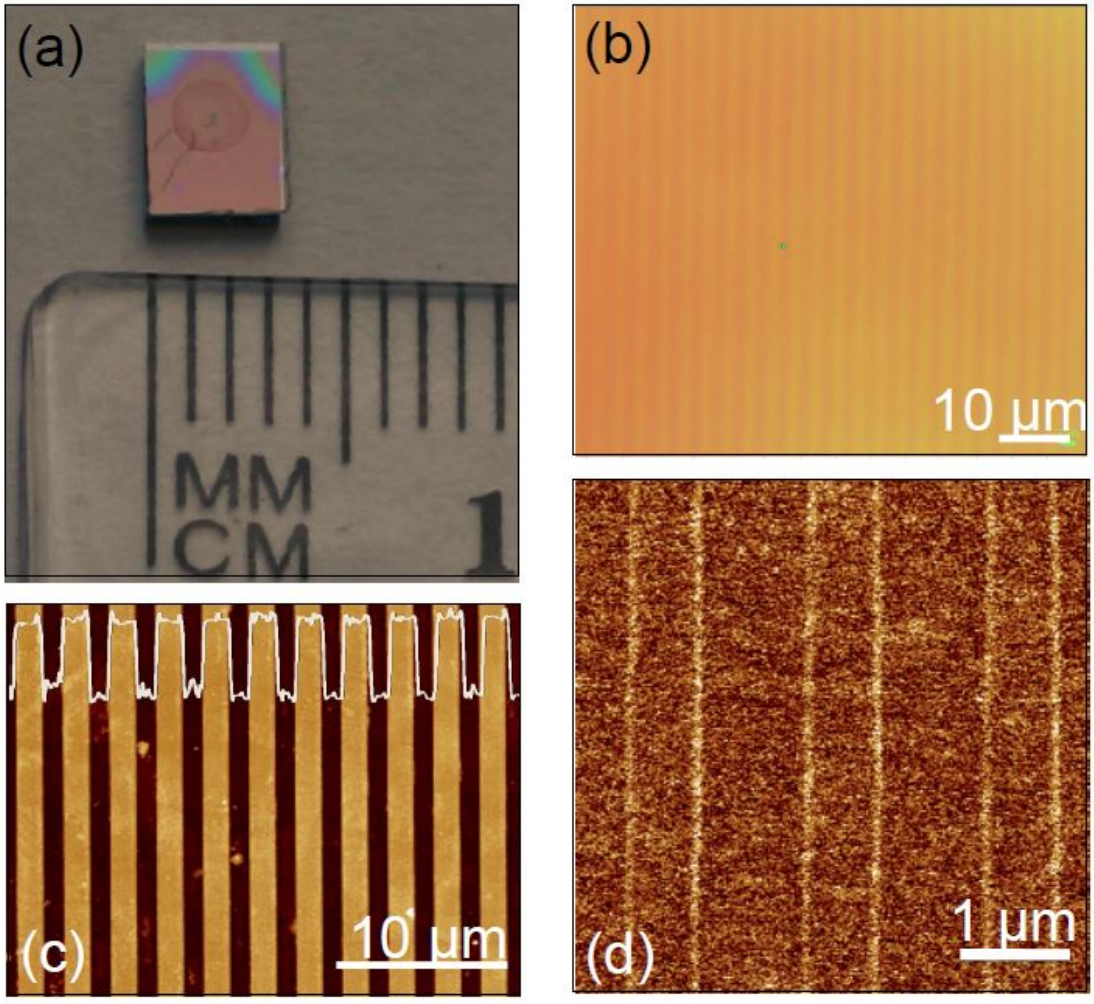

Figure 5.6: Surface characterization of the Si layer bonded with Si-face structured graphene. (a)Optical images of 3.5 mm × 4.5 mm sample after wafer bonding. The bulk purple region of the sample is successfully bonded. (b) Optical image of the structures on SiC seen through the transparent SiC sample. The structures remain intact after the wafer bonding (c) and (d) AFM topography and electrostatic force microscopy (EFM) images of the sidewall graphene structures on Si-face SiC after growth and prior to wafer bonding. The depth of the trenches is 20nm, and the lines with brighter contrast in (d) are the 40nm wide sidewall graphene nano-ribbons.

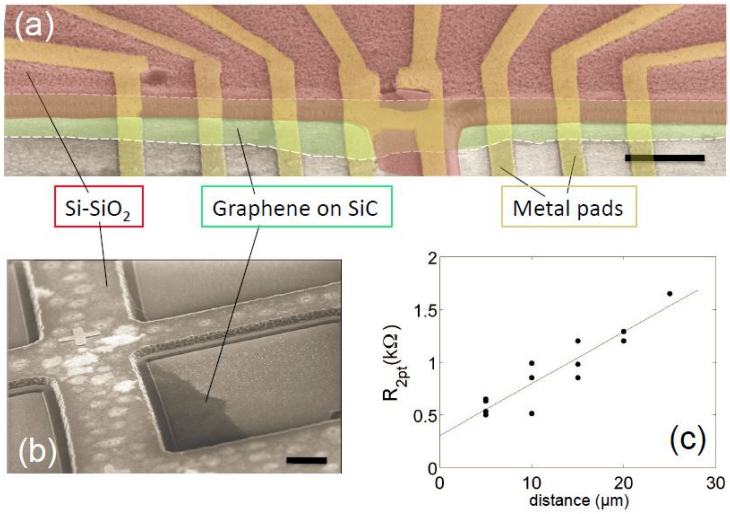

Figure 5.7: SEM images of regions on the C-face EG/SiC with transferred Si, and windows are opened in Si layer for metal contact fabrication on graphene, along with electrical measurement results. (a) False-colored SEM image of the multi-probe graphene device with metallic leads on Si layer. (b) Graphene region (darker) in the opened window (square). Scale bars in (a) and (b) are both 5 μm. (c) 2-point resistance of graphene device with various contact separations. The resistance approximately increases linearly with contact separation distance.

5.3.2 Electrical Characterization of After-Integration Graphene Devices

To demonstrate the possibility of electrical contacts on graphene through the etched holes in Si/SiO_2, multiple contacts are patterned with e-beam lithography on C-face graphene in the region where the upper materials are etched away. Ti/Pd/Au is deposited and lifted-off to form the metal leads extended to the remaining transferred Si region. Fig. 5.7 (a) shows a false-colored SEM image of the as-fabricated device, where the pink region is the un-etched Si, yellow stripes are the metal contacts, and the green region is graphene partially covered by Si/SiO_2. For better contrast between exposed regions in SiC with and without graphene, Fig. 5.7 (b) shows an SEM image of the sample before contact fabrication, and the darker region in the square window is graphene. Note that the metal leads in Fig. 5.7 (a) are continues at the boundary of Si/SiO_2 region. These proof-of-principle electrical contacts to graphene demonstrate the possibility of vias through the etched holes, which would

serve as the inter-platform connections in the scheme of EG/Si-CMOS integration.

Two-point resistance measurement is performed on the devices, and the result is shown in Fig. 5.7 (c). Linear fit of the data points for resistances at different contact separation distances indicates graphene sheet resistivity of 200∼300 Ω/sq, and contact resistance between graphene and the metal leads $R_C \sim 600\ \Omega\mu$m. These results agree well with the resistivity of doped mono-layer and multi-layer graphene, and metal to graphene contact resistances. Further tests for the robustness of the metal contacts at large input current show that these contacts could withstand current density as high as 1.5 mA/μm without observable degradation.

5.4 Discussion on Future Prospectives

In the above sections, the critical step of a graphene-silicon integration scheme is demonstrated, in which the two wafers are monolithically integrated and act as interconnected parallel electronic platforms. The process is flexible for development of electronic devices on both platforms. On the top layer, the transferred mono-crystalline Si, whose thickness can be varied according to the H implantation depth in the smart-cut technique, can be utilized for CMOS fabrication. Ion implantation, epi-layer growth and standard lithography techniques can be implemented on this top Si platform without damaging the underlying graphene structures, as long as the vias are fabricated at the last step. Moreover, EG on SiC could withstand temperatures up to 400 °C in air and 1200 °C in vacuum, thus could survive the annealing steps in CMOS processing. For the EG/SiC platform, high frequency transistors have already by demonstrated on the C-face in the previous chapter [34]. On the Si-face of SiC, sidewall graphene nano-ribbons with ballistic carriers have a strong potential for novel device concepts.

The major obstacle for successful wafer bonding and smart-cut in this study is particle contamination. However, considering the small sample size and non-stringent

clean-room environment used here, this process still has a strong industrial potential with expected yield improvement as wafer-size bonding and industrial level clean-room are utilized. Compared with previously reported graphene transfer or printing techniques, this EG/SiC to Si integration method takes full advantage of the mono-crystalline substrate and epitaxial growth process (well defined and reproducible interface, production grade substrate, nano-structures availability, no transfer induced damage). Beyond graphene for only electrodes and interconnects, this hybrid system provides an alternative to the current Si-CMOS and III-V material based technology, and is envisioned for future high performance nano-electronics, such as high frequency electronics, spintronics, optoelectronics, etc.

5.5 Summary

In conclusion, here a unique EG/SiC to mono-crystalline Si integration method is demonstrated, and the resulting 3D stacked strucutre is fully compatible with VLSI technology while preserving the integrity and nano-structures of graphene. Different from conventional graphene transfer technique, thin layers of mono-crystalline Si are transferred to EG/SiC using the well-developed SOI wafer bonding and smart-cut technology. Si-CMOS devices can be fabricated on the transferred Si layer and connected to EG devices through metallic vias, while posing no degradation on the graphene nano-structures that are protected and could withstand high temperature processes.

CHAPTER VI

CONCLUSION

To summarize, mono-layer C-face epitaxial graphene was investigated for its high carrier mobility and possible applications in high speed electronics. The CCS approach for epitaxial graphene formation on SiC was optimized for mono-layer growth on C-face, and a combined characterization method using AFM and Raman spectroscopy was proposed for mono-layer identification. Along with techniques to control the resist residue on top, as-fabricated graphene Hall bars exhibited room temperature carrier mobility above 10,000 cm^2/Vs, and low temperature mobility up to 40,000 cm^2/Vs. Quantum Hall effect was observed on the devices at 4.2K and magnetic field as low as 3.5T, further confirming the intrinsic high quality of mono-layer C-face graphene.

To fabricate top-gated graphene devices, several gate dielectric deposition techniques were experimented, including the NFC polymer + ALD Al_2O_3 apporach, slow deposition of Al for AlO_x, and finally, Al seed layer + ALD Al_2O_3 on lithographically patterned structures for compatibility with self-aligned contacts. The surface quality of these dielectric layers were examined, and the resulting device performance were characterized. This study helped the determination of the dielectric deposition scheme for high performance graphene RF transistor fabrication.

Based on the high quality mono-layer C-face epitaxial graphene and the above chosen dielectric deposition method, RF transistors were fabricated featuring T-gate and self-aligned source/drain design. With a low contact resistance and high on-state current, high power gain performance was achieved on the as-made devices. $f_{max} = 70$ GHz was observed on 100nm gate devices, along with a maximum $f_T = 110$ GHz.

This f_{max} after de-embedding is higher than those of any graphene RF transistors in previous reports, and was attributed to the T-gate design, self-alignment, and low contact resistance. This improvement opens a path towards better power gain performance on graphene-based high speed devices.

Considering the limit of graphene in digital electronics due to the absence of a band gap, possible integration of epitaxial graphene devices and Si-CMOS was investigated. Different from the traditional graphene transfer method, a new scheme was proposed that involves thin Si layer transfer onto EG/SiC platform, which, in principle, does not have ion and polymer residue problems. SOI and smart-cut techniques were adopted in the integration process, and thin mono-crystalline Si layers were successfully transferred onto C-face SiC with epitaxial graphene grown on top. Wafer bonding between Si and Si-face SiC with sidewall nano-ribbons was also achieved. Holes are etched in the bonded Si-layer for inter-platform via fabrication, and electrical measurements using these inter-layer contacts confirmed that the underneath graphene was not harmed by the integration process. This EG/Si hybrid system provides an alternative to the current Si-CMOS/III-V material technology for electronics, and has its potential in future nano-electronics with new device concepts.

APPENDIX A

SCATTERING PARAMETERS FOR HIGH FREQUENCY DEVICE CHARACTERIZATION

Scattering parameters (S-parameters) characterizes the relation between electromagnetic waves into and out of a system. They are important in microwave devices and circuits because they are easier to measure and work with at high frequencies compared with other parameters. In this study, S-parameters of the devices-under-test (DUT) can be directly obtained through a network analyzer, and can be used to calculate more relevant parameters such as current gain and power gain of the devices. The derivation of S-parameters, as well as their relation to some other parameters of the system will be briefly introduced as follows [74].

Consider a general two-port network as shown in Fig. A.1 (a). The left port is designated for the input signal (I_1 and V_1), while the right port is for the output signal (I_2 and V_2). Define the normalized incident voltages of the two ports as

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} \tag{A.1a}$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}}, \tag{A.1b}$$

where Z_0 is the reference impedance of both two ports, and is 50Ω in most microwave systems. Similarly, define the normalized reflected voltages as

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} \tag{A.2a}$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}}. \tag{A.2b}$$

Schematic diagram of the incident and reflected waves of the network is shown in

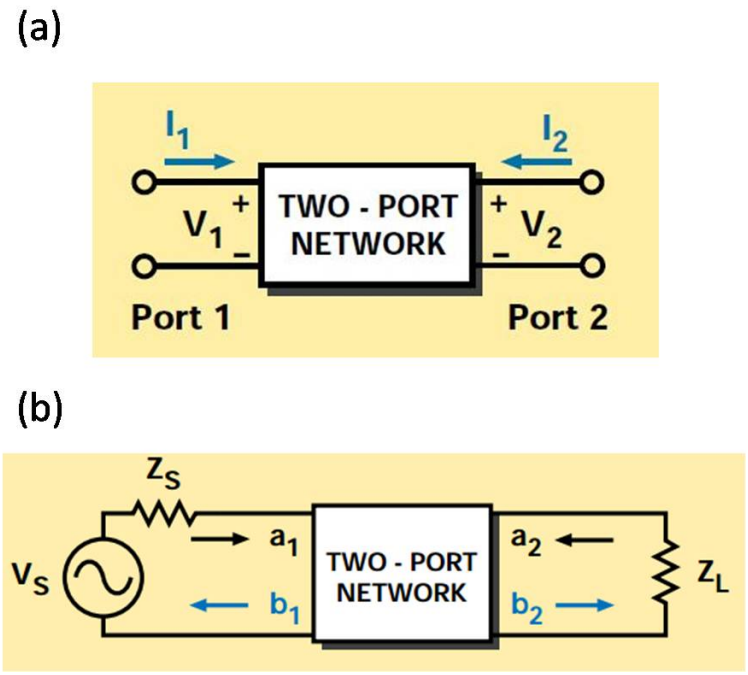

Figure A.1: Schematic diagram of a 2-port network (a) with input I_1/V_1 and output I_2/V_2, and (b) with incident voltage a_1/a_2 and reflected voltage b_1/b_2 (both normalized) [74].

Fig. A.1 (b). The linear equations describing this network are:

$$b_1 = s_{11}a_1 + s_{12}a_2 \tag{A.3a}$$

$$b_2 = s_{21}a_1 + s_{22}a_2. \tag{A.3b}$$

Here the S-parameters are: s_{11} and s_{22} are the input and output reflection coefficients with matched output or input load ($Z_L = Z_0$ or $Z_S = Z_0$), while s_{21} and s_{12} are the forward and reverse transmission gain with matched output or input load.

The (forward) current gain is defined as

$$h_{21} = \frac{I_2}{I_1}|_{V_2=0} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22}+s_{12}s_{21})}. \tag{A.4}$$

For FET at high frequencies, the output AC current amplitude does not significantly change with frequency, as long as the input voltage amplitude is constant. On the contrary, the input current is approximately proportional to the frequency at constant input voltage amplitude, since the input impedance primarily comes from the gate

capacitor, and is inverse proportional to the signal frequency. As a result, the current gain is approximately inverse proportional to the input signal frequency, and is often referred to as the "20dB/dec" rule in the $|h_{21}|^2$ versus frequency relation (would be 10dB/dec for $|h_{21}|$ versus frequency).

As for the power gain of the devices, there are several parameters used in literatures, such as maximum available gain, maximum stable gain, and Mason's unilateral gain. The parameter used in this study is the Mason's unilateral gain (MUG or U), which is defined as a power gain of a two-port network without output-to-input feedback, and the input and output being conjugately impedance matched to signal source and load, respectively. It is expressed with S-parameters as

$$U = \frac{|s_{12}s_{21}s_{11}s_{22}|}{|(1-|s_{11}|^2)(1-|s_{22}|^2)|}. \tag{A.5}$$

The frequency dependance of the power gain is complicated, and will not be explained in details here. But in some high frequency ranges, it also follows the 20dB/dec rule, as shown for the graphene RF transistors in Chapter 5.

The cutoff frequency f_T is defined as the frequency at which the current gain of the device reaches unity $|h_{21}| = 1$. In a simplified device model, the cutoff frequency is expressed by DC parameters as

$$f_T \approx \frac{g_m}{2\pi C_G}, \tag{A.6}$$

where $g_m = dI_{DS}/dV_G$ is the transconductance of the device, and C_G is the gate capacitance. In short-channel devices, g_m is approximately independent of the channel length, while C_G is proportional to the channel length. As a result, f_T increases with decreasing channel length.

As for the high frequency power gain performance, the maximum oscillation frequency f_{max} is defined as the frequency at which the power gain reaches unity ($|U| = 1$). Its relation to static parameters and f_T of the device is

$$f_{max} \approx \frac{f_T}{2\sqrt{2g_D(R_G + R_{SD}) + 2\pi f_T R_G C_G}}, \tag{A.7}$$

where $g_D = dI_{DS}/dV_{DS}$ is the drain/source differential conductance (output admittance), R_{SD} is the drain/source access resistance, R_G is the gate resistance.

APPENDIX B

RADIO FREQUENCY TRANSISTOR STRUCTURE — T-GATE AND SELF-ALIGNMENT

From the relation between f_{max} and static parameters of the device, it is obvious that to obtain a high f_{max}, small g_D, R_{DS} and R_G are required beside a high f_T. A small g_D requires current saturation of the device, which is absent in graphene, thus it will not be explained here in details. The device design techniques to improve the other two parameters are introduced as follows.

First, for a small gate resistance, a large gate cross section area is required, indicating thick gate metal and large gate length. Meanwhile, a small gate length is needed for a high f_T, whereas too large gate thickness/length aspect ratio would result in mechanical instability and device failure. To solve this problem, a mushroom-shaped gate structure (T-gate) was proposed that enables both small gate length and large gate cross section, as shown in Fig. B.1 (a) [84]. Generally, multi-layer photo or e-beam resist with different dose requirements on each layer is used to pattern the T-gate structures, as shown in Fig. B.1 (b). T-gate is now widely used in high frequency devices to minimize gate resistance.

Second, drain/source access resistance of FETs primarily contains contact resistance and un-gated channel resistance. Contact resistance depends on the properties of the channel material, the contact metal, and the interface between them. The un-gated channel region is introduced to the device to tolerate the alignment error between the lithography steps of gate structures and contact regions, so that the gate is not shorted to the source/drain contacts. The alignment error strongly depends on the lithography technology. To minimize the un-gated channel area (resistance),

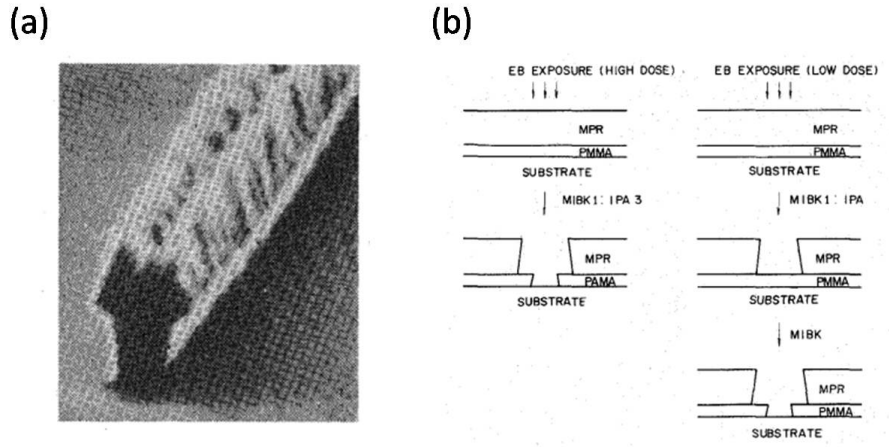

Figure B.1: (a) SEM image at the cross section of a T-gate structure. (b) E-beam lithography processes on bilayer resist to define T-gate structures, the left diagram is a one-step exposure process, and the right one is a two-step exposure process [84].

a lithography-independent alignment method for the gate and the source/drain was introduced. Here the gate structure is used as part of the mask to isolate the source from the drain in the contact fabrication without being shorted to the drain/source. This method is referred to as 'self-alignment'.

Another structural feature for RF transistors in this study that needs some explanation is the two-finger design, as shown in Fig. 4.4. This design is used so that the input and output current flow is symmetric to the gate and drain contacts, which is beneficial for high frequency measurements. Details about multi-finger design for RF transistors can be found in Ref. [91].

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