EFFICIENT PRODUCTION TESTING OF HIGH–PERFORMANCE RF MODULES AND SYSTEMS USING LOW–COST ATE

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LIST OF ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
ADSL	Asymmetric Digital Subscriber Line
AM	Amplitude Modulation
ANN	Artificial Neural Network
ATE	Automated Test Equipment
ATPG	Automatic Test Pattern Generator
AWG	Arbitrary Waveform Generator
BIST	Built-In-Self-Test
CODEC	Coder-Decoder
COT	Cost-of-Test
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition Card
DCR	Direct-Conversion Radio
DfT	Design-for-Testability
DiB	Device Interface Board
DNL	Differential Nonlinearity
DOT	Defect-Oriented-Testing
DSP	Digital Signal Processor
DUT	Device-under-Test
EVM	Error Vector Magnitude

FFT	Fast Fourier Transform
GA	Genetic Algorithm
GSM	Global System for Mobile
HBT	Hetero-junction Bipolar Transistor
IF	Intermediate Frequency
IFFT	Inverse-FFT
IIP3	Third-order Input Intercept Point
IMD	Inter-Modulation Distortion
INL	Integral Nonlinearity
ITRS	International Technology Roadmap for Semiconductors
KGD	Known Good Die
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-pass filter
MARS	Multivariate Adaptive Regression Splines
MTPR	Multi-Tone Power Ratio
MVNA	Modulated Vector Network Analyzers
NF	Noise Figure
P1dB	1-dB Compression Point
PA	Power Amplifier
PAE	Power-Added-Efficiency
PAR	Peak-to-Average
PER	Packet Error Rate

PFD	Phase-Frequency Detector
PiB	Probe-interface Board
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RTP	Release-to-Production
RX	Receiver Subsystem
SFDR	Spurious-Free Dynamic Range
SiP	System-in-Package
SOC	System-on-Chip
SUT	System-under-Test
TDMA	Time-Domain Multiple-Access
TDR	Time Domain Reflectometry
THD	Total Harmonic Distortion
TOI	Third-Order Intercept
TX	Transmitter subsystem
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer
VSA	Vector Spectrum Analyzer
WLAN	Wireless Local Area Network

SUMMARY

The proliferation of wireless communication devices in the recent past has increased the pressure on semiconductor manufacturers to produce quality radio frequency (RF) and system-on-chip (SoC) devices at a low cost. This entails reducing manufacturing test cost as well, since the cost of testing modern RF devices can be up to 40% of the manufacturing cost. The high test cost of these devices can be mainly attributed to (a) the expensive nature of the RF automated test equipment (ATE) used to perform wafer-level and fully packaged RF functionality tests, (b) limited test point access for the application and capture of test signals because of signal integrity problems, (c) the long test development and test application times resulting from the complex nature of the required tests, and (d) the lack of diagnostic tools to evaluate and improve the performance of loadboards and test resources in high-volume tests.

In this thesis, a framework for the efficient production testing of high-performance RF modules and systems using low-cost ATE is proposed. This framework uses low-speed, low-resolution test resources to generate reliable tests for complex RF systems. Also, the test resources will be evaluated and improved ahead of high-volume tests to improve test yield and throughput. The components of the proposed framework are as follows:

(1) **Genetic ATPG for reliable test stimulus generation using low-resolution test resources:** A genetic algorithm (GA) based automatic test pattern generator (ATPG) to optimize the *alternate test stimulus* for reliable testing of complex RF systems using low-resolution, low-cost test resources. These test resources may be on-chip or off-chip. The stimulus will be optimized to overcome uncertainties in the test resources.

(2) **Concurrent voltage/current alternate test methodology:** A testing framework for efficiently testing the high-frequency specifications of RF systems using low-frequency spectral and/or transient current signatures. Suitable on-chip and/or off-chip design-for-test (DfT) resources are used to enable the source and capture operations of the test signals using low-cost ATE resources.

(3) **Loadboard checker:** A checker tool to accurately characterize/diagnose the DfT resources on the RF loadboards used to enable test of RF devices/systems using low-cost ATE. This tool will provide significant improvement in the yield and throughput of the generated RF tests during high-volume production testing.

(4) **Advanced test signal processing algorithms**: The performance of the low-cost ATE resources, in terms of their linearity/resolution, will be evaluated and improved to enable the accurate capture of the test response signals.

All the above mentioned components contribute to enabling efficient production testing of high-performance RF modules and systems using low-cost, low-speed ATE. The contribution of each of these components in developing the efficient testing framework is highlighted in Figure 1.

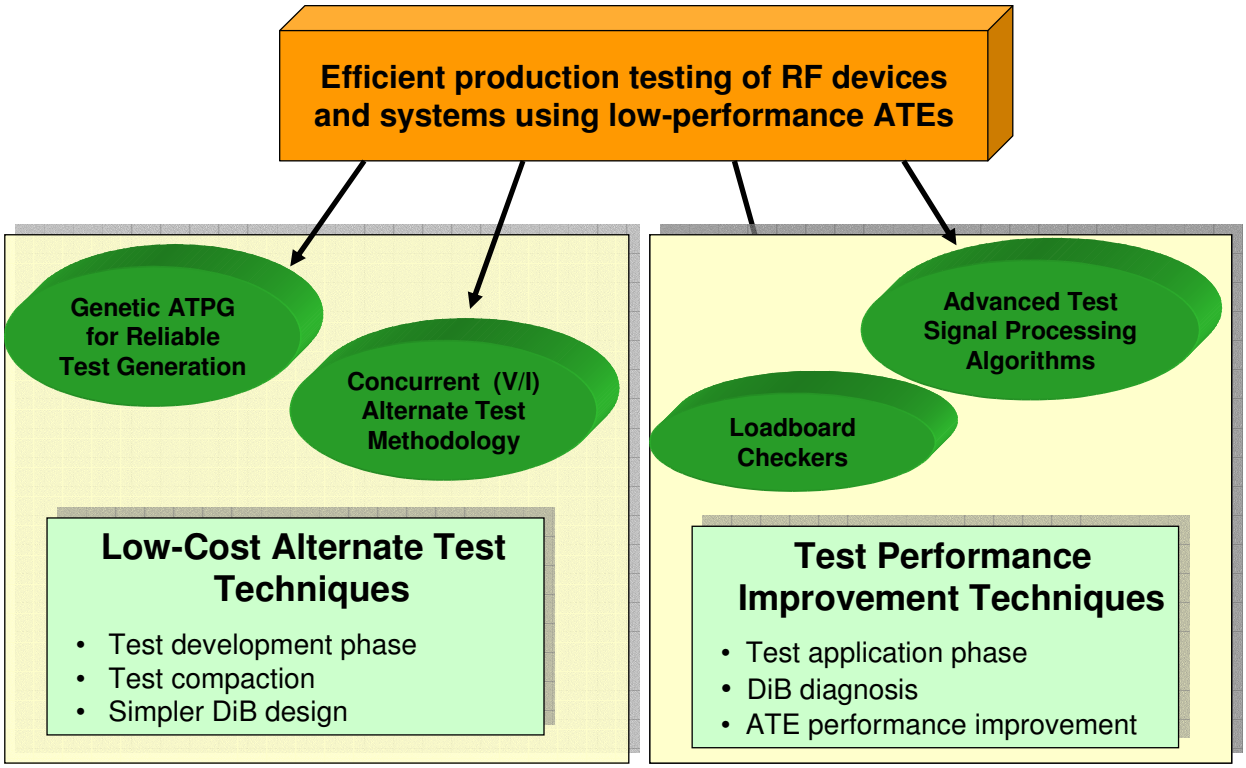


Figure 1. Block diagram of the efficient production testing framework highlighting the contribution of the different components in lowering the overall test cost of RF modules and systems.

Chapter 1

INTRODUCTION

The proliferation of wireless communication devices in recent past has increased the pressure on semiconductor manufacturers to produce quality radio frequency (RF) devices and systems at low costs. Testing these devices for manufacturing variations that affect the component values plays a significant part in the quality assurance process. The changes in component values in turn affect the overall functionality of the device-under-test (DUT) that is usually presented in terms of the specifications of the device. The manufacturer needs to carefully test for these specifications to ensure that the effect of the process variations on the specifications are within specified bounds. The test cost of modern RF devices is mainly driven by (a) the expensive nature of the RF automated test equipment (ATE) used to perform wafer-level and fully packaged RF functionality tests, (b) the limited test point access for application and capture of test signals due to signal integrity problems, (c) the long test development and test application times due to complex nature of the required tests, and (d) the lack of diagnostic tools to evaluate and improve the performance of loadboards and test resources in high-volume tests. Due to some/all of these factors, the test cost of the RF devices and systems is estimated to be upto 40% of their total manufacturing cost.

The procedure of testing the ICs for their performance specifications is performed at two different stages during the IC development cycle. The flow of a typical design cycle is shown in Figure 2. As shown in Figure 2, the characterization testing is performed right after the IC design procedure to evaluate the performance of the IC and to provide feedback to the designers on the IC performance. Normally, high-performance instrumentation is used for these tests as they are

performed only on few ICs in controlled laboratory conditions. Once the specifications of the customer are met, these ICs are released for high-volume production which involves mass manufacture and test of the ICs. The high-volume production testing of semiconductor devices is done in two phases: (1) wafer-level testing and (2) final fully-packaged testing. Wafer-level testing is performed on fabricated wafers to prevent bad dies from being passed through further production steps. Final testing is done on the packaged wafers to guarantee the performance of the device at the end of the production line. In both these phases, tests are conducted over millions of devices, which call for the use of ATE.

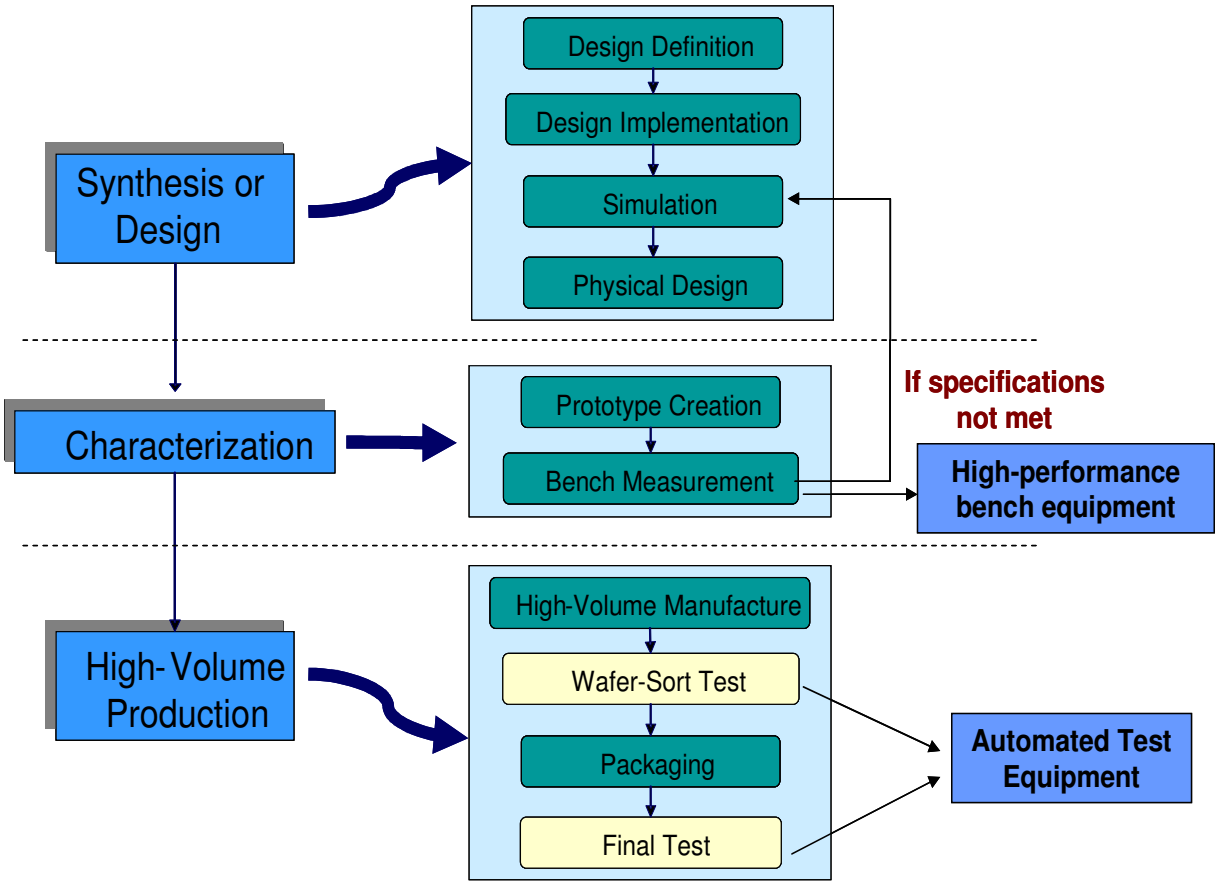


Figure 2. Typical IC development cycle.

1.1 AUTOMATED TEST EQUIPMENT

ATE (also known as tester) (see Figure 3) consists of a workstation, a mainframe, and a test head. The workstation provides the human interface to the ATE and the vendor provides specific tools to develop test programs for this purpose. The mainframe consists of the power supplies and the measurement instrumentation. The test head contains most of the sensitive measurement electronics that require close proximity to the DUT. The DUT is placed on a performance evaluation board (also known as the loadboard), which is mounted on the test head. This provides the electrical contact between the DUT and the measurement instruments in the ATE. Wafer-level testing requires the use of special probes that connect the I/O pins on the die to the electrical resources of the ATE through the probe-interface board (PiB). The PiB is synonymous with the loadboard that is mounted on the test head of the ATE in the final production testing phase. A picture of a Teradyne (ATE vendor) 'Catalyst' ATE that can be used to test high-performance SOCs is shown in Figure 3.

Figure 3. Teradyne 'Catalyst' high-performance ATE.

1.2 TEST ECONOMICS

Continuous improvements in process technologies and trimming techniques allow design engineers to add more functionality on a single chip. This increases the complexity of the chip and hence, their testing requirements. The test cost of modern RF devices and systems is the fastest growing portion of their manufacturing cost and is currently estimated to be around 40% of their total cost. A simple expression commonly used to estimate cost-of-test (CoT) [1] is

$$CoT = \frac{(Fixed\ cost + Recurring\ cost)}{(Yeild * Throughput)} \qquad \textbf{Equation 1}$$

where *Fixed cost* represents the ATE cost, the probe/handler cost, and the installation costs. Recurring cost consists of the ATE maintenance costs and per-device test cost, which is about 10% of the fixed costs. Yield is the ratio of the total number of good devices to the total number of tested devices. Throughput is the ratio of the total number of good devices to the time taken to test all the devices.

The CoT is highly sensitive to the cost of the ATE used to test the devices for a constant processes yield and throughput. RF ATE is expensive and is projected to cost around $2 million each. This cost translates to around three to five cents per second of the test time. This could be significant when one considers that these devices require complex and long tests. Moreover, averaging needs to be performed to guarantee the repeatability of the results. The high cost of the ATE can be mainly attributed to the expensive RF instrumentation in the mainframe and the pin electronics in the test head. The pin electronics refer to the sensitive electronic components in the test head of the ATE. The goal of the proposed work is to enable testability and to perform efficient testing of these devices on low-cost ATE platforms.

1.3 INTRODUCTION TO RF MODULES AND SYSTEMS

A few years back, RF test engineers used to perform tests on discrete RF devices such as mixers, low-noise amplifiers, power amplifiers (PAs), and RF switches. The emergence and advances in SoC technologies have enabled different RF devices/modules to be integrated into a single chip/package. A standalone RF transceiver system is used to perform the functionalities of both the transmission and the reception of the RF signals. Furthermore, the integration levels are such that the transceiver systems contain baseband (analog) functionality as well as digital functionality along with the RF functionality [1]. The block diagram of a typical direct conversion type RF transceiver SoC is shown in Figure 35.

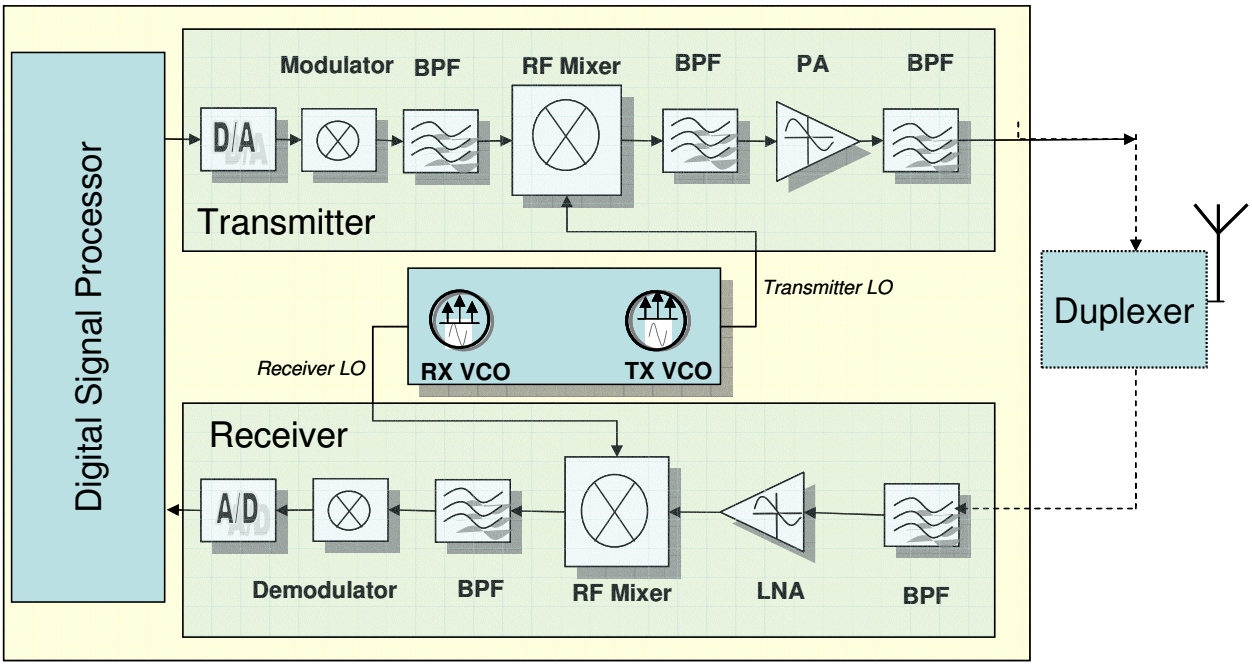


Figure 4. Block diagram of a typical direct conversion RF transceiver.

As shown in the Figure 4, the transceiver consists of a transmitter (TX) subsystem, a receiver (RX) subsystem, and a digital signal processor (DSP). The baseband/RF interface in the transmitter performs the desired modulation and the mixer is used to provide the required frequency conversion to the RF bandwidth. Carefully designed amplifiers and matching networks are employed to deliver the required power to the antenna. Suitable BPFs are used to attenuate undesirable signals at each stage. The low-noise amplifier (LNA) in the receiver amplifies the received signal with the addition of very little noise. The down-conversion mixer coverts the signal bandwidth from the RF ranges to a lower range that is within that of the baseband circuitry. The baseband/RF interface in the receiver is used to perform the desired demodulation. The analog-to-digital (A/D) converter and the digital-to-analog (D/A) are used to interface the DSP with the analog modules. The RF submodules that are integrated to form the transceiver system are described in detail below.

Low Noise Amplifier (LNA): The LNA in the receiver chain is used to provide amplification of the weak signals received by the antenna with the addition of very little noise. Since the LNA is the first gain stage of the receiver chain, its noise figure directly adds to that of the system [2]. Thus, the noise figure of the LNA is often the most critical parameter that is tested in production. Resources for typical LNA designs emphasizing techniques suited to integration in very large scale integration (VLSI) technologies can be found in [2][3].

Power Amplifier (PA): The PAs are used in the transmitter chain to boost the transmitted signal to a relatively high power for it to traverse long distances. PAs are typically the most power hungry blocks of the RF transceiver. The large gain requirements of the PA invariably produce large amounts of heat. Also, the PAs are in the 20-30% efficiency range and, thus, they drain the battery life significantly. In most applications, additional PAs (often called RF front-end or pre-

PAs) that are not part of the RF transceiver are used to provide additional gain to the transmitted signal. Since large amounts of heat are produced in these devices, they are often realized in specialized manufacturing processes like silicon germanium (SiGe) and gallium arsenide (GaAs), which are very different, form that of the other RF devices. The specifications of the PA commonly measured during production test include gain, second and third harmonics, power-added-efficiency (PAE), noise figure (NF) and stability factor (k). Additional resources for PA designs and considerations can be found in [2][3].

Mixer: A mixer is used in RF transceivers to provide upconversion or downconversion of the signal to be transmitted or received respectively. The operation of the mixer can be visualized as a multiplier circuit and is based upon its nonlinear performance as opposed to the other RF devices. The mixer is a three-port device whose individual ports are denoted as RF, intermediate frequency (IF), and local oscillator (LO). The LO port is used to provide the carrier signal (f_c) for upconversion/downconversion purposes. A block diagram of a mixer, with its ports highlighted, is shown in Figure 5. Typically single-ended or double-balanced or image-rejection mixer configurations are used based on the design requirements. Additional resources for mixer operation, performance and designs can be found in [2][3].

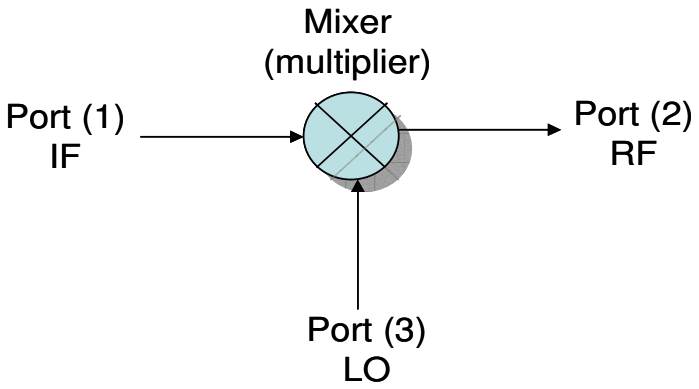


Figure 5. Block diagram of a mixer highlighting the individual ports.

Modulators: A modulator is a device that is used to encode the baseband digital data onto an output IF signal. The type of encoding or modulation is dependant on the wireless communication standard employed. Information on different types of modulation schemes can be found in [4]. A typical configuration of an IQ (I denotes in-phase and Q denotes quadrature-phase) type modulator is shown in Figure 5. It consists of two mixers, a phase splitter and a power combiner. The phase splitter creates a 90-degree phase shift between the signals that drive the LO port of the mixer. These signals are then combined with the baseband I and Q data from the DSP by the respective mixers to provide the modulated IF signal to the rest of the transmitter chain.

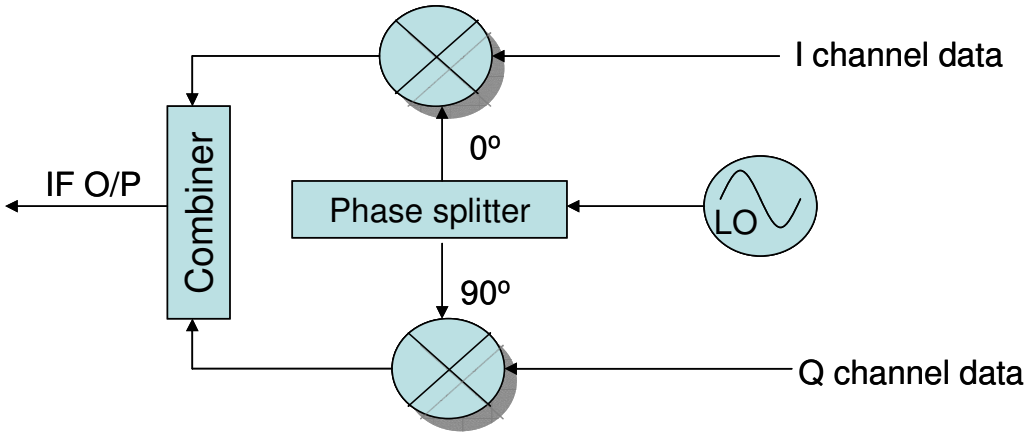


Figure 6. Block diagram of a typical IQ type modulator.

Demodulators: A demodulator is analogous to the modulator in terms of its operation. It does the exact reverse operation of the modulator to provide the baseband I and Q data from the IF signal. The IF signal is input from the downconversion mixer in the receiver chain and this signal is split using the power combiner/splitter to obtain the I and Q baseband data after the mixing operation with the respective LO signals. A block diagram of a typical IQ type demodulator is shown in Figure 7.

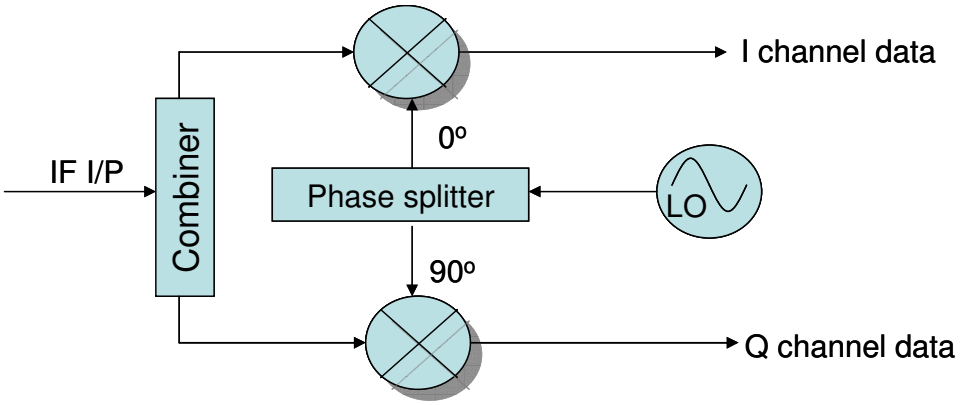


Figure 7. Block diagram of a typical IQ type demodulator.

1.4 COMMERCIALLY AVAILABLE RF SOLUTIONS

Solutions for wireless communication are currently available in a typical three-chipset configuration. The three chips include the baseband chip, the RF transceiver chip and the RF front-end chip. The baseband chip consists of the analog-to-digital converter (ADC), the digital-to-analog converter (DAC), and DSP functionalities. The transceiver chip typically contains highly integrated TX and RX chains in either the direct-conversion architecture or the super-heterodyne architecture. The front-end chip contains the PA that is normally used to boost the power level of the transmitted signal. These PAs produce power levels of the tune of 20 to 30 dBm, which causes heat dissipation and other reliability issues. Also, exotic technologies like GaAs and SiGe are used to fabricate these 'power-hungry' devices. Hence, a discrete or an isolated version of this module is normally preferred.

Block diagrams of two such commonly employed wireless solutions in the handset market [5] and the wireless LAN market [6] are shown in Figure 8 and Figure 9 respectively. It can be observed from both these figures that a direct-conversion radio (DCR) or zero-IF or homodyne transceiver is employed. In the DCR architecture, only one mixer stage is used to

convert the desired signal directly to and from the baseband without any IF stages and without the need for external filters. A block diagram of the DCR architecture [7] is shown in Figure 10. The advantages of this architecture is that fewer number of components are required in comparison to superheterodyne architectures and also all the RF blocks like the mixer, voltage controlled oscillator (VCO), LNA and baseband filters can be integrated onto one single die. Some of the common problems in these architectures include the DC offset, the LO pulling and the flicker noise [1][2].

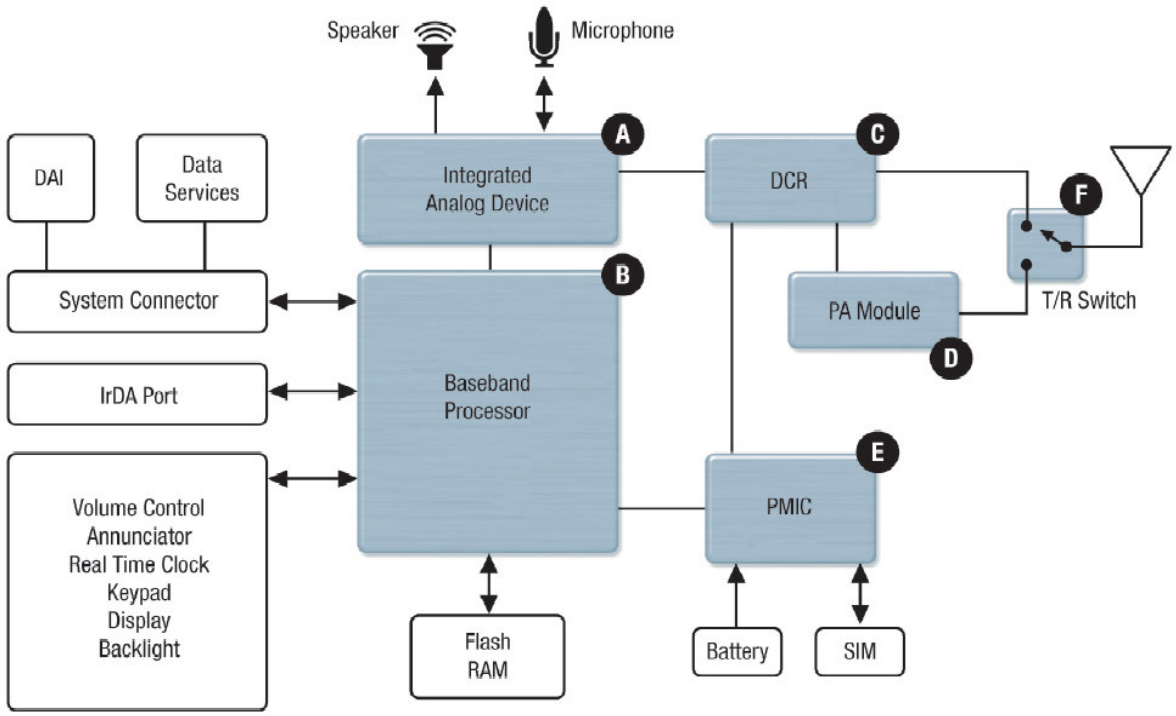


Figure 8. Block diagram of a typical GSM/GPRS system solution [5].

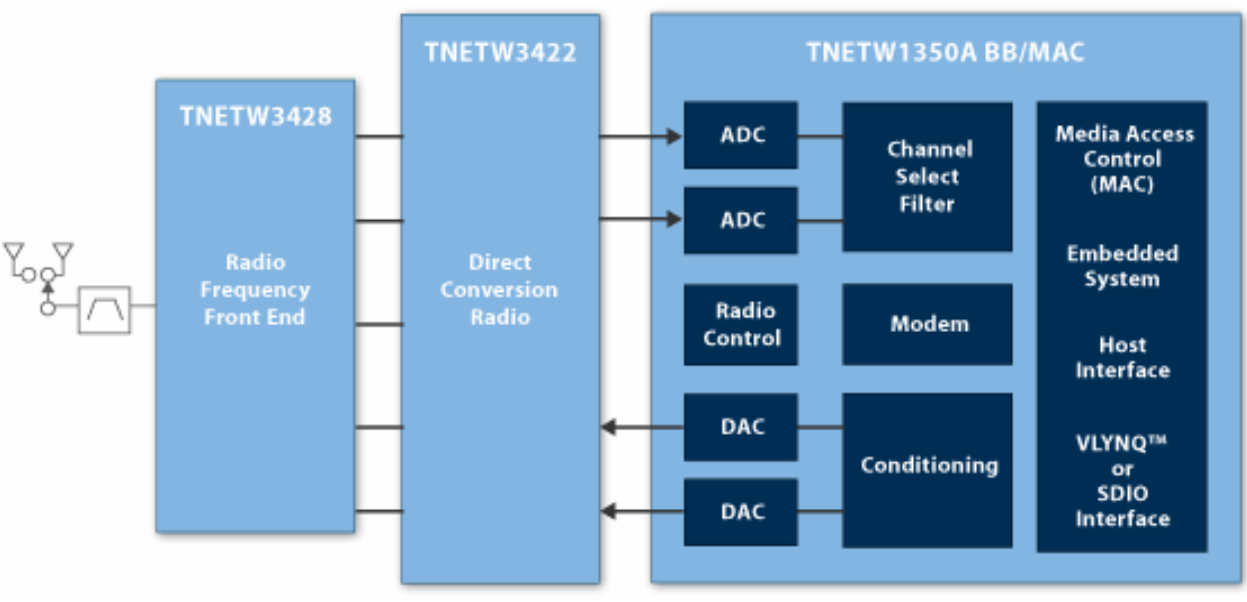


Figure 9. Block diagram of a WLAN 802.11 b/g system solution [6].

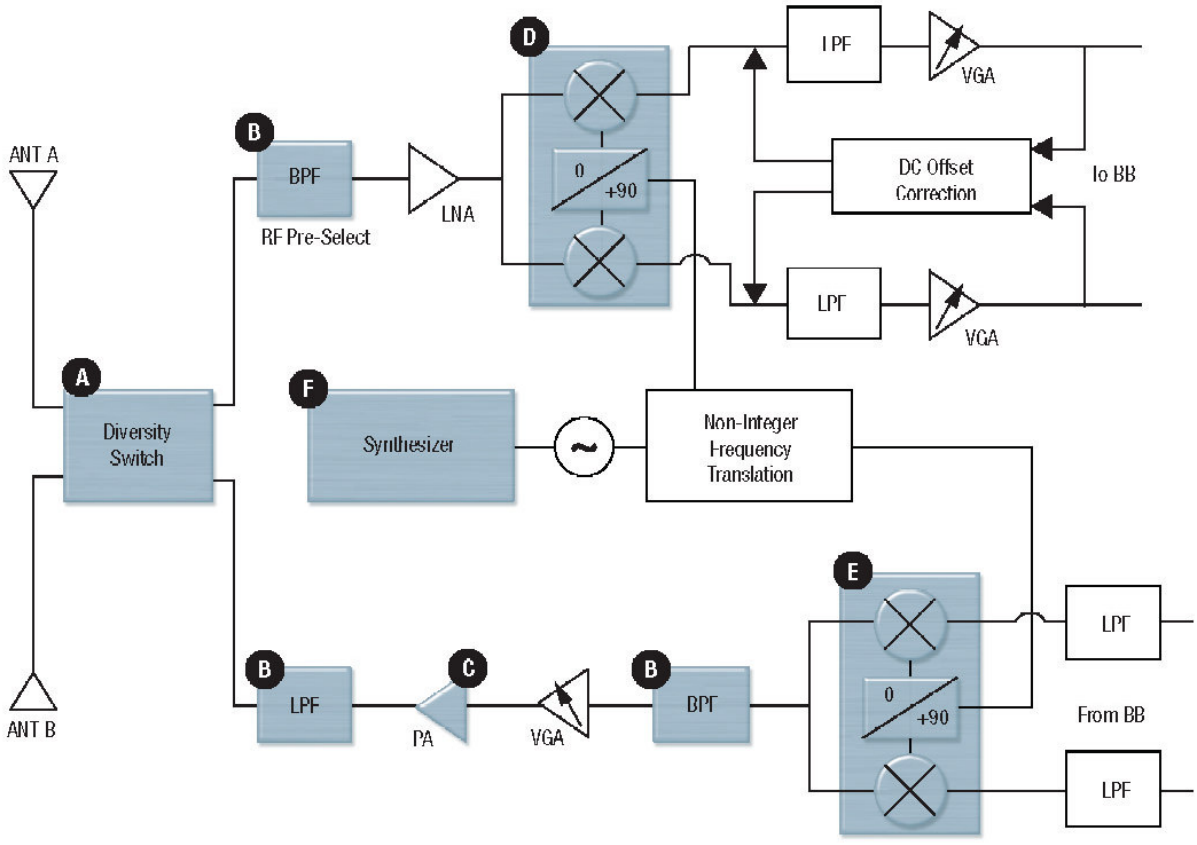


Figure 10. Block diagram of a DCR or zero-IF architecture [7].

The other commonly used configuration is the superheterodyne configuration which is considered as the classic radio architecture. A block diagram of the superheterodyne architecture [7] is shown in Figure 11. In this architecture, the received signal is down converted to baseband frequency in two stages. The incoming RF signal is first down converted to an IF frequency. This kind of architecture allows image suppression and channel selection by filtering out any unwanted signals [1][2]. This kind of architecture has two stages of downconversion and hence, it is generally more complex and expensive due to increased number of components.

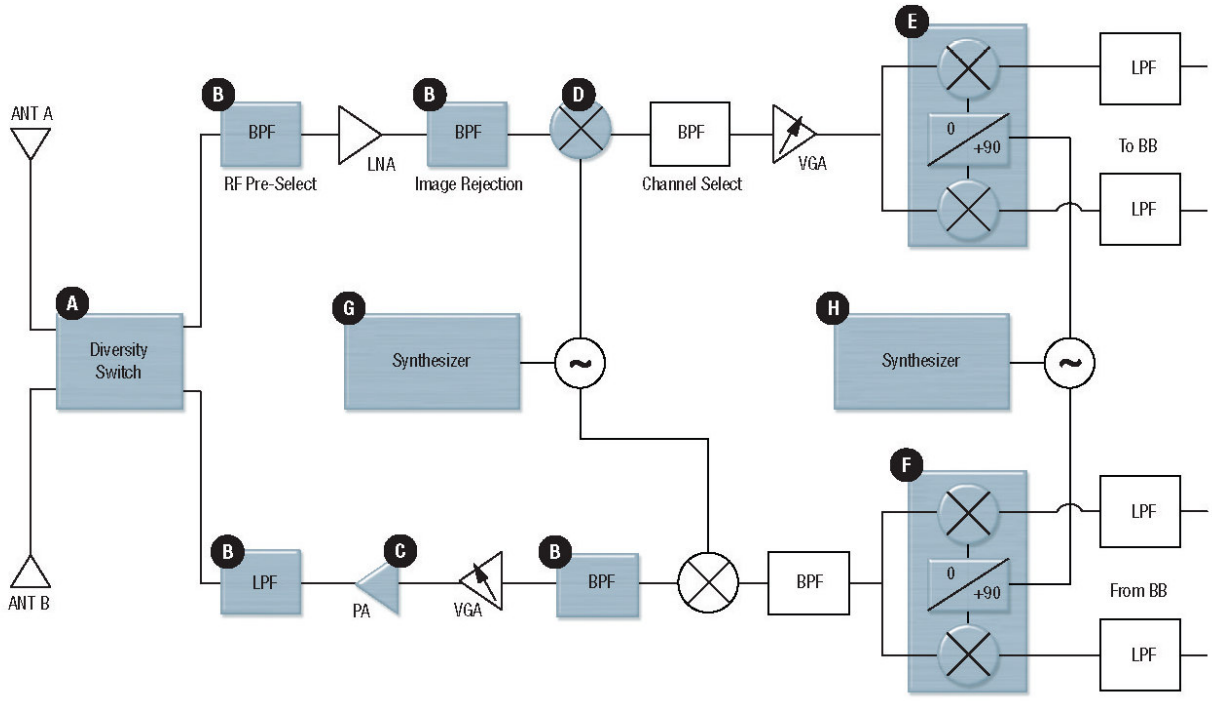


Figure 11. Block diagram of a super-heterodyne architecture [7].

1.5 RF TEST SPECIFICATIONS

Some of the standard specifications that are used to test RF devices/systems during high-volume tests are the gain, the 1-dB compression point (P1dB), the harmonic distortion, the third-order input intercept point (IIP3), the adjacent channel power ratio (ACPR), the NF and the error vector magnitude (EVM). Most of the specifications involve power measurements at the input and output pins of a DUT and its harmonic components. These specifications in general characterize the performance of a RF device/system and hence, are considered critical from the test perspective.

1.5.1 Gain specification

Traditionally, gain measurements for standalone RF devices involved power measurements at the input and at the output pin of the device. However, gain specification measurement has become more complex with the advent of wireless SoC devices. The complexity arises from the power-level requirements and frequency translations that take place inside the system.

In the case of an RF transceiver SoC (block diagram shown in Figure 12), the power measurements are made separately for the receiver and transmitter paths and the gain specification of these paths are computed as

$$G_{receiver} = P_{out|baseband} - P_{in|RF} \qquad \textbf{Equation 2}$$

$$G_{transmitter} = P_{out|RF} - P_{in|baseband} \qquad \textbf{Equation 3}$$

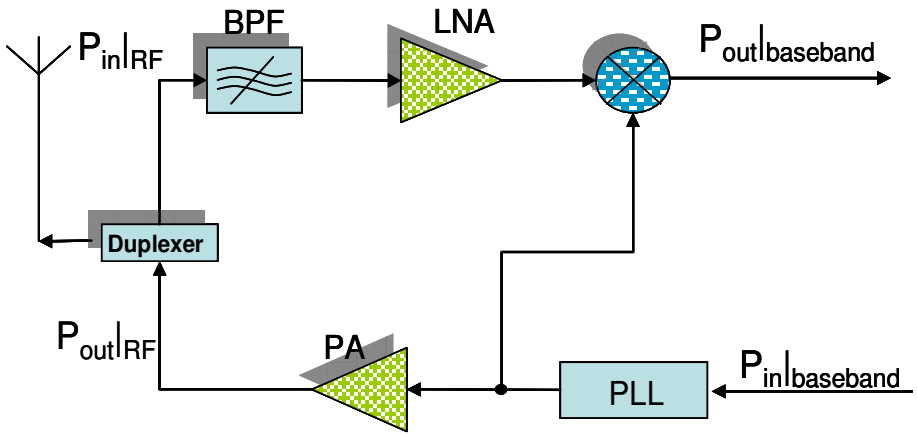


Figure 12. Block diagram of a RF transceiver SoC highlighting the baseband and RF access points for gain specification measurement.

In each of these cases, the output power at the appropriate node corresponding to the input test tone is measured. It should be noted that in the cases where the test system does not have the ability to measure the input power, it is assumed that the DUT consumes the requested input power. However, this assumption is based on the power-level calibration and performance of the loadboard impedance matching circuitry.

1.5.2 1 dB compression point (P1dB)

The 1 dB compression point is another common RF specification that characterizes the performance of an RF device. P1dB limits the upper bound of the dynamic range of the system and hence needs to be measured in an accurate manner. Ideally, the output power of a system tracks the input power supplied to the system. However, beyond a particular input power, the output power does not track the input linearly. This is because the device is driven into compression. P1dB is defined as the input power at which the output power of a system is 1 dB below its ideal value. This phenomenon is pictorially presented in Figure 13.

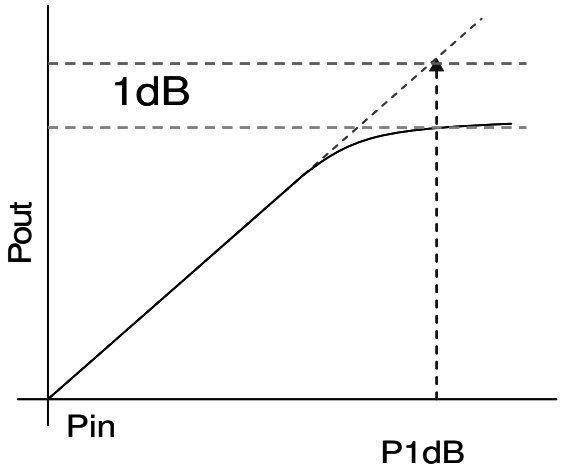


Figure 13. Pictorial presentation of the 1 dB gain compression behavior of RF devices/systems.

A detailed testing mechanism for this specification is to sweep the input power in finite steps comparing at each step against the extrapolation of the gain in the linear region of the DUT. The complexity for such a test is decided based on the test quality requirements of the semiconductor manufactures.

1.5.3 Harmonic distortion

Harmonic distortions usually occur when some of the output power from the device/system is transferred to the harmonic frequencies of the desired fundamental frequency. RF ICs are specifically prone to such distortions at high power levels of operation. Total harmonic distortion (THD) is a measure of the harmonic distortion that involves measuring the power levels at the first seven harmonic components of the fundamental signal. The sum of all these powers divided by the power at the fundamental frequency is commonly referred to as the THD of the device/system. These measurements are usually made with a single sinusoidal input tone. This specification quantifies how efficiently the device conserves the energy at the

fundamental signal frequency (S) in comparison to the distortion components (D) due to the nonlinear performance. It is expressed in dBc as shown in Equation 4.

$$\text{THD (dBc)} = 10 \log_{10}\left(\frac{D}{S}\right) \qquad \textbf{Equation 4}$$

In cases like wireless local area network (WLAN) solutions, the fundamental is at 5.6 GHz, which poses challenges towards the measurements of even the second and third-order harmonic components.

1.5.4 Third-order input intercept point (IIP3)

The nonlinearity of the RF devices/systems is further characterized by the intermodulation characteristics of the device. IIP3 describes the effect of the third-order harmonics on the RF device/system performance. It is defined as the input power at which the third-order harmonic power is equal to the fundamental output power of an RF device/system. This is pictorially described in Figure 14. Conventionally, a two-tone input (f_1 & f_2) with a small frequency deviation is provided as the input stimulus to the RF DUT. The spectral response of the nonlinear DUT to this stimulus in shown in Figure 15.

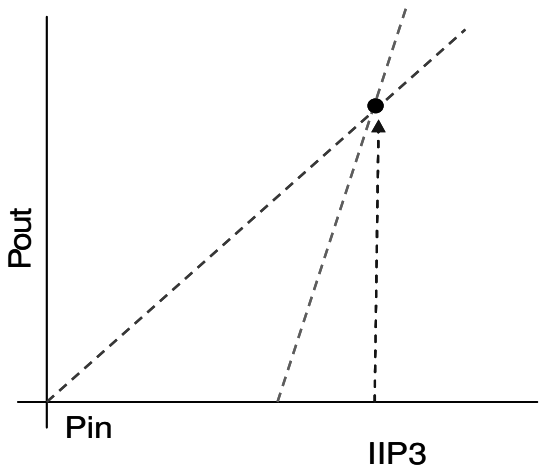


Figure 14. Pictorial representation of the IIP3 performance of an RF device/system.

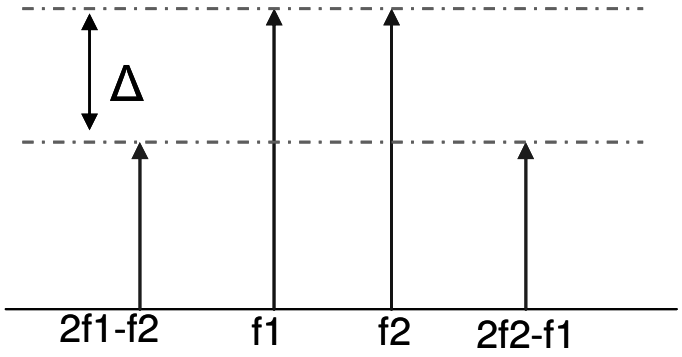


Figure 15. Frequency spectrum of a response of a typical nonlinear device to a two-tone input stimulus.

The difference (Δ) in the amplitude values between the f_1 or f_2 tones and the $2f_1$-f_2 or $2f_2$-f_1 tones is defined as the third-order intercept (TOI) of the system. From the TOI value, the IIP3 specification is then calculated as follows.

$$\text{IIP } 3 = \frac{\Delta}{2} + P_{in} \qquad \textbf{Equation 5}$$

1.5.5 Adjacent channel power ratio (ACPR)

ACPR is defined as the ratio of the average power in the adjacent frequency channel to the average power in the transmitted frequency channel as depicted in Figure 16. ACPR is an important figure-of-merit for transmitters employed in CDMA applications due to the complex nature of the modulation scheme employed. In CDMA transmitters, the data is assigned a unique pseudo noise signal and is coded along the entire spectrum. Hence it becomes imperative to characterize the ACPR of such a spread-spectrum technology.

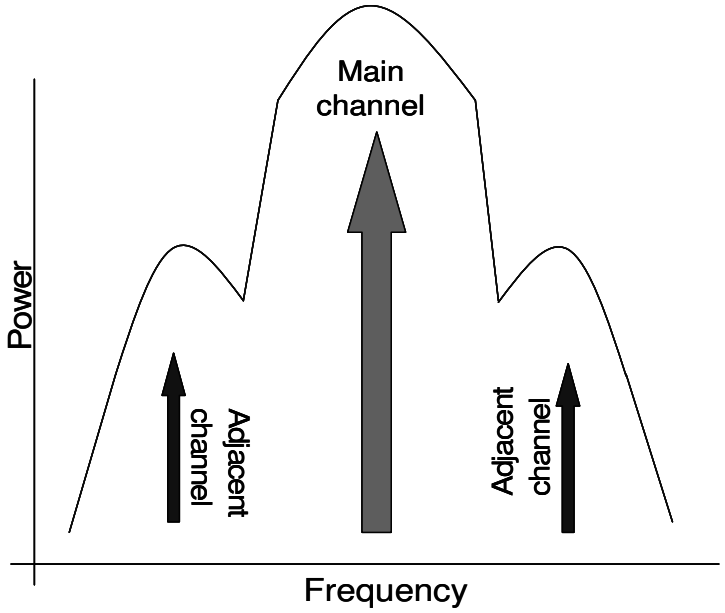


Figure 16. Block diagram of a super-heterodyne architecture.

Standard test procedures for ACPR measurement in the industry employ a pseudo-random bitstream as the test stimulus. Consequently, the output power from the receiver is spread over a large number of FFT 'bins', where each 'bin' corresponds to a small range of frequencies. For ACPR measurement, it is required that the discrete amplitudes of all the frequency components in the main and adjacent channels be measured, and the ratio be calculated. Due to the large number of output bins in the case of pseudo-random bitstreams, this computation is time consuming [8]. In addition, a lot of time is required to perform averaging in case of lower energy frequency components, which are close to the noise floor. It should be noted that the test system should have a wide-enough bandwidth and a large-enough dynamic range to make these measurements without multiple captures. Additional captures often adds to the test complexity and incurs additional test cost and time.

1.5.6 Error vector magnitude (EVM)

The EVM specification is used to characterize the correct operation of a RF receiver chain. During this test, a modulated time domain signal is used to drive the DUT, and the corresponding response is captured and plotted in the I/Q format as shown in Figure 17. This plot is then compared with a reference signal to compute the error vector. The ratio of the magnitude vector to the reference vector expressed in the percentage form is referred to as the EVM.

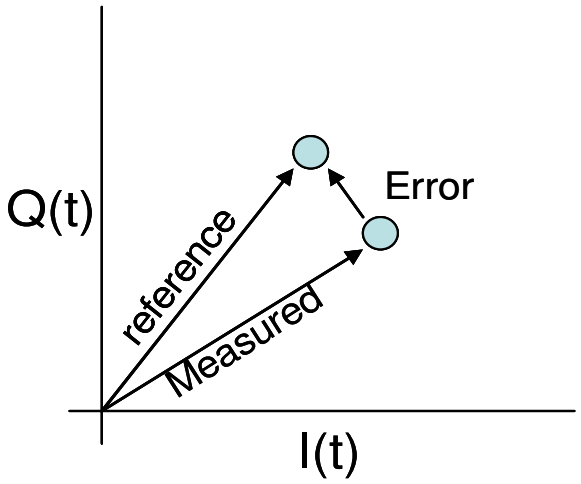


Figure 17. Typical I/Q plot used to compute the EVM specification.

EVM is a common figure-of-merit for the receiver chain and is quite a challenging test because the test system needs to make measurements in the time domain. Further, adding complexity is the fact that the reference signal estimation is very critical to avoid inducing any measurement error. Even though the EVM measurements are correlated to measurements from other traditional tests that quantify a DUT, the test complexity and time required to do such measurements create bottlenecks to the test community.

1.6 CONVENTIONAL APPROACH FOR PRODUCTION TEST

The production test community follows a sequential approach to test for each specification of the device, as shown in Figure 18. Each test configuration involves the hardware setup, the application of the test stimulus, the settling time of the DUT, and the specification measurement time. Also, the entire process requires switching (using relays) among different setups during the testing process, which increases the total test time. The production test cost of current generation RF modules and SoC devices has been consistently increasing over the last few years and is estimated to be about 40% of the total manufacturing cost. The increase in cost can be attributed to some/all of the RF test challenges listed below.

1.7 ANALOG/RF TEST CHALLENGES

- ***Expensive ATE requirements*:** Conventional testing methodologies use expensive ATE that could cost a few million dollars. This cost can be mainly attributed to the expensive nature of the RF spectrum analyzers, the modulated signal generators, and the modulated vector network analyzers (MVNA) that are required to perform complex RF specifications tests.
- ***Increasing complexity:*** The complex integration of many components on a single chip calls for elaborate specification tests on expensive test equipment. Also, in certain cases the current generation devices exceed performance of the ATE.
- ***Growing test development and production test times*:** The test development and application times increase with the number of complex specifications to be verified and the required precision.

- ***Signal integrity requirements:*** Accurate RF testing calls for clean socket-to-board-to-tester signal path (50 ohm), good electromagnetic isolation, and noise immunity.
- ***De-embedding:*** Loss due to mechanical/electrical components on loadboard needs to be carefully de-embedded from the test measurements to guarantee test quality.

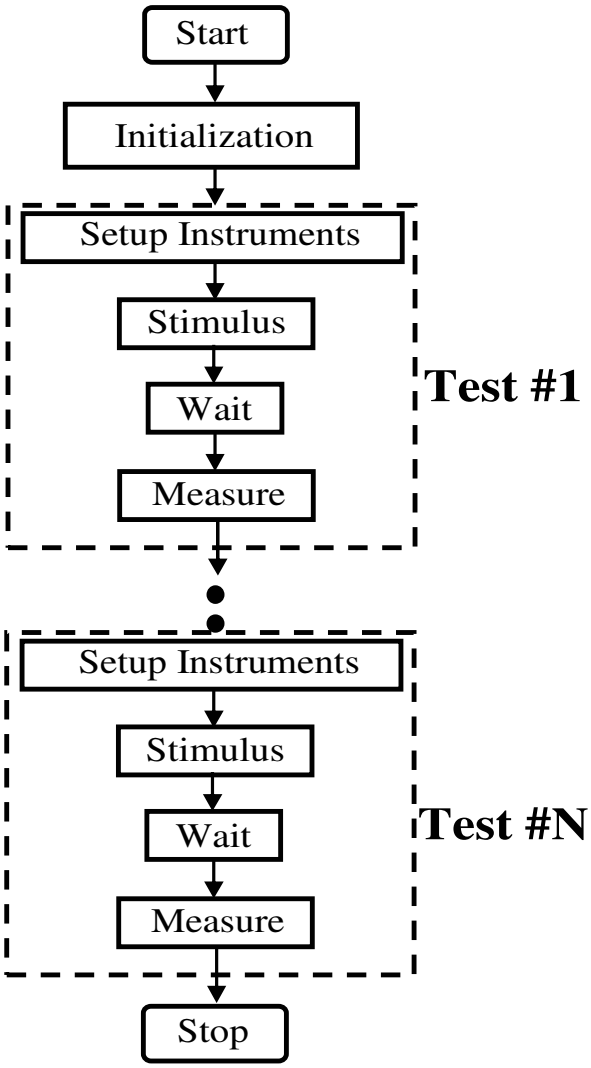


Figure 18. Sequential test method followed during standard specification test.

1.8 PREVIOUS RESEARCH EFFORTS TO LOWER TEST COST OF ANALOG/RF CIRCUITS

Significant research has been done in the field of digital testing to lower the test cost of complex devices. Research in the area of analog/RF circuits is quite primitive when compared to their digital counterparts. Previously developed approaches in the analog/RF test area can be broadly classified into four research areas. Each of these areas is briefly discussed below:

Built-In-Self-Test (BIST): BIST allows the DUT to evaluate its own quality without elaborate ATE support. In this approach, suitable test circuitry embedded in the chip is used to source and analyze test signals. The BIST circuitry generates a pass/fail decision based on the analysis. Analog/RF BIST technology has constantly lagged behind digital BIST [9][10] because of the difficulties involved in generating accurate on-chip test signals. Also, the BIST circuitry suffers from similar process variations as the DUT itself. Thus, calibrating these BIST circuits might become critical. Moreover, these approaches cannot be applied to test complex RF systems because of the limited test access problems that arise from high levels of integration and advanced packaging techniques.

Design-for-Testability (DfT): DfT techniques are design efforts employed within the DUT to improve their testability. A variety of well-defined DfT software tools that drive digital circuits to testable designs are currently available in the market [11][12][13][14]. Analog/RF DfT is less standardized since the failure mechanisms of these circuits are not well understood and these circuits have more severe testing requirements. Also, the digital circuits can be separated into sub-circuits using a divide-and-conquer approach. These approaches do not guarantee the specifications of analog/RF circuits, as they are more prone to crosstalk problems and other interactions between circuit blocks.

Defect-Oriented-Testing (DOT): This is a test cost reduction methodology that is based on the assumption that some or all of the circuit's major failure mechanisms can be understood through mathematical analysis and related to a reduced set of measured parameters. The DOT involves an analysis of failure mechanisms through the simulation and/or collection of empirical data to build the required fault models. These models are used to predict failures that would normally require lengthy, expensive tests. The Iddq test is one type of DOT that efficiently tests for undesirable current leakage in the presence of faults. Many Iddq test methodologies have been developed in the past for digital systems [15][16][17]. While tests like Iddq remain common to digital systems, there is little application of this concept to RF circuits [18].

Alternate test: In [19] and [20], an alternate test framework that generates transient tests for computing the specifications of analog circuits is presented. An optimized transient test signal is applied to the DUT and the transient response of the circuit is sampled and analyzed to compute all the circuit's specifications. The test time of these devices is reduced by replacing the conventional specification tests, either fully or partially, with shorter, easy-to-perform tests. Alternate tests also ensure that there is no loss in terms of yield or fault coverage. The key highlights of alternate tests are as follows:

- **Test compaction:** Most of the specifications of the DUT are computed from a single transient measurement. This reduces the overall test time of the DUT.
- **Simplified loadboard design:** Since a single test is used to test all the specifications, the need for different hardware setups on the loadboard for each test in the sequential approach is reduced.

- **Parallel test capability:** Because of the relaxation in hardware requirements on the loadboard, the available real estate on the board increases. This enables the simultaneous testing of multiple devices, provided the test resources are available.

In this work, the alternate test framework that was previously applied to analog circuits is used to generate a specification-oriented test methodology for RF modules and systems using low-cost The fundamentals of the alternate test framework are explained in the next section.

1.9 ALTERNATE TEST FRAMEWORK

As described in [19][20][21][22], any variation of process or circuit parameters, such as width of a FET, the value of a resistor, etc., in the process or circuit parameter space P affects the circuit specification S by a specific sensitivity factor. The variation in these parameters also affects the measurement data in the measurement space M (for example, the DUT's transient current response or the DUT's output spectrum) of the circuit by a corresponding sensitivity factor. Figure 19 illustrates the effect of the variation of one such parameter in P on the specification S and the corresponding variation of a particular measurement data in M. For any point p in the parameter space P, a mapping function onto the specification space S, f: P→S can be computed. Similarly, for the same point p in P, another nonlinear mapping function onto the measurement space in M, f: P→M can be computed. Therefore, for a region of acceptance in the circuit specification space S, there exists a corresponding allowable region of variation of the parameters in the parameter space P. This in turn defines a region of acceptance of the measurement data in the space M. A circuit can be declared faulty if the measurement data lies outside the acceptance region in M. Alternatively, the mapping function f: M→S could be constructed for the circuit specifications S from all measurements in the measurement space M

using nonlinear statistical multi-variate regression. Given the existence of the regression model for S, an unknown specification of a system-under-test can be predicted using the measured data.

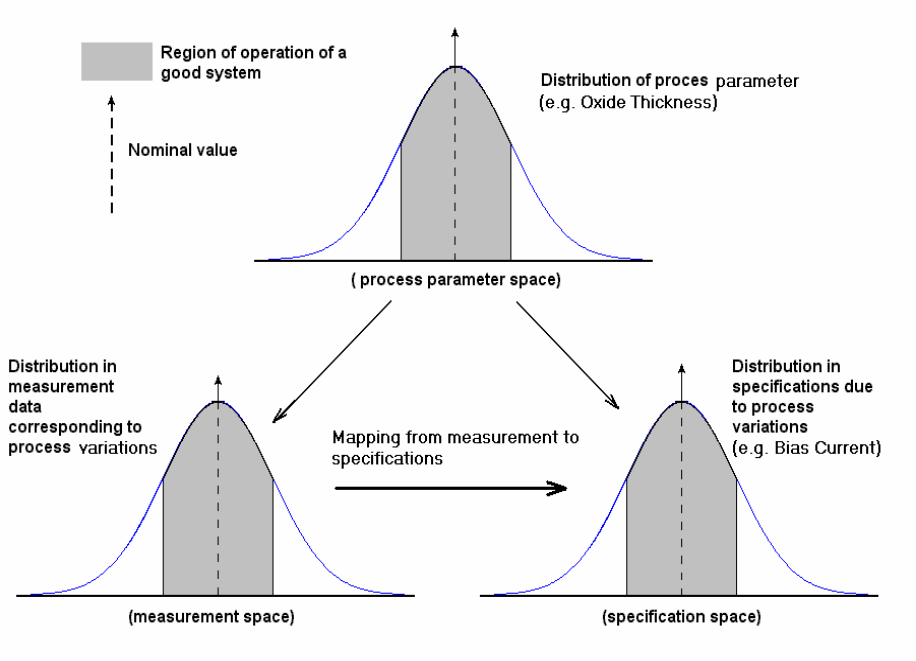


Figure 19. Effect of process/circuit parameter variation.

Alternate tests use this paradigm to compute the specifications of the DUT from the response measurements using nonlinear regression functions. The test stimulus applied to the DUT is optimized to reduce the specification computation error. To generate the nonlinear regression function, a set of training DUTs is chosen from different production lots. The test stimulus is applied to each of these DUTs and their resulting test responses are sampled and stored. Simultaneously, the output specifications of these devices are measured using the conventional specification test setup. The sampled transient measurements are mapped onto the specifications of the device using nonlinear regression functions. During production testing, the measured response of the DUT is mapped onto the specifications using these functions. A flow diagram of the alternate test procedure is shown in Figure 20.

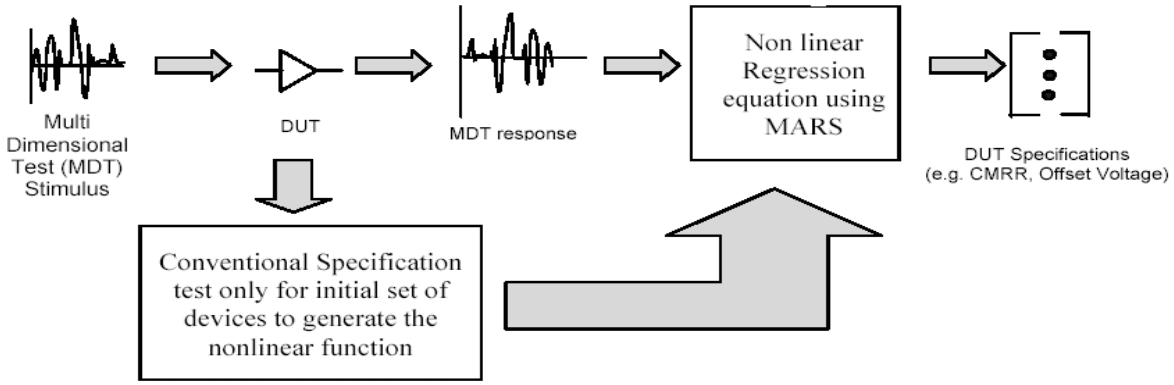


Figure 20. Alternate test flow.

1.10 SUMMARY OF CONTRIBUTION OF THIS THESIS

In this thesis, a framework for efficient production testing of high-performance RF modules and systems using low-cost ATE is presented. This framework uses low-speed, low-resolution test resources to generate reliable tests for complex RF systems. Also, the performance of the test resources will be evaluated and improved ahead of high-volume tests to improve the test yield and throughput. The main components of the developed framework are as follows:

(1) **Genetic ATPG:** A genetic algorithm (GA) based automatic test pattern generator (ATPG) for spectral signature-based alternate testing of RF systems. The generated 'test stimuli' is optimized for the RF system along with the low-resolution test resources of typical low-cost ATE platforms used to process the test signals.

(2) **Concurrent alternate test methodology:** A methodology for efficient production testing of high-frequency specifications of RF modules and systems using low-frequency transient current and/or spectral signatures. Suitable on-chip and/or off-chip design-for-

test (DfT) resources are used to source and enable capture of test signals using low-cost ATE resources.

(3) **Loadboard checker:** A checker tool to accurately characterize/diagnose the DfT circuitry on RF loadboards used to enable test on low-cost ATE platforms. This tool will provide significant improvement in the overall test yield and throughput of RF tests during high-volume production testing.

(4) **Advanced test signal processing algorithms**: The performance of the low-cost ATE resources, in terms of their linearity/resolution, will be evaluated and improved ahead of the high-volume tests to enable accurate capture of test response signals.

The proposed concurrent alternate test methodology eliminates the need for expensive ATE, due to its ease in implementation on low-cost ATE. Also, DC probes integrated to low-cost ATE platforms could be used to monitor the current and spectral features in order to perform pre-packaged wafer-level tests for pass/fail distinction of individual dies. Addition of wafer-level tests helps to reduce the overall packaging cost of complex RF systems and improve the yield of the overall manufacturing test process. The proposed method also attempts to solve the limited test access problem associated with integrated RF systems. The genetic ATPG algorithm is proposed to generate reliable tests using the low-cost, low-resolution test resources. Also, the test stimulus is optimized to compute multiple performance specifications from a single test response capture (test compaction), which in turn reduces the overall test time. The loadboard diagnostic tool is proposed to periodically characterize/diagnose the DfT paths on the loadboard, to maintain a high precision in the developed RF tests. The framework also proposes an approach to evaluate and improve the range of possible dynamic measurements by the test resources. This

would enable use of low-cost ATE to accurately capture the system response signals for specification computation purposes.

The rest of this thesis is organized as follows. Chapter 2 presents a current signature-based alternate test methodology for efficient specification prediction of RF devices. Chapter 3 presents a spectral signature-based test methodology along with a genetic ATPG algorithm to provide optimized digital bitstreams to test RF front-end/transceiver architectures. Chapter 4 couples the capabilities of both the current and spectral signatures to form a concurrent test methodology for an increased accuracy in specification computation. Also in Chapter 4, a loopback DfT approach that can be coupled with the concurrent test methodology for low-cost wafer-level test of VCO modulating RF transceivers is presented. Chapter 5 presents the developed checker tool used to characterize/diagnose the RF paths in the DfT resources used to enable the proposed test methodologies. Chapter 6 and Chapter 7 present the advanced test signal processing algorithms developed to evaluate and improve the performance of low-cost ATEs, in terms of linearity/resolution ahead of the high-volume tests.

Chapter 2

EFFICIENT SPECIFICATION TESTING OF RADIO FREQUENCY DEVICES USING TRANSIENT CURRENT SIGNATURES

In this section, a test methodology for the fast and accurate testing of RF devices using their transient current response/signature to a time-varying control voltage stimulus is presented. The proposed methodology does not require complex RF instrumentation and hence it can be easily implemented on low-cost ATE. This test methodology is mainly applicable to RF PAs in the front-end chips and to some extent can be also applied to the TX and RX subsystems in RF transceiver.

RF devices like the PA used in time-domain multiple-access (TDMA) applications are operated in different modes (on and low-power). Normally, a control voltage terminal is provided in these devices to switch between modes. Here, control voltage refers to the input voltage provided to the bias circuit of the device. This voltage prevents the device from drawing excessive current, especially in the low-power mode. During production testing, all the specifications of the PA are measured at each of these control voltage values to ensure device performance [28][29]. Certainly, it is time consuming to measure all the specifications at each of these voltage values. In the proposed methodology, the transient current signature of the DUT is used to compute all the specifications of the device at different voltage levels using a single (compact) transient current test.

As shown in Figure 21, the output power of an RF device is proportional to the square of the control voltage applied to the bias circuit. Providing an optimized transient voltage stimulus

that discretely ramps the control voltage to the DUT drives the transistors in the DUT through different regions of operation (sub-threshold, linear, and nonlinear). This causes the process variations in the DUT to alter the transient current signature in a particular manner. The same process variations also affect the specifications in a similar manner. The plots of variations in the transient current signature and specification value for variations in the various circuit components obtained from an RF PA are shown in Figure 22. These plots illustrate the relationship for a single component variation only. Because the goal of this experiment is to validate the use of transient current measurements as the measurement space for the alternate test framework, only a single parameter variation is considered. In Section 6, the current measurement space has been validated for multiple parameter variations on a TDMA PA DUT. The variation in the transient current (left) and magnitude of the gain (right) of the DUT for the corresponding variation in the load impedance is illustrated in Figure 22 (a). From Figure 22 (a), it can be observed that the parameter variation affects the measurement space 'M' and the specification space 'S' in a similar manner. Similar plots for variation in parameters like supply voltage and inter-stage matching impedance are shown in Figure 22 (b) and Figure 22 (c), respectively.

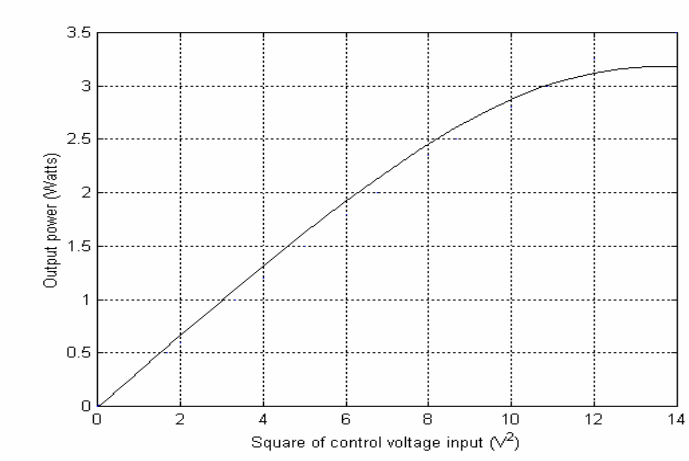


Figure 21. General transfer function of a PA.

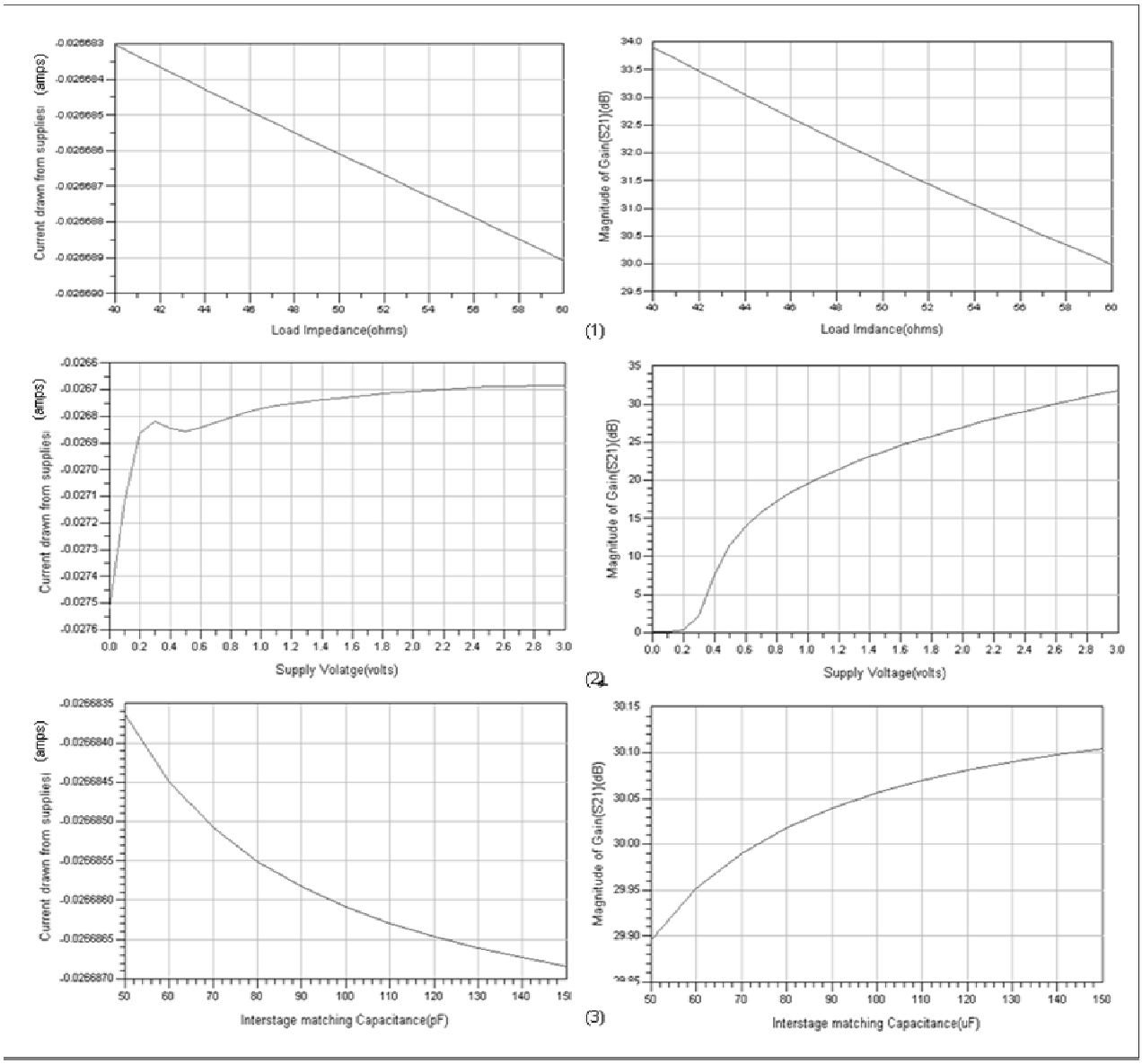


Figure 22. Variations in the transient current and specification for variations in (a) Load impedance, (b) Supply voltage, and (c) Inter-stage matching capacitance.

Since the variations affect the measurement and the specifications in a similar manner, statistical regression equations are computed to map the signature of the DUT to the corresponding specifications over a training set. Hence, from subsequent signature measurements, all the specifications can be computed in a fast and accurate manner. The proposed methodology has been validated through the simulation of a PA designed for TDMA

applications. Simulation results show that the specifications of the DUT can be computed within an error of +/- 5%. Also, a test time reduction of more than a factor of three could be achieved. The proposed approach can specifically benefit the production testing of multi-band devices, as a single transient current measurement can be used to compute all the specifications of the device in each mode of operation.

In the past, several Iddq and Iddt test methodologies were developed for the specification and wafer-level testing of digital circuits [15][17]. In [18], the authors propose the use of the transient current signature for fault-detection purposes in the wafer-level testing of RF circuits. This approach is suited only for defect-based testing and not for specification testing, in which the manufacturer determines whether the device passes the specification compliance tests to meet customer demands.

2.1 PROPOSED TEST METHODOLOGY

In this section, the methodology used to reduce the test time of RF devices is presented. The proposed methodology has three major components: (1) the transient test stimulus generation algorithm, (2) the transient current monitoring technique, and (3) the methodology used for computing the specifications from the transient current measurements.

2.1.1 Test Stimulus Generation

As explained earlier, the production test procedure of the PA is time consuming because of the different control voltage values involved. To reduce the test time of these devices, a simple test signal to replace all the control voltage signals of different amplitudes will be required. This signal should be capable of measuring all the test specifications at the different amplitude levels

of the control voltage. To achieve these requirements, a time-varying ramp signal whose amplitude ranges from low to high values of the control voltage defined in the conventional test plan is used. A conceptual flow diagram of the optimization engine is shown in Figure 23.

The parameters of this ramp signal are optimized for the measurement capabilities of the ATE and the circuit parameters of the device. The high and low control voltage values of the conventional test approach determine the voltage step size of the ramp. The optimization of the test stimulus is done for a set of training devices chosen from different production lots. Since the statistics of the process parameters change from one lot to another, it becomes necessary to optimize the test stimulus across different lots.

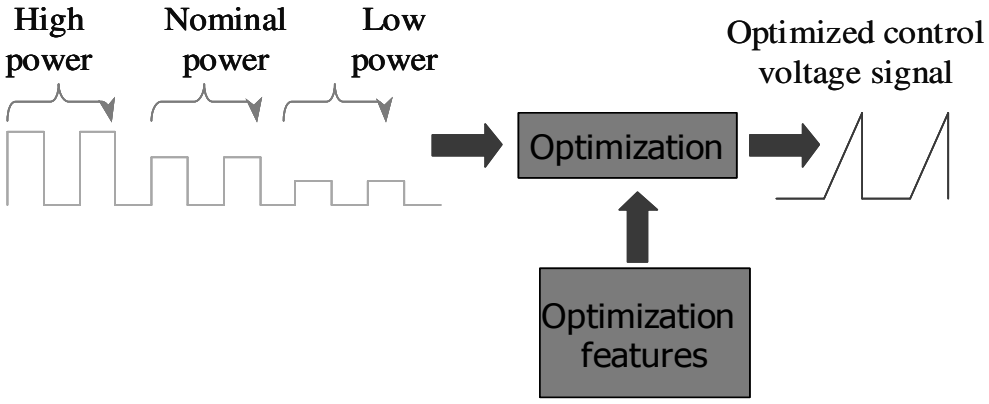


Figure 23. Optimization engine for ramp generation.

The optimization algorithm for determining the time step of the ramp is shown below. The inputs to the algorithm are (1) the number of devices in the training set (N) and (2) the digitizer speed (D_t) of the low-cost ATE in seconds.

```
for i=1:N
        T_i=settling time of i-th device in seconds
        if i=1
                T_max=T_i
        elseif T_i>T_max
                T_max=T_i
        end
end
R_s=max (T_max, D_t)
```

Based on the above-obtained ramp speed, the test stimulus is generated as shown in Figure 24. An offset time period is included to synchronize the digitizer and the source of the ATE. The voltage of the ramp is varied from the low to high control voltage amplitudes in equal increments at each time step of the ramp (maximum ramp speed). A practical non-zero ramp fall time is used to return to the low control voltage amplitude level. Also, the '3GPP standard' [30] specifies the maximum rise time of the control voltage of the PA used for TDMA communications. This has to be taken into consideration for developing ramp signals for production testing purposes.

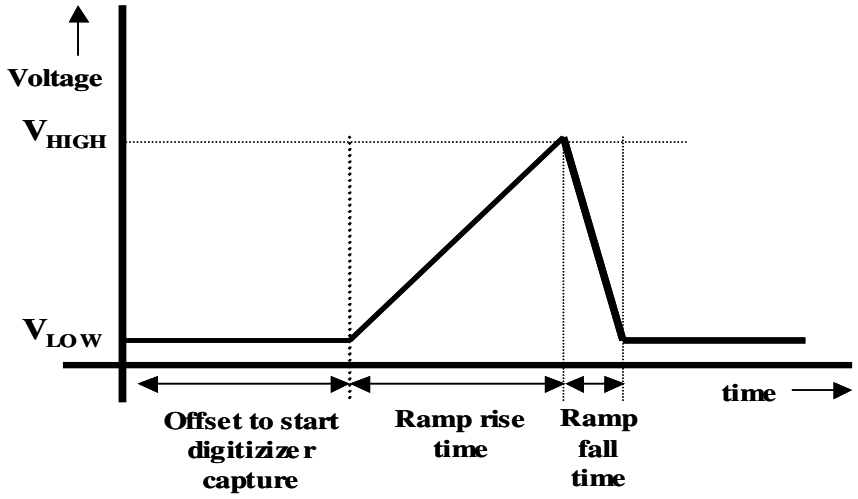


Figure 24. Transient ramp stimulus.

Piecewise linear test stimulus generation algorithms for fast transient testing as in [22] [31] can also be used for optimization purposes. The purpose of a cost function for such a test-generation procedure would be to lower the computation error of the specifications from the observed test signature. Since the proposed methodology resulted in little loss in test accuracy (<5%) during validation, a simple test stimulus like the ramp signal is used for this work.

2.1.2 Transient current behavior of DUT

The general transfer function of a PA, as shown in Figure 21, indicates that the output power is linearly proportional to the square of the control voltage of the bias circuit. The ramp signal applied to the control voltage terminal controls the output power of the PA in a linear fashion. For any given PA, the voltage gain produced in each stage is proportional to the current drawn from the power supply. Hence, the current drawn by each stage from the power supply changes with the applied transient control voltage signal. To demonstrate this, the transient current behavior of a typical bias circuit used in PAs is presented in the next subsection. The schematic of this bias circuit is shown in Figure 25. A short description of the bias circuit is presented before the discussion on its transient current behavior.

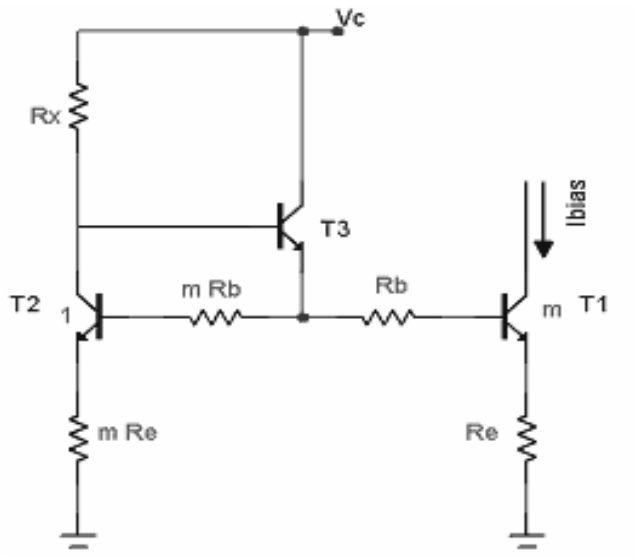


Figure 25 Schematic of bias circuit used

2.1.3 Bias circuit description

In this circuit, the biasing is provided by the current mirror principle. This circuit is a modification of the simple two transistor current mirror (T_1 and T_2), which takes into account the β helper (finite β of the BJT) provided by transistor T_3. The transistor T_1 refers to the transistor in the amplifier gain stage. The circuit differs slightly from the normal β helper circuit in the presence of the resistor R_b. This resistance is necessary to prevent grounding of the base of the BJT. For close matching requirements, a resistance must be connected to the base of the transistor T_2. Also, the ratio of the resistance must be equal to the ideal current ratio in the current mirror (i.e. the area ratio of the transistors T_1 and T_2) [33]. In Figure 25, "m" refers to the multiplication factor of the BJT device. The ballast resistor R_e is used in the emitter of the amplifier stage to exclude thermal runaway condition. To account for the ballast resistor R_e in the emitter of the transistor T_1, the emitter degeneration in the transistor T_2 is performed. I_{bias} for this circuit is given by,

$$I_{bias} = \frac{V_c - V_{be1} - V_{be3}}{\frac{R_x}{m}(1 + \frac{m+1}{\beta(1+\beta)}) + \frac{R_e}{\alpha} + \frac{R_b}{\beta}}$$ **Equation 6**

From Equation 1, it is clear that I_{bias} (the current in the collector of the amplifier stage) is linearly proportional to the bias circuit control voltage V_c. Hence a linear change in the bias circuit control voltage causes almost a linear change in the amplifier stage collector current. To show this linear relationship, an optimized ramp signal was applied at the input of the control voltage terminal of the bias circuit and the response of the circuit was observed. The waveforms of the transient voltage and current are shown in Figure 26. From these waveforms, it is clear that the control voltage can control the current drawn from the power supply, which in turn controls the output power of the DUT. For TDMA applications, the specifications are defined for different operating modes of this circuit. Because the control voltage of the circuit controls the switching between different operating modes, there arises the need to test at different control voltage values.

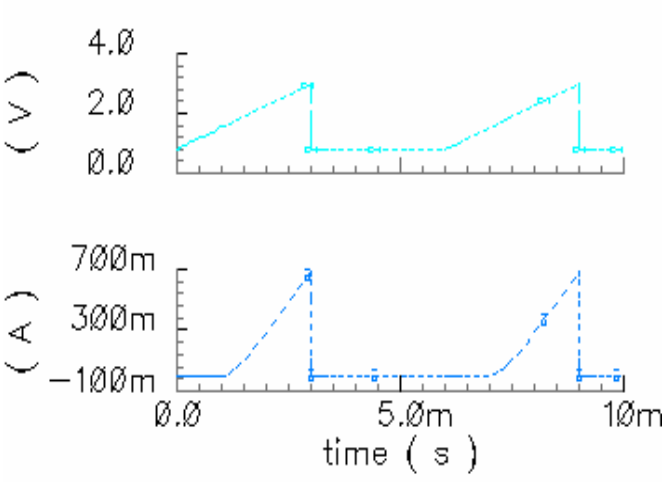


Figure 26. Ramp control voltage input and transient current output waveforms for bias circuit.

2.1.4 Transient Current Measurement Techniques

To reduce the test time of these devices, different control voltage signals are replaced by a single slow-ascending ramp signal with the same time period of the original signal, and the corresponding transient signature of the device is captured by monitoring the current drawn from the supplies as the voltage of the ramp changes. A DC voltage source with an accurate current measuring capability can be used to track the transient signature. To check the accuracy of the proposed method, the transient signature of a TDMA PA was measured on an Agilent 84000 RF ATE platform. The evaluation board, along with the clamp fixture used for the purpose of demonstrating the transient current behavior of a MMM5062 Motorola PA [28], is shown in Figure 27. The input signal to the control voltage terminal was a ramp signal from 0 to 3.5 V with a period of 1.2 seconds. The current signature of the device to the ramp signal was captured using a DC source in the ATE with a built-in current measurement capability. The captured transient signature of the device is shown in Figure 28. The transient signature shows a spike in its current waveform as soon as the PA turns "on" (enters the active region). In the case when the ATE DC source does not have an accurate current measurement capability, a small resistance (1 Ω) can be placed in the path of the current on the loadboard and the differential voltage across this resistor can be used to track the current signature.

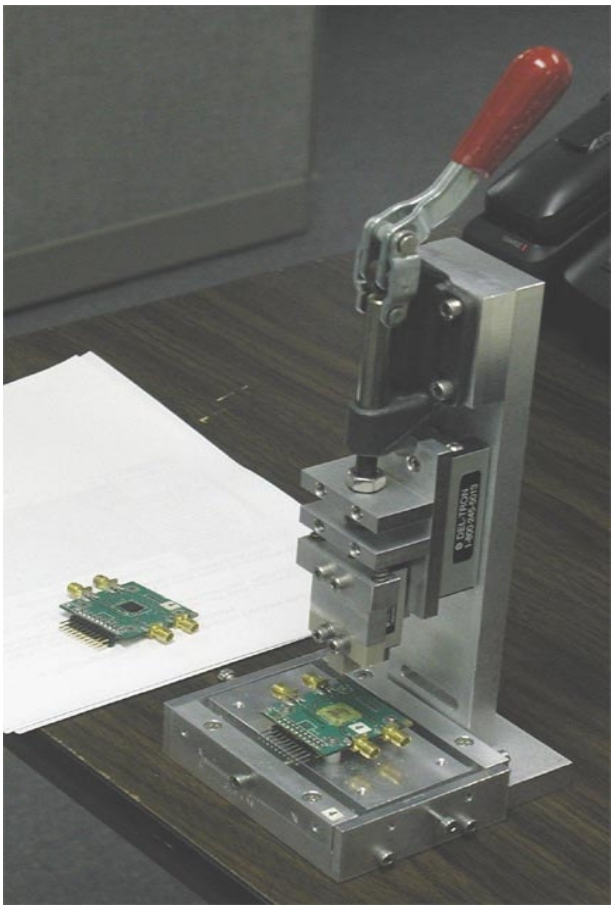


Figure 27. Evaluation board along with clamp fixture for transient current measurement.

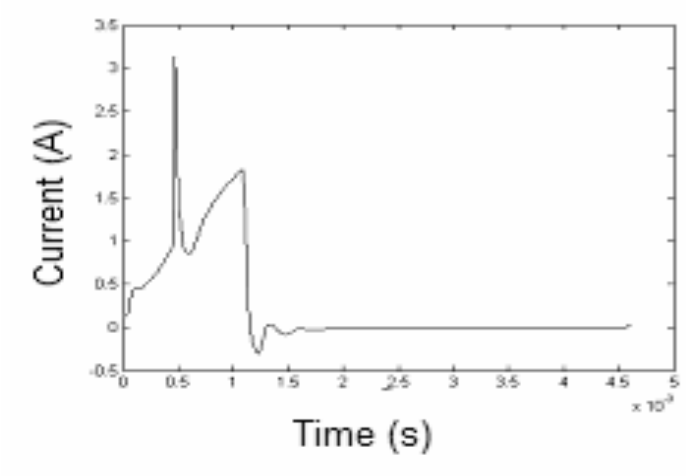


Figure 28. Transient signature measured using current measuring capability of a DC source.

2.1.5 Calculating Specifications from the Sampled Transient Current Response

Ideally, one would like to have a deterministic expression for computing the output specifications from the discrete amplitude values in the sampled transient response of the PA, but the relationship of the amplitudes in the sampled transient response to the specifications is unknown. Hence, the alternate test framework [19][20][21] is used to compute these specifications. This is a signature-based specification measurement (computation) technique in which the response of the circuit (transient signature) to a specially crafted transient test stimulus is used to compute the specifications of the device using nonlinear regression functions.

To generate such a nonlinear regression function, a set of training devices is chosen from different production lots. The optimized ramp signal is applied to the control voltage terminal in each of these devices and the resulting transient response of the devices is sampled and stored. The output specifications of these devices are also measured using the conventional test setup at the different DC control voltage values. A nonlinear regression function is built from the measured output specifications to the discrete amplitude values in the transient response. These nonlinear regression functions are computed using multivariate adaptive regression splines (MARS) [32]. Once these regression functions are computed, the sampled transient responses of the devices to be tested can be mapped in real time to their corresponding specifications. The general flow of the proposed current signature-based specification test methodology for RF circuits is shown in Figure 29. In the proposed methodology, a sinusoidal stimulus near the center frequency of operation is also applied to the input port of the RF PA DUT.

MARS are used for developing the nonlinear models that relate the process parameters to the test specifications of the DUT. The MARS algorithm mainly depends on the selection of a set of basis functions and a set of coefficient values corresponding to each basis function to

construct the nonlinear model. The model can also be visualized as a weighted sum of basis functions from the set of basis functions that span all values of each of the independent variables. MARS use two-sided truncated functions of the form $(x\text{-}t)_+$ and $(x\text{-}t)_-$ as basis functions for the linear and nonlinear relationships between the dependent and independent variables, t being the knot positions. The basis function has the form

$$(x-t)_+ = \begin{Bmatrix} x-t & x>t \\ 0 & otherwise \end{Bmatrix} \qquad \textbf{Equation 7}$$

The basis functions together with the model parameters are combined to generate the predicted values from the values of the independent variables. The MARS model for a dependent variable y and M independent terms can be expressed as

$$y = f(x) = \beta_0 + \sum_{m=1}^{M} \beta_m H_{km}(x_{v(k,m)}) \qquad \textbf{Equation 8}$$

where the summation is over the M independent variables. β_0 and β_m are parameters of the model (along with the knots t for each basis function, which are also estimated from the data). The function H can be expressed as

$$H_{km}(x_{v(k,m)}) = \prod_{k=1}^{K} h_{km} \qquad \textbf{Equation 9}$$

where $x_{v(k,m)}$ is the k^{th} independent variable of the k^{th} of the m^{th} product. During the forward step-wise placement, basis functions are constantly added to the model. After this implementation, a backward procedure is applied when the basis functions associated with the smallest increase in the least-square fits are removed, producing the final model. At the same time, the generalized

cross validation error, which is a measure of goodness of fit, is computed to take into account the residual error and the model complexity. The above equation can be further decomposed into the sum of linear, square, cubic products, and so on. Introducing a larger or smaller number of basis functions can also change the accuracy.

Using MARS, the amplitudes of the discrete components in the transient response are related to the measured specifications of the device using the conventional method. The relationship is of the form

$$(\overline{s}) = \Psi(p) \cdot (p) \qquad \textbf{Equation 10}$$

where s represents the output specifications and p represents the amplitudes of the sampled transient response. Once this nonlinear regression function is computed, the specifications of the devices to be tested can be calculated from the amplitudes of the sampled transient response.

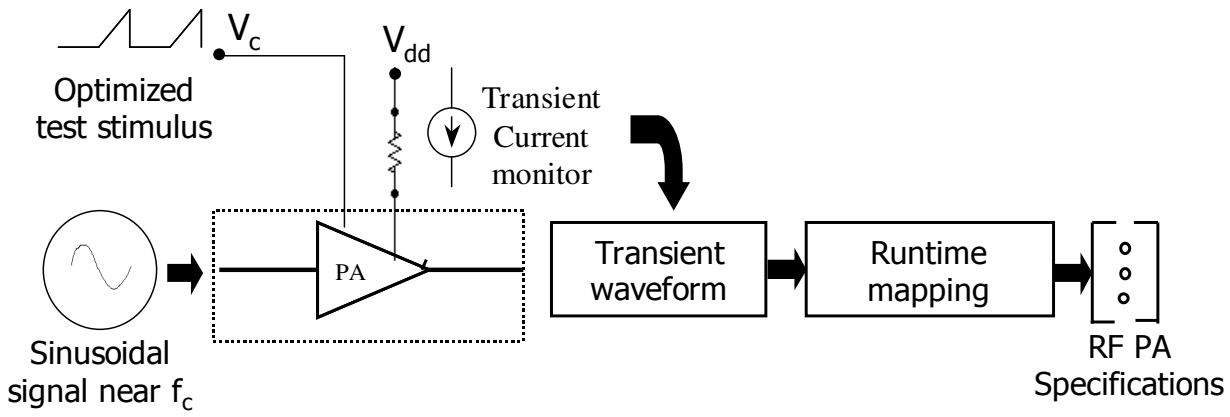


Figure 29. General test flow.

2.2 VALIDATION OF PROPOSED METHODOLOGY

To validate the proposed methodology, a two-stage PA was used as the test vehicle. The PA designed for validation is a SiGe hetero-junction bipolar transistor (HBT) PA used in cellular handsets [33]. Specifications such as output power, PAE, NF, stability factor, and second-harmonic power were considered in this design. It is important to describe the relationship of some of these specifications to the transient current behavior of the circuit.

Output Power: This is dependant on the S_{21} (gain) of the circuit. Any variation in the S_{21} parameter will affect the gain parameter because the gain produced by each stage of the PA is directly proportional to the current it draws from the supplies.

Power added efficiency (PAE): This is calculated as $(P_{out} - P_{in})/P_{DC}$. Since this specification is dependant on the output power (P_{out}) and the supply power (P_{DC}), it can be concluded that any variation in the PAE will be reflected in the transient current of the circuit.

Noise Figure (NF): It is the ratio of the signal-to-noise ratio (SNR) at the input to the SNR at the output. This is dependant on the P_{out} and the system noise, which will be reflected in the transient current.

Stability factor (*k*): The stability factor (k) can be computed as follows.

$$k = \frac{1 - |S11|^2 - |S22|^2 + (S12S21 - S11S22)^2}{2|S12S21|} \qquad \textbf{Equation 11}$$

The stability factor is a function of the S-parameters, which vary with the transient current. The S_{21} factor (gain) varies due the chance in the currents drawn from the supplies. Any change in S_{11} (input matching) and S_{22} (output matching) will be directly reflected in the current drawn from the supplies, since the performance of the system degrades.

In Table 1, the goals used in the design of the PA are described and the simulation results obtained using Agilent's (HP) advanced design system (ADS) suite are compared with the goals. The SiGe HBT model was used in the design of the PA because of its lower knee voltage and higher breakdown voltage. A block diagram of the PA is shown in Figure 30. The first stage or the driver stage was designated to provide 20 dB gain and 20 dBm power to the output stage. In the output stage, i.e., the power stage, a gain of 10 dB was delivered to provide the specified 30 dBm output power. This output stage is usually the power-hungry stage because it consumes a large amount of DC power to deliver high power levels such as 30 dBm. The number of SiGe HBT power cells required for each stage was determined by employing DC-IV curve tracer simulations. The driver stage employed 100 cells and the output stage employed six cells to deliver the required power. Suitable input, inter-stage, and output matching circuits were used.

Table 1. Design specifications and the simulation results of the PA.

Specification	Desired	**Achieved**
Linear gain	>30 dB at 0 dBm input	35.48dB
PAE	> 35%	~ 42.885%
Noise figure (NF)	<2	1.433
Stability factor	Unconditionally Stable, K > 1	K > 1 (200 MHz – 2 GHz)
Second harmonic ($2f_o$)	<20dB	19.45dB

A schematic of the RF PA is shown in Figure 31. The schematic displays the terminals at which the optimized ramp-like signal was applied and the terminals at which the transient current behavior was observed. The control voltage terminals of both stages were tied to the same V_{DD}

ramp and the transient current from the two stages was added to generate the transient current signature of the circuit for the optimized input signal. In the simulated circuit, bond wires were also modeled to account for the parasites of the off-chip connections. These bond wires are not displayed in Figure 31 to improve the clarity of the schematic.

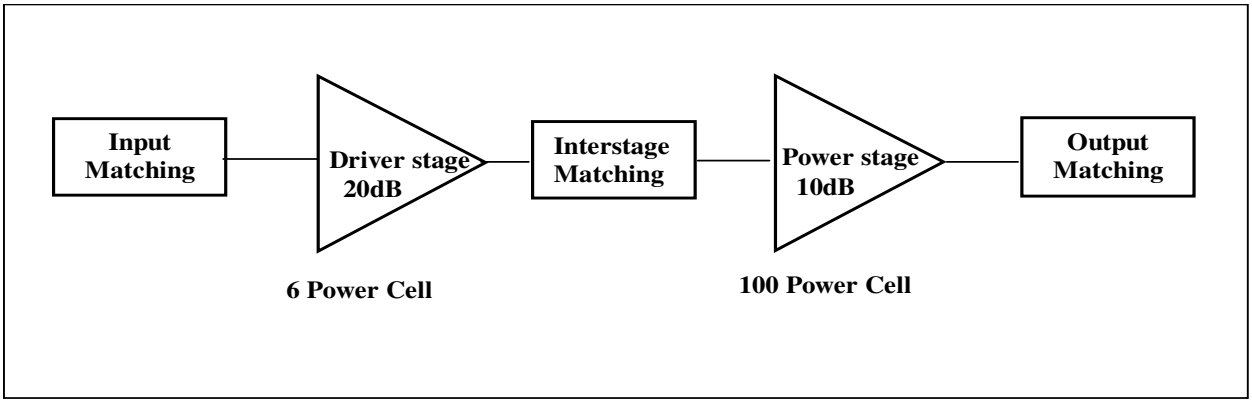


Figure 30. Block diagram of the PA.

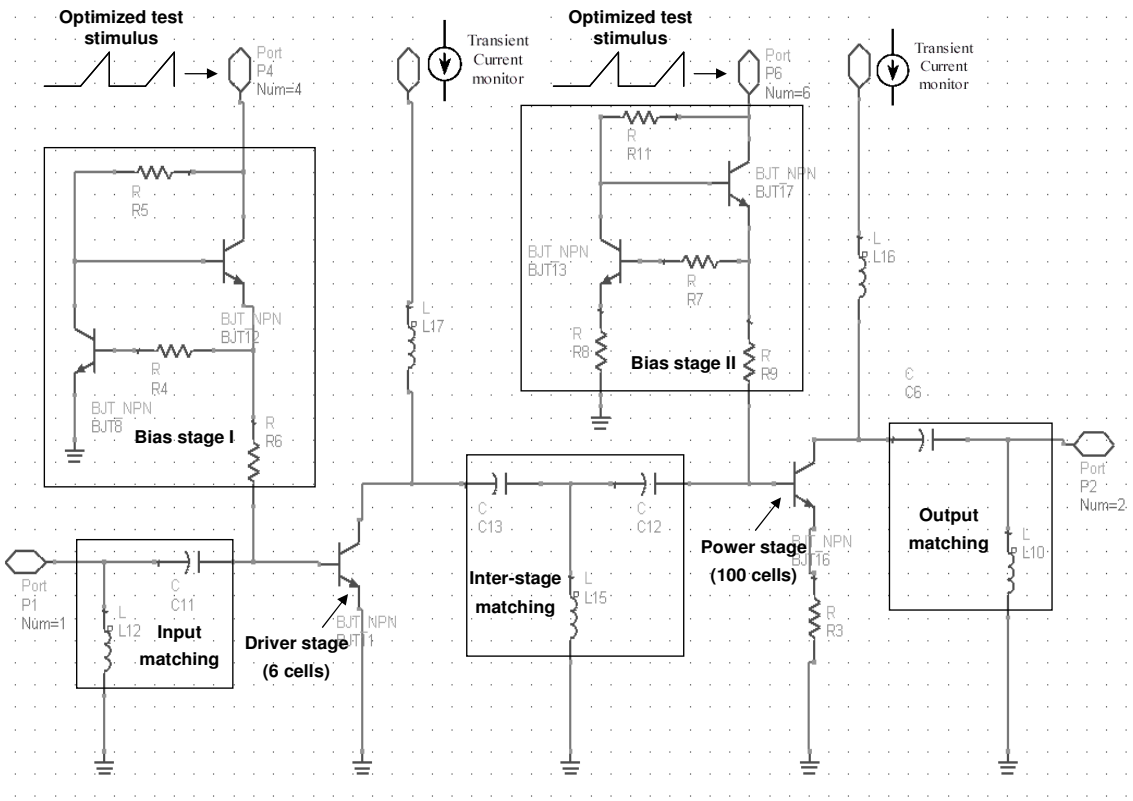


Figure 31. Schematic capture of the RF PA.

2.2.1 Transient Current Measurement

The circuit parameters of the PA were perturbed to generate different instances of the circuit. In this experiment, a set of 60 training instances was created. Test stimulus optimization was performed, as explained in 2.1.1. The optimized ramp signal for these training instances is shown in Figure 32. The time step of the ramp was calculated to be 10 ns and the total time period of the ramp was 1.1 μs. Since the TDMA PA was designed to operate in the global system for mobile (GSM) bandwidth of 830-850 MHz, a sine wave of 840 MHz with 0 dBm amplitude was used as the RF input stimulus to the DUT. The test stimulus was applied to the control voltage terminal of each of the 60 devices. The corresponding transient current signatures for each of these devices are shown in Figure 33. These transient signatures were captured and stored for further processing. Simultaneously, the output specifications of these devices were also measured using the conventional specification method. The nonlinear regression function was built to map the sampled transient current data onto the corresponding test specifications using MARS.

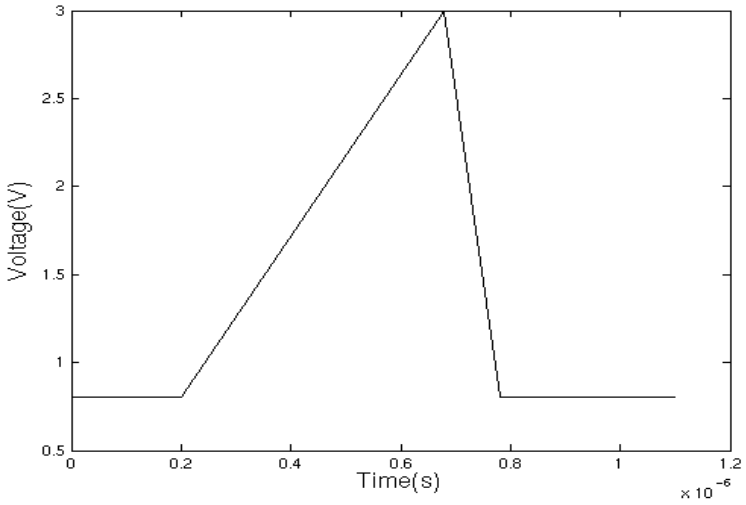


Figure 32. Test waveform applied to the control voltage input.

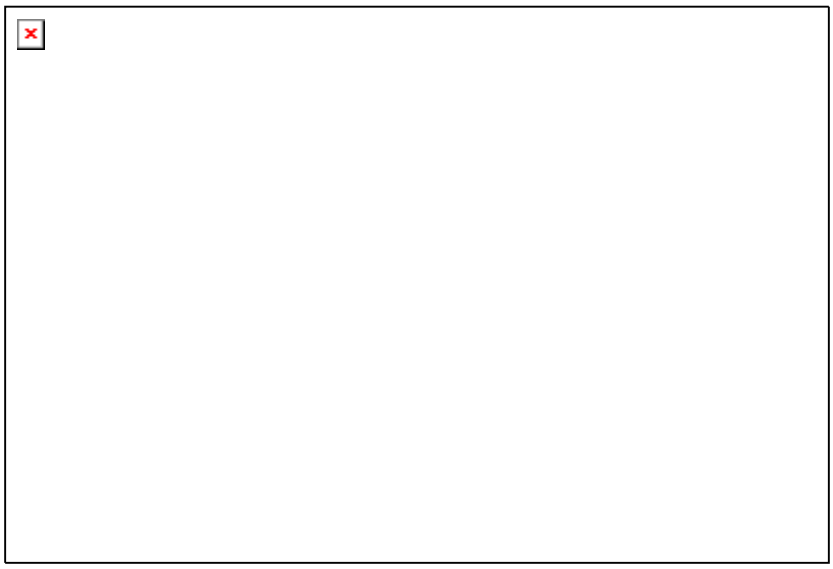


Figure 33. Current signatures for all device instances.

2.2.2 Computation of nonlinear regression equations

MARS was used for the purpose of building regression equations form the sampled transient response to the corresponding specification for the same instance. These regression equations are built for each specification in an individual manner. The transient response was sampled and five hundred sample points ere obtained. The constructed regression equations are in the form,

$$y = A_0 + A_1(x - x_1)_+ + A_2(x - x_1)_- + A_3(x - x_2)_+ + A_4(x - x_2)_- .. \quad \textbf{Equation 12}$$

where y is the output specification, A_0 is a bias constant, A_1,A_2 are the basis function coefficients, x_1,x_2 are the knots for the basis function, and x is the discrete amplitude of the sampled response. MARS uses two-sided truncated functions of the form $(x-x_1)_+$ and $(x-x_1)_-$ as basis functions for linear and nonlinear relationships between the dependent and independent variables, x_1 being the knot position. The basis coefficients and the corresponding knots for the gain and PAE specification are tabulated in Table 2 and Table 3 respectively. The constant terms in the

regression equation for the gain and PAE specifications were 35.0818 and 40.0415 respectively. The number of basis functions required for accurate prediction of each specification is listed in Table 4.

Table 2. Knot placement and basis function coefficients for gain specification.

Knot placement	Basis function coefficients	
	Positive	**Negative**
(In276-0.1396)	108.792	------
(In476-0.4888)	-5.89236	-142.588
(In270-0.1327)	-82.1106	------
(In120-0.0087)	-425.152	------
(In58-0.0016)*(In476-0.4888)	------	245024
(In8-0.0001)*(In276-0.1396)	186816	------
(In24-0.0001)*(In276-0.1396)	-85344.1	------
(In179-0.0652)*(In476-0.4888)	-462.147	------
(In100-0.0057)*(In476-0.4888)	-25781.2	-18255.3
(In101-0.0059)*(In476-0.4888)	26316.3	------
(In2-1.144e-05)*(In101-0.0059)*(In476-0.4888)	------	-6.165e+10

Table 3. Knot placement and basis function coefficients for PAE specification.

Knot placement	Basis function coefficients	
	Positive	**Negative**
(In282-0.1466)	544.048	------
(In198-0.0590)	-551.973	------
(In290-0.2213)	455.171	------
(In417-0.3757)	-210.546	------
(In357-0.3325)	-278.163	-71.4495
(In26-0.0002)*(In282-0.1466)	635443	-157480
(In38-0.0008)*(In290-0.2213)	-234038	-8.25506e+06
(In6-9.096e-05)*(In282-0.1466)	-1.19718e+06	-801369
(In157-0.0348)*(In290-0.2213)	-5148.32	-10850.2
(In87-0.0046)*(In290-0.2213)	44527.3	-2.87421e+07
(In2-1.159e-05)*(In157-0.0338)*(In290-0.2213)	7.62496e+08	6.39901e+09

Table 4. Number of basis functions for each specification.

Knot placement	**Number of basis functions**	
	Positive	**Negative**
Gain	9	4
PAE	11	7
Noise Figure	9	10
Stability Factor	8	7
2^{nd} Harmonic	8	10

2.3 EXPERIMENTAL RESULTS

The validation of the computed regression equations was performed for a set of 40 validation instances. The optimized ramp signal was applied to the control voltage terminal of each of these devices and their transient current signatures were captured and stored. Simultaneously, the test specifications of these devices were also measured using the conventional specification method. The specifications of the validation instances were computed using the regression equations, which were compared with the specifications measured using the conventional method to calculate the maximum prediction error of the proposed methodology.

The maximum prediction errors obtained in this experiment for the various specifications of the PA are shown in Table 5. These errors depict the typical maximum error obtained for a particular instance using the transient current method. An accurately predicted specification would track the actual specification value. The scatter plots and the prediction error plots of the gain and PAE specifications are presented in Figure 34. The closer the predicted specification values are located to the straight line having slope +1 (representing error-free predictions), the higher the effectiveness. As shown in Figure 34, the proposed methodology had good tracking of the RF PA specifications. In the case of the gain specification, the maximum prediction error was less than ± 0.7 % of the nominal value (35.48 dB). In the case of the PAE specification, the prediction error was less than ± 4 % of the nominal value (42.885 %). The test times for the proposed and conventional methods are compared in Table 6. A test time savings of more than a factor of three can be achieved using the proposed method.

Table 5. Prediction errors for the transient current methodology.

	Gain	PAE	Noise Figure (NF)	Stability factor (K)	$2f_o$
% Prediction error	0.7	4.2	1.5	2.2	1.9

Table 6. Performance comparison.

	Proposed method	Conventional method
Test Time	330ms	1450ms

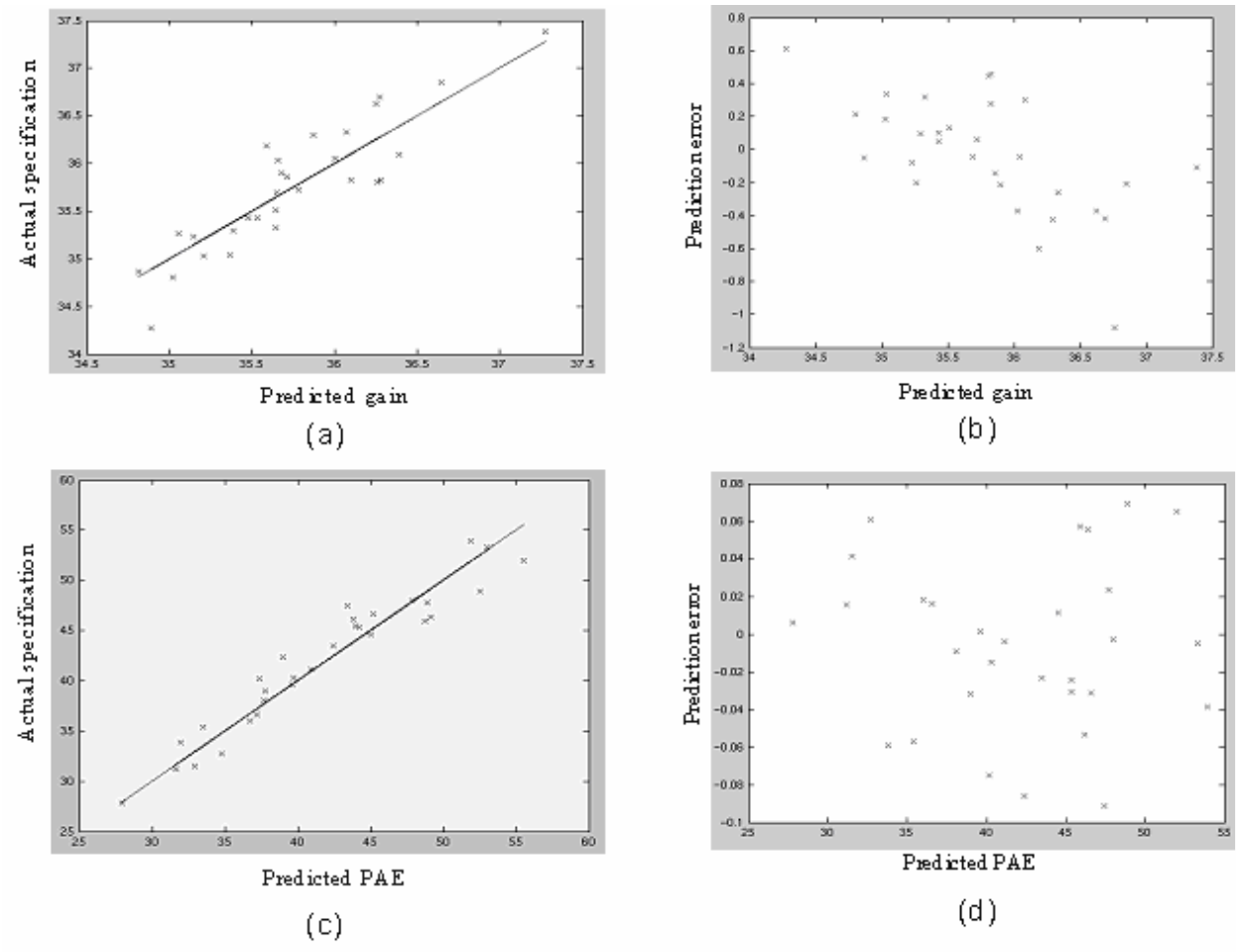


Figure 34. (a) Scatter plot of gain specification, (b) Prediction error plot of gain specification, (c) Scatter plot of PAE specification, and (d) Prediction error plots of PAE specification.

Chapter 3

SPECTRAL SIGNATURE BASED ALTERNATE TEST: GENETIC ATPG FOR RELIABLE TEST USING LOW-PERFORMANCE TEST RESOURCES

The proliferation of wireless communication devices has increased the pressure on semiconductor manufacturers to produce low-cost and highly integrated RF transceiver radios. Until a few years back, RF test engineers used to perform specification tests on discrete RF devices such as mixers, low-noise amplifiers, PAs, and RF switches. The emergence and advances in SoC technologies have seen different RF devices/modules integrated into a single chip/package. A standalone RF transceiver system is used to perform the functionalities of both transmission and reception of the RF signals. The block diagram of a typical direct conversion type RF transceiver is shown in Figure 35.

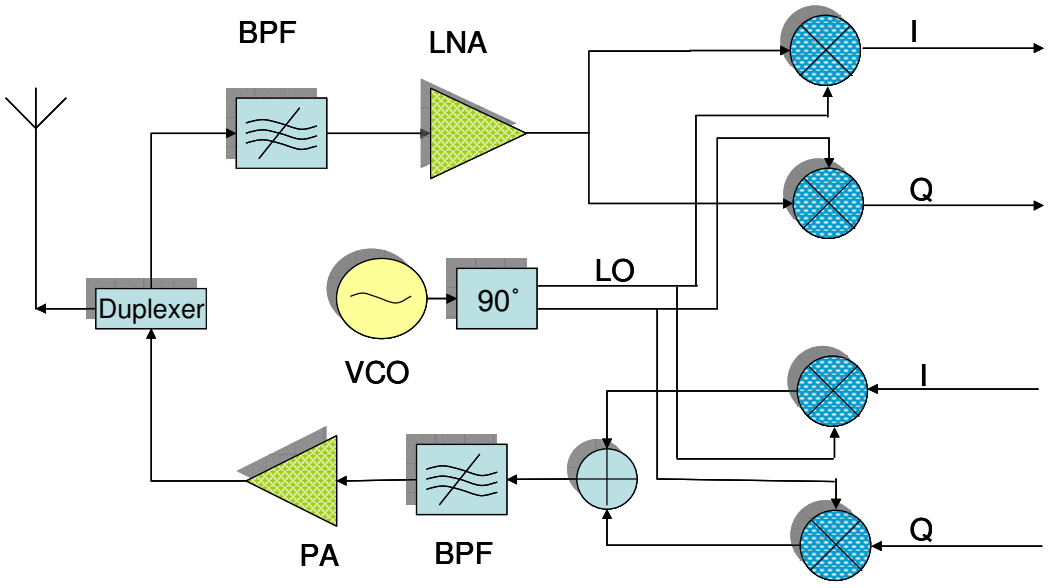


Figure 35. Block diagram of a typical direct conversion RF transceiver.

A typical transceiver radio contains a TX and a RX chain and follows an RF-IF or an RF-baseband configuration. In a RF-IF configuration, the RF frequencies are up-converted or down-converted to IF frequencies using a PA/mixer or an LNA/mixer pair respectively. This kind of configuration is normally found in super-heterodyne type of transceiver architectures (Section 1.3 & 1.4), in which the IF frequencies (usually a few hundred MHz) are translated to baseband frequencies using an additional mixer stage (Section 1.4). In a RF-baseband configuration (direct-conversion architecture), as shown in Figure 35, the signals are converted all the way from RF to IQ baseband frequencies (usually a few tens of MHz). Due to the high-levels of integration and matching considerations of different cascaded modules, the most viable test access points for applying the test stimuli and measuring the test responses of the TX and RX subsystems without affecting their performance are usually limited to the access points available at the baseband (or IF) and the RF input/output pins of the subsystems. Stringent requirements in the subsystem specifications of the transmitter and receiver, viz. IIP3, P1dB, ACPR, NF, call for complex and long tests to be performed on expensive RF ATE platforms as in the case of the conventional test approaches [41][42].

The most expensive component in the ATE systems is the RF receiver, or spectrum analyzer and most ATE systems are only configured to handle only one receiver-per-system [27]. These receivers must be capable of handling a frequency range of 100 MHz to 6 GHz with high levels of linearity. Also, these receivers must posses very high noise immunity to produce repeatable measurements. These stringent requirements limit the capabilities of most of the current generation RF ATE to single-site architectures. As discussed in Section 1.2, the *fixed cost* or *capital cost* of these expensive ATE platforms are estimated to be about $ 2 million in addition to the test handler costs. This boils down to 5 cents per second of test time if these

testers are operated continuously for their projected life span of five years. Also, conventional test procedures employ a sequential approach to test each specification of the TX and RX subsystems. Since the performance requirements on the wireless devices is always on the rise, their testing becomes more complex and often several averaging operations are required to establish repeatability of the test measurements.

In addition to the test hardware requirements, RF testing also lags behind the digital and to some extent the analog counterparts in terms of the CAD tools for ATPG. Researchers in the field digital testing have developed several well established ATPG tools whose variations are currently used in high-volume production. These tools are mostly based on well established fault models, fault excitation, and fault propagation procedures. Some of the well known tools include D-algorithm [44], path-oriented decision making (PODEM) [45], fanout-oriented TG (FAN) [46], sensitizing method for algorithmic random testing (SMART) [47], random path sensitization (RAPS) [48] among many others.

ATPG tools for analog circuits, speaking form the viewpoint of ATPG for digital circuits and systems, do not exist [49]. There is no generalized ATPG tool like PODEM, which can process a netlist based on an accepted fault or specification list and generate a set of test stimulus and a measure of their expected quality. But some of these tools have generated some degree of success for different applications. Some of these include signal flow graphs (SFG) based ATPG [50], sensitivity-based ATPG [51][52], linear programming-based ATPG [53], IDD-based ATPG [54], and pseudo-random ATPG [55].

To reduce the test cost of RF SoC devices and to enable test on low-cost baseband ATE, a spectral signature-based alternate test methodology that employs a custom developed genetic ATPG for fast test generation purposes is presented in this Chapter. In the proposed

methodology, suitable DfT resources are used to up-convert or down-convert the RF test signals to a frequency bandwidth that is within the range of the low-cost ATE. Such an approach would be limited by the test capabilities of the low-cost ATE (analog/Baseband) as RF tests require high-precision socket pressure, good electromagnetic isolation, and narrow-bandwidth RF measurements. To optimize the test stimulus and to extract the best possible performance from the low-cost ATE, a genetic ATPG-based computer aided design (CAD) framework in presented to optimize the test stimulus for the spectral signature based tests.

The CAD framework employs a custom developed genetic algorithm and behavioral-level simulator for the purpose of fast test vector generation. The generated digital test pattern is modulated onto sine waves and is blasted to the RF systems through low-cost DfT resources. The corresponding spectral signature of the system is captured and processed to compute multiple specifications of the system-under-test (SUT) using the alternate test framework. The main highlight of this work is that the generated test vectors are also optimized to generate reliable tests in the presence of measurement uncertainties presented by the ATE and/or DfT resources used to process the test signals. The key contributions of this work can be summarized as follows:

- Expensive RF ATE instrumentation can be avoided and it addresses the specification test problem of RF subsystems in a tester independent architecture.
- Since a single bitstream sent from the baseband is used for the entire test, the overall test time for multiple specifications is reduced.
- This approach also attempts to solve the limited test access problem associated with testing such integrated RF subsystems.

- Also, the issue of high simulation cost of RF systems is addressed by using behavioral models to simulate the RF subsystem-under-test, the ATE resources, and the DfT resources for fast test generation.
- This approach is the first-of-its-kind to co-simulate the RF systems along with low-cost test resources to generate reliable tests in the presence of measurement uncertainties.

3.1 PROPOSED TEST ARCHITECTURE

In the proposed testing methodology, frequency translating devices such as mixers are used to upconvert or downconvert test signals to a frequency bandwidth within that of the baseband test instrumentation of the low-cost ATE. A conceptual representation of this architecture is presented in Figure 36. Most of the other forms of on-chip (built-in sensors)/off-chip test resources could also be used to test the RF SoC devices using the proposed CAD framework. The only overhead requirement would be to develop and update the CAD framework with their behavioral models so as to optimize the test stimulus for these resources.

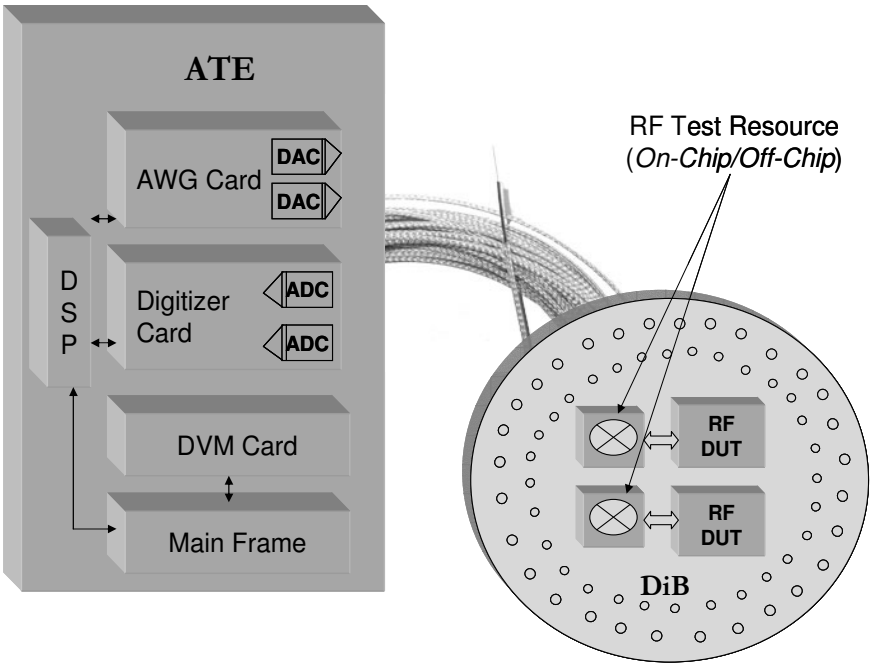


Figure 36. A conceptual representation of the proposed spectral signature based testing methodology.

In the case of a transmitter test, the optimized bitstreams are modulated onto sine waves in the DSP of the ATE and is sourced to the input of the transmitter using the DAC converter circuitry in the arbitrary waveform generator (AWG) card of the ATE. The response of the TX subsystem to this optimized bitstream is simultaneously translated to baseband frequencies using a passive on-board down-conversion mixer and is captured using the ADC converter in the digitizer board of the ATE. The DSP of the ATE is then used to process this captured signal to compute the specifications of interest from the observed signature using the regression functions computed from the alternate test framework.

To test the receiver section, the optimized test stimuli is modulated in the DSP onto sine waves and this signal is translated to RF frequencies through the passive on-board mixer and applied to the RF terminal of the RX subsystem. The corresponding response at the RX baseband output of the transceiver can be captured using the digitizer in the ATE for further processing.

Also, since the most of the transceivers are designed for half-duplex applications only the RX or the TX subsystem is turned on at any point of time. Hence, the passive mixer could be shared between the RX and TX section, which reduces the overall loadboard real estate requirements. But such an approach would require some additional switches to enable the *'share'* operation. A typical loadboard design for such a share operation is presented in Figure 37. Also, the sharing operation would help in simultaneous parallel testing of multiple devices to lower the overall test cost of these complex systems.

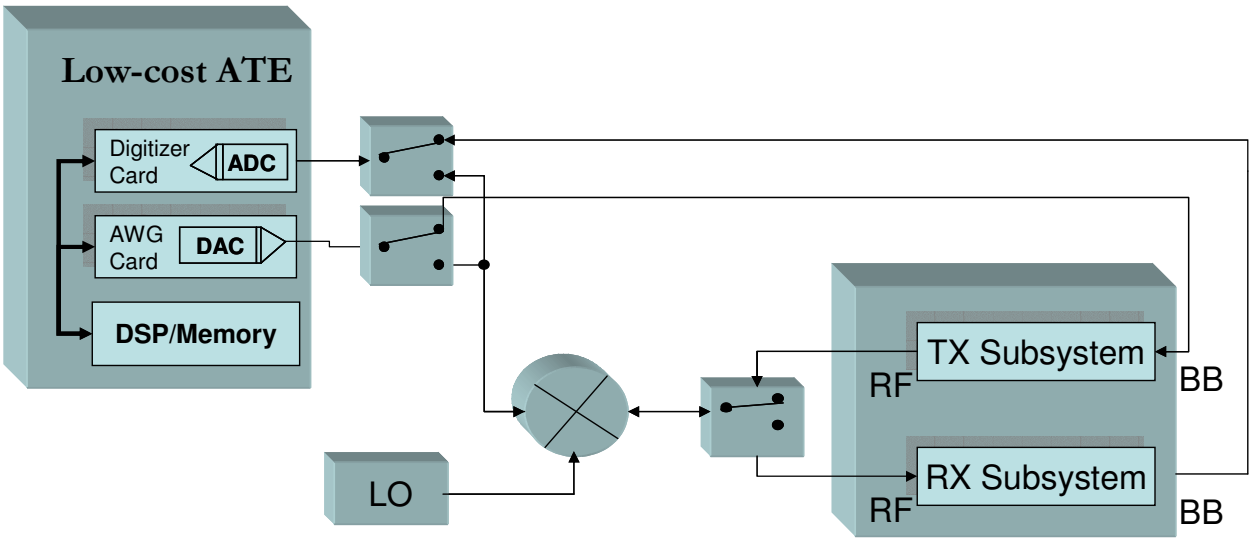


Figure 37. Loadboard design to enable share operation of RF radios for spectral signature-based testing.

3.2 BEHAVIORAL MODEL DEVELOPMENT FOR FAST TEST VECTOR GENERATION

Transistor-level simulations for all the sub-modules and test resources can yield high-accuracy for bench characterization and/or circuit verification purposes. But, these transistor-level descriptions are impractical for test vector/pattern generation purposes due to the following reasons.

(1) The primary objective of a test vector/pattern generation is to determine the optimal set of test stimuli, rather than to verify the functionality of the design. Hence, as long as the behavioral approximations preserve the relative "goodness" of one possible test stimulus versus another, they do not affect the quality of the tests.

(2) The larger the size of the process and circuit parameter space as in the case of transistor level descriptions, the more the number of iterations of the test generation algorithm.

(3) The proposed test methodology uses regression functions to compute multiple specification of interest from the observed test signature. This process requires the computation and evaluation of such regression functions during the fitness function evaluation in each iteration of the test generation algorithm. In the case of transistor level descriptions, this becomes expensive in terms of time and memory requirements.

Due to the above mentioned reasons and for the purpose of fast test vector generation, behavioral models abstracted from specific measurements made on the SUT are used for test generation purposes. The underlying assumption for the use of behavioral models is that the variations in the specification data and measurement data follow the same statistical trend under behavioral parameter perturbations as they would for transistor-level parameter perturbations.

3.2.1 Behavioral models for building blocks of the RF systems

A block diagram of a typical direct down-conversion radio transceiver architecture is shown in Figure 35. Form the figure, it can be observed that the submodules that need to be modeled for test generation purposes include the PA, the LNA, the BPF, the phase locked loop (PLL), and the mixer. These models will suffice to construct behavioral TX and RX chains for most commonly developed transceiver solutions (direct-conversion and super-heterodyne).

In the past, several modeling techniques have been developed to model the nonlinear effects in RF devices. The most common approaches include Volterra series based models [56] and artificial neural network (ANN) based models [57]. Models based on classic Volterra series are cumbersome to develop and is not so accurate for highly nonlinear devices [57][58] due to some convergence problems. To overcome some of the problems, many modifications were performed to improve the accuracy of these models [59]. In [59], a powerful behavioral modeling mechanism based on modified Volterra series, so-called sliding kernels dynamic Volterra series model is presented. On the other hand, ANN based models provide accurate models at the higher input levels, but they do not behave like polynomials for small input signals [58][60]. In this work, polynomial based models [58][62] are used to model nonlinearities in the system as prior work has proved that there provide sufficient accuracy for test generation purposes [61][62].

Since the proposed test methodology uses the amplitude spectrum (i.e. amplitude vs. frequency) of the test response as the measurement space, the simulation of all blocks in the transmitter/receiver chain is performed in the frequency domain. This also helps to reduce the overall simulation time. Traditional time-domain simulators like SPICE require excessive simulation time because of steady state solution requirements [63]. The analog/microwave circuit

needs to be simulated until the transient solution vanishes [63]. Also, the ratio between the lowest frequency present in the modulation and the frequency of the carrier is a measure of the relative frequency resolution required of the simulation. Hence, the transient analysis performed by SPICE is expensive when it is necessary to resolve low modulation frequencies in the presence of a high carrier frequency because the high-frequency carrier forces a small time step while a low-frequency modulation forces a long simulation interval [64].

Frequency domain simulation requires nonlinear behavioral models to relate the tones in the input spectrum to the output spectrum. In [64], a black box modeling technique of nonlinear behavior in frequency domain is presented. This involves construction of describing functions using ANN or Volterra series, which maps the complex information in the input components to each of the spectral components in the output signal. This simulation time encountered in such an approach is directly proportional to the number of tones in the input spectrum which makes it unsuitable for the proposed methodology. In the proposed methodology, closed from algebraic descriptions that relate the input spectral components to the output spectral components are used to model the nonlinear behavior of the device. This helps to perform inexpensive simulation of nonlinear RF systems to the required level of accuracy for test generation purposes. The models developed for the individual components in the RF subsystem are described below.

Amplifier: The amplifiers of the RF sub-system (e.g. LNA, PA) are realized by implementing a third order polynomial function [2] of the type,

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \qquad \textbf{Equation 13}$$

where α_0 is the DC offset, α_1 is the small signal gain, α_2 and α_3 are the nonlinearity coefficients. The α_1, α_2, and α_3 coefficients are used to model the linear (gain) and nonlinear (harmonics and

inter-modulation terms) effects of the amplifier. For inputs with sufficiently low amplitude levels, as is the case for RF subsystems, the higher order terms (viz. α_4, α_5) can be ignored as they have little effects compared to the lower order terms [2]. It is also assumed that the DC offset does not propagate across the cascade of sub-modules in narrowband RF subsystem and hence the α_0 parameter is set to zero.

The time domain input-output behavior in Equation 13 can be represented in frequency domain as mapping the sum of different input tones (in both magnitude and phase) to the corresponding output tones (magnitude and phase). Given that Equation 13 is a polynomial in x(t) of order three, it can be shown that, for a 3-tone input, $x(t) = V_m\cos(2\pi f_m t+\phi_m) + V_n\cos(2\pi f_n t+\phi_n) + V_p\cos(2\pi f_p t+\phi_p)$, the harmonic and intermodulation terms of the output spectrum will be generated as summarized in Table 7. Hence these closed from algebraic equations can be used for fast frequency domain simulation of the RF device. In Table 7, the amplitude values viz. V_i are complex quantities representing magnitude and phase components.

Table 7. Amplitude vs. frequency output for a nonlinear transfer function.

Frequency	Output amplitudes
0	$0.5\ \alpha_2\ V_i^2$
f_i	$\alpha_1\ V_i\ (1 + 0.75\ V_i^2)$
$2f_i$	$0.5\ \alpha_2\ V_i^2$
$3f_i$	$0.75\ \alpha_3\ V_i^3$
$\lvert\pm f_i\rvert$	$0.75\ \alpha_3\ V_i^3\ (-1 + {}^{N}\Sigma_k\ (V_k^2/\ V_i^2))$
$\lvert\pm f_i \pm f_j\rvert,\ (i-j)^2>0$	$0.5\ \alpha_2\ V_i\ V_j$
$\lvert \pm f_i \pm f_j \pm f_k\rvert,$ $(i-j)^2(i-k)^2 + (j-i)^2(j-k)^2 + (k-i)^2(k-j)^2 > 0$	$0.75\ \alpha_3\ V_i\ V_j\ V_k$

The α_1, α_2, and α_3 coefficients can be computed using any one of the following approaches for test generation purposes.

Transfer function approach: In this approach, the input-output (amplitude modulation (AM) – AM) transfer function of the DUT is obtained by sweeping the input power to the DUT until the 1-dB compression point and observing the corresponding output. This can be effortlessly performed during the characterization test phase of the IC development cycle (Section 1.1). Normally, high-performance test instrumentation is used during the characterization phase as these tests are performed only for a few devices in controlled laboratory conditions. A vector spectrum analyzer (VSA) and an RF signal generator connected to the PC through the GP-IB interface is used to extract the transfer function. Any automated test support software like Matlab is used to control the signal generator and the spectrum analyzer and to automate the process. A conceptual view of this transfer function measurement methodology in presented in Figure 38. A higher-order polynomial could be used to fit the transfer function using the least squares error method. The α_1, α_2, and α_3 coefficients obtained from this polynomial can be used in the behavioral modeling of the device for test generation purposes. The phase effects of the device are not modeled as they provide negligible improvement for test generation purposes. Also, since only the spectral amplitudes of the tones are used in the proposed testing methodology, the phase effects do not provide significant information for test generation purposes.

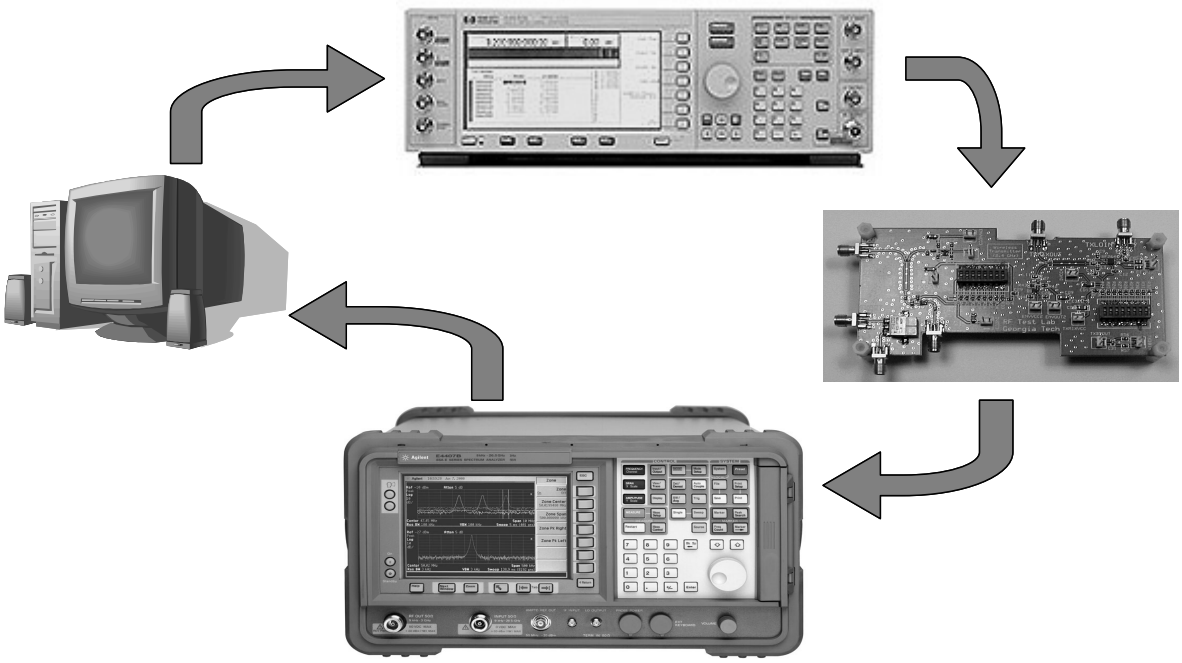


Figure 38. Conceptual view of the methodology used to measure the transfer function of the RF modules for test generation purposes.

Harmonic approach: For highly nonlinear devices, such as for PAs, the α_2 parameter can be estimated from the magnitude of the 2nd harmonic component at the output of the PA. Similarly, the α_3 parameter can be estimated from the magnitude of the 3rd harmonic component at the output of the amplifier. The α_1 parameter can then be estimated form the small-signal gain of the device. The equations used to compute the α_1, α_2, and α_3 parameters for an input signal of the form $A\cos(\omega t)$ are listed below.

$$\alpha_1 = \frac{P_1}{A} - \frac{3\alpha_3 A^2}{4}$$ **Equation 14**

$$\alpha_2 = \frac{2P_2}{A^2}$$ **Equation 15**

$$\alpha_3 = \frac{4P_3}{A^3}$$ **Equation 16**

where P_1, P_2, and P_3 are the amplitude levels at the fundamental, first harmonic and second harmonic frequencies.

Specification-based approach: In this approach, the α_1 and α_3 parameters are computed from the combination of gain and IIP3 specification values or the combination of gain and P1dB specification values. This approach is used for nonlinear devices that exhibit an odd symmetry, implying α_2, α_4, α_6, etc. are zero. For highly nonlinear devices, such as for PAs, one of the above mentioned combinations is used to compute the parameters. The equations used to compute the α_1 and α_3 parameters form the gain and P1dB specification values are listed below.

$$\alpha_1 = \frac{\mathrm{P1dB}^2\ \alpha_3}{0.145}$$ **Equation 17**

$$\alpha_3 = \frac{P_0}{\frac{\mathrm{P1dB}^2\ A}{0.145} + \frac{3A^2}{4}}$$ **Equation 18**

where P_0 is the amplitude at the fundamental frequency output and A is the amplitude of the input tone. The equations used to compute the α_1 and α_3 parameters form the gain and IIP3 specification values are listed below.

$$\alpha_1 = \frac{3\ IIP3^2\ \alpha_3}{4} \qquad \textbf{Equation 19}$$

$$\alpha_3 = \frac{1.33P_0}{IIP3^2\ A + A^3} \qquad \textbf{Equation 20}$$

Mixer*:* For test generation purposes, the mixer of the RF subsystem is modeled as a nonlinear transfer function followed by an ideal multiplier. The nonlinear transfer function is realized in the same manner as is done for the amplifier. The frequency mixing operation is realized by the multiplication operation.

$$y(t) = C\ x_1(t)x_2(t) \qquad \textbf{Equation 21}$$

The constant C is computed using the conversion gain of the mixer. Assuming a narrowband system, the conversion gain is effectively constant over the narrow range of frequencies of interest.

Filter*:* The transfer function of the band-pass filters of the RF subsystem (e.g. band-select filter) are realized as linear transfer functions with different gains at different frequencies. The output of the filter is given by

$$Y(f) = [H(f)]\,\mathrm{diag}\left([X(f)]\right) \qquad \textbf{Equation 22}$$

where f is the frequency of operation, X(f) is the input spectrum, and Y(f) is the output spectrum. The different gain values corresponding to different frequencies are characterized by the center-frequency, filter-Q, and frequency roll-off. H, X, and Y are complex quantities representing the amplitude and phase values.

Phase locked loop (PLL): PLLs are primarily used as frequency synthesizers in RF transceivers to provide the LO signal for the RX and TX chains. The building blocks of a typical PLL, as shown in Figure 39, consist of a phase-frequency detector (PFD), a loop filter, a VCO and a frequency divider.

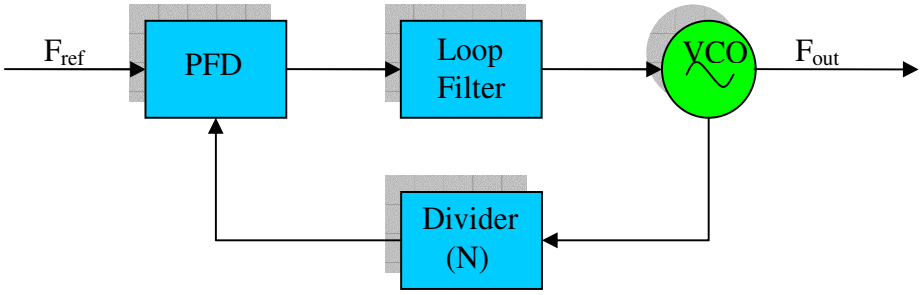


Figure 39. Block diagram of a typical PLL architecture.

In this work, the PLL is modeled by a linear gain block followed by a phase noise model. The linear gain is computed based on the transfer function of the constituent blocks of a PLL system. For example, the output signal of the PLL block shown in Figure 40 can be represented as shown in Equation 23.

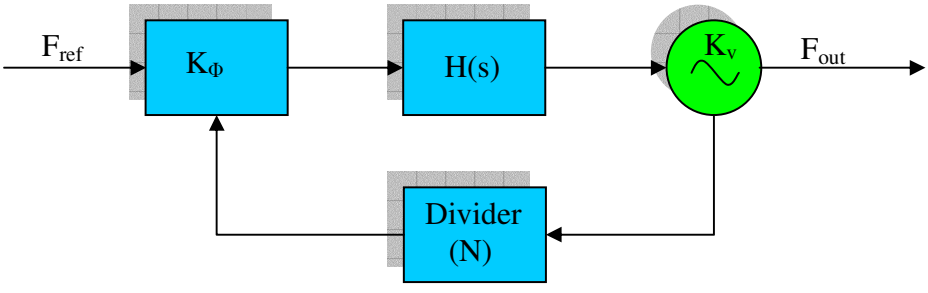


Figure 40. Transfer functions of the constituent blocks.

$$V_{out} = \frac{K_{\Phi} * H(s) * K_v}{1 + \frac{K_{\Phi} * H(s) * K_v}{N}} \qquad \textbf{Equation 23}$$

where H(s) represents the transfer function of a second-order loop filter, K_Φ represents the gain factor of the PFD, K_v represents the gain of the VCO circuitry, and N is the divide-by factor in the feedback path of the PLL. The output of the linear gain model is fed to the phase noise block that is modeled based on Leeson's phase noise model. The algorithm used to implement the phase noise model is shown below.

Table 8. Algorithm to compute phase noise based on Leeson's phase noise model.

Create random samples of the instantaneous phase values Filter the random values with 3 FIR filters with carefully chosen cut-off frequencies The cut-off frequencies are chosen based on the phase noise specifications of the PLL device The filtered values of the instantaneous phase (Φ_{fil}) are then added along with the time domain input signal ($A\cos(\omega t)$) at each time instant 't' as shown in Equation 24

$$PLL_{out} = \left[\left(\Phi_{fil}(t) * A\cos(\omega t)\right) + A\sin(\omega t)\right] \qquad \textbf{Equation 24}$$

where PLL_{out} corresponds to the output RF signal from the PLL. The peak amplitude value in the signal corresponds to the local oscillator center frequency. The amplitudes of the frequency bins adjacent to this bin fall-off based on the phase noise of local oscillator.

A block diagram of the behavioral models used for test generation of an RF transmitter and receiver are shown in Figure 41.

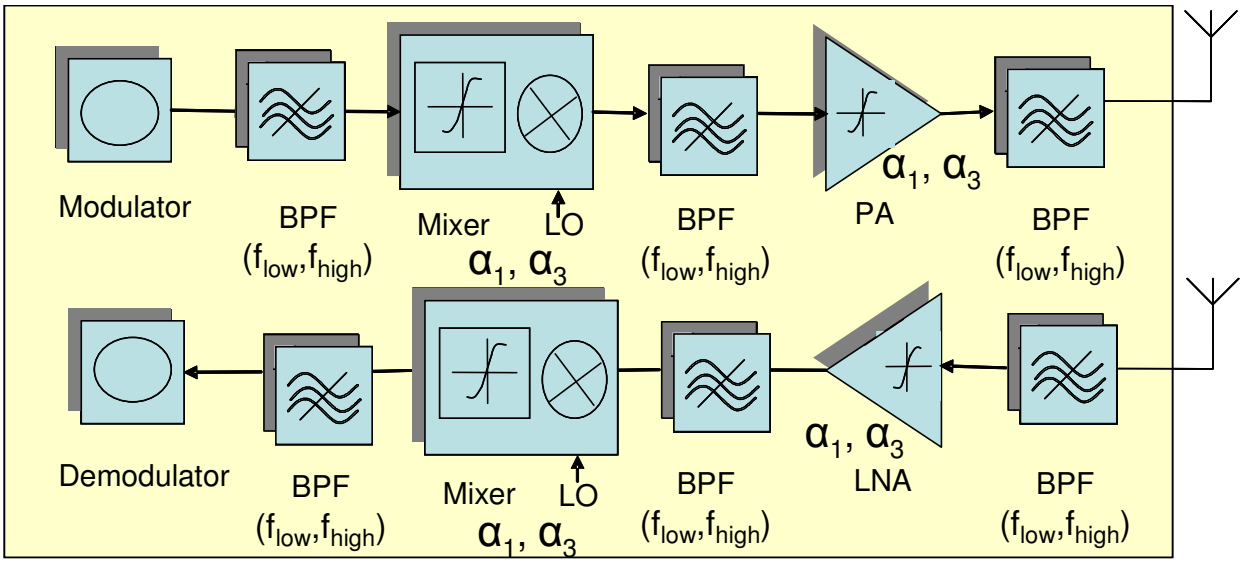


Figure 41. Block diagram of the behavioral models used for test generation of an RF transmitter and receiver subsystem-under-test.

3.3 BEHAVIORAL MODEL DEVELOPMENT OF TEST RESOURCES

In conventional test approaches, the test development is performed based on the assumption that the test resources are ideal. This assumption though valid for an expensive ATE that is electrically quiet and possesses the ability of sampling DUT signals with high-resolution and low-jitter. Tighter margins for noise and linearity translate into increased test challenges, because manufacturers need ATE with higher dynamic range and noise precision to accurately test these parts while maintaining an affordable cost-of-test. Advanced tester platforms similar to Credence ASL 3000 [84] and certain configurations of Teradyne Catalyst have been developed in the past to support such high sensitivity measurements. To fuel continued growth of the RF device/systems in the wireless communication market, it becomes impossible, if not difficult, to provide such high-cost test solutions.

The transition of ATE platforms to low-cost rack-and-stack ATE or baseband ATE for production testing of RF systems adds another dimension to this problem. These ATEs typically provide resolutions of 12 to 14-bit based on their configuration. Also, in the case of baseband ATE, specific test resources need to be added onto the loadboard (BALUNs, mixers) to process the test signals. Due to these reasons, it becomes necessary to model the nonlinearities and gain/loss characteristics of (1) the test resources (ADC and DAC) used to source and capture the test signals to and from the DUT and (2) the DfT resources on the loadboard used to relay the test signals to and from the DUT to the ATE for reliable and accurate test generation purposes.

The suite of components that need to be modeled in the case of a low-cost baseband ATE (Figure 42) include (1) the mixed-signal resources like the source (DAC) and digitizer (ADC), (2) the DfT resources like passive mixers, SMA connectors, RF coaxial cables, attenuators, BALUNs, and matching networks, and (3) the PLL used to provide the local oscillator(LO) signal to the DfT mixers used to provide up-conversion and down-conversion of the test signals. The passive DfT components are modeled using a simple S_{21} (magnitude and phase) transfer function model. The active components are done is a similar methodology as proposed for the amplifiers/mixers in the RF system-under-test. The DfT PLL model is also modeled using the PLL model developed for modeling the RF system-under-test. In addition to these models, the developed ADC and DAC models are explained below.

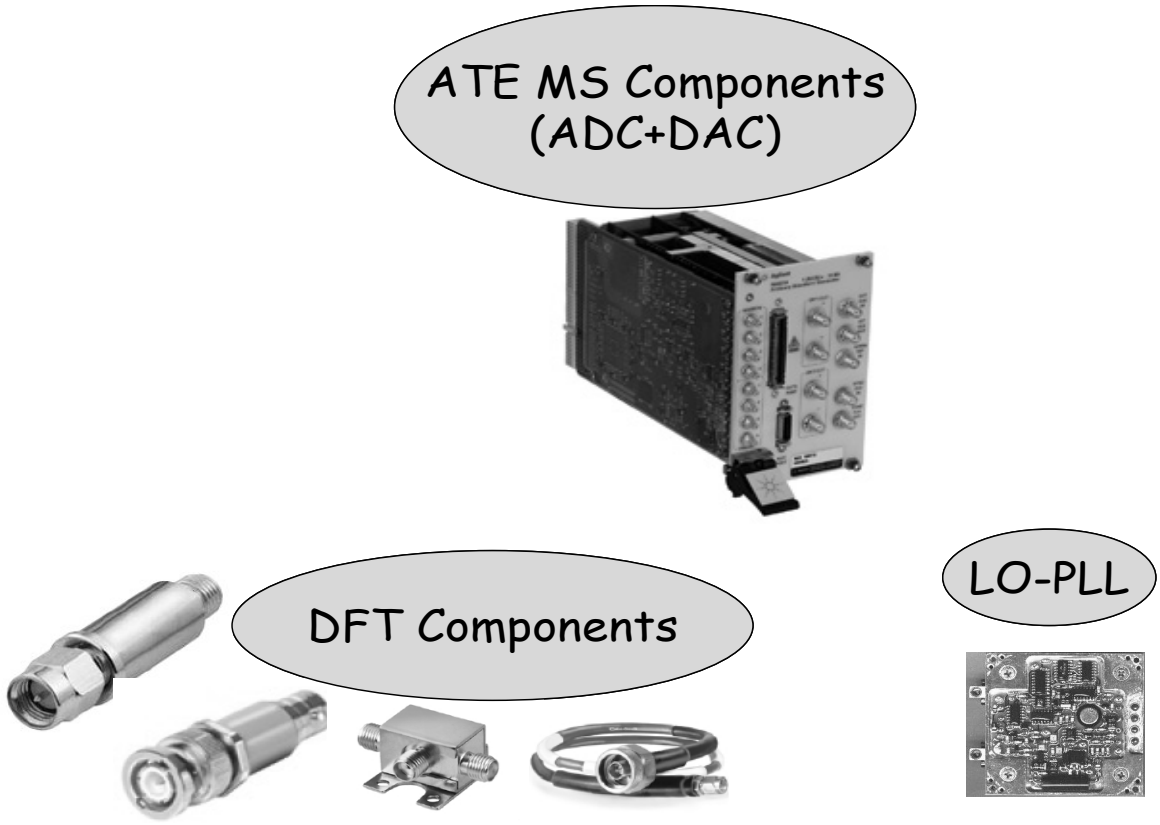


Figure 42. Suite of components that need to be modeled for accurate test generation using low-cost baseband ATE.

3.3.1 Behavioral model development for the ATE mixed-signal components

The ATE components like the DAC (AWG) and ADC (digitizer) were modeled with suitable gain, offset, integral nonlinearity (INL) and differential nonlinearity (DNL) errors in their code edges. This model is a time domain-based model as accurate frequency domain-based models for these components do not exist. Since the RF system, DfT components and other test resources are modeled in the frequency domain, fast Fourier transform (FFT) and inverse-FFT (IFFT) operations are used in conjunction with this block to provide a suitable interface with the rest of the CAD framework.

The nonlinear static errors, i.e. the INL and DNL errors, to be used in this model, can be obtained by simple ramp tests. Based on the transfer function computed from the ramp tests, the

DNL at the code edges are computed by the conventional histogram method [107][108]. The corresponding INL error at the n^{th} code edge is the cumulative sum of DNL errors up to the n^{th} code and can be represented as:

$$INL\ (i) = \sum_{j=1}^{i} DNL\ (i) \qquad \textbf{Equation 25}$$

These static nonlinearities were incorporated in the model by altering the quantization code edges accordingly with suitable gain and offset errors (obtained from the data sheet). The algorithms developed to perform the ADC and DAC operation are explained below. Binary search was employed in both these algorithms for fast test generation purposes.

Table 9. Pseudo code for digital to analog conversion (DAC operation).

ncde: Number of code edges in the DAC
input: Digital codes of the MTPR waveform
analog_output: Analog waveform corresponding to input digital codes

Input: (ncde, input)

```
1)  While i < ncde
2)      If i = ncde
3)          index = find(input = i)
4)          analog_output(index) = DAC_code_edge(i)
5)      Else
6)          index = find(input = i)
7)          analog_output(index) = (DAC_code_edge(i) + DAC_code_edge(i+1))/2
8)      End if
9)  End while
```

Output: (analog_output)

Table 10. Pseudo code for analog to digital conversion (ADC operation).

nob: number of bits in the ADC
Input: Analog MTPR waveform
digital_output: Digital codes corresponding to input MTPR waveform**.**

Input: (nob, input)

```
1)  digital_output = 0
2)  While i < nob
3)        digital_output = digital_output + (2(nob- i))
4)        index = find (ADC_code_edge(digital_output) > input)
5)        digital_output(index) = digital_output(index) –  2(nob – i)
6)  End while
```

Output: (digital_output)

3.4 GENETIC ATPG FOR FAST TEST VECTOR COMPUTATION

In this work, a genetic algorithm based ATPG is used to optimize the test patter/vector for the alternate test framework.

3.4.1 Introduction to genetic algorithms:

Genetic algorithms (GAs) are the most popular of the evolutionary computation (EC) algorithms based on the mechanics of natural selection and natural genetics [65][66]. They combine the idea of survival of fittest among the potential candidates with a structural yet randomized information exchange to form a search algorithm. In every step of the evolution process, a new set of candidates (strings) is created using genes of the fittest of the old candidates. An occasional new candidate is also evaluated for good measure. The main differences of the GA from other optimization and search procedures are,

(1) GAs use the objective function in a direct manner to find the fitness rather than derivatives (gradient search) or other auxiliary knowledge.

(2) GAs search from a population of points and not from a single point like many other methods

(3) GAs use probabilistic transition rules and not deterministic rules.

(4) GAs tend to be best suited for problems in which the objective function evaluation involves expensive simulations.

GA terminology: Since the GAs have their roots in both genetics and computer science, the terminology employed is a mixture of both these worlds [66]. A *'chromosome'* or '*genetic string'* is used to represent each candidate in the population in some encoded form. This chromosome is a collection *'genes'*, which play a role in the algorithm's iteration process in a way similar to the biological role of genes in natural evolution. The central idea of the GA is to move a set of chromosomes from an initial collection to a point where the fitness function is optimized. This optimization process is performed through certain basic operations like *elitism*, *selection*, *crossover* or *reproduction* and *mutation*, which are explained in detail in the following subsection.

3.4.2 GA based ATPG algorithm

Most forms of GA use encoding schemes to represent the operator for optimization purposes. Usually, genetic strings are used to represent the operator as they facilitate the operation of the GA. In the past, many forms of encoding schemes have been proposed. A few to mention would include binary digit (0,1), gray coding, and multiple-character schemes. In most GA applications, constraints are enforced on the operator values and during each iteration all the chromosomes in the population collection would need to be decoded to enforce these constraints. Also, to compute the objective function decoding needs to be performed to convert the operator to a meaningful physical value.

Since the bit space can be directly used for fitness computation purposes in the proposed CAD framework, these bitstreams could be directly used as the chromosomes. This would eliminate the need for an encoding scheme and thus reduce the overall computation time. In the rest of this subsection, each operation involved in the GA optimization routine is presented. The flowchart of the complete optimization routine is presented in Figure 43. The input parameters to the algorithm along with their descriptions and sample values are summarized in Table 11.

Table 11. Description of the input parameters to the genetic ATPG along with sample values.

Name	Description	Sample values
N	Size of each chromosome (no. of genes)	10
Num_Bits	Total number of bits in the test stimulus packet	100
Pop_Size	Number of individual chromosomes in the population collection of each iteration	20
Elite	No. of elite chromosomes to be retained for subsequent iteration	6
Cross_Prob	Crossover probability	0.9
Mutat_Prob	Mutation probability	0.08
DELTA	Number of iterations to be counted for the termination criteria.	20
EPSILON	Range that the fitness must change in the termination criteria	0.05
MAX_Iterations	Number of times the loop will run before the EPSILON-DELTA termination condition is met	100

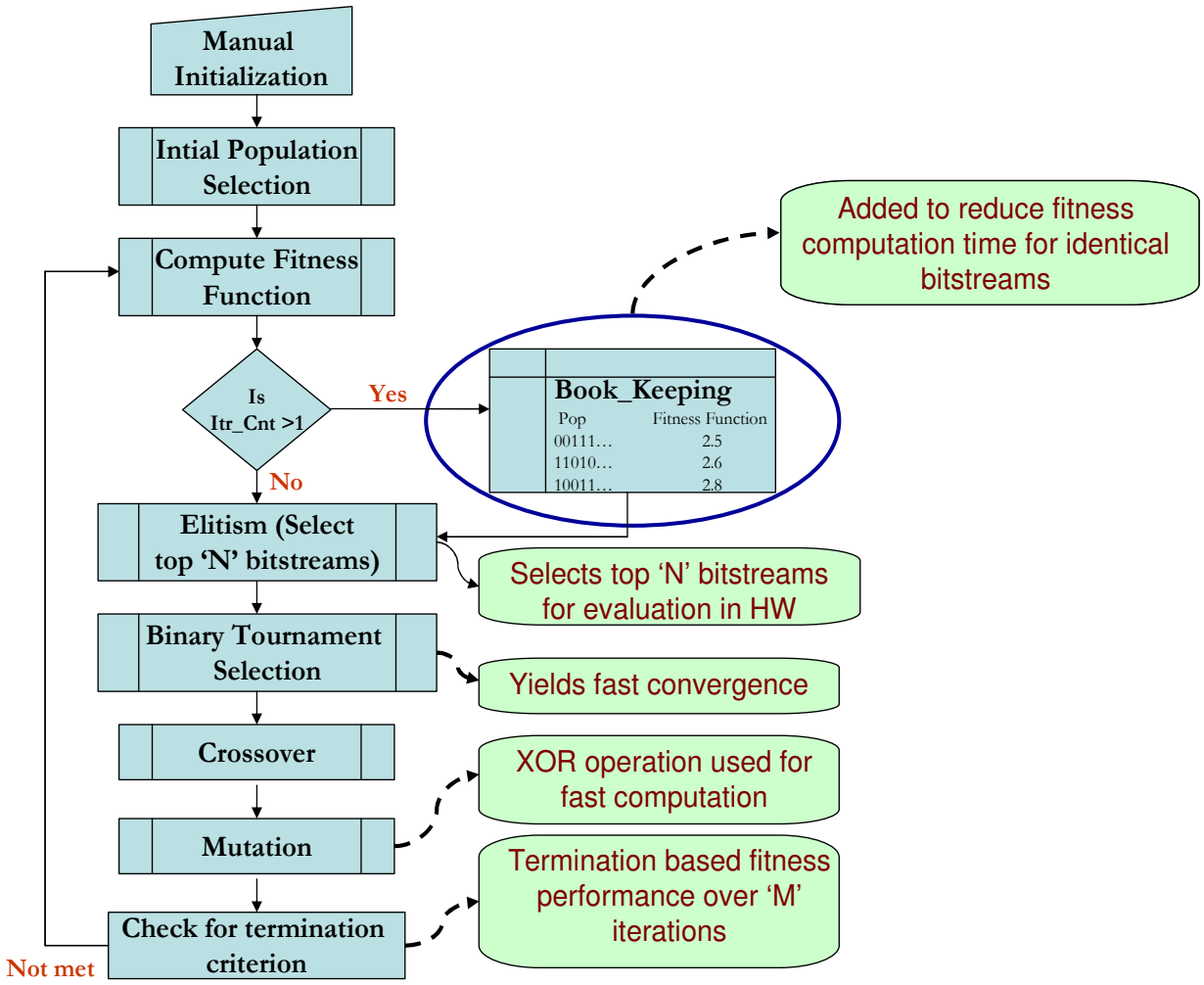


Figure 43. Flowchart of the GA based optimization routine.

In the developed ATPG, the initial population of the GA is chosen at random form a set of all possible configurations of digital bitstreams of the specified size 'N'. This kind of approach ensures that the initial population for the GA contains bitstreams with varied spectral features. To establish the concept of 'survival of the fittest', and to ensure that parents with stronger genes are selected for reproduction, the fitness of the genetic strings is computed during each iteration. This fitness computation might be simple when the objective is to optimize the operator (e.g. θ) in a linear or nonlinear equation to maximize or minimize the objective function

f(θ). In the case of test generation for highly complex nonlinear systems using statistical regression, as in the proposed framework, the chromosomes need to be applied to multiple instances of the modeled SUT instances to evaluate the quality of the computed regression models. The flowchart of the algorithm used to compute the fitness of each chromosome in the population is shown in Figure 44. The candidate stimuli are first modulated onto sine waves based on the user-specified modulation details e.g. type, data rate, baseband carrier frequency, etc. The modulation details are based on the type of modulation scheme employed by the transceiver during application in wireless communication (e.g. GMSK for GSM, GFSK for Bluetooth) and the configuration of the transmitter or receiver chain. For FSK modulation standard, the input parameters to the algorithm, description of these input parameters and sample values are presented in Table 12.

Table 12. Description of the modulation parameters input to the APTG along with their sample values.

Name	Description	Sample values
`baseband_Clk`	Data rate of the baseband information	`25e3`
`baseband_Carrier`	Baseband carrier frequency	`200e3`
`Sampling_Freq`	Sampling frequency of the DAC and ADC used to source and capture the baseband signals	`8*baseband_Carrier`
N_{FFT}	Number of FFT points used in frequency domain simulation and spectral signature extraction	`3200`

The modulated signals are applied to a set of behavioral instances of the RF system derived with a statistical distribution close to that observed in high-volume production. The behavioral models of the subsystem-under-test and the test resources are developed as explained in Section 3.2 based on the configuration of the subsystem-under-test and the employed ATE resource. For example, in the case of ZIF TX subsystem tests, the blocks that need to be modeled include the DAC in the ATE, the mixer/PA combination with suitable BPFs, loadboard resources employed to downconvert the TX RF signals to baseband frequencies and relay them to the ATE, and the ADC resources of the ATE used to capture the test response.

The behavioral parameters of the developed TX subsystem model are perturbed to generate a set of 'training' and 'validation' instances. The modulated signals are passed through the set of training instances and the response for each of the 'N' chromosomes in the current population are captured and stored. The FFT of each of these test responses are computed and the amplitude values at specific predetermined bins are selected and stored for further processing. The specific bins are determined by their presence in the spectral signature of a nominal device. Simultaneously, the specifications are measured for each of the transmitter instances using the standard testing procedure. After this operation is performed over all the training instances, N individual nonlinear regression models are built, one for each chromosome, using MARS [32].

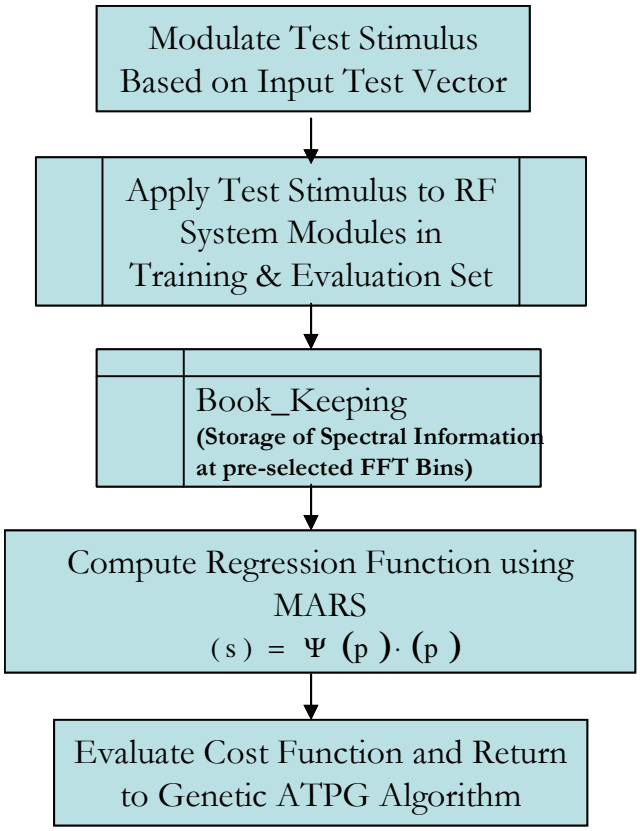


Figure 44. Flowchart of the GA based optimization routine.

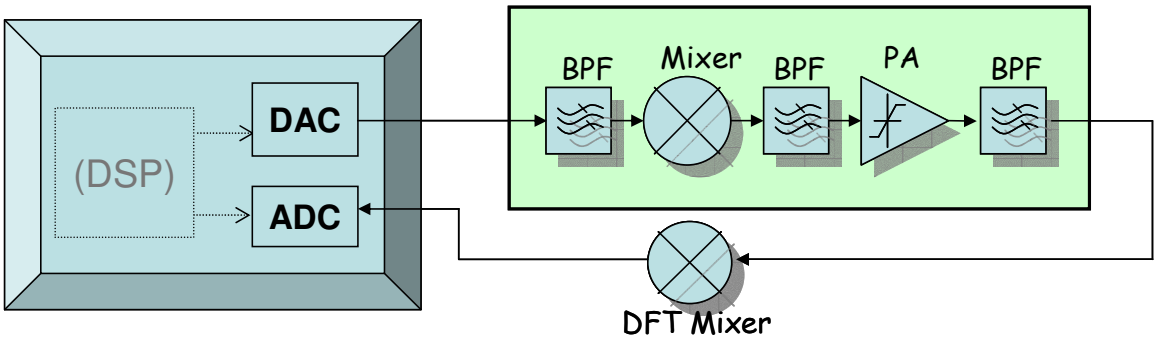


Figure 45. Flowchart of the GA based optimization routine.

In the validation step, the modulated signals corresponding to the N chromosomes are input to a set of validation instances. These instances are generated using a different set of behavioral model parameters than the ones used for generating the training set, but with the same statistical properties (mean and variance). The spectral signatures computed from the test response of these systems are then input to the corresponding regression model to predict their specification values. Simultaneously, the specification values of these devices are also measured with the standard test set-up. Finally, the specifications obtained from the model are compared to the specifications obtained through measurement to compute the fitness function.

In this work, the objective was to maximize the *inverse* of the maximum prediction error (i.e. absolute difference) between the measured specification matrix S obtained using the standard measurement approach and the computed specification matrix $\hat{S}$ obtained using the proposed approach. The inversion was performed to convert the error minimization problem to a maximization problem which is more suited for GAs. The fitness function (f_{cost}) can represented as the minimum of the difference matrix D, where $D = \left| S - \hat{S} \right|$.

$$f_{cost} = \min(d_{ij})$$

where i corresponds to the i^{th} device in the training set and j corresponds to the j^{th} specification of interest. An alternative to the maximum error will be the sum of errors in the computation of different specifications weighted by their total test cost in the conventional approach (function of test time and test resource). In this work, the assumption was that all tests are equally expensive and hence the maximum error over all the specifications is used to optimize the bitstream.

A novel bookkeeping operation was introduced to GA based optimization algorithms. In this operation the fitness of the chromosomes at each iteration are stored in a table for future reference. This saves considerable time in the overall optimization process as the fitness for

repeated bitstreams can be easily picked-off from this table using a fast search algorithm. An elitism step is performed after computing the fitness function of all the chromosome in the current population, to place $N_e < N$ fittest chromosomes in the population for the next iteration. This guarantees the preservation of the fittest chromosomes commonly referred to as the 'elite chromosomes'. Also, these elite chromosomes are available for the reproduction operations like crossover and mutation performed at a later stage of this algorithm.

In the selection stage of the GA algorithm, the parents with stronger genes that need to mated to create $N-N_e$ offsprings for the next iteration are chosen. The main aim is to emphasize the fitter chromosome in the selection process so that the derived offsprings tend to have higher fitness functions. It must also be noted that very high preference given to fitter chromosomes may lead to premature convergence. In this work, binary tournament selection was used to select the parents as it tends to have faster convergence properties as opposed to the forms of selection methods commonly associated with GAs. In binary tournament selection, two individual chromosomes are selected at random and the fitter of the two is chosen for reproduction.

Crossover and mutation operations were performed to mimic the reproduction in the evolution process. Crossover operation creates offspring of pairs of parents selected by the selection operation. A crossover probability determines if the offspring will represent a blend of the chromosomes of the parents. If crossover does not take place the offspring's are exact clones of the parents. In this work, a single-point crossover operation was employed. This operation is pictorially described in Figure 46.

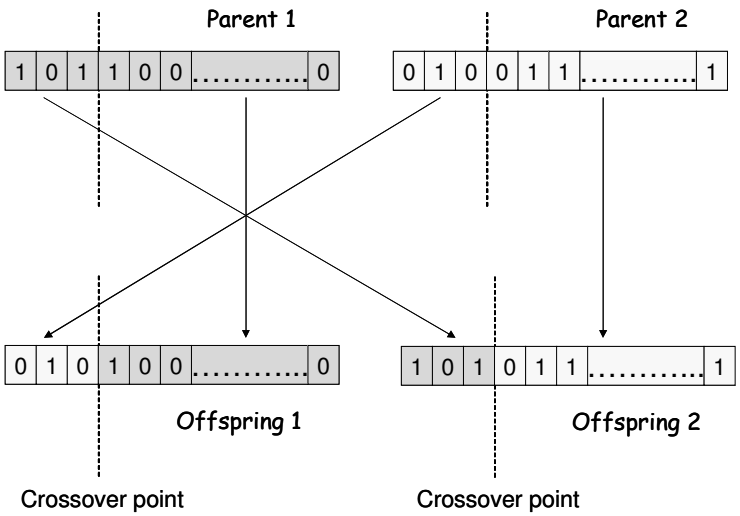


Figure 46. Pictorial description of the single-point crossover operation for reproduction in the GA.

Since it may not be possible to find the optimal solutions via crossover alone, the GA uses the mutation operation, in which the chromosomes are flipped in a random fashion. This operation is also based on a particular probability that is much smaller compared to the crossover operation, to preserve the good chromosomes created by the crossover operation. To increase the speed of this operation, an XOR type of mutation operation is introduced. In this type of mutation operation, a matrix with the same size of the current population elements, generated in a random manner based on the input mutation probability (P_m), is XORed with the new created population to yield the population for the next iteration.

The termination of the optimization algorithm was based on the total number of iteration (specified in the MAX_Iterations variable input by the user) or by detecting less than 'epsilon' change in the error values of the elite bitstreams over 'delta' number of iterations. The epsilon and delta values are set by the user depending on the test application. One of the above two phenomena are used to terminate the algorithm based on their precedence of occurrence.

3.5 HARDWARE VALIDATION OF THE PROPOSED CAD FRAMEWORK

A 1.5 GHz wireless RF transmitter prototype was used as a test vehicle to demonstrate the proposed genetic ATPG for spectral signature-based tests. The hardware setup implemented for this demonstration is shown in Figure 47.

3.5.1 Hardware Setup

The baseband processor (implemented in Matlab) is used to modulate the optimized digital bitstream using the specified modulation technique. This data is then input to the transmitter prototype through the DAC in the data acquisition card (DAQ) PCI 6115 manufactured by National Instruments. The modulated data is then up-converted and amplified by a 1.5 GHz transmitter prototype. The spectral output of the transmitter is then downconverted to baseband frequency using a wideband passive mixer DfT resource (Minicircuits ZX05-series). The downconverted spectrum is then captured by the ADC in the same DAQ card and fed back to the baseband processor. The DAQ card was used as a low-cost ATE replacement in this experiment.

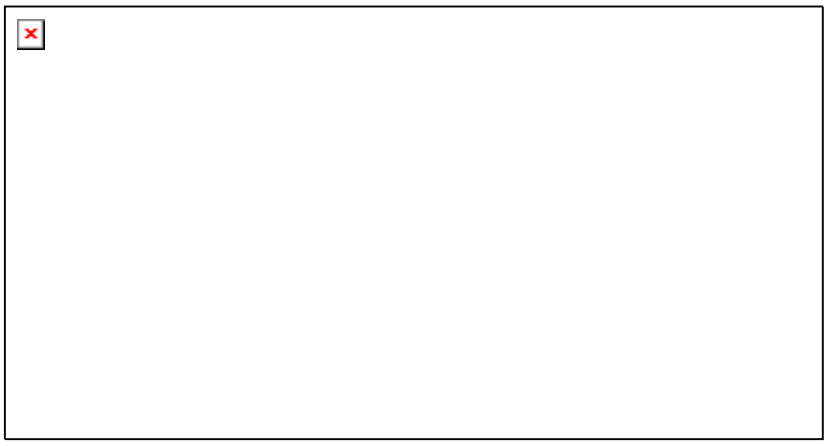


Figure 47. Hardware setup of the 1.5GHz transmitter prototype.

In the transmitter prototype, the incoming modulated data bitstream is unconverted by a CDMA up-converter/modulator RF2641 (manufactured by RFMD) with an operating frequency

range of 300 to 2700 MHz. The LO signal for upconversion was a 1575 MHz sine wave with an amplitude level of -10 dBm. The mentioned power level is the desired power level at the LO input terminal of the mixer. Hence, suitable de-embedding algorithms were performed to compensate for any losses along the RF path.

The upconverted signal is then amplified by a PA, UPC 2763TB (manufactured by NEC electronics), designed to operate in frequency range of 900-2700 MHz. This amplified spectrum is then downconverted by the passive DFT mixer to baseband frequencies within the capture bandwidth of the DAQ card. The LO signal for the passive mixer was fixed at a center frequency of 1575 MHz with and an amplitude level of -10 dBm (considerations similar to that of the upconverter are required to ensure the delivery of a correct power level to the LO terminal of the passive mixer). A picture of the RF prototype highlighting the mixer and the PA devices along with suitable matching circuits is shown in Figure 48. The PCI 6115 DAQ card can operate at a maximum sampling speed of 10 Msps with a maximum data output rate of 4 Msps at 12-bits of resolution.

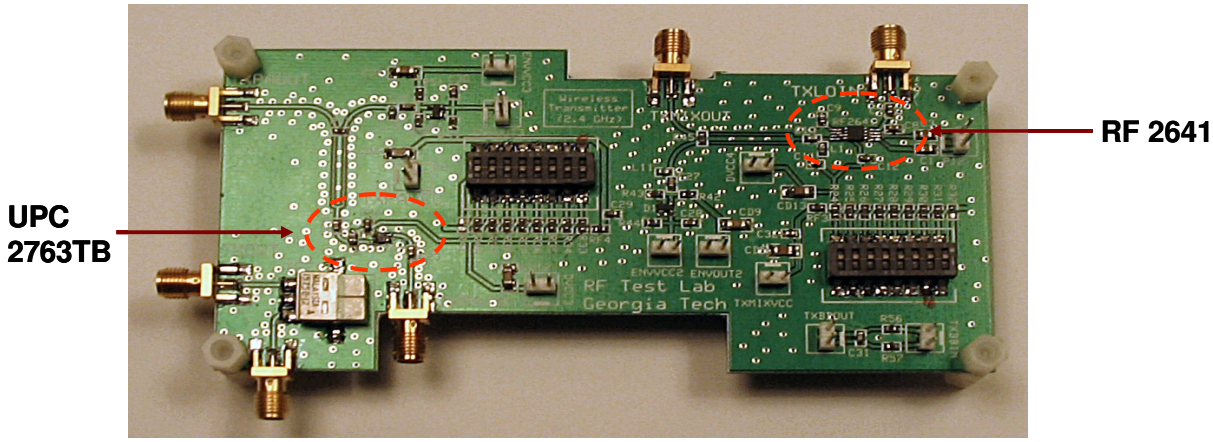


Figure 48. 1.5 GHz RF transmitter prototype.

To generate the training and validation instances, multiple instances of the transmitter prototype were generated by varying the supply voltage of the active components in the RF

front-end. The nominal operating supply voltage for the PA and mixer was 3 V each. The supply voltage of the PA was varied from 2.2 to 3.6 V and for each of these values the supply voltage of the mixer was varied from 2.4 to 5 V. In total, 405 transmitter instances were generated using this approach for the purposes of training and evaluation. Instances can also be created using multiple ICs via test sockets on the prototype board. However, the supply voltage variation has the following advantages:

- The range of variation of the specifications is much larger than the ones obtained using multiple off-the-shelf components, thereby depicting a worst case scenario for a prediction based methodology
- Unlike sockets they do not act as a source of random invariability

3.5.2 Conventional specification based tests

The specifications of the transmitter chain such as gain and IIP3 were computed using the conventional test setup and test equipments for the purposes of training and evaluation of the proposed test approach. The test setup used to perform the conventional specification-based tests on the transmitter prototype is shown in Figure 49. An Agilent spectrum analyzer E4407B was used to capture the RF output spectrum of the transmitter prototype. A HP signal generator 8648D is used to provide LO to the mixer module of the RF transmitter prototype. Keithley source meters are used to provide the required supply voltages to the component modules of the prototype.

3.5.2.1 Gain specification test

A single tone test input was provided to the transmitter prototype by an arbitrary waveform generator HP33120A to test for the transmitter system gain of each instance of the

prototype. The corresponding spectrum output for each instance is observed with the help of the spectrum analyzer. GPIB commands were used to control the measurement equipments from the Matlab environment to automate the entire process.

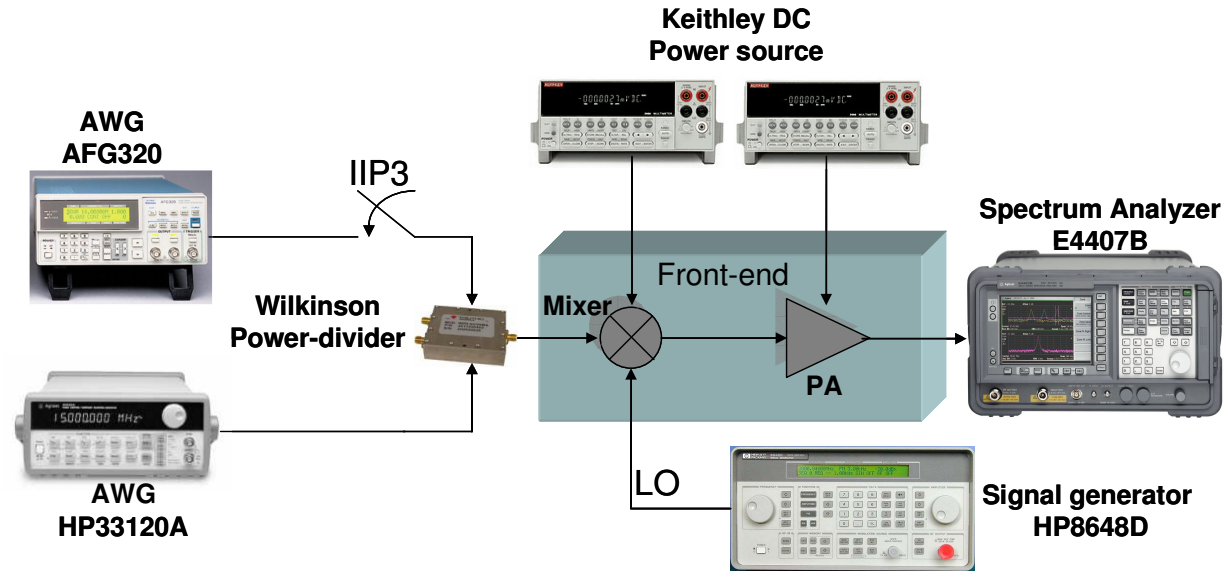


Figure 49. Test setup to measure the performance specifications of the transmitter instances using the conventional approach.

3.5.2.2 IIP3specification test

For this specification, two AWGs HP33120A and AFG320A were utilized to provide two input tones with closely placed frequencies and identical amplitudes. These tones were combined using a Wilkinson power combiner designed to operate at 1.5 GHz. The RF spectrum at the output of the transmitter is observed with the help of the spectrum analyzer and the corresponding IIP3 values are computed form the observed RF spectrum. Similar to the previous test case, GPIB codes are developed to automate the measurement process.

3.5.3 Test generation using the Genetic ATPG algorithm

The behavioral parameters of the component modules were characterized by their input–output transfer curves. The characterization curves for the upconverter and the power amplifier are shown in Figure 50 and Figure 51 respectively.

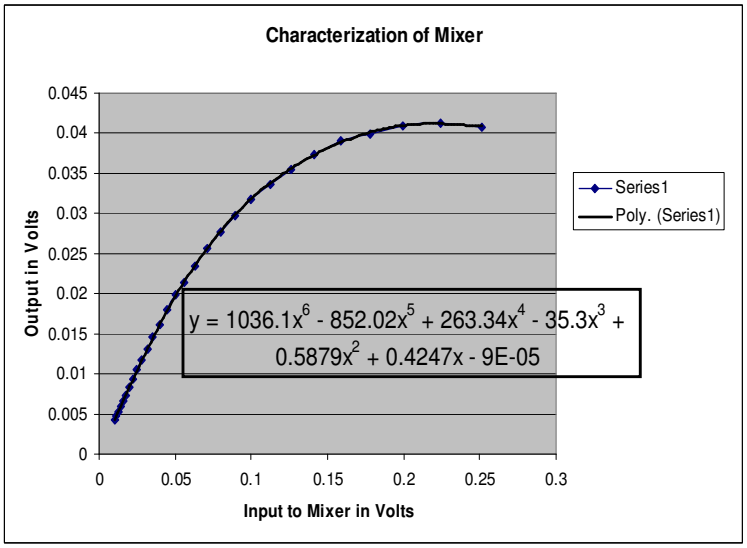


Figure 50. Characterization curve for up-conversion mixer.

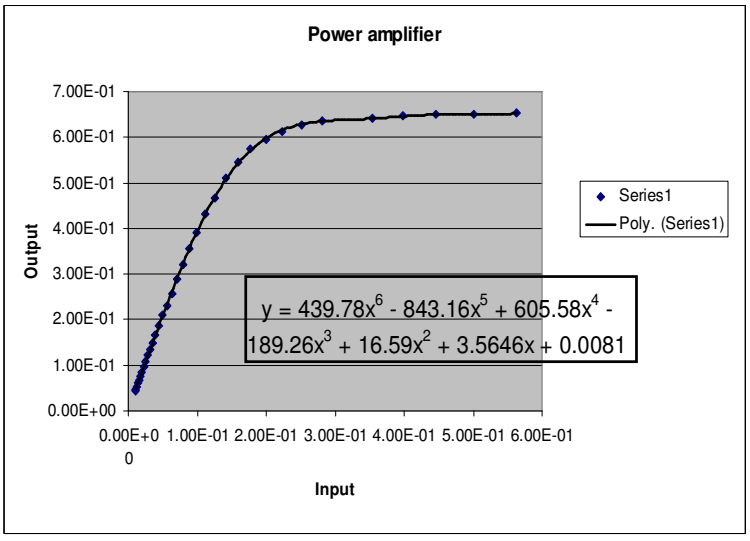


Figure 51. Characterization curve for the power amplifier.

The INL, DNL, gain and offset error for the ADC and DAC resources in the DAQ card were obtained from the datasheet. The optimization was performed for these models using the CAD framework for two modulation schemes FSK and GMSK (BT=0.3). A plot of the average fitness of the elite chromosomes as a function of iteration count for both these modulation schemes is shown in Figure 52. To study the impact of the performance of the low-cost test resources on the developed tests, the optimization was also performed for a 10-bit resolution limitation in the DAQ card. The plots of the fitness obtained in this experiment as a function of the iteration count is shown in Figure 53.

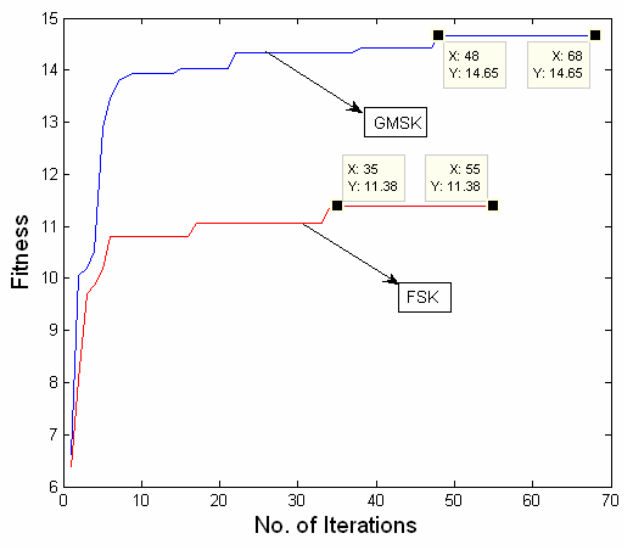


Figure 52. Plot of average fitness of the elite chromosomes as a function of iteration count for 12-bit DAQ card.

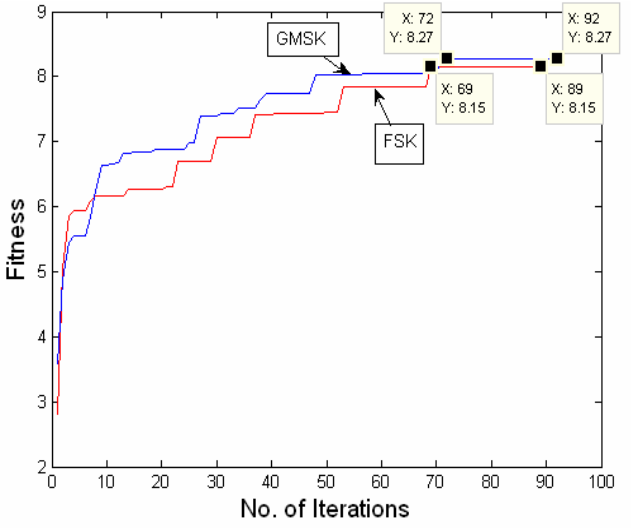


Figure 53. Plot of average fitness of the elite chromosomes as a function of iteration count for 10-bit DAQ card.

The fittest bitstreams generated by the genetic CAD framework were used in the hardware experiments to show the validity of the proposed ATPG tool. As explained earlier, 405 instances of the transmitter prototype were created, of which 320 devices (training set) were used to build the nonlinear regression equations. The conventional specifications for the training set of devices were also measured using the test setup presented in Figure 49. The spectral measurements were also preformed on these transmitter instances using the setup shown in Figure 54. The spectral measurements and the specification data were input to MARS to compute the nonlinear regression equations. The computed model was then evaluated for its quality with the help of the remaining 85 instances (evaluation dataset) of the transmitter prototype.

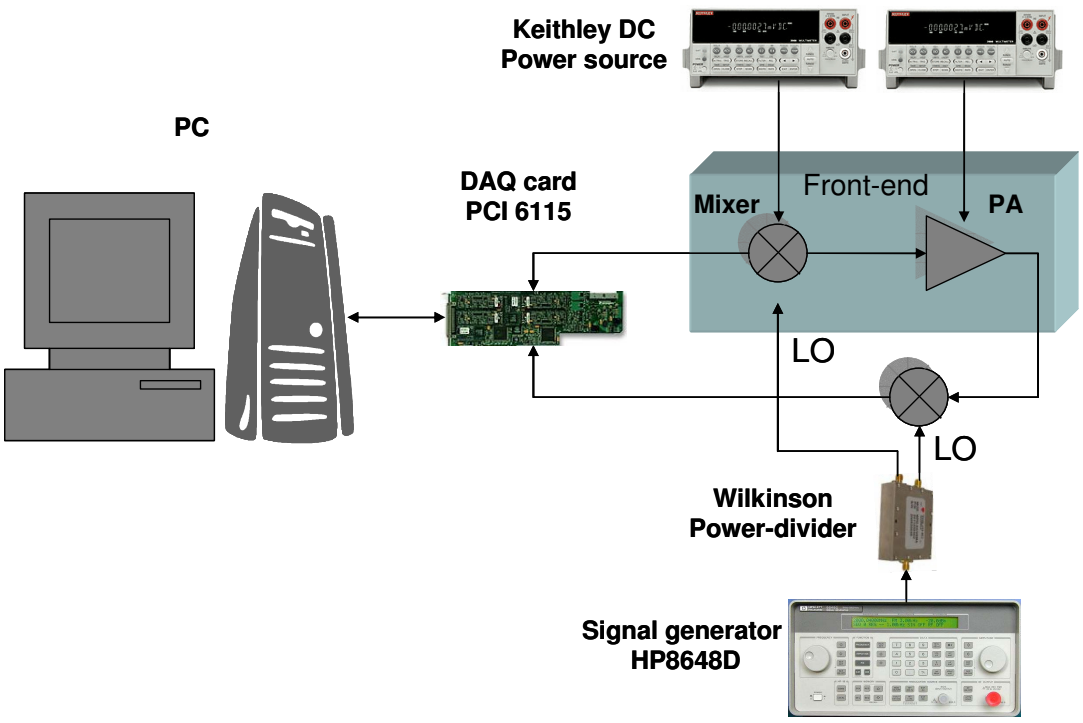


Figure 54. Measurement setup for the proposed alternate test methodology.

The following subsections discuss the observations of different case studies conducted on the prototype. Five different case studies are presented to analyze the validity of the test generation algorithm and to analyze the techniques that can impact the quality of the tests performed on the prototype.

3.5.4 Case Study 1: Performance of the optimized bitstream generated for the FSK and GMSK modulation schemes

In this case study, the observations of the prediction quality for the best fit bitstreams generated for the FSK and GMSK modulation schemes are presented. The spectrum of the best fit bitstream for the FSK modulation case to be transmitted through the DAQ card is shown in Figure 55. The corresponding transient response and its frequency spectrum captured by the DAQ card are shown in Figure 56.

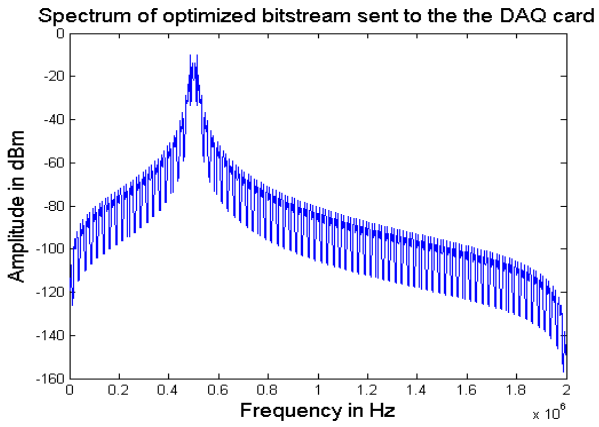
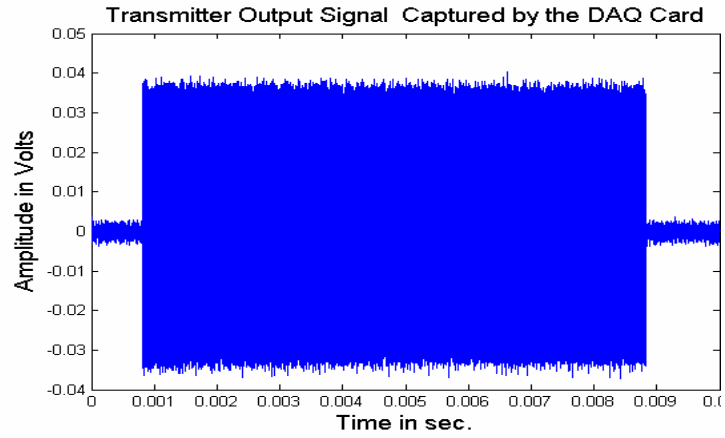
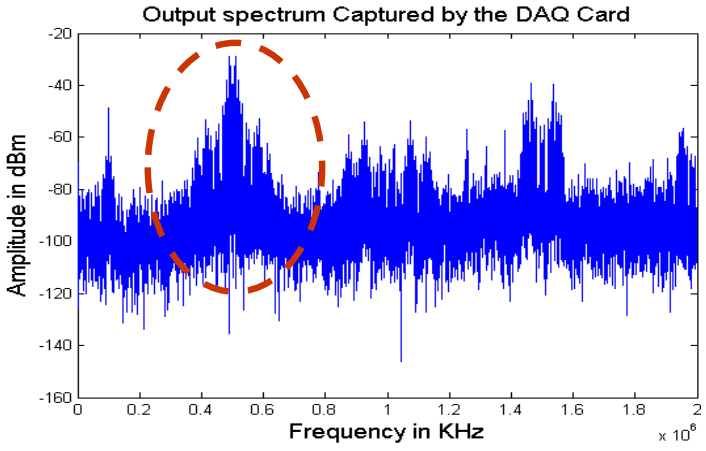


Figure 55. Spectrum of the optimized bit stream sent to the DAQ card.



(a)



(b)

Figure 56. Transmitter output captured by the DAQ card in (a) Time domain and (b) frequency domain.

In this work, scatter plots and statistics of the prediction error were used as the measures to qualify the accuracy of the proposed CAD framework. The scatter plot of the gain and IIP3 specification values for the evaluation set of devices for the FSK modulation scheme are shown in Figure 57. The scatter plots of the gain and IIP3 specification values for the evaluation set of devices for the GMSK modulation case are shown in Figure 58.

Table 13 summarizes the statistics (mean and standard deviation) of the prediction errors (measure of test quality) between the specification values measured using the conventional approach and the proposed approach for the FSK and GMSK modulation schemes. In the rest of the case studies only the results obtained for the FSK modulation scheme are presented.

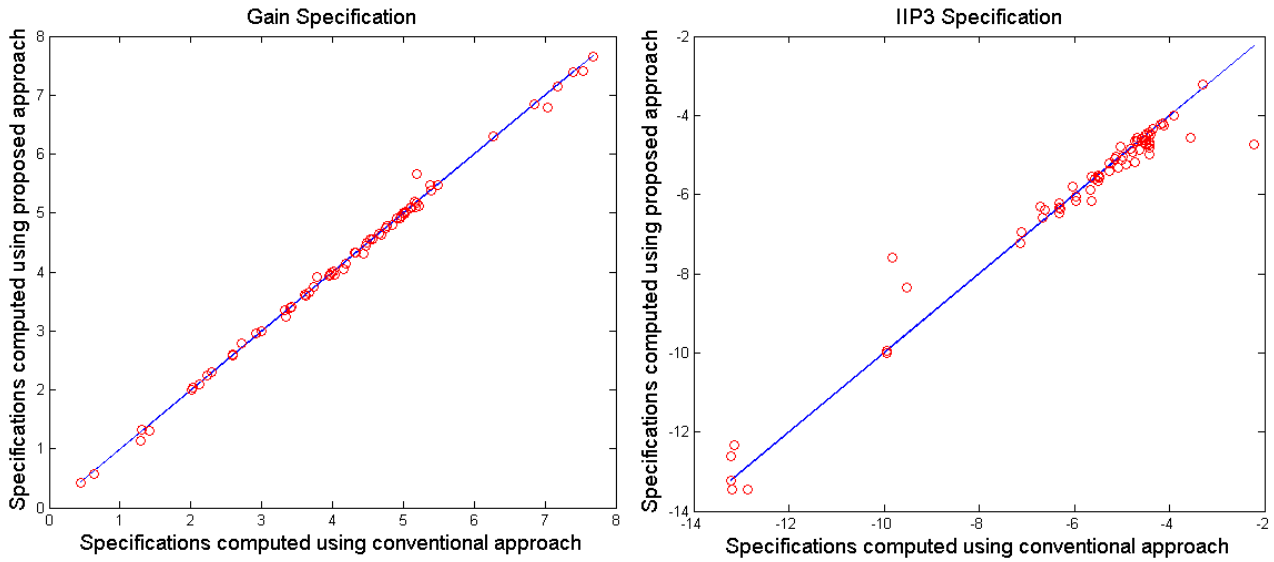


Figure 57. Scatter plots of the Gain and IIP3 specification values for the best fit bitstream using the FSK modulation scheme.

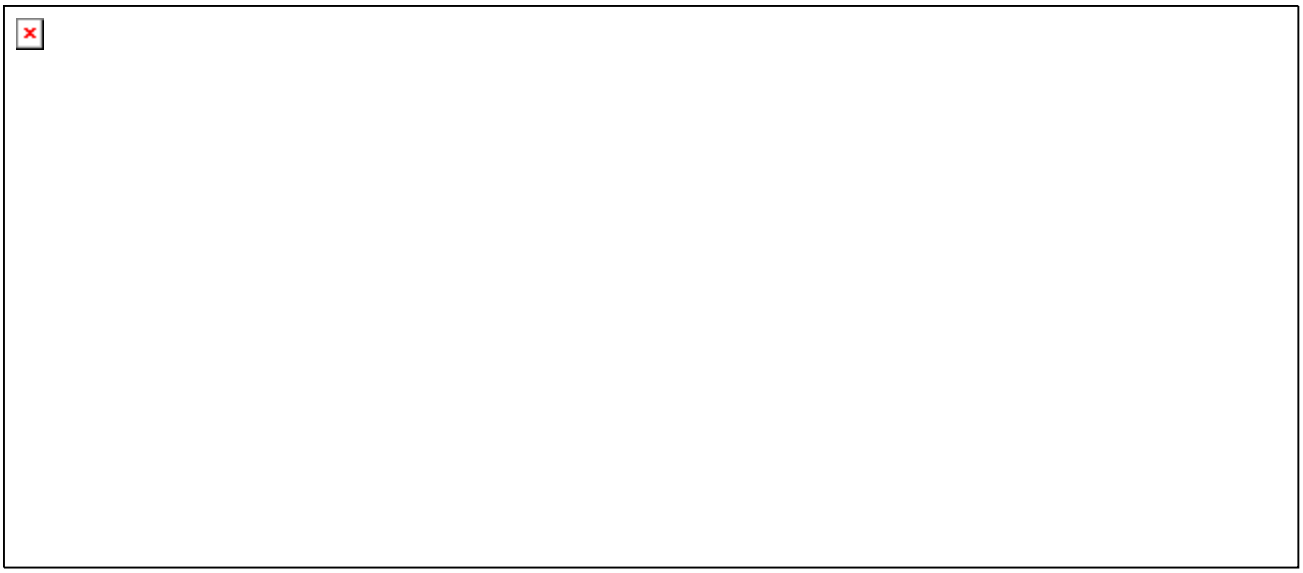


Figure 58. Scatter plots of the Gain and IIP3 specification values for the best fit bitstream in the using the GMSK modulation scheme.

Table 13. Summary of statistics of the prediction error obtained in the specification values for the FSK and GMSK modulation schemes.

FFT Complexity	Gain computation		IIP3 computation	
	Avg. (μ) dB	Std (σ) dB	Avg. (μ) dB	Std (σ) dB
FSK	0.04	0.07	0.25	0.42
GMSK	0.08	0.15	0.20	0.37

3.5.5 Case Study 2: Analysis of the prediction quality based on the length of the bit stream

In this case study, the summary of results observed during analysis of the effect of the length of the bit stream on the prediction quality of the proposed test approach is presented. The bitstream with the highest fitness value in the FSK modulation case was used for this purpose.

The length of the bitstream was repeated 10 times and is compared against the prediction achieved by repeating it 20 times. The resulting prediction errors are summarized in Table 14.

Table 14. Summary of the prediction error for two different bitstream lengths.

No. of times the bitstream was repeated	Gain computation		IIP3 computation		Response Capture Time (ms)
	Avg. (μ) dB	Std (σ) dB	Avg. (μ) dBm	Std (σ) dBm	
10	0.05	0.07	0.27	0.60	5
20	0.04	0.07	0.25	0.42	10

It can be observed that the prediction quality increases with the increase in the bitstream length. However, it should also be noted the test time required to capture the response is also on the rise. It's a tradeoff that is best decided by the quality of the required test.

3.5.6 Case Study 3: Analysis of the prediction quality based on the length of data that needs to be captured

This case study analyzes the effect of the length of data captured by the DAQ card to build the nonlinear models based on their prediction quality. The bitstream with best possible fitness was again used in this case study. The prediction quality of the model computed based on the entire spectrum (fundamental and harmonics) captured by the DAQ card is compared against the model built on the band limited (DSP band pass filtering) output of the transmitter consisting of only its fundamental output spectrum. The captured spectrums with and without DSP-based BPF are shown in Figure 59 and Figure 60 respectively. The statistics of the prediction error values for both these cases are summarized in Table 15. The scatter plots for the gain and IIP3 specifications for the case without the BPF are already presented in Figure 57. The corresponding scatter plots with the employed BPF are shown in Figure 61. In the rest of the case

studies only the band limited output is used to demonstrate the accuracy of the proposed approach

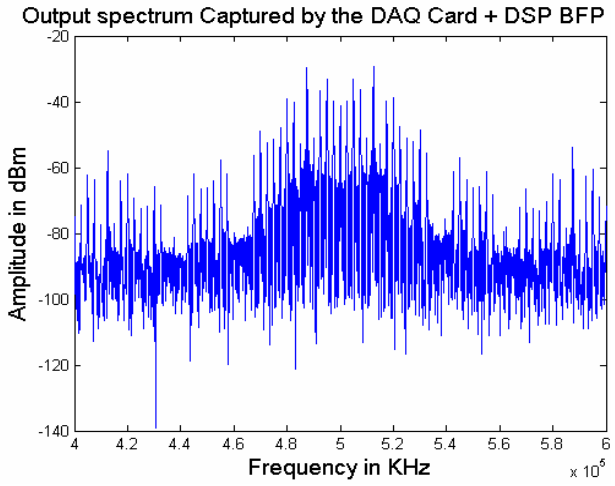


Figure 59. Output Spectrum of the transmitter with DSP-based BPF.

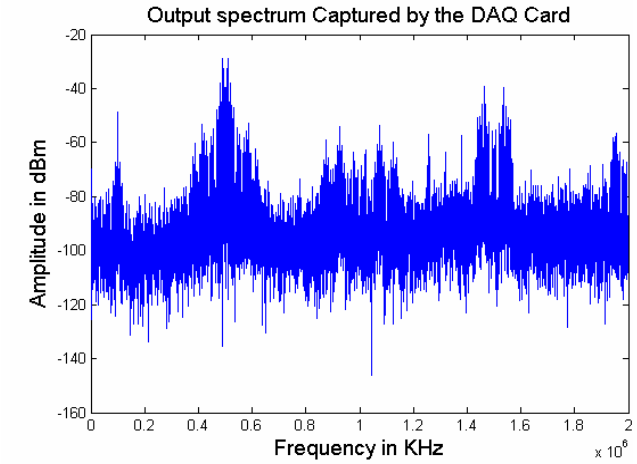


Figure 60. Output Spectrum of the transmitter without DSP-based BPF.

Table 15. Summary of Prediction errors with and without the BPF filtering.

Type of Filtering	Gain computation		IIP3 computation	
	Avg. (μ) dB	Std (σ) dB	Avg. (μ) dB	Std (σ) dB
With BPF	0.18	0.24	0.35	0.48
Without BPF	0.04	0.07	0.25	0.42

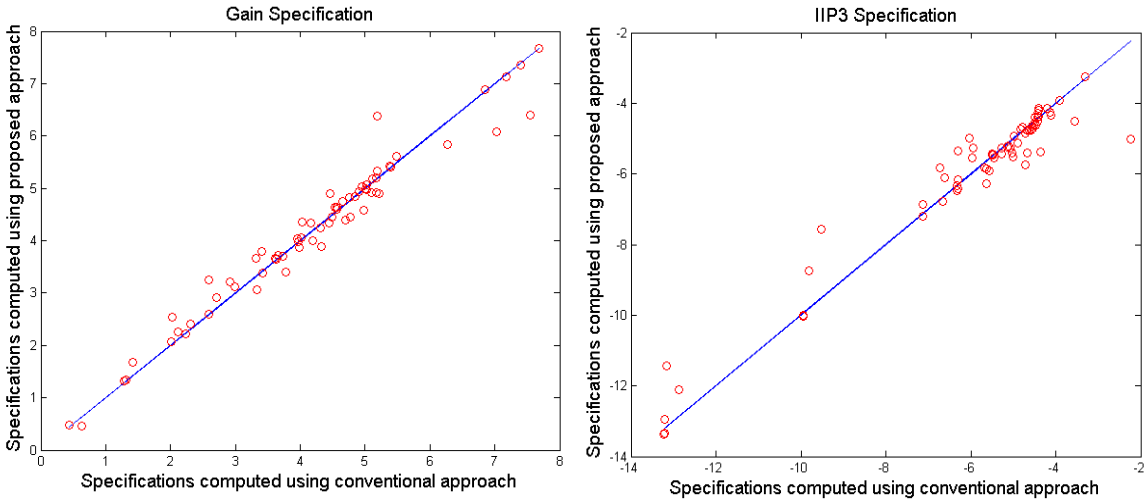


Figure 61. Scatter plots of the Gain and IIP3 specification values for the best fit bitstream using the FSK modulation scheme with the baseband BPF.

3.5.7 Case Study 4: Analysis of the prediction accuracy for the top '3' best fit bitstreams

Table 16 summarizes the top six elite bitstreams and their corresponding fitness values as generated by the GA-based ATPG. Table 17 summarizes the prediction errors for top three of these six bitstreams observed during the hardware validation process. From the Table, it can be observed that the mean prediction error in the Gain specification increases with the decrease in fitness value, thereby following the CAD performance.

Table 16. Summary of the fitness values of the top 6 bit streams observed during optimization.

Rank	Optimized bitstreams										Fitness
1	0	0	1	1	0	0	1	0	1	0	12.76
2	1	1	0	1	0	0	1	1	0	1	12.76
3	1	1	1	0	0	1	0	0	0	1	11.23
4	1	0	0	0	0	0	0	0	1	1	11.23
5	1	1	0	0	0	0	0	0	0	1	11.23
6	0	0	1	1	1	1	0	1	0	0	11.13

Table 17. Summary of the Prediction error for the top 3 bitstreams observed in the hardware experiment.

Optimized stimuli	Gain Prediction		IIP3 Computation	
	Mean error	Standard deviation	Mean error	Standard deviation
1	0.18	0.24	0.35	0.48
2	0.19	0.22	0.39	0.58
3	0.22	0.24	0.31	0.44

3.5.8 Case Study 5: Analysis of the prediction quality based on the FFT complexity

The time domain output response captured by the DAQ is operated upon by an FFT algorithm implemented in the DSP, to result in the frequency domain information. Based on the resulting spectral signature the regression models are computed. In this case study, the effect of number of points required to perform the FFT operation on the prediction quality of the model is analyzed. The bit stream with best possible fitness is chosen for this purpose. The statistics of the prediction errors in the speciation values as a function of the FFT complexity is summarized in Table 18. It can be observed that the prediction quality is better for FFT operations with higher number of points.

Table 18. Analysis of Prediction errors for different FFT complexities.

FFT Complexity	Gain Prediction		IIP3 Computation	
	Mean error	Standard deviation	Mean error	Standard deviation
40 K	0.18	0.39	0.35	40 K
20 K	0.29	0.46	0.42	20 K
10 K	0.44	0.51	0.74	10 K

In addition to the above-mentioned case studies, a repeatability study of the proposed approach was performed on a single selected instance of the RF transmitter. The results of this

study are summarized in Table 19. These values cannot be compared to any particular standard, as the standards are very much device dependant. But past experience shows that these error values are in the same orders of magnitude as other standard industry approaches. Also, the validation experiments of the proposed CAD framework show that all these specifications could be measured within 10 ms of test time (only measurement time) in a reliable and repeatable manner on low-cost ATE architectures (~1 cent-per-second). Standard test approaches followed by the industry suffer from increased test times due to the sequential approach on expensive RF ATE architectures (~5 cents-per-second)

Table 19. Summary of repeatability analysis performed on a single instance of the transmitter prototype.

Repeatability Analysis	Std. in Gain Computation (dB)	Std. in IIP3 Computation (dBm)
Proposed Approach	0.08	0.14

Chapter 4

LOOPBACK DfT FOR CONCURRENT LOW-COST WAFER-LEVEL ALTERNATE TESTING OF SoC TRANSCEIVER ARCHITECTURES

RF systems developed to provide wireless communication in electronic components used in day-to-day life need to be manufactured at extremely low-costs to meet the stringent market demands. One such case is the transceiver solution developed for Bluetooth applications, a global wireless standard that is the cheapest replacement for a cable. A chart of the numerous applications that employ the Bluetooth standard is shown in Figure 62. Such solutions need to target the current market value of $2.5, with a 50% profit margin. Hence, there is a steady race among the semiconductor manufacturers to go for highly integrated low-cost solutions to reduce the overall manufacturing costs. One approach to reduce the testing cost of these devices is through the introduction of well-structured and low-cost wafer-probe tests that can enable fault detection at an early stage of the production cycle to avoid some of the unnecessary costs.

The recent advances in SoP and SoC technologies have enabled high levels of integration in transceiver technologies. In this context, some of the current generation devices have an RF-to-digital configuration. This means that the SoC/SoP device contains (1) RF blocks viz. TX chain and RX chain, (2) analog/baseband blocks viz. variable gain amplifiers and low-pas filters (LPFs), (3) digital blocks viz. decoders/demodulators, discriminators, memories, counters and (4) digital control loops to individually control/tune circuits in the other blocks. A block diagram of one such transceiver SoC is shown in Figure 63. The test requirements of these devices are

usually limited to functional system-level tests as opposed to conventional testing for all specifications of each building block. Functional testing of a wireless SoC device can be defined as a set of tests that are performed to test entire chains of the device as a functional block in a manner that more closely approximates how the device will be used in the real world.

Figure 62. Common applications of the Bluetooth standard.

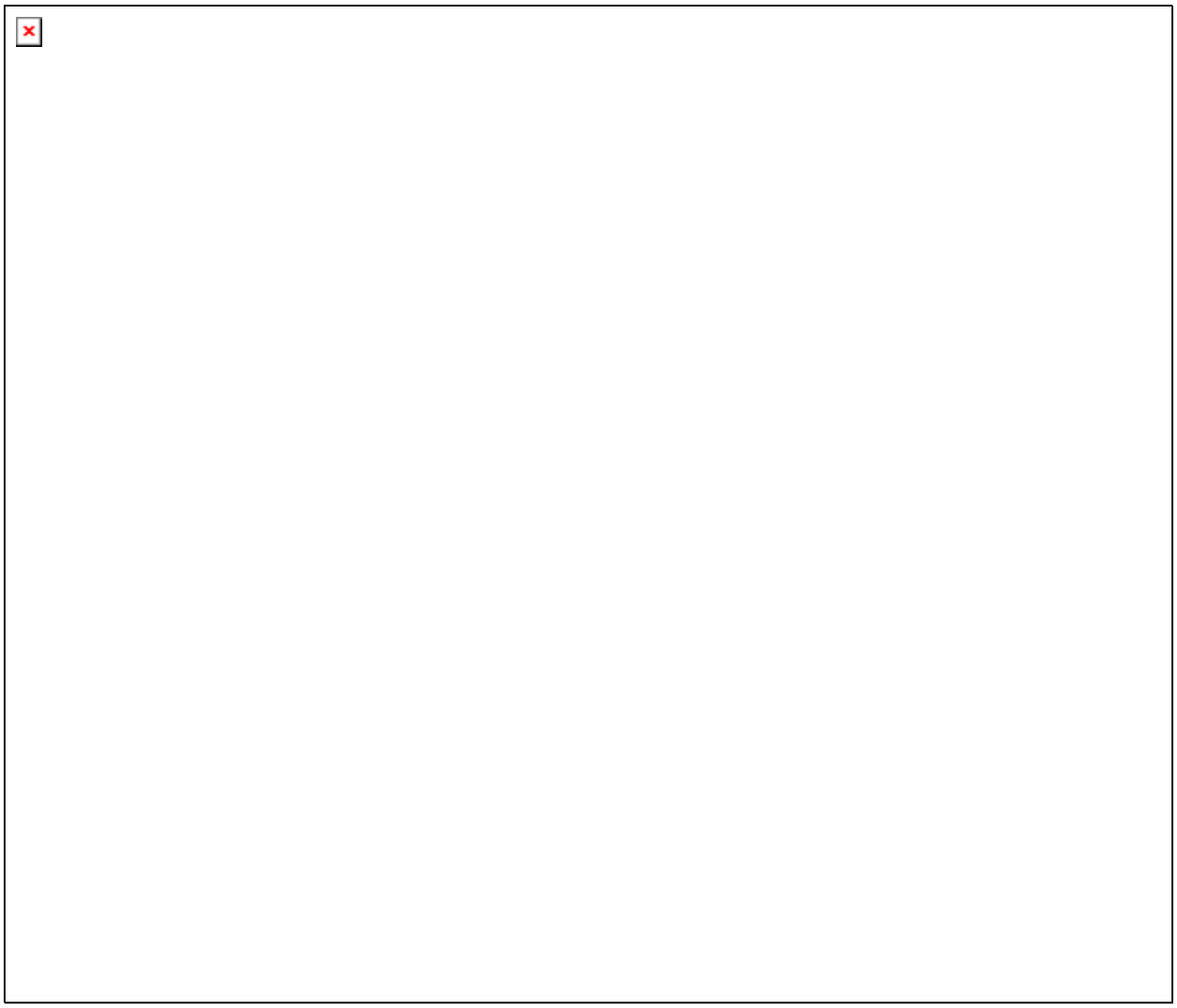


Figure 63. A typical block diagram of RF-to-digital type VCO modulation transceiver SoC [73].

Wafer-level testing at RF frequencies is difficult to develop and perform at the IC production sites as it incurs a high investment cost (RF ATE cost + RF probe development cost). High-volume probe solutions for wafer-level testing are very much limited to the analog and digital paths on the SoC devices. Needle DC probe cards are typically used to provide contact between the DUT and the PiB board. The parasites of the needle make this method inappropriate for use in RF circuits. On the other hand, wafer-level diagnosis of RF paths in the pre-packaged wafers is anticipated to be almost mandatory in the near future due to the following reasons.

- The increasing complexity of SoC devices lowers the overall manufacturing yield which in turn causes the package costs to increase.
- International technology roadmap for semiconductors (ITRS) has predicted that packaging costs may well exceed die manufacturing costs beyond 2007.
- The manufacture of integrated systems-in-packages (SiPs) requires the use of known good dies (KGD) from the IC manufacturer. RF tests for KGD can be performed only at wafer sort before the package assembly.

Due to the relatively relaxed testing requirements (functional tests), a possible method for cost reduction in the wafer-level testing of these transceivers is through the employment of dedicated rack-and-stack RF equipment integrated to low-cost ATE architectures to replace the expensive RF ATE for functionality tests. These reconfigurable testers have a cost advantage over expensive RF ATE. However, the test cost of integrated RF transceivers can be further reduced by eliminating the need of dedicated RF rack-and-stack and by looping back the transmitted RF output signal to the receiver input. This enables source and measure capabilities at lower frequencies and/or digital pins of the device. Hence, standard digital ATE that costs approximately one-fifth of the RF ATE cost can be used to perform functionality tests on these devices.

In this chapter, a novel loop-back DfT for VCO modulating transceiver architectures is proposed to overcome limitations in previously proposed loopback approaches such as, (a) modulation cancellation in continuous wave signals, and (b) half duplex operation which makes synchronization between the TX and RX operations difficult. In the proposed approach, phase/frequency dividers are combined with frequency-offset mixers in the loop-back path to resolve problems due to (a). Also, the PLL is locked to the modulated continuous wave signal

generated by the low-cost ATE to resolve problem (b). The looped-back spectral signature at the RX baseband is used to compute all the linear and the nonlinear transmitter as well as receiver specifications using the alternate test framework. The genetic ATPG (Chapter 3.4.2) is used to generate optimized bit stimuli that are used to drive the system for the spectral signature-based tests.

In addition to the spectral signature, the transient current signature is simultaneously extracted through V_{DD} ramp methods as proposed in Chapter 2. Additional or multiple predictor variables, i.e. the signatures of the RF system, typically provide a higher degree of accuracy as compared to single predictor variables. Since both the spectral and current signatures have a high-correlation to the RF performance parameters (viz. NF, IIP3, Gain) as shown in Chapter 2 and Chapter 3, the joint correlation regression mapping increases the accuracy of the computed nonlinear regression equations.

4.1 LOOPBACK DFT FOR VCO MODULATING ARCHITECTURES

To reduce the design cost of integrated wireless transceivers, a single VCO structure is shared by the TX as well as the RX chain. Also, the time division duplex nature of its applications in the GSM communications, WLAN, and Bluetooth market makes this VCO sharing policy a smart, cost-effective and viable one. The architecture of a typical VCO modulating RF transceiver is shown in Figure 64. The VCO in the integrated PLL is capable of generating a modulated signal that is amplified by the PA and transmitted during TX mode. The same VCO is used to provide a modulated LO signal for the down-conversion mixer in the RX mode.

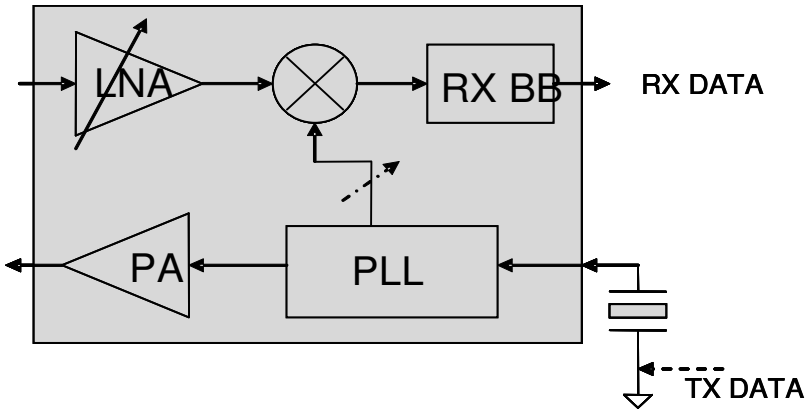


Figure 64. VCO modulating RF transceivers.

4.1.1 Limitations of Previously Proposed Loopback Approaches for VCO Modulating Architectures

Digital modulation methods used in the GSM, ISM and WLAN wireless communication standards employ continuous wave nonlinear modulation [4], which can be described as

$$s(t) = A * \cos\left[2 * \Pi * f_c * t + \phi_0 + \phi(t;I)\right] \quad \textbf{Equation 26}$$

where ϕ_0 is the initial phase of the carrier and $\phi(t;I)$ is the time-varying phase of the signal. Based on the phase/frequency modulation scheme employed, viz. FSK, MSK, GFSK, the $\phi(t;I)$ component varies.

Direct loop-back mechanisms i.e., connecting the transmitter output to the receiver input as proposed in [41] result in a DC signal at the output of the down-conversion mixer because of the VCO sharing policy. Frequency offset loop-back mechanism, as proposed in [69], results in an un-modulated signal at the down-conversion mixer output due to the cancellation of modulation. This cancellation mechanism can be better understood from Equation 27 and Equation 28. Assuming that the transmitter output is offset by a specified frequency and looped-

back to the input of the receiver, the corresponding input to the down-conversion mixer is as follows,

$$s(t) = B * \cos\left[2 * \Pi * f_{c+offset} * t + \phi_o + \phi(t;I)\right] \qquad \textbf{Equation 27.}$$

Mixing the signals in Equation 26 and Equation 27 yields,

$$s_{mix}(t) = C * \cos\left[2 * \Pi * f_{offset} * t\right] \qquad \textbf{Equation 28}$$

From Equation 28, it can be concluded that previously proposed loop-back mechanisms cannot be directly applied to diagnose modern transceivers as the modulation is lost in the loopback process. Further, any phase offset in the loop-back path will result in the same phase offset of the received signal at the offset frequency and will not help to recover the modulation in the transmitted signal.

In [70][71], delayed RF path-based measurements are proposed for diagnosis of catastrophic faults as well as for measuring path gain and SNR of RF transceivers in the loopback mode. This approach is limited by the specifications that can be measured and the fault models that can be computed from the looped-back signature. Complex specifications like IIP3 and P1dB, which are often required for device debugging and diagnosis, cannot be computed through this approach. Also, the proposed approach has not been supported by hardware measurements.

4.1.2 Proposed Loopback DfT Methodology

In order to overcome the limitations of the conventional loopback approaches a novel loopback DfT approach for wafer-level 'concurrent test' of RF transceivers is proposed. The

block diagram of the proposed DfT methodology that was applied to the Texas Instruments (TI) TRF6903 transceiver IC is shown in Figure 65. The loop-back DfT circuit consists of an attenuator, a phase/frequency divider, an offset mixer and a BPF to remove the spurious emissions. The transmitter output signal for a continuous wave nonlinear phase/frequency modulation can be described as in Equation 26. The 'N' phase/frequency divider performs the divide by N operation, the output of which can be expressed as:

$$s_{mix}(t) = C * \cos\left[2 * \Pi * f_{offset} * t\right] \qquad \textbf{Equation 29}$$

Most of the wireless standards require the TX and RX chains to operate at offset frequencies so as to avoid interference. This frequency adjustment for the looped-back signal is done by the offset mixer. The LO signal for the offset-mixer could be generated using an integrated PLL soldered on the loadboard or by using a stand-alone signal source, which is a cheap and reliable option in high-volume testing. High quality BPFs are used to remove unwanted spurious emissions of the offset-mixer and the TX chain. Subsequent input to the RX chain can be expressed as:

$$s(t) = C * \cos\left[2 * \Pi * \left(\frac{f_c}{N} + f_{offset}\right) * t + \frac{\phi_0}{N} + \frac{\phi(t;I)}{N}\right] \qquad \textbf{Equation 30}$$

In the RX chain, this looped-back signal is amplified and mixed with the LO signal generated from the VCO of the integrated synthesizer. Since the same modulated VCO signal is used to drive the PA and the down-conversion mixer in the receiver, the signal available at the LO terminal of the RX mixer can also be expressed as in Equation 9. The corresponding output signal of the RX mixer can be expressed as:

$$s_{mix}(t) = D * \cos\left[2 * \Pi * f_{offset} * t + \left(1 - \frac{1}{N}\right)\phi(t;I) \right] \qquad \text{Equation 31}$$

From Equation 31, it is clear that the modulation is retained in the mixer output and this signal is demodulated by the baseband circuitry in the RX chain to decode the data. This solves limitation (a) mentioned in the introduction of this Chapter. Although the TX and RX front-ends of these transceivers could be turned on simultaneously by the use of digital switches, it is not possible to turn on the entire TX and RX chain together in order perform modulation and demodulation simultaneously. The problem arises mainly due to limitation (b) mentioned in the introduction of this Chapter. The transceiver can be operated either in the TX mode or in the RX mode.

The approach commonly used by integrated VCOs to generate phase/frequency modulation in the TX mode is shown in Figure 66. The external crystal clock, which is used to provide the reference frequency for the synthesizer is either loaded by an external capacitor (during TX mode) or is grounded (during RX mode) [73]. During the TX mode, the loading effect of the capacitor pulls the crystal frequency slightly below or above the center frequency depending on the transmitted baseband bit. This loading provides the phase/frequency modulation at the PLL output. During the RX mode, the external crystal is grounded in order to provide an unmodulated LO signal to the RX mixer. This makes it impossible to turn on both the chains simultaneously. In this work, the ATE is used to source the clock reference signal to the synthesizer. The digital baseband data (periodic bitstreams) can be used to modulate the clock signal. The only requirement in such a methodology is to have the data switching rate within the VCO loop filter bandwidth.

In conjunction with the phase/frequency division mechanism, the transceiver could be effectively operated in the full-duplex mode during test. The loop-backed response at the RX baseband is used to compute specifications such as system-level gain, BER etc. In this work, the spectral signature at the output of the RX mixer coupled with the current signature obtained through V_{DD} ramp tests are used for the purpose of concurrent alternate test of RF systems.

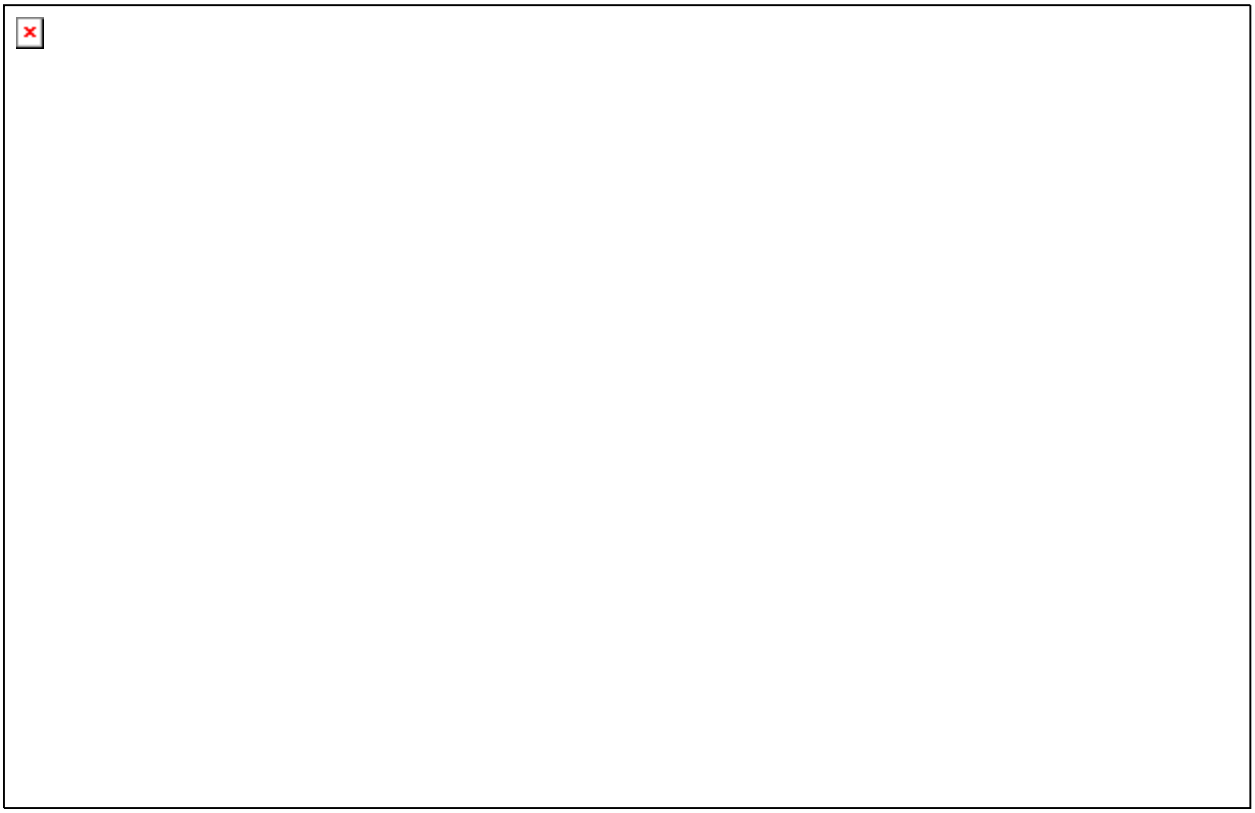


Figure 65. Loopback DfT test architecture for testing VCO modulated RF transceivers.

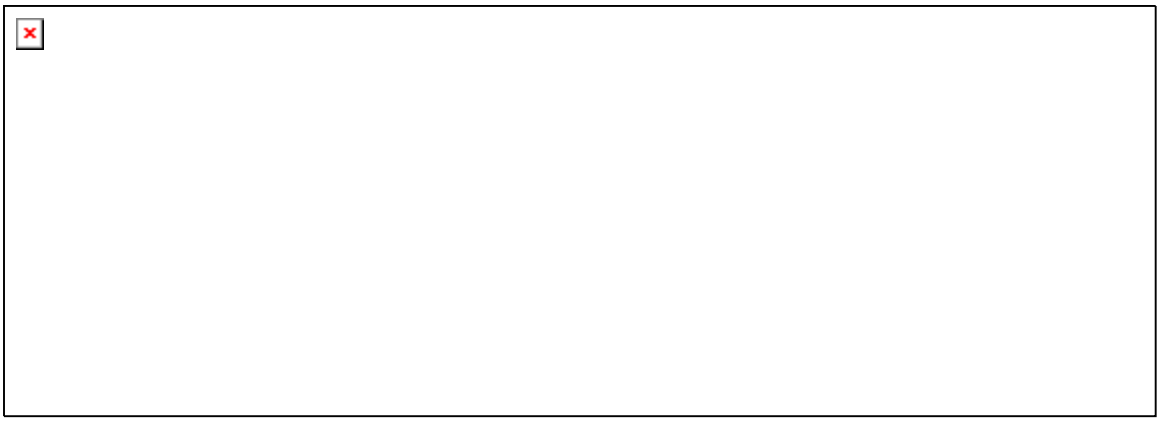


Figure 66. Architecture of integrated synthesizers [73].

4.2 CONCURRENT ALTERNATE TEST METHODOLOGY

As described in [19][20], the variations in the process parameters affect both the measurements (signatures) and the specifications (performance parameters) by specific sensitivity factors. The alternate test framework [19][20] employed in spectral signature-based test methodology uses this concept to compute the specifications of the system from the amplitudes of the captured spectrum using statistical regression. The efficiency of such a regression-based test methodology would depend on the sensitivity or correlation of the spectral signature to the performance parameters of the RF system.

Multi-regression mapping is one approach to improve the accuracy of statistical regression equations through additional predictor variables. In this context, the current signatures of the RF devices that are integrated to form the RF transceiver system have a high correlation to the large-signal performance parameters (specifications), as shown in Chapter 2. The concurrent alternate test methodology presented in this chapter uses this additional predictor variable (current signature) along with the spectral signature of the device to compute the multi-regression equations for an increased accuracy in specification computation.

To extract the current and spectral signatures, optimized control voltage (generated as explained in Chapter 2) and optimized periodic bitstream stimuli (generated as explained in Chapter 3) are applied to the RF system in a sequential manner. The V_{DD} optimization is performed using the same algorithm presented in Chapter 2. In this work, the V_{DD} is applied to the RF transceiver in the loopback mode. Hence, additional optimization features such as the digitizer or digital voltmeter setting time, device permissible V_{DD} range, and the PLL lock time were used to control the slope and speed of the V_{DD} ramp stimulus. The additional parameters were included to extract accurate current signatures. These features can be extracted for the datasheet of the RF and ATE systems.

The optimization for the spectral signature is performed as explained in Chapter 4. The optimization is performed for the bitstream stimuli (digital data) that can be directly applied to baseband input of the TX section (RF-to-baseband type configuration). The corresponding output of the transmitter is looped back to the receiver through suitable DfT resources. The looped back signature at the RX baseband is captured using suitable baseband ATE recourses. Hence, for this optimization additional blocks of the system-under-test are added to simulate the entire transceiver system for test generation purposes. Also, suitable test resource models (ATE resources + DfT resources) are included in the simulation model for reliable test generation purposes.

The captured current and spectral signatures for the optimized test stimuli are normalized based on their nominal value and input to the MARS algorithm [32]. MARS ranks the measurements based on their relative contribution for accurate specification computation and drops the less contributing measurements. This operation is done during the forward and reverse knot placement operations for basis function computation as explained in Chapter 2. Using the

computed basis functions along with their coefficient values, the sub-system specifications of interest (viz. TX gain, IIP3, P1dB, RX gain) can be computed from subsequent captures of the looped-back spectral signature and transient current signature with no access to the TX output. The concept and flow of multi-regression is pictorially presented in Figure 67.

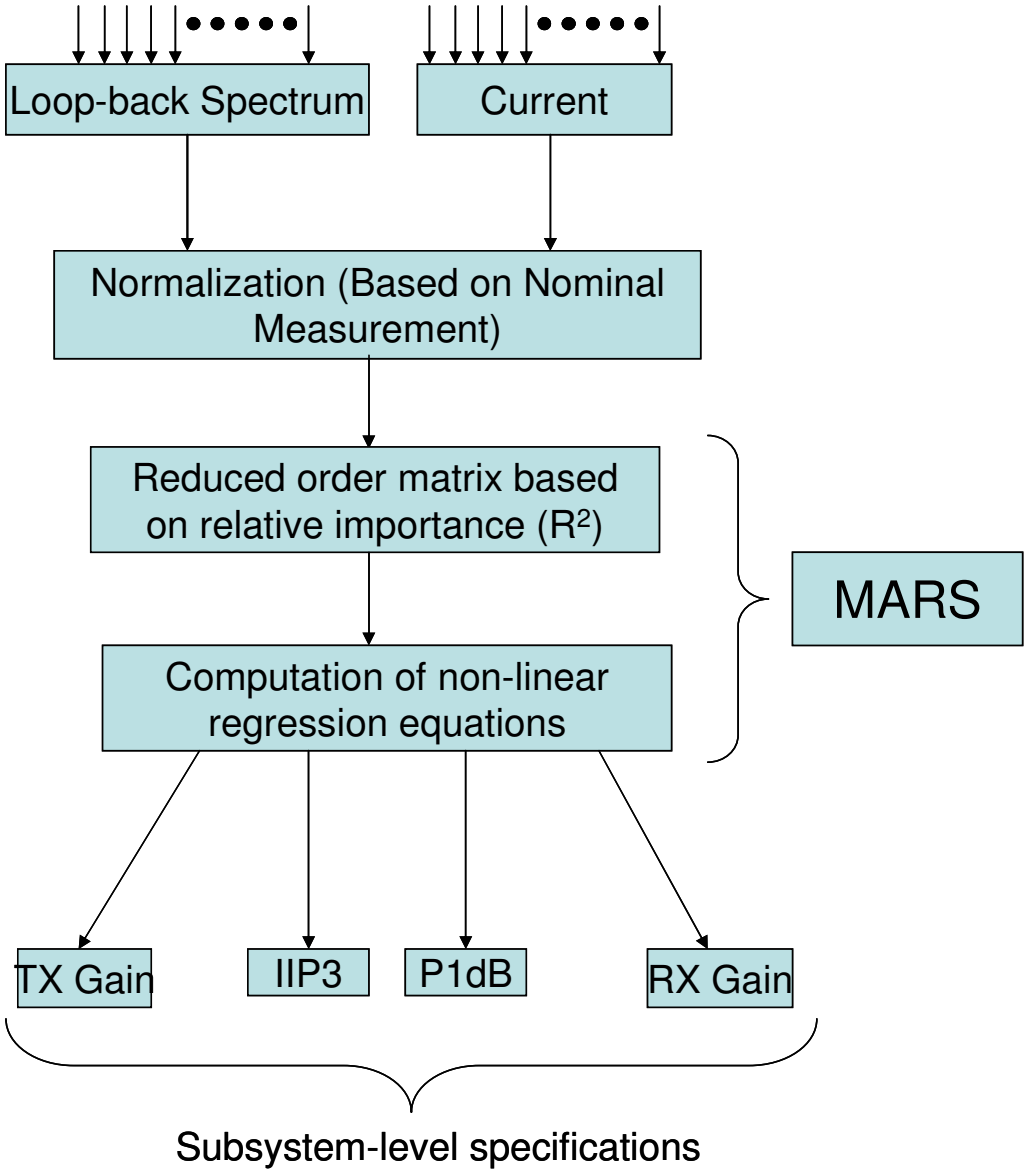


Figure 67. The methodology to compute multi-regression functions for accurate specification prediction using concurrent test methodology.

4.3 VALIDATION RESULTS OF THE PROPOSED LOOPBACK DFT APPROACH

The validation of the loopback DfT approach was performed on commercially available TI's TRF 6903 transceivers. TRF 6903 is a single-chip, half duplex, multi-band, low-cost RF transceiver for the 315, 433, 866, and 915 MHz ISM bands. This system is designed to support FSK/OOK modulation techniques. The transmitter consists of an integrated VCO, a complete N-integer synthesizer, and a power amplifier. The transmitter is capable of producing up to 8 dBm of output power. The integrated receiver consists of an LNA, a mixer, a limiter, an FSK demodulator, LPF amplifier, a data slicer, and an integrated data bit synchronizer. The TRF 6903 die contains serial registers which are used to control various parameters of the transceiver [73]. Commercially available PC-based software distributed along with the TRF 6903 evaluation board can be used to program these control registers through the parallel port of the PC [72].

For proof-of-concept purposes, the proposed approach was demonstrated on the TRF6903 evaluation board. The hardware setup used to demonstrate the proposed approach is shown in Figure 68. A hand probe socket was fitted on the evaluation board to enable the test of multiple ICs. The loop-back DfT circuit was set up using a stand-alone offset-mixer and a BPF. The attenuator and the phase/frequency divider were available in the IC itself. The test modes available in the IC are used to turn on the TX and RX front-ends simultaneously. In this work, FSK modulation scheme was used to demonstrate the proposed approach. A clock signal of 19.6608 MHz that is required to drive the integrated synthesizer of the IC was generated by an external signal generator with digital modulation capability. This source will be replaced by the AWG of the ATE during final probe test. Periodic bit streams were used to modulate the clock signal. The repeatability of the spectrum is highly dependant on the periodicity of the bitstream. Hence, a periodic "0101" bitstream was used in this demonstration. A baseband data rate of 1

kHz with a modulation index of 1 was used to produce the FSK modulated signal. The baseband rate multiplied by the divider ratio of the integrated synthesizer determines the frequency deviation of the FSK modulated RF signal. The periodic bitstream was continuously sourced and the spectral signature of the IC at the RX baseband was captured using a low frequency active probe integrated to a spectrum analyzer.

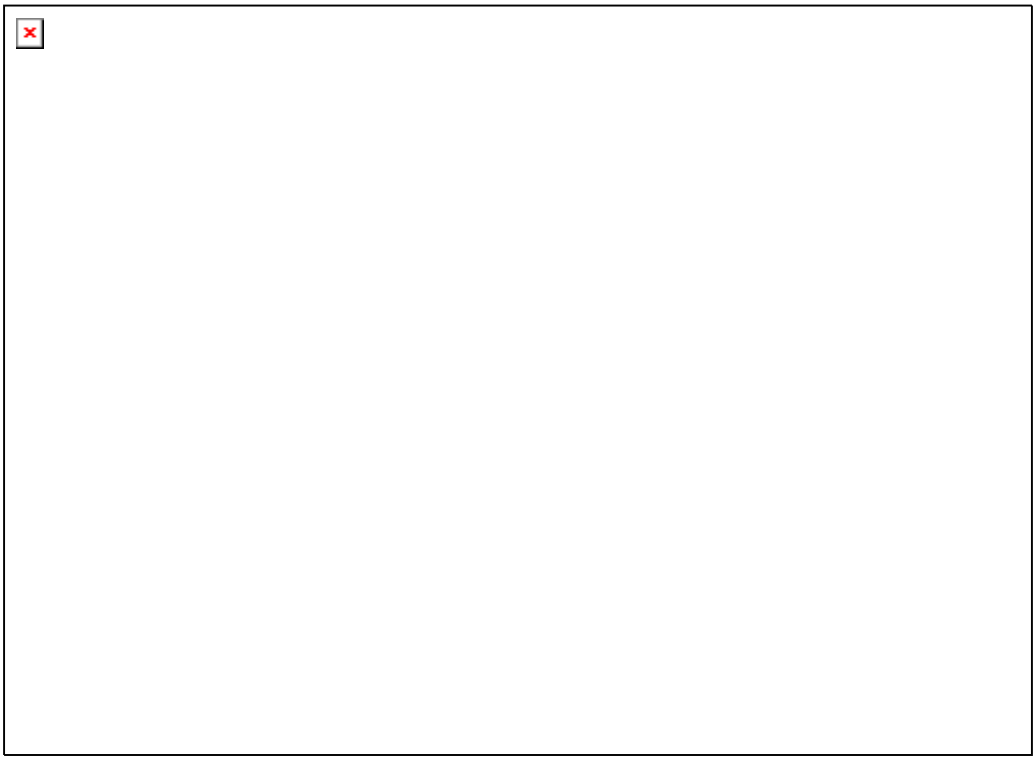
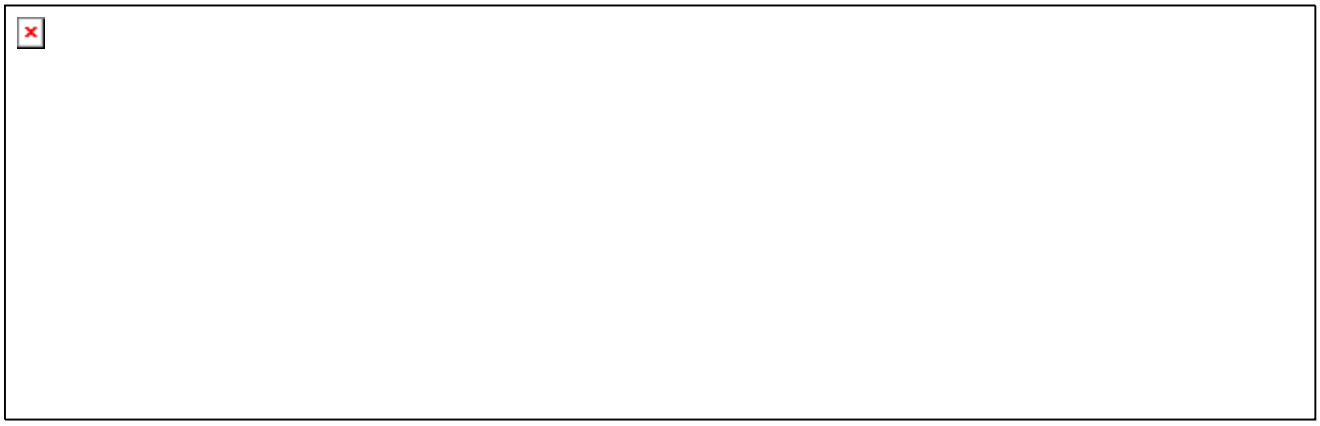


Figure 68. Hardware set-up used for validation.

The TX section was operated at a frequency of 915 MHz and the RX section was operated at a frequency of 925.7 MHz. The divide ratio of the phase/frequency divider was set to be three. The FSK modulated signal at the output of the transmitter was centered at 915 MHz with a deviation of 254 kHz between the two frequency peaks. The frequency spectrum of this signal is shown in Figure 69 (a). The signal at the end of the phase/frequency divider was

centered at 305 MHz with a frequency deviation of 81.6 kHz between the two frequency peaks. This signal was mixed with an external LO signal centered at 620.7 MHz by the passive offset-mixer. The output of the mixer is filtered by a SAW BPF to remove the spurious emissions. The spectrum of the resultant signal that is centered at 925.7 MHz with a frequency deviation of 81.6 kHz between the two frequency peaks is shown in Figure 69 (b). This signal is looped-back to the input of the receiver for detection and demodulation. This signal is amplified by the LNA and then down-converted by the RX mixer to a frequency of 10.7 MHz with a frequency deviation of 169 kHz between the two frequency peaks. The spectrum of the signal at the output of the RX mixer is shown in Figure 69 (c). This signal contains the resultant FSK modulation after mixing the integrated VCO output signal and the looped-back signal at the RX mixer input. The characterization data observed at each of these test points for a 'golden KGD' is summarized in Table 20.



(a) (b) (c)

Figure 69. Signal spectrum captured at (a) TX output, (b) RX input, and (c) RX mixer output.

Table 20. Characterization data at various test points for golden KGD.

Test Points	Maximum Amplitude (dBm)	Amplitude deviation between peaks (dBm)	Frequency deviation between peaks (dBm)
Transmitter O/P	-26.9	0.2	255.26
Phase divider O/P	-29.3	0.2	82.08
Receiver I/P	-42.5	0.2	82.08
Receive mixer O/P	-22.6	2.9	168.17

4.4 VALIDATION RESULTS OF THE PROPOSED CONCURRENT TEST METHODOLOGY IN CONJUNCTION TO THE LOOPBACK DFT

The concurrent test approach was validated on the TRF6903 device operating in the loopback mode. In the loopback configuration, the device had two RF paths: (1) TX path that contains an N-PLL with integrated VCO followed by a PA, and (2) RX path that contains the integrated LNA and mixer combination. The TX path was diagnosed for output power and the RX path was diagnosed for gain, IIP3, and P1dB. Since the VCO output signal is amplified by the PA, the specifications corresponding to the second and third order nonlinearities are not measured for the TX chain. A set of 53 ICs chosen from two different production lots were used for this experiment. Forty five ICs were used for the purpose of training (computation of nonlinear regression equations using MARS) and eight ICs were used for the purpose of validation. The spectral signatures and transient current signatures were captured for the training devices using a low-frequency active probe integrated with a spectrum analyzer and a Keithley power source respectively. The Keithley power source has an inbuilt current measurement capability that was used in this work. A custom developed program in the Lab view test

automation environment was used to automate the entire current and spectral signature capture process.

The optimized V_{DD} ramp applied to the control voltage terminal of the training devices and their corresponding captured current signatures are shown in Figure 70. For the spectral measurements, a frequency span of 1 MHz was used and the amplitudes of the spectrum at 1000 frequency bins were captured. A resolution and video bandwidth setting of 3 kHz was used for the signature capture. The spectral signatures of the training devices are shown in Figure 71. Simultaneously, the TX and the RX chain functional specifications of these training ICs were measured using the sequential approach on a Teradyne A580 ATE platform.

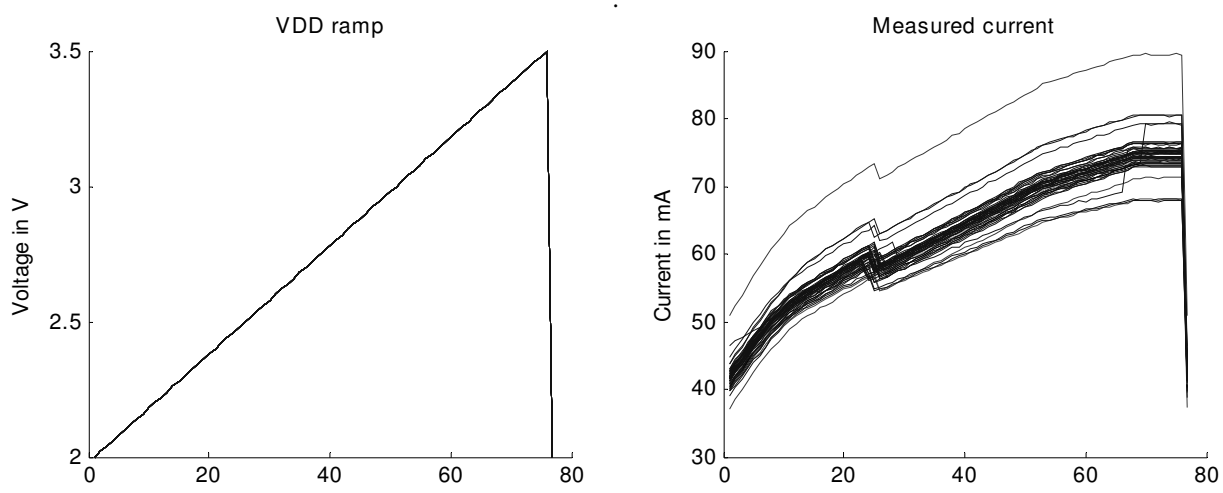


Figure 70. The optimized VDD ramp (on the left) applied to the control voltage terminal of the training devices and their corresponding captured current signatures.

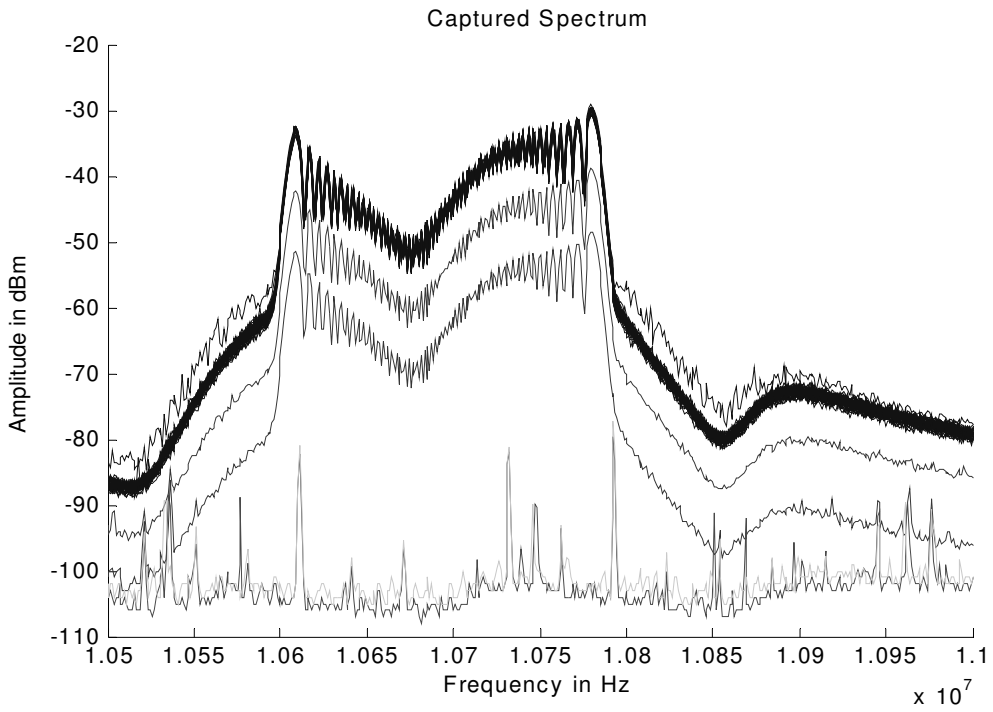


Figure 71 Captured spectral signatures of the training devices using the low-frequency probe interfaced to a spectrum analyzer.

MARS was used to build the regression equations from the captured signatures to the measured specifications. The signatures captured from the validation devices using the similar process were later fitted into the regression equations to compute the specifications of interest. Table 21 summarizes the mean and standard deviation values of the observed computation error in each specification by the concurrent approach. Also, to show the improved accuracy of specification prediction using the multi-regression concept in the concurrent test methodology, the mean and standard deviation of the errors obtained in specification computation when only voltage signatures are used is summarized in Table 22.

Table 21. Summary of mean and standard deviation values of the computation error incurred for the concurrent test methodology.

Error	TX Output power (dBm)	RX Gain (dB)	RX IIP3 (dBm)	RX P1dB (dBm)
Mean	0.48	0.11	0.08	0.14
Std. (σ)	0.41	0.08	0.05	0.09

Table 22. Summary of mean and standard deviation values of the computation error incurred for the spectral signature-based test methodology.

Error	TX Output power (dBm)	RX Gain (dB)	RX IIP3 (dBm)	RX P1dB (dBm)
Mean	0.62	0.15	0.08	0.17
Std. (σ)	0.48	0.11	0.07	0.08

Chapter 5

CHECKERS FOR DIAGNOSIS OF RF PATHS ON LOADBOARDS USED FOR HIGH-VOLUME PRODUCTION TEST

As explained in Chapter 1, loadboards (a.k.a. DiBs) are used in high-volume IC production testing to provide the required electrical contact between the DUT and the test instrumentation in the ATE. The loadboard contains the device socket and the required DfT circuitry that is used to deliver a suitable test stimulus to the DUT and relay the test response back to the ATE. During high-volume production, low yielding lots can often result from problems related to the loadboard itself rather than from a low IC manufacturing quality. Poor storage conditions, improper handling, and a short lifetime of the components used on the loadboards can cause mechanical/electrical defects that serve as potential reasons for a low test yield. For digital and analog circuits, a board check methodology is standard in release-to-production (RTP) process. However, in the RF area, board checking algorithms and their failure diagnosis is very much an open research issue.

The requirement of precision in the multi-parameter production test of RF devices entails RF test engineers to develop automated loadboard checking tools that accurately characterize/diagnose the RF paths on the loadboards. Also, it becomes very crucial to use these checking algorithms in the proposed spectral-signature based test approaches in Chapter 3 and Chapter 4, where the test resources are moved to the loadboard to use low-cost ATE to efficiently test RF devices. Magnitude and phase calibration of the RF paths on the loadboard

needs to be done periodically to avoid measurement errors and low yielding lots. The key objectives of such an automated tool in high-volume RF production testing are:

- Calculation of magnitude and phase loss in the RF signal path for initial calibration purposes
- Periodic calculation of network S-parameters to check for the compatibility of the loadboard in high-volume tests
- Capture site-to-site variations (in multi-site testing) to dynamically set pass/fail bands for specification tests in multiple test sites
- Detect parametric deviations in the RF paths to compensate for their deviations
- Detect catastrophic failures in the RF paths to avoid low yielding lots

Due to the absence of expensive RF bench equipment at production test sites, it becomes difficult, if not impossible, to probe the RF signal path for initial path loss calibration and to find the root cause for low yielding lots. Typically, vector network analyzers (VNAs) are used to characterize RF paths on the bench set-up. But this approach cannot be directly applied to automatic loadboards since only a single RF port is often available for the purpose of input/output interface with the DUT (one good example will be the integrated RF transceiver). This RF port is connected to the trace of the die through the RF path. Accurate calibration of this path is required to maintain the high degree of precision in multi-parameter production test of RF devices.

The signal available at the RF output port of the ATE is already well characterized using the internal VNA resources of the ATE. The ATE vendor provides accurate calibration standards and algorithms to perform this calibration in the forward and reverse directions [74]. Since loadboards are developed at the test development site and not at the ATE vendor site, the

reference place for this calibration still remains at the ATE output port and not at the die trace as desired. Accurate die-level wafer probe stations [75] that could be used to diagnose the loadboard are very expensive to develop and maintain at the production test sites. Also, wafer probes of the required pitch dimensions need to be developed and maintained.

Time domain reflectometry (TDR) [76] is a well-established technique for verifying the impedance and quality of signal paths in components, interconnects, and transmission lines. TDR measurements require accurate high-frequency pulse generators that are expensive to develop and maintain at the production test sites. Also, TDR measurements only provide impedance information and often this information is not sufficient for accurate calibration/diagnosis purposes. In [77], a methodology to test matching networks for RF attenuation using harmonics in the frequency response of the network to lower frequency AC square waves is proposed. Often due to driver loading, it is difficult to generate very high-frequency harmonic signals using lower frequency AC square waves. Even if this is possible, the power level of the resulting signal is generally incompatible with the power level requirements of the RF path being tested. Also, it is often required to calculate more than the just power attenuation to enable accurate diagnosis of the RF loadboard.

In this chapter, a production-ready tool for seamless diagnosis of multi-port active and passive RF networks on ATE loadboards is presented. This tool uses reflection coefficient measurements made at the input port of the loadboard upon suitable termination of all other ports to compute the complex S-parameters of the RF network. A software 'checker module' that incorporates a set of 'derived checker equations' is developed to compute the complex S-parameters of the network based on the reflection coefficient measurements. This module can be included in the main test program and executed periodically during the high-volume tests.

Different combinations of the commonly used termination standards, (1) open, (2) short, (3) characteristic 50-ohm or any other impedance termination (other than characteristic impedance) are used to terminate the network based on the total number of ports. These termination standards can be easily fabricated on special 'dummy' ICs with the same wafer material as the RF DUT to improve the accuracy. Also, faulty ICs that exhibit non-50 ohm impedances at their input could be used for this purpose. Results obtained from experiments conducted for production validation of the proposed loadboard checker tool is presented in Section 5.6. These experiments were conducted on loadboards used for high-volume production test of WLAN (2-2.2 GHz) transceivers. The results show that the developed checker has a high degree of accuracy in performance even for 'not-so-accurate' termination standards. Also in Section 5.6, the performance of the tool for commonly occurring parametric and catastrophic failures on these boards during high-volume tests is presented.

5.1 CHECKER FRAMEWORK FOR 2-PORT PASSIVE NETWORKS

The proposed checker module uses reflection coefficient measurements made at the input port of the network with suitable terminations of the RF paths to check/diagnose the loadboard. These reflection measurements are then fitted into the software checker module on-the-fly to compute the network S-parameters. The checker module incorporates a set of equations to perform the computations. The set of equations for a two-port case is presented in this section. In the next section, the equations for a generalized multi-port case are presented.

A two-port network with the direction of the incident and reflected powers at each port is shown in Figure 72. S-parameter equations for this network can be expressed as

$$b_1 = S_{11}\ a_1 \quad + \quad S_{12}\ a_2 \qquad \textbf{Equation 32}$$

$$b_2 = S_{21}\ a_1 \quad + \quad S_{22}\ a_2 \qquad \textbf{Equation 33}$$

where S_{11}, S_{12}, S_{21}, S_{22} are the S-parameters of the network, a_1 and a_2 are the incident powers at the input and output ports respectively, b_1 and b_2 are the reflected powers at the input and output ports respectively.

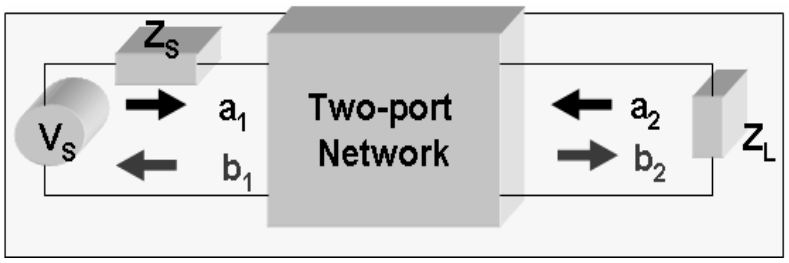


Figure 72 Block diagram of a two-port network highlighting the direction of incident and reflected powers.

Terminating the two-port network with a suitable termination at the output port yields $a_2 = \Gamma_2 b_2$ [80], where Γ_2 is the complex reflection coefficient at the output port. Substituting this condition in the S-parameter equations and solving them to compute the complex reflection coefficient at the input port (Γ_1) yields

$$\Gamma_1 = \frac{b_1}{a_1} = S_{11} + \frac{\Gamma_2 S_{12} * S_{21}}{1 - \Gamma_2 S_{22}} \qquad \textbf{Equation 34}$$

This representation of Γ_1 makes it simpler to express the reflection coefficient at the input for different terminations at the output port.

- Terminating the output port of the two-port network with the characteristic impedance results in $\Gamma_2 = 0$. Substituting this condition in Equation 34 yields

$$\boxed{\Gamma_{load} = \frac{b_1}{a_1} = \overline{S_{11}}} \qquad \textbf{Equation 35}$$

where Γ_{load} is the measured complex reflection coefficient at the input port with the characteristic 50-ohm terminating the output port and $\overline{S_{11}}$ is the derived S_{11} parameter.

- Terminating the output port with an open termination results in $\Gamma_2=1$, i.e.,

$$\Gamma_{open} = \frac{b_1}{a_1} = S_{11} + \frac{S_{21}S_{12}}{1 - S_{22}} \qquad \textbf{Equation 36}$$

- Terminating the output port with an short termination results in $\Gamma_2= -1$, i.e.,

$$\Gamma_{short} = \frac{b_1}{a_1} = S_{11} - \frac{S_{21}S_{12}}{1 + S_{22}} \qquad \textbf{Equation 37}$$

where Γ_{open} is the measured complex reflection coefficient at the input port with an open termination and Γ_{short} is the measured complex reflection coefficient with a short termination.

Terminating the network with the characteristic impedance standard (50-ohm) yields the complex S_{11}-parameter. Using this S_{11} measurement and the reflection coefficients measured with the open and short standards, S_{22} can be calculated from the following equation.

$$\boxed{\overline{S_{22}} = \frac{\Gamma_{open} - \Gamma_{short} - 2\overline{S_{11}}}{\Gamma_{open} - \Gamma_{short}}} \qquad \textbf{Equation 39}$$

, where $\overline{S_{22}}$ is the derived S_{22} parameter. For any passive network, $S_{12}=S_{21}$. Substituting this condition in Equation 36 yields

$$\overline{S_{12}} = \overline{S_{21}} = \sqrt{\frac{1 - \overline{S_{22}}}{\Gamma_{open} - \overline{S_{11}}}} \qquad \textbf{Equation 41}$$

, where $\overline{S_{12}}$ and $\overline{S_{21}}$ are the derived S_{12} and S_{21} parameters respectively.

Hence, using only reflection measurements and Equation 35, Equation 39, and Equation 41 it is possible to completely characterize the passive two-port network. Also, in certain cases it might be required to calculate the gain/loss of the network for a complex load (non 50-ohm ICs) during high-volume testing. This could be done either by using another impedance termination (other than characteristic impedances like a 200-ohm termination) or terminating the network with a KGD. Terminating the two-port network with a KGD yields,

$$a_2 = \Gamma_{(KGD)}\, b_2 \qquad \textbf{Equation 42}$$

where $\Gamma_{(KGD)}$ is the unknown complex reflection coefficient of the network when loaded with a KGD or any other termination used. Substituting Equation 42 in the S-parameter equations and solving for $\Gamma_{(KGD)}$ yields

$$\Gamma_{(KGD)} = \frac{b_1}{a_1} = \frac{\Gamma_{(in)} - \overline{S_{11}}}{2\overline{S_{12}}\overline{S_{21}} + \Gamma_{(in)}\overline{S_{22}} - \overline{S_{11}}\overline{S_{22}}} \qquad \textbf{Equation 43}$$

where, $\Gamma_{(in)}$ is the measured complex reflection coefficient with the KGD terminating the network.

5.1.1 RF path gain/loss calculation for complex load ICs

The gain/loss of the RF path for a complex load is defined as the ratio of the power delivered from the network to the power supplied to the network. From Figure 72, the gain/loss of an RF network can be represented as,

$$Loss = \frac{|b_2|^2 - |a_2|^2}{|a_1|^2} \qquad \textbf{Equation 45}$$

Since

$$a_2 = \Gamma_{(\mathrm{KGD})}\, b_2 \qquad \textbf{Equation 47}$$

and

$$\frac{b_2}{a_1} = \frac{S_{21}}{1 - S_{22}\Gamma_{(\mathrm{KGD})}} \qquad \textbf{Equation 49}$$

The gain/loss of the network can be represented as,

$$\boxed{Loss = \frac{|S_{21}|^2 (1 - |\Gamma_{(\mathrm{KGD})}|^2)}{|1 - S_{22}\Gamma_{(\mathrm{KGD})}|^2}} \qquad \textbf{Equation 51}$$

5.2 LOADBOARD CHECKER EQUATIONS FOR MULTI-PORT RF NETWORKS

Almost all high-performance test instrumentation including sampling oscilloscopes and VNA are single-ended, ground-referenced, 50-ohm instruments. However, the majority of the current generation RF devices employ a differential architecture to improve the device

performance. Hence, test engineers use BALUNs on the loadboard to enable testability of these devices using the standard ATE resources. Also, high-precision multi-parameter RF test requires well matched signals and DC blocking capacitors in the RF path of the loadboard. In some ATE configurations, amplifiers might be required on the loadboards to boost the signal power levels. The proposed checker is used characterize/diagnose these active/passive multi-port RF paths during high-volume production. Although the proposed approach is scalable with the order of the RF network, the rest of this section presents the derived equations with respect to a commonly used three-port configuration. For most practical purposes, typical RF DfT paths on the loadboards do not exceed 3 ports.

A three-port network with the direction of the incident and reflected powers at each port is shown in Figure 73. S-parameter equations for this network are shown in equations 13, 14, and 15. To characterize/diagnose a three-port network, nine unknown network S-parameters needs to be computed. Since the proposed checker uses only reflection measurements made at the input port of the network to compute the entire network S-parameter matrix, nine different combinations of termination standards are used to provide the corresponding reflection measurements and reflection equations. This enables to form a nonlinear set of equations that could be reverse solved to compute the network S-parameters. Since the network can contain up to two output ports based on its architecture, commonly used termination standards open, short, and 50-ohm load are used in pairs to generate nine different combinations. The different combinations are: (1) Characteristic impedance on both ports (50-ohm), (2) open--open, (3) short--short, (4) 50-ohm--short, (5) short--50-ohm, (6) open--50-ohm, (7) 50-ohm--open, (8) open-short and (9) short-open.

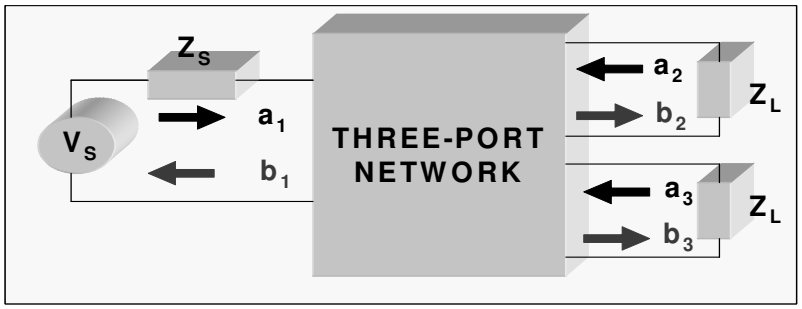


Figure 73. Block diagram of a three-port network highlighting the direction of incident and reflected powers.

$$b_1 = S_{11}\ a_1 \quad + \quad S_{12}\ a_2 \quad + \quad S_{13}\ a_3 \qquad \textbf{Equation 52}$$

$$b_2 = S_{21}\ a_1 \quad + \quad S_{22}\ a_2 \quad + \quad S_{23}\ a_3 \qquad \textbf{Equation 53}$$

$$b_3 = S_{31}\ a_1 \quad + \quad S_{32}\ a_2 \quad + \quad S_{33}\ a_3 \qquad \textbf{Equation 54}$$

- When the above mentioned three-port network is terminated with the characteristic impedance at both the output ports, their complex reflection coefficients at these ports are equal to zero, i.e., $\Gamma_1 = 0$ & $\Gamma_2 = 0$. The reflection coefficient measurement $\Gamma_{(load)}$ at the input port directly yields the complex S_{11} parameter of the network. i.e. substituting $\Gamma_1 = 0$ & $\Gamma_2 = 0$ in Equation 52, Equation 53, Equation 54 and solving for the Γ at the input port yields,

$$\boxed{\Gamma_{load} = \frac{b_1}{a_1} = \overline{S_{11}}} \qquad \textbf{Equation 55}$$

where, Γ_{load} is the measured complex reflection coefficient and $\overline{S_{11}}$ is the derived S_{11} parameter

- When the above mentioned three-port network is terminated with the open termination standard at both the output ports, the complex reflection coefficients at both the output

ports are equal to +1. The corresponding reflection coefficient $\Gamma'_{(\text{open, open})}$ measurement at the input port is shown in Equation 56.

$$\Gamma_{(\text{open,open})} = S_{11} + S_{12}\left(\frac{S_{12} + \frac{(S_{13}S_{23})}{(1-S_{33})}}{1-\left(S_{22} + \frac{(S_{23}S_{32})}{(1-S_{33})}\right)}\right) + \frac{S_{13}S_{31}}{1-S_{33}} + \left(\frac{S_{13}S_{23}\left(\frac{\left(S_{12} + \frac{S_{13}S_{23}}{1-S_{33}}\right)}{1-S_{22}+\left(\frac{S_{23}S_{32}}{1-S_{33}}\right)}\right)}{1-S_{33}}\right) \quad \textbf{Equation 56}$$

- When the above mentioned three-port network is terminated with an open standard in the first output port and a short standard at the other, the corresponding complex reflection coefficients are +1 and -1 respectively. The corresponding reflection coefficient measurement $\Gamma'_{(\text{open, short})}$ at the input port can be expressed as,

$$\Gamma_{(\text{open,short})} = S_{11} + S_{12}\left(\frac{S_{12} + \frac{(S_{13}S_{23})}{(-1-S_{33})}}{1-\left(S_{22} + \frac{(S_{23}S_{32})}{(-1-S_{33})}\right)}\right) + \frac{S_{13}S_{31}}{-1-S_{33}} + \left(\frac{S_{13}S_{23}\left(\frac{\left(S_{12} + \frac{S_{13}S_{23}}{-1-S_{33}}\right)}{1-S_{22}+\left(\frac{S_{23}S_{32}}{-1-S_{33}}\right)}\right)}{-1-S_{33}}\right) \quad \textbf{Equation 57}$$

- Similarly, when the above mentioned three-port network is terminated with an short standard in the first output port and an open standard at the other, the corresponding

complex reflection coefficients are -1 and +1 respectively. The corresponding reflection coefficient measurement $\Gamma'_{(\text{short, open})}$ at the input port can be expressed as,

$$\Gamma_{(\text{Short,Open})} = S_{11} + S_{12}\left(\frac{S_{12} + \frac{(S_{13}S_{23})}{(1-S_{33})}}{-1-\left(S_{22} + \frac{(S_{23}S_{32})}{(1-S_{33})}\right)}\right) + \frac{S_{13}S_{31}}{1-S_{33}} + \left(\frac{S_{13}S_{23}\left(\frac{\left(S_{12} + \frac{S_{13}S_{23}}{1-S_{33}}\right)}{-1-S_{22}+\left(\frac{S_{23}S_{32}}{1-S_{33}}\right)}\right)}{1-S_{33}}\right) \qquad \textbf{Equation 58}$$

Similar reflection coefficient equations could be derived for the other six termination standards mentioned earlier. To compute the nine unknown complex S-parameters, nine independent checker equations would be required. This set of nonlinear equations could be reverse solved to compute the S-parameters as a function of the measured reflection coefficients at the input port. Solving a linear set of N-equations to determine N-unknowns may be simple. When similar concepts are applied to solve a complex set of nonlinear equations, hand calculations are impossible. Hence, a software procedure was used to solve the system of nonlinear equations for a set of in-determinates (S-parameters) occurring in the equations. The output of the software module for the complex S_{12}, S_{13}, S_{22} and S_{33} parameters as a function of the reflections coefficients made at the input port are listed in Equation 59, Equation 60 Equation 61 and Equation 62 respectively. These equations were obtained by solving a set of six equations for the first six of the nine listed standards for three-port networks. Similar equations can be obtained for all the other complex S-parameters by solving a set of nine equations for the nine termination standards.

$$S_{12} = \left(\frac{\sqrt{2}((\Gamma_{(\text{Short},50)} - \Gamma_{(\text{Open},50)})(\Gamma_{(\text{Short},50)}\Gamma_{(\text{Open},50)} - \Gamma_{(\text{Short},50)}S_{11} - S_{11}\Gamma_{(\text{Open},50)} + {S_{11}}^2))^{\frac{1}{2}}}{\Gamma_{(\text{Short},50)} - \Gamma_{(\text{Open},50)}} \right) \quad \textbf{Equation 59}$$

$$S_{13} = \left(\frac{\sqrt{2}((\Gamma_{(50,\text{Short})} - \Gamma_{(50,\text{Open})})(\Gamma_{(50,\text{Short})}\Gamma_{(50,\text{Open})} - \Gamma_{(50,\text{Short})}S_{11} - S_{11}\Gamma_{(50,\text{Open})} + {S_{11}}^2))^{\frac{1}{2}}}{\Gamma_{(50,\text{Short})} - \Gamma_{(50,\text{Open})}} \right) \quad \textbf{Equation 60}$$

$$S_{22} = \frac{\Gamma_{(\text{Open},50)} - 2S_{11} + \Gamma_{(\text{Short},50)}}{\Gamma_{(\text{Short},50)} - \Gamma_{(\text{Open},50)}} \quad \textbf{Equation 61}$$

$$S_{33} = \frac{-\Gamma_{(50,\text{Open})} - 2S_{11} + \Gamma_{(50,\text{Short})}}{\Gamma_{(50,\text{Short})} - \Gamma_{(50,\text{Open})}} \quad \textbf{Equation 62}$$

5.3 PRODUCTION DEPLOYMENT OF RF LOADBOARD CHECKERS

The proposed loadboard checker tool uses the VNA or the MVNA module in the RF ATE to make reflection coefficient measurements upon suitable termination of the output ports of the RF network using the proposed standards. These terminations can be fabricated as 'dummy ICs' on the same wafer material as the RF DUT and hence these ICs could be directly placed in the die socket. Fabricating the termination standards on the same material helps to improve the accuracy of the calculations [79] . Based on dimensions of the die these terminations could be fabricated on the same die or on different dies. A custom developed software module is used to compute the S-parameters of the network using the reflection coefficient measurements. This module is loaded in the mainframe of the ATE ahead of the high-volume tests. It is included in the main test program and is invoked when the check/diagnosis needs to be performed.

Typically, these checks are performed at the start of each new production lot and at periodic intervals within each lot. The handler can be programmed to place the dummy ICs in the socket when these checks need to be performed. The checker module is very generic and is scalable across different IC products and ATE platforms.

5.3.1 Software checker module

The block diagram of the 'checker software module' that highlights the inputs and outputs to and from the module are shown in Figure 74. The required inputs for the software module are:

- Order of the RF network under investigation
- Employed termination standards for reflection measurements
- S-parameters (in determinates) that need to be computed

Based on these inputs, suitable checker equations are selected and a system of nonlinear equations is formed. These equations are reverse solved using numerical iteration to provide equations that relate the S-parameters that need to be computed as a function of the measured reflection coefficients. The reflection coefficient measurements are fitted into these equations to compute the complex S-parameters (magnitude and phase) of the RF network. The module can also calculate, the gain/loss of the network for a complex load environment with additional reflection measurements. Figure 75 shows a conceptual presentation of the checker module along with the equation of one of the in-determinates (S_{12}) as a function of the input reflection coefficient values. Similar equations can be obtained for the other S-parameters using the 'checker module'.

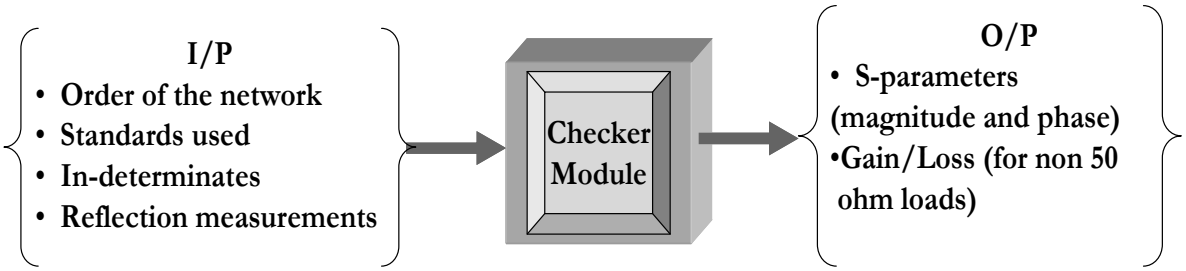


Figure 74. Block diagram of the *'Checker module'*.

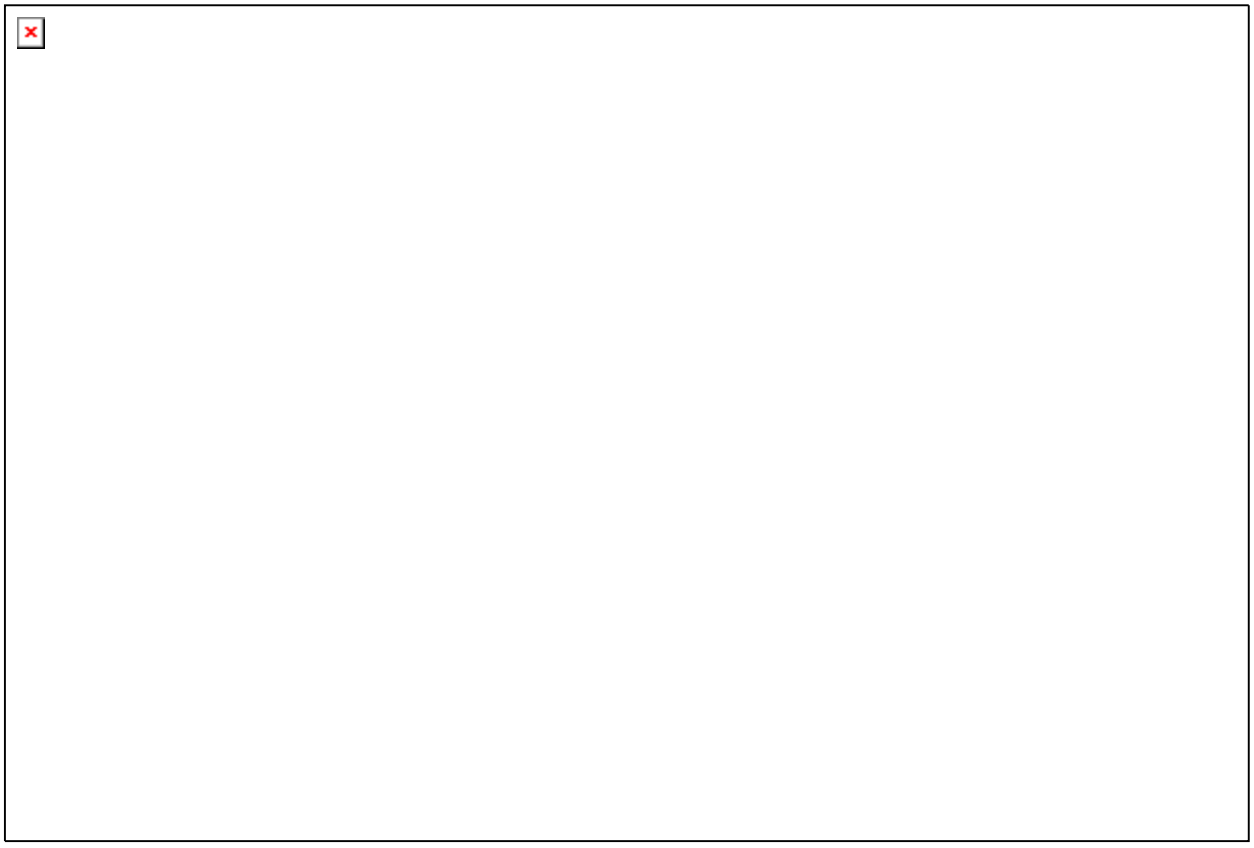


Figure 75. Conceptual representation of the *'Checker module'*.

The computed complex S-parameter values are used to characterize and diagnose the RF network on the loadboard. The RF parametric deviations and faults in any part of the network will reflect in the calculated S-parameter values. The checker module in the mainframe compares the calculated S-parameters to the expected S-parameters to make a suitable decision on the

loadboard. A conceptual representation of the methodology proposed to implement the checker module is shown in Figure 76. The key functionalities of the developed RF checker in high-volume production test are:

- Calculation of complex S-parameters before the commencement of each test run for initial calibration purposes and comparison with the corresponding bench data to maintain yield.
- Subsequent periodic calculation of network S-parameters at regular intervals to maintain board performance over a huge volume of tested devices.
- Comparison of S-parameters from multiple test sites to dynamically set power levels and pass/fail bands for the RF tests
- Detection of parametric deviations in the RF paths to initiate performance compensation
- Detection of catastrophic failures in the RF paths to render the loadboard 'useless'

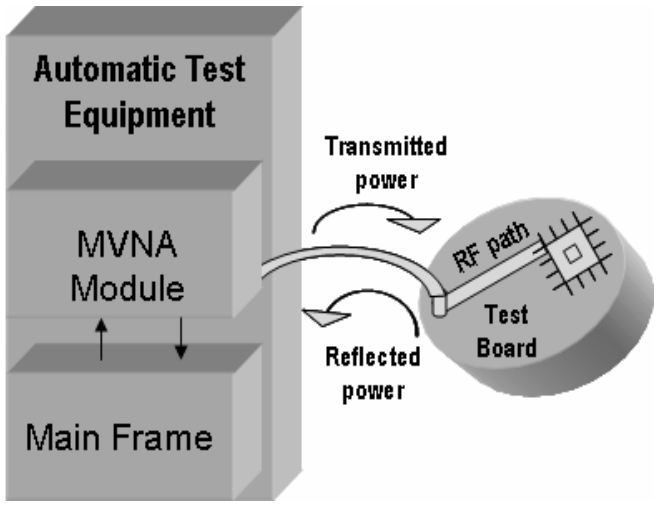


Figure 76. Conceptual representation of the methodology proposed to implement the checker module.

5.4 DEPLOYMENT ON LOW-COST RF ATE

The proposed checker can be also used to test loadboards using low-cost test resources as it requires only reflection measurements to compute the network S-parameters. The 'checker module' can be easily deployed across any test mainframe and the 'dummy ICs' can also be manufactured at negligible cost (for high-volume production). The only overhead cost would be the requirement of a VNA (typically not a part of the low-cost ATE) for the reflection measurements. The block diagram of a typical VNA set-up [78] is shown in Figure 77. The VNA utilizes a synthesized-frequency source, a directional coupler, a tuned receiver detector and a mainframe processor to compute the S-parameters. A low-cost RF source could be built into the ATE as presented in [81] and a high-performance directional coupler could be interfaced to the source near the test head to make these measurements.

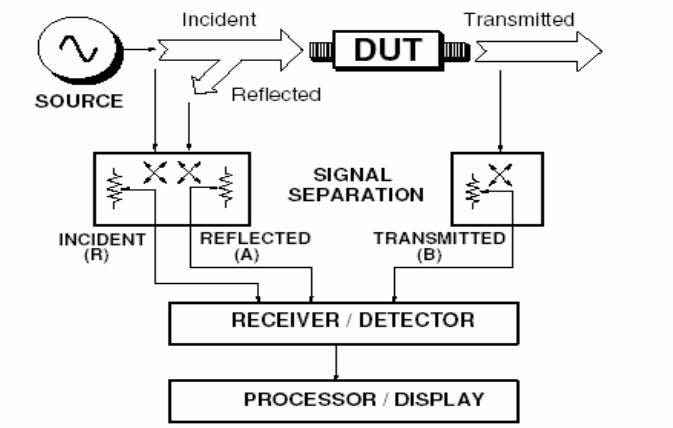


Figure 77. Block diagram of typical VNA set-up.

5.5 VALIDATION OF PROPOSED APPROACH THROUGH SIMULATION OF MODELED BLOCKS

Since it is beneficial and permissible (as opposed to hardware measurements) to evaluate the performance and coverage of the fault checkers in a broad and elaborate manner using circuit simulators, simulations results are presented to validate the proposed approach. Also, it is highly impractical to inject multiple RF faults on expensive production loadboards. The simulations were performed using Agilent's ADS tool. The pilot vehicle used to demonstrate the production worthiness of the proposed methodology was a typical RF signal path used in RF WLAN loadboards (2 GHz). Figure 78 shows the schematic of the RF signal path, which consists of an RF transmission line in the unbalanced side, followed by the BALUN, followed by RF lines on each of the balanced lines with suitable DC blocking capacitors. Normally, matching circuits are used on the balanced side to compensate for any mismatch between the die traces and the BALUN. But this was omitted in this work, since the goal of this work was to evaluate the checker performance and not to design an ideal loadboard circuit. Also, the BALUN is the most critical component on the loadboard. A behavioral model of the BALUN was used in the simulations. This model gives us freedom to inject gain and phase imbalances in the two balanced lines to mimic the real case. The transmission lines were designed using the passive circuit design tool in ADS. The parameters of the BALUN and the transmission lines were optimized to operate in the 2 GHz range.

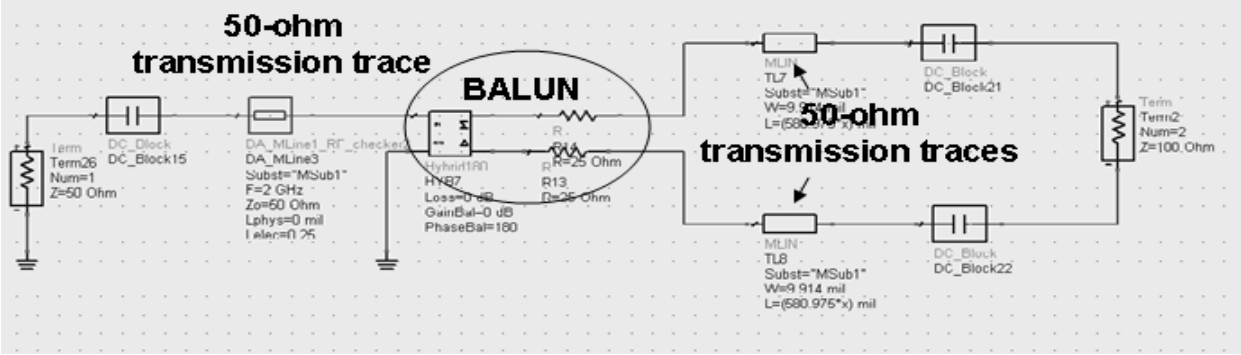


Figure 78. RF-path on loadboard.

Although the signal path is a three-port network, it can be treated as a two-port network by shorting the two output ports. This enables the two-port equations to be used to check/diagnose the network. The termination standards used by the checker were set-up in simulation as follows:

(1) The open termination standard on both the output ports were zero length open terminations

(2) The short termination was obtained by shorting the two output terminals through a zero-ohm resistance.

(3) The characteristic impedance was a 100-ohm termination used between the output ports (similar to using 50-ohm impedances on each output port).

(4) The fourth standard used to calculate the path loss was a 200-ohm termination between the output ports instead of the KGD.

Due to the difficulty in fabricating accurate termination standards on wafer a 5% random Gaussian distribution of the resistance values was used in the termination standards to mimic the real case. Also, a 5% random Gaussian distribution in the phase balance of the BALUN and the transmission line parameters was used to mimic the real case. The ‘checker equations’ were also

set up in ADS to verify the proposed methodology. Equation 35, Equation 39, Equation 41 and Equation 51 presented in Section 5.1 were used to the purpose of diagnosis of the RF signal path. Table 23 compares the actual measurement values and the calculated values using the proposed approach for a 'no fault' case. From the table it can be noted that the developed checker accurately calculates both the magnitude and phase of the network parameters and the path loss.

Table 23. Checker performance for a 'no-fault' case.

	Actual Measurement	'RF checker' Measurement
S_{11} (Mag/Phase)	0.182/-10.555	0.177/-10.574
S_{12},S_{21} (Mag/Phase)	0.629/-94.971	0.632/-94.918
S_{22} (Mag/Phase)	0.235/17.559	0.220/19
RF path loss(dB)	-3.870	-3.840

5.5.1 Fault analysis

To perform the fault analysis of the proposed checker methodology, commonly occurring RF faults on loadboards were injected in the signal path. The faults included the following:

(1) Short on the unbalanced line

(2) Open on the unbalanced line

(3) Open on each of the balanced lines

(4) Short on each of the balanced lines

(5) Short between the balanced lines

These open and short faults were modeled using 1 uH inductors and 1 nF capacitors respectively. The schematic of the signal path highlighting the injected fault models is shown in Figure 79. Table 24 summarizes the results for the above mentioned fault cases. The values of S_{12}, S_{21}, S_{22}, $\Gamma_{(200\ ohm)}$ and the RF path loss computed using the reflection measurements and

derived 'checker equations' are compared to the actual measured values. $\Gamma_{(200\ ohm)}$ is the reflection coefficient of the network to a 200 ohm impedance standard between the output ports. This measurement is required to compute the RF path loss of the network as explained in Section 3.1.1. The numbers in the above mentioned fault list directly correspond to the numbers in the fault condition column of the table. Since the output ports of the BALUN have a symmetric structure, the open and short faults on each of the balanced lines will have the same effect. Hence, only the open and short fault on one of the lines is shown in the table. Also since the RF signal path was a passive structure (S_{21}= S_{12}), S_{12} and S_{21} are displayed the same column. The checker results for the network S-parameters clearly indicate the location of the fault and the calculated path loss accurate tracks the actual path loss for each injected fault.

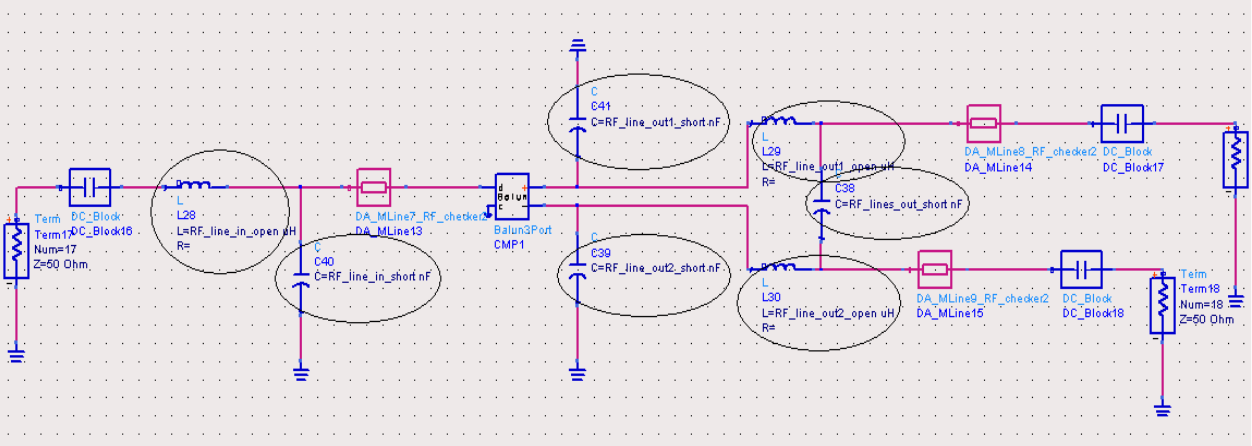


Figure 79 Schematic with various fault models

Table 24. Checker performance for typical RF faults.

Fault Condition	S_{12}, S_{21} (mag/phase)		S_{22} (mag/phase)		$\Gamma_{(200\ ohm)}$ (mag/phase)		RF path loss in dB	
	Measured	Calculated	Measured	Calculated	Measured	Calculated	Measured	Calculated
(1)	0.002/176.8	0.002/176.82	0.56/2.40	0.55//2.50	0.333	0.31/8e-10	-54.14	-54.16
(2)	0.006/173.26	0.006/173.39	0.30/145.68	0.31/147.62	0.333	0.31/7.8e-11	-45.52	-45.44
(3)	0.310/-85.74	0.31/-85.77	0.39/-175.57	0.41/-175.78	0.333	0.308/1e-13	-11.77	-11.68
(4)	0.04/-174.47	0.04/-174.4	0.1/4.83	0.1/4.98	0.333	0.308/1e-11	-25.66	-25.77
(5)	0.001/179.75	0.001/179.78	1/2.33	1/2.40	0.333	0.308/1.4e-8	-54.470	-54.577

5.5.2 Multiple-Fault Analysis

The performance of the checker was also evaluated for multiple faults injected in the RF path simultaneously. The faults injected were an open and a short faults in the balanced lines. Table 25 summarizes the results obtained for the multiple faults case. The results show a high degree of accuracy in tracking the measured parameters for the multiple-fault cases too.

Table 25. Checker performance for multiple fault case.

	Actual Measurement	'RF checker' Measurement
S_{11} (Mag/Phase)	0.286/-29.70	0.286/-29.69
S_{12},S_{21} (Mag/Phase)	0.001/-179.73	0.001/-179.66
S_{22}(Mag/Phase)	1/4.84	1/4.99
$\Gamma_{(200\ ohm)}$	0.333/0.0	0.308/-8.27e-8
RF path loss(dB)	-53.83	-53.93

5.5.3 Fault Coverage

Different instances of the faults were generated by sweeping the capacitance and inductance values of the fault model to establish the fault coverage. The capacitance value ranged from 0 (no fault) to 1 uF (near short fault). Also, the inductance value ranged from 0 (no fault) to 1 mH (near open fault). Only the RF path loss measurement comparisons are presented in this section to qualify the proposed approach, since the path loss employs all the parameters that are calculated by the checker as shown in Equation 51. The path loss will be calculated accurately only if the intermediate parameters are also calculated in an accurate manner. The distribution of the measured path loss for 130 different faults injected in the signal path is shown Figure 80. The distribution of the calculated path loss using the proposed checker for the same faulty instances is shown in Figure 80. The distributions show the range of the path losses for the different faults injected and also the accuracy of the checker for diagnosing these faults. The key highlights of this experiment were found to be:

- Max error in path loss calculation for 130 different faults = 0.1 dB
- 100 % RF fault coverage

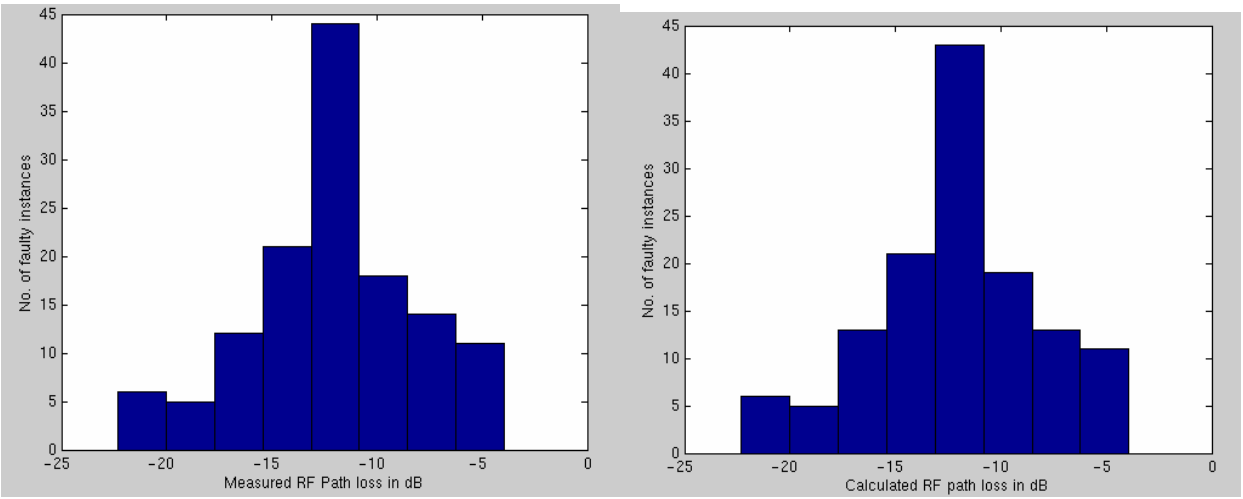


Figure 80. Distribution of measured and calculated path loss for multiple faulty instances.

5.6 HARDWARE VALIDATION OF PROPOSED LOADBOARD CHECKER MODULE

Hardware validation of the developed checker tool was performed on a loadboard used for high-volume testing of WLAN transceiver systems. The schematic of the path used for validation is shown in Figure 81. This passive RF path contains (from the right) an RF port, a matching network in the unbalanced side, a BALUN with suitable biasing circuitry, 50-ohm matched transmission lines on each of the balanced lines, and matching networks at the end of each of balanced paths. The balanced output from the matching networks is connected to the die trace on the board. This RF path, optimized to operate in the 2-2.2 GHz band, is a three-port passive RF network ($S_{12}= S_{21}$, $S_{13}=S_{31}$, $S_{23}=S_{32}$) and hence, six different S-parameters need to be measured to characterize the network. The following combination of termination standards were used on the two output ports of the network.

- Characteristic impedance on both ports (50-ohm)
- Open -- open
- 50-ohm -- short
- Short -- 50-ohm
- Open -- 50-ohm
- 50-ohm -- open

These terminations were developed as follows:

Open: An ideal open termination was employed, in which no connection was formed. The open standard from the calibration kit cannot be used for this purpose due to the inherent extension in their reference planes (32 ps in a 3.5 mm calibration kit). This extension modifies the reflection coefficients at the output ports.

Short: Conducting paper was used to provide the interface between the SMA connector pin and the SMA ground. Again, the calibration short cannot be used due to the inherent extension in their reference plane.

50-ohm load: The 50-ohm standard from the calibration kit was used to provide the characteristic impedance. The performance of this standard does not depend on their inherent extension.

During production deployment, these standards can be developed on the same wafer material as the die to reduce any errors due to material mismatch.

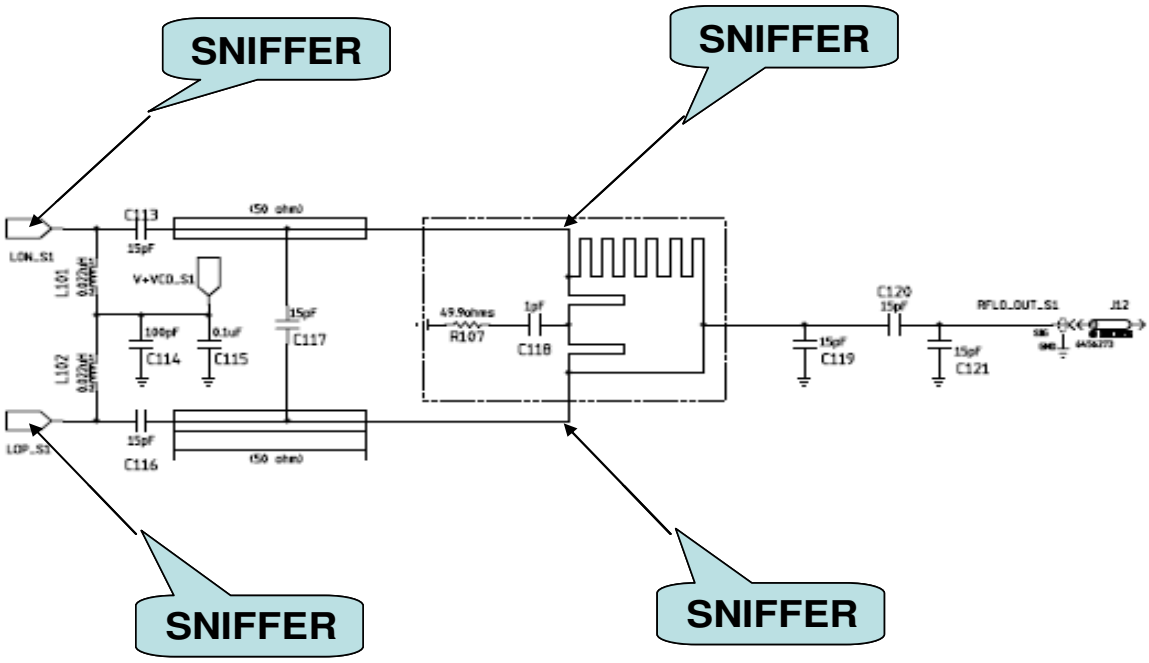


Figure 81. Schematic of the RF path on the loadboard used for the production testing of WLAN transceivers.

5.6.1 Case Study 1: Performance of checker for fault-free RF path

Different combinations of termination standards were used to terminate the output ports and their corresponding reflection coefficient measurements were made using a VNA. The network configuration, the indeterminates and the VNA measurements were input to the 'checker module'. The checker module was implemented in MATLAB to evaluate the developed methodology. This module could be effortlessly ported to the mainframe of the ATE. The blue line in Figure 82 and Figure 83 corresponds to the respective magnitude and phase values of the computed S-parameters of the RF path.

Verifying the accuracy of these results poses the same problem as the motivation for this work. The absence of a physical port at the output makes it impossible to verify these S-parameter measurements. In order to overcome this problem, small pieces of coaxial cable with a SMA connecter (commonly referred to as a 'SNIFFER' in characterization labs) were soldered on to the two balanced die traces. This enables three-port S-parameter measurement using a VNA. All the measurements presented in this section use the SMA end of the coaxial cable as the reference plane. The S-parameters measured using this procedure corresponds to the red lines on the plots of Figure 82 and Figure 83. Table 26 summarizes the maximum error values obtained between the computed and measured values of all the S-parameters over a 200 MHz bandwidth. From this table, it can be observed that the magnitude and phase values of the S-parameters could be calculated very accurately using the proposed loadboard checker tool.

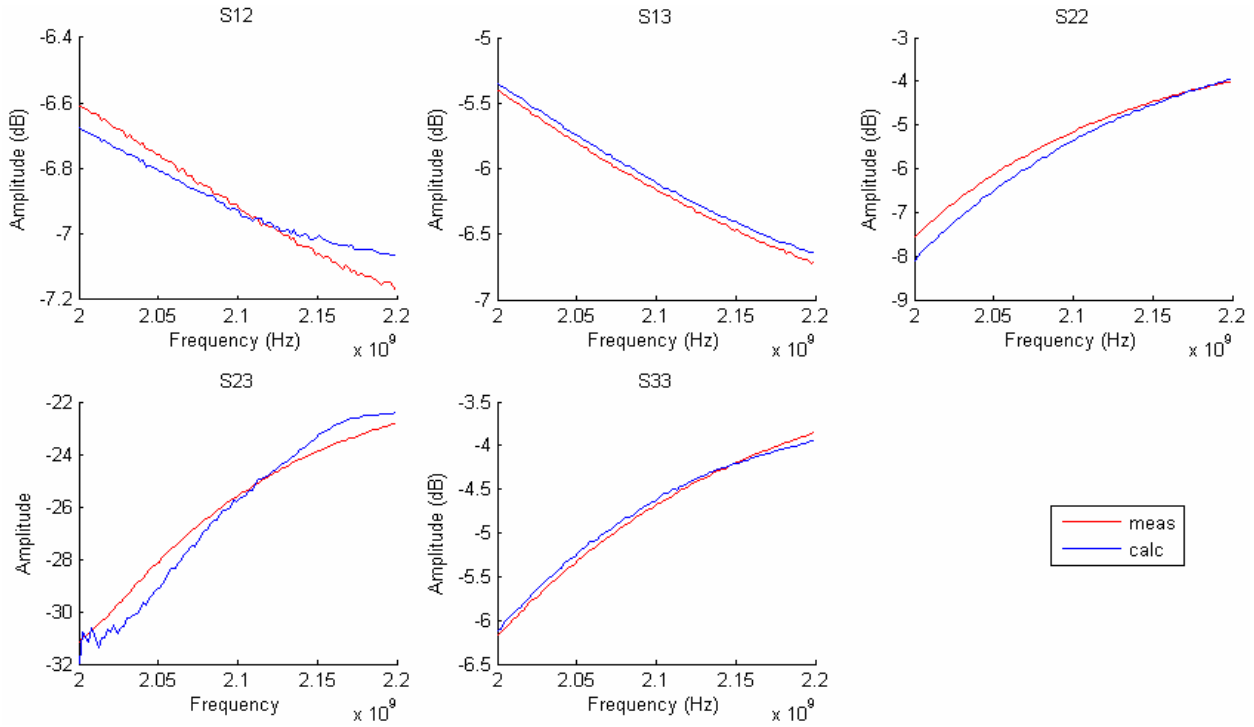


Figure 82. Magnitude comparison of computed and measured S-parameters for fault-free case.

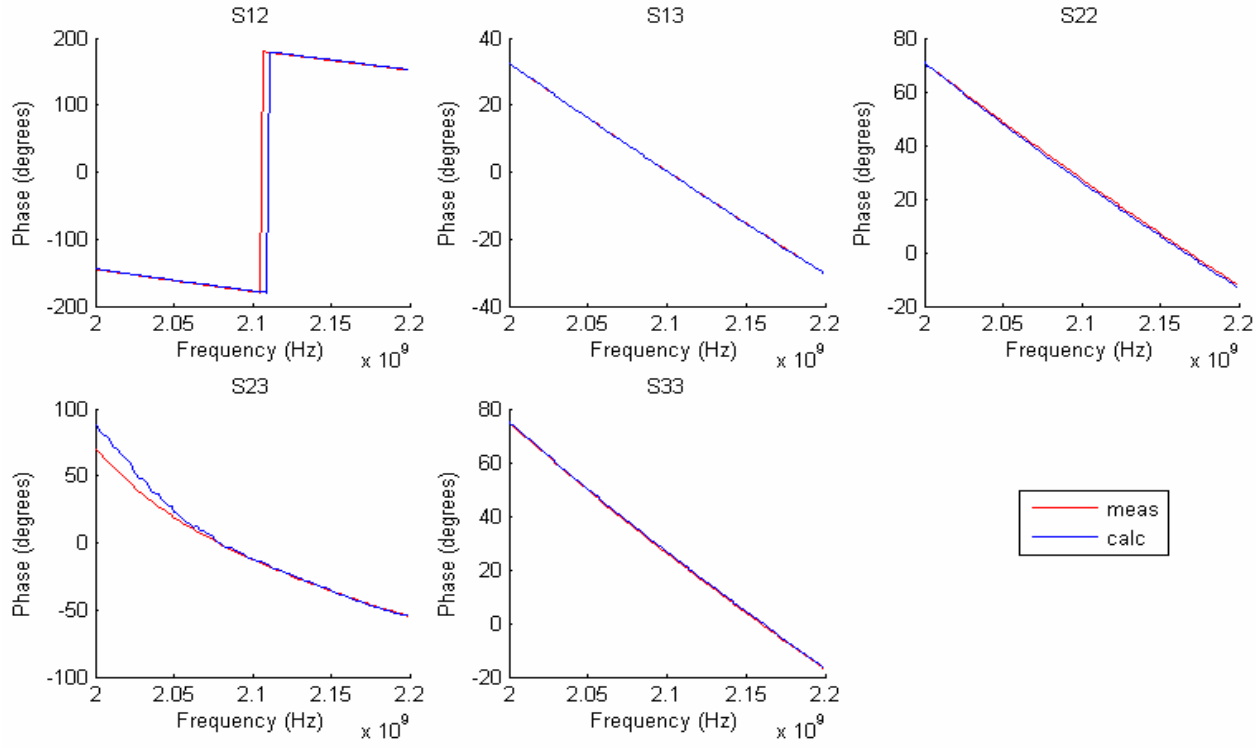


Figure 83. Phase comparison of computed and measured S-parameters for fault-free case.

Table 26. Checker performance for a 'no-fault' case.

Maximum Error in 200 MHz bandwidth	Magnitude (dB)	Phase (degree)
S_{12}, S_{21}	0.10	0.09
S_{13}, S_{31}	0.07	0.23
S_{22}	0.54	1.13
S_{33}	0.09	0.69
S_{23}, S_{32}	1.17	18.79

5.6.2 Case Study 2: Performance of Checker for Parametric Faults

Poor storage conditions, improper handling and, the short lifetime of the components used on the loadboards can cause mechanical and/or electrical defects which serve as potential reasons for a low test yield. Hence, it is required to check the performance of the checker tool for commonly occurring parametric faults on the loadboards. Since measurements made on expensive production loadboards are used to validate the proposed tool, it was highly impractical to evaluate multiple fault cases. Hence, in this work, the performance of the checker for three parametric fault cases at different ports of the RF network was evaluated by manually replacing the good components with faulty ones. The injected parametric faults are listed below:

- Component C116 changed from 15pF to 1pF
- Component C120 changed from 15pF to 1pF
- Component C113 changed from 15pF to 39p

The schematic of the RF path wherein each of these parametric fault cases is highlighted is presented in Figure 84. The reflection measurements were made for each of these cases with the same termination standards as in the previous case. The checker module was used to compute the S-parameters for each of these cases using their corresponding reflection measurements. The computed magnitude and phase values of the key S-parameters S_{12}, S_{13}, S_{22} and S_{33} using the

checker tool along with their corresponding measured values (using a VNA) for the parametric fault case (1) is shown in Figure 85 and Figure 86. The measurement of S-parameters for validation purposes was performed using the methodology explained in the fault-free case (under normal circumstances this would not be possible). Just as in the fault-free case, the blue legend in the figure is used to represent the computed values and the red legend in used to represent the measured values. Similar plots comparing the magnitude and phase values of the computed and measured values for the second and third parametric fault case is presented in Figure 87, Figure 88, Figure 89, and Figure 90. Table 27 summarizes the maximum errors obtained for the magnitude and phase values of the four key S-parameters (S_{12}, S_{13}, S_{22}, S_{33}) in each of these parametric fault cases. As shown in the table, the proposed checker can be used for accurate detection of RF parametric faults on loadboards.

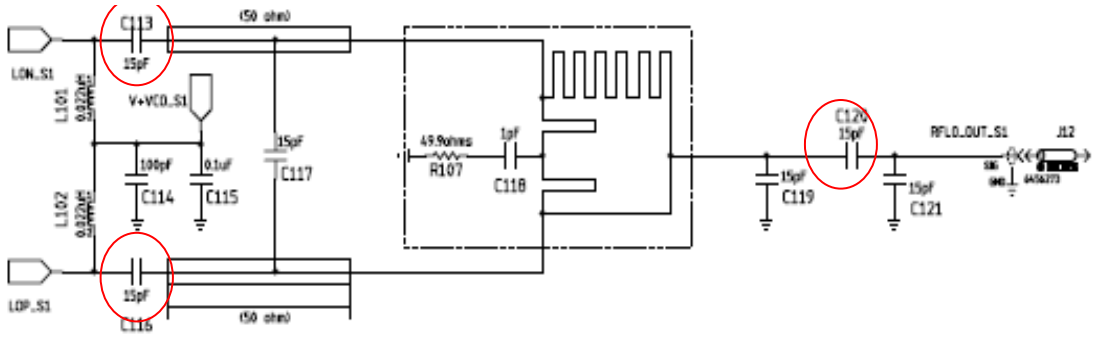


Figure 84 Schematic of the RF with the injected parametric faults highlighted

Table 27. Summary of results for the parametric fault analysis.

Parametric fault case	S_{12} (Max. error in 200 MHz bandwidth)		S_{13} (Max. error in 200 MHz bandwidth)		S_{22} (Max. error in 200 MHz bandwidth)		S_{33} (Max. error in 200 MHz bandwidth)	
	Magnitude (dB)	Phase (degree)	Magnitude (dB)	Phase (degree)	Magnitude (dB)	Phase (degree)	Magnitude (dB)	Phase (degree)
1	0.02	3.1	0.05	5.9	1.3	1.7	1.4	0.8
2	0.10	4.0	0.30	7.0	1.6	13	2.5	15.0
3	0.05	3.2	0.08	5.3	0.9	2.5	1.3	5.8

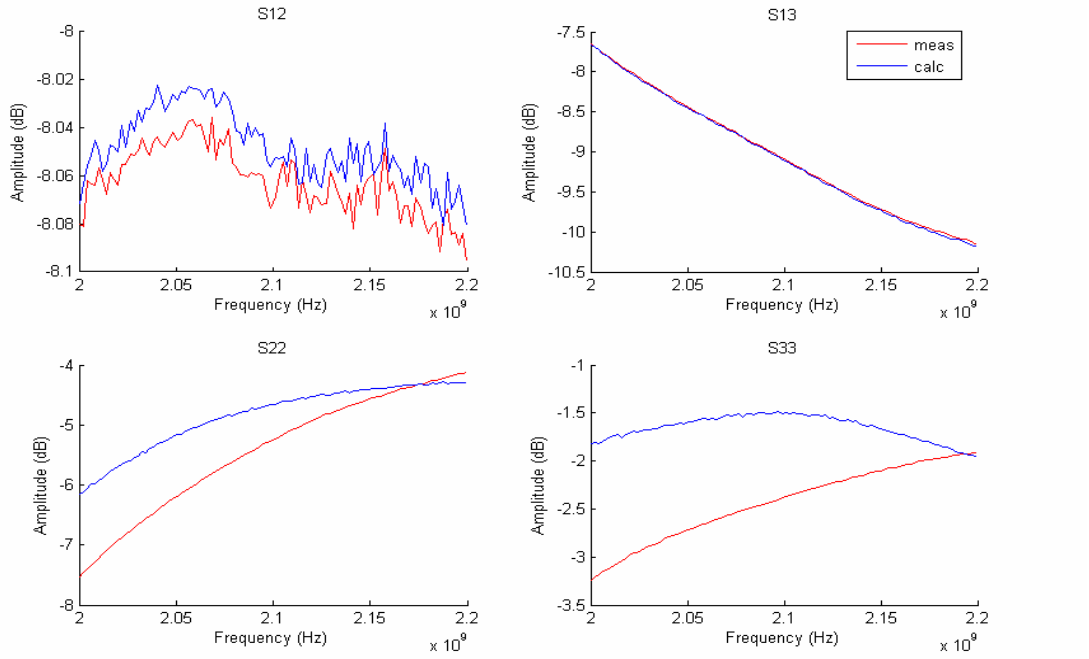


Figure 85. Magnitude comparison of computed and measured S-parameters for parametric fault case (1).

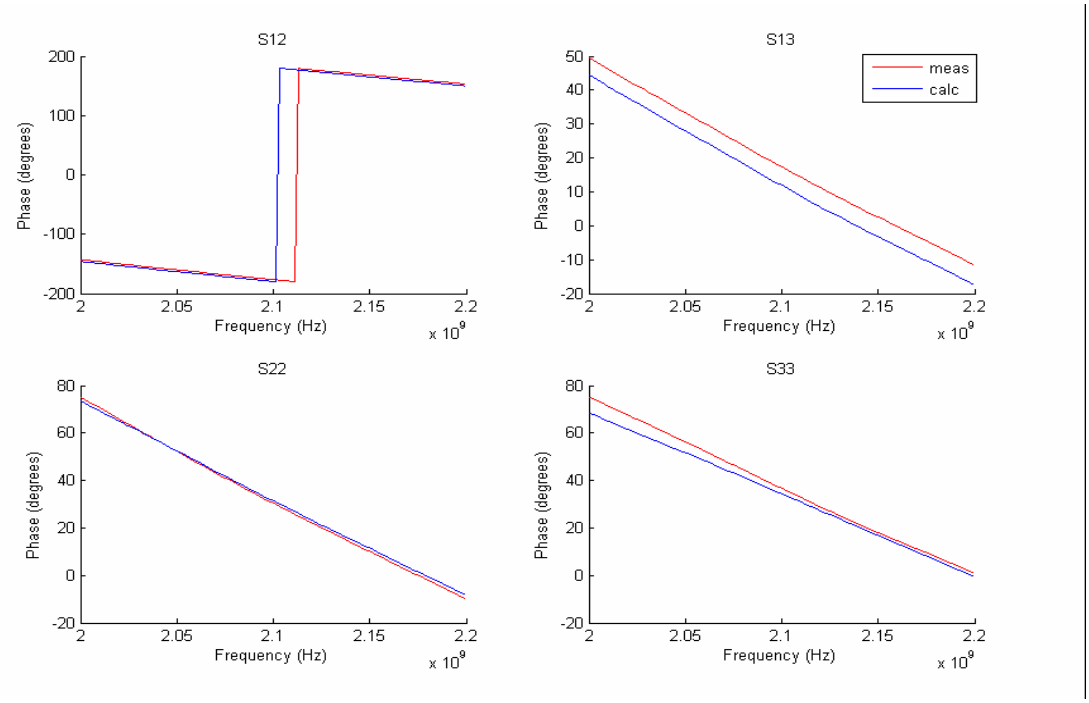


Figure 86. Phase comparison of the computed and measured S-parameters for parametric fault case (1).

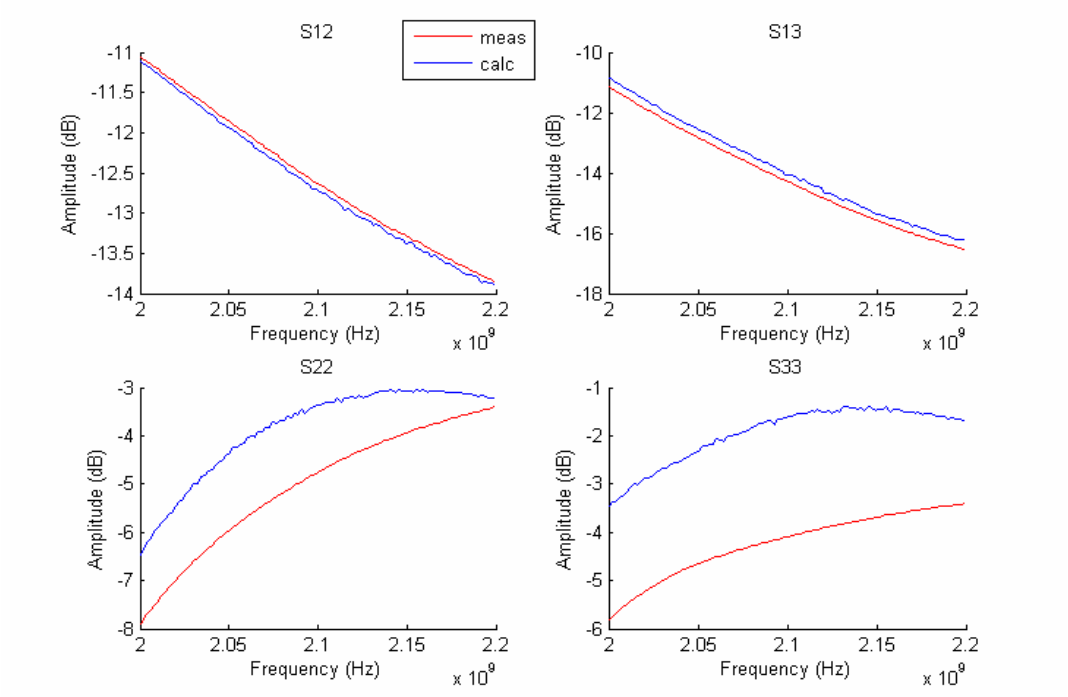


Figure 87. Magnitude comparison of the computed and measured S-parameters for parametric fault case (2).

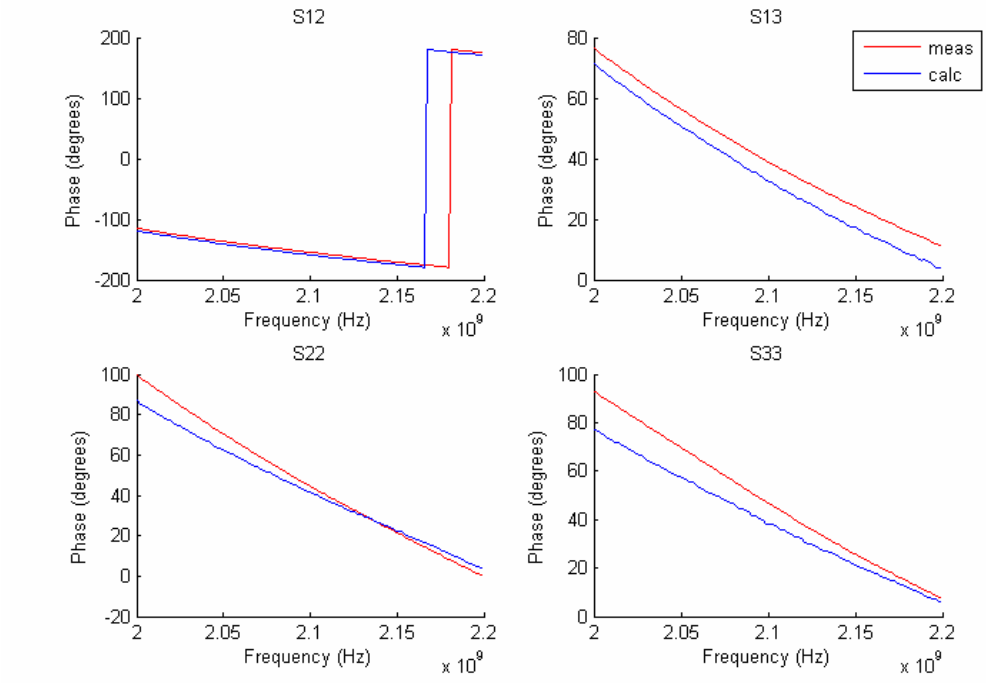


Figure 88. Phase comparison of the computed and measured S-parameters for parametric fault case (2).

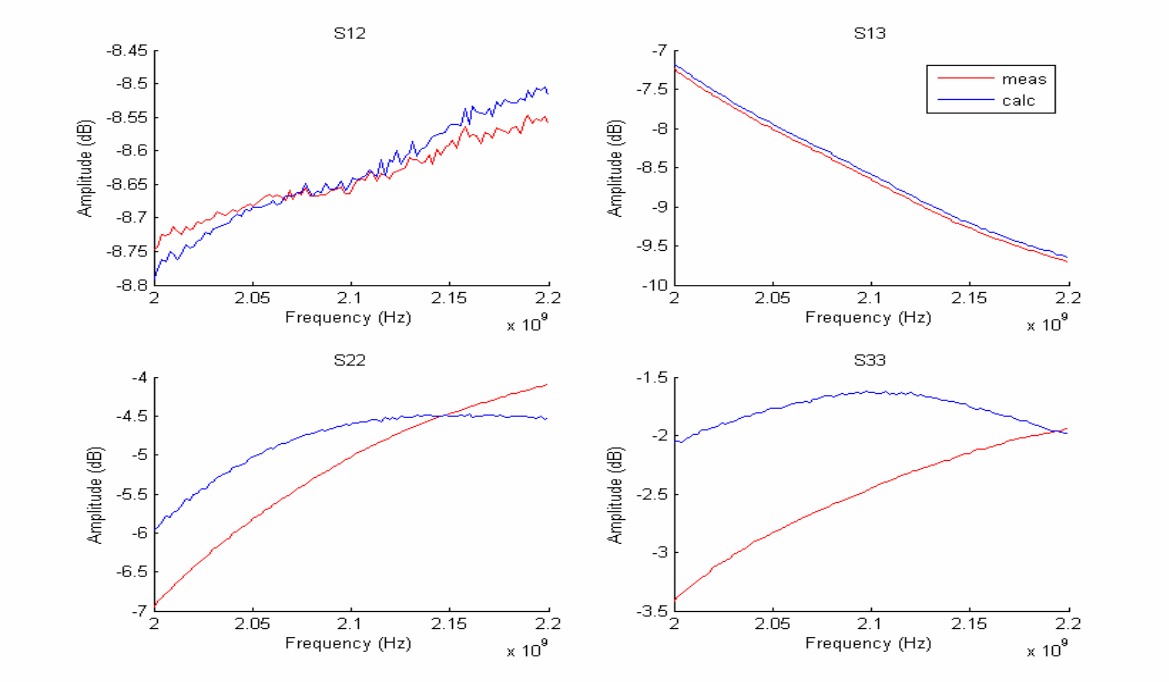


Figure 89. Magnitude comparison of the computed and measured S-parameters for parametric fault case (3).

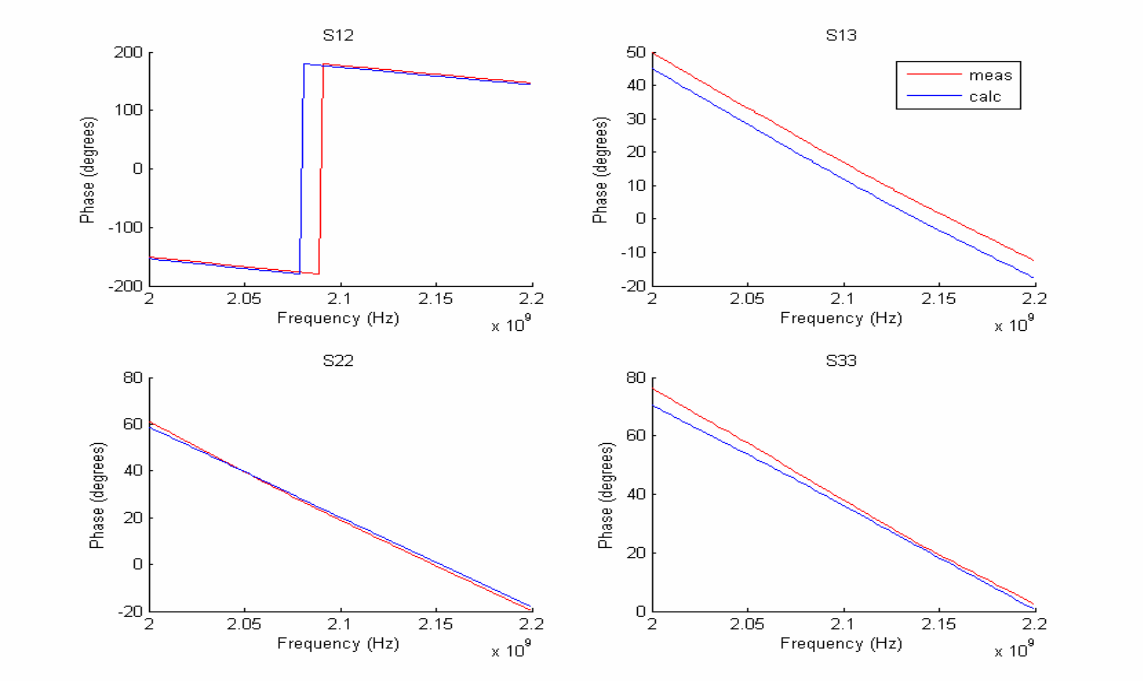


Figure 90. Phase comparison of the computed and measured S-parameters for parametric fault case (3).

5.6.3 Case Study 3: Performance of Checker for Catastrophic Faults

Poor storage conditions and improper handling could also cause components or printed lines on the loadboard to be permanently damaged. Hence, the performance of the proposed checker in detecting commonly occurring catastrophic faults was also evaluated. The following catastrophic faults were considered in this work.

(1) Open on the unbalanced line

(2) Short on the unbalanced line

(3) Open on each of the balanced lines

(4) Short on each of the balanced lines

(5) Short between the balanced lines

Figure 91 shows the schematic of the RF path on the loadboard with each of the catastrophic fault cases highlighted. As shown in the figure, these open and short faults were modeled using 1 uH inductors and 1 nF capacitors, respectively. The reflection measurements were made for each of these cases with the same termination standards. The checker module was used to compute the S-parameters for each of these cases using their corresponding reflection measurements.

Table 28 summarizes the maximum computation errors obtained for magnitude values of the four key S-parameters (S_{12}, S_{13}, S_{22}, S_{33}) for the first four catastrophic faults. In this case study, only the magnitude measurements were used to validate the checker, because only detection is required in the case of catastrophic fault analysis as opposed to the other two case studies. The table also highlights some of the error values in S-parameter computation. These errors arise due to the uncertainties in the reflection measurements caused by the location of the catastrophic fault. In the case of open fault on the unbalanced line, the fault is located at the input

port used for the reflection measurements. For this case, the magnitude of the computed S-parameters S_{12}, S_{13}, S_{22} and S_{33} and their corresponding measured values are compared in Figure 92. Again, the measurement of S-parameters for validation purposes was done using the methodology explained in the fault-free case study. Even with the uncertainty in the reflection measurements due to the location of the fault, the checker can identify these faults due to their large deviation in S-parameter values from their fault-free ones. From the figure, it can be observed that the computed S_{12} and S_{13} are far away from their 'fault-free' expected values (approximately -35dB). For these kind of values, accuracy is not expected as the checker would render the board 'useless'. Similar plots for other catastrophic faults listed in Table 28 are presented in Figure 93, Figure 94, and Figure 95 respectively.

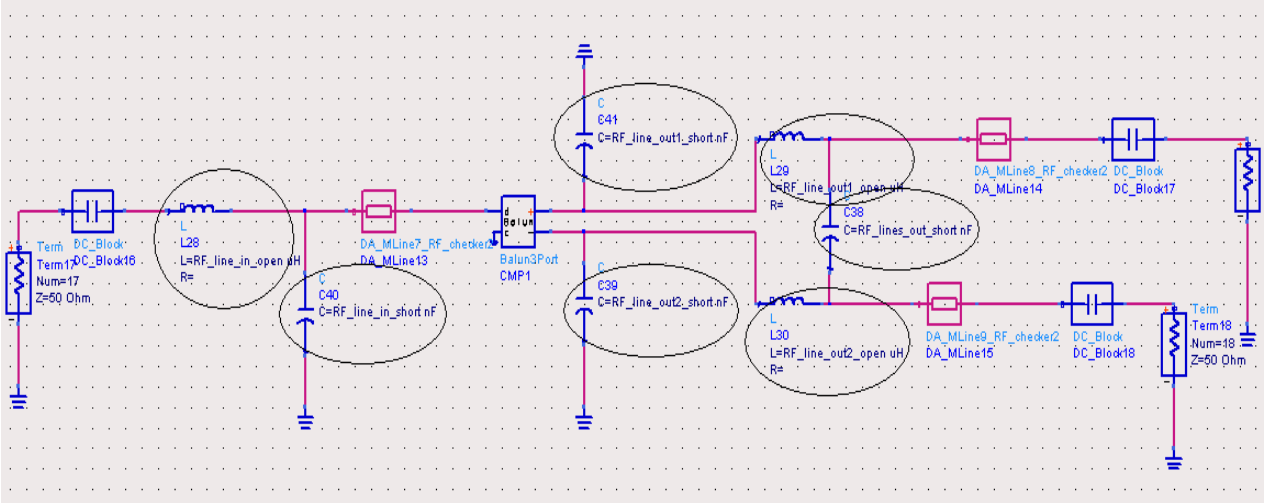


Figure 91. Schematic of the RF with injected catastrophic faults highlighted.

Table 28. Summary of results for the catastrophic fault analysis.

Catastrophic fault case	S_{12} (Max. error in 200 MHz bandwidth)	S_{13} (Max. error in 200 MHz bandwidth)	S_{22} (Max. error in 200 MHz bandwidth)	S_{33} (Max. error in 200 MHz bandwidth)
	Magnitude (dB)	**Magnitude** (dB)	**Magnitude (dB)**	**Magnitude (dB)**
Unbal. open	7	9	17	22
Unbal. short	0.2	0.1	1.3	1.9
Bal. open	0.08	9	1.7	12.2
Bal. short	0.09	0.1	1.9	1.5

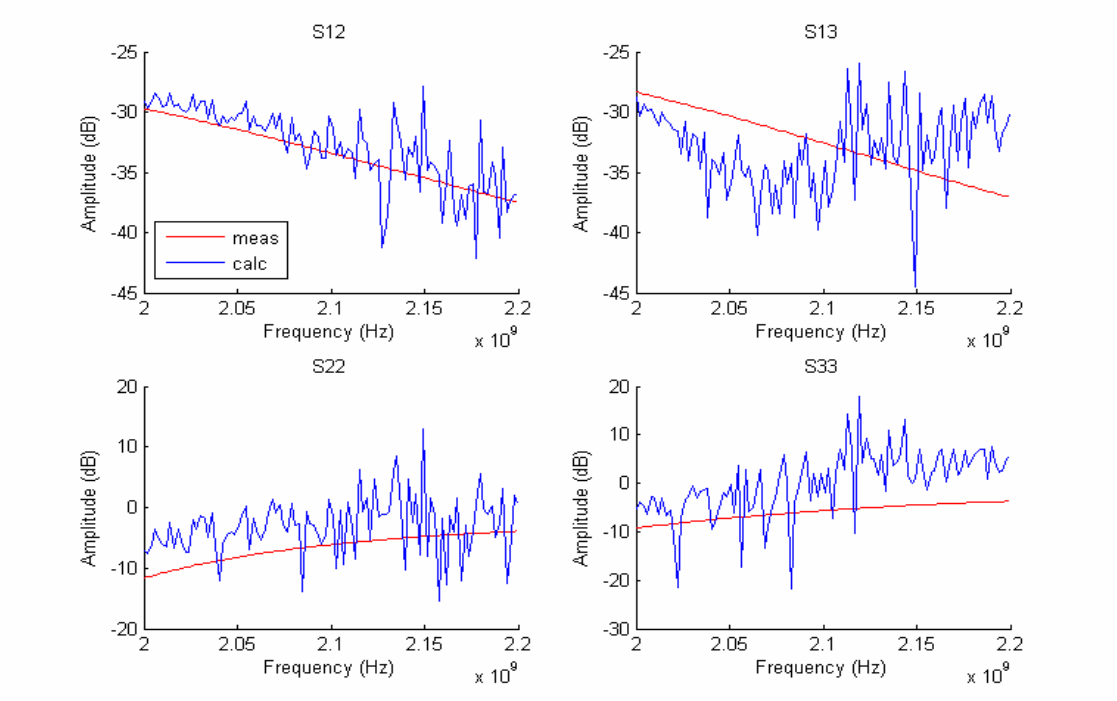


Figure 92. Magnitude comparison of computed and measured S-parameters for an RF open fault on the unbalanced line.

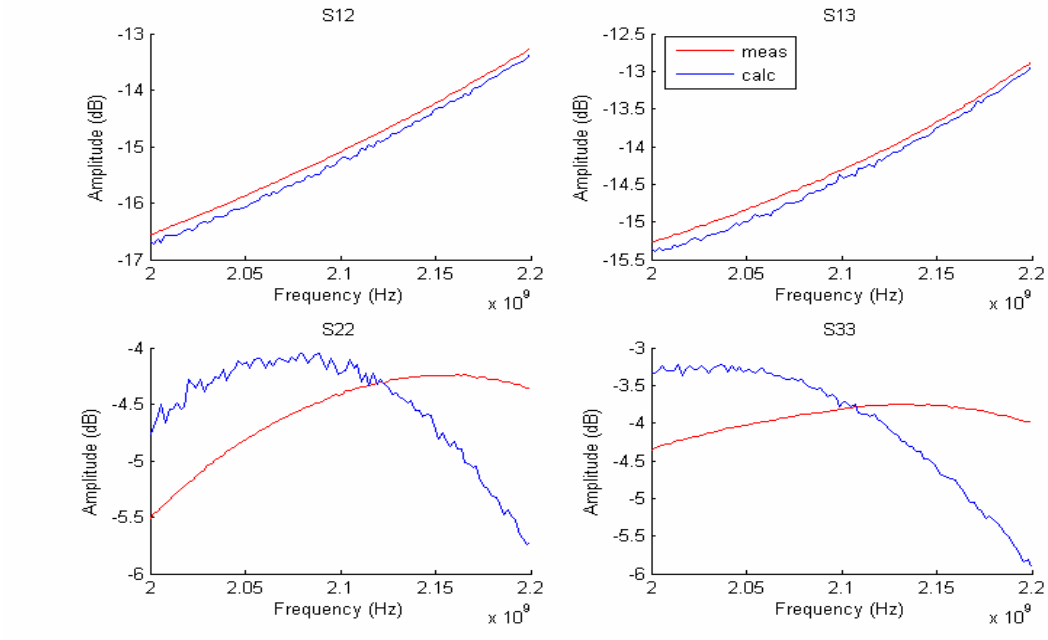


Figure 93. Magnitude comparison of computed and measured S-parameters for RF short fault on one of the balanced lines.

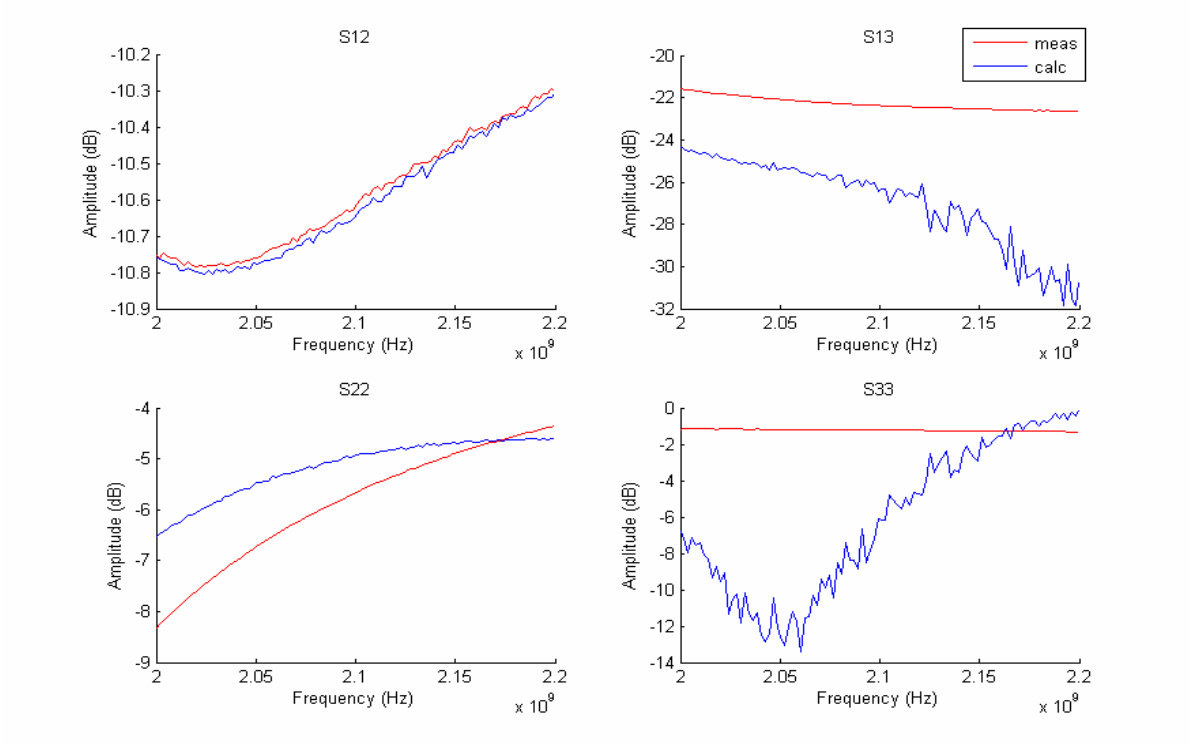


Figure 94. Magnitude comparison of computed and measured S-parameters for an RF open fault on one of the balanced lines.

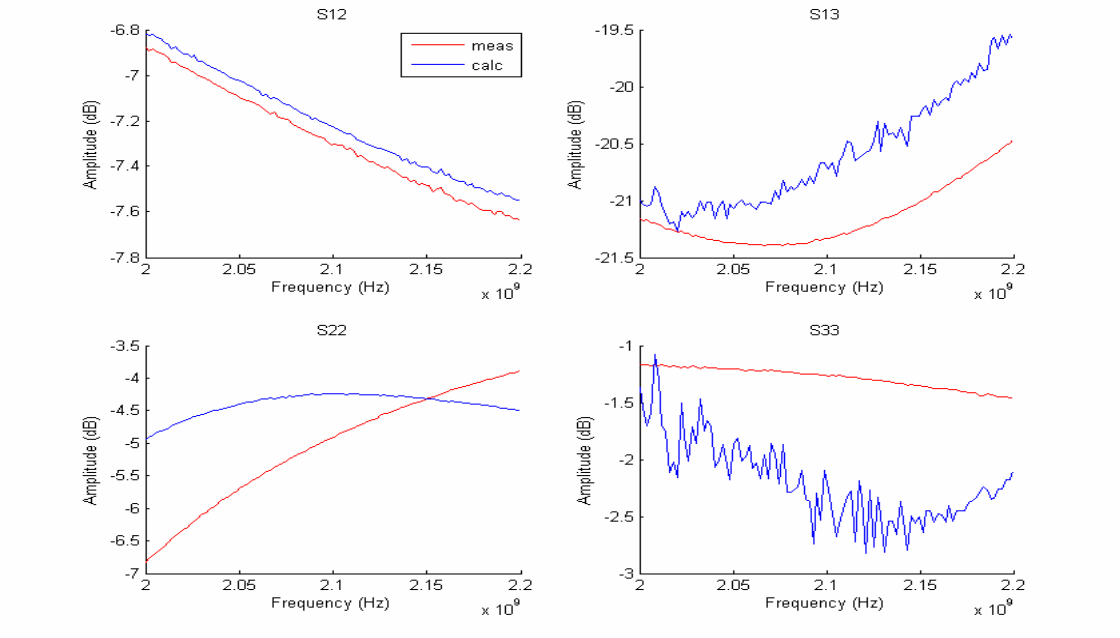


Figure 95. Magnitude comparison of computed and measured S-parameters for an RF short fault on one of the balanced lines.

5.7 STUDY OF ACCURACY OF THE CHECKER FOR 'NOT-SO ACCURATE' TERMINATION STANDARDS

In the proposed approach, different combinations of the commonly used termination standards (1) open, (2) short, (3) characteristic 50-ohm are used to terminate the network based on the total number of ports. These termination standards can be fabricated on "dummy" ICs with the same wafer material as the RF DUT. In certain cases, it might not be possible to fabricate accurate standards. Hence, a study was conducted to compare the accuracy of the checker to the accuracy of the termination standards employed.

The 'checker module' uses the following ideal reflection coefficients of the termination standards to derive the checker equations,

- Open : $\Gamma'=1$
- Short : $\Gamma'=-1$
- Load : $\Gamma'=0$

Normally, due to process variations in the employed termination standards, the reflection coefficients at the output port might vary from their ideal values. The drift in the processes could cause a shift in the resistance or reactance values. To study the performance of the checker for variations in the termination standards, the S-parameters were computed for a set of hundred open and short terminations within 10% of their ideal reflection coefficient values. These values were compared with the measured parameters to study the performance of the checker.

In Section 5.6.1, the S-parameters of the network were computed using the proposed checker for a fault-free performance over a 2-2.2 GHz band. From this experiment, the reflection coefficient measurements at a frequency of 2 GHz were used to evaluate the performance of the checker for variations in the termination standards. A set of hundred checker equations were

generated based on the set of hundred open or short termination standards generated by changing their reflection coefficient values. The reflection coefficient measurements for various combinations of standards at 2 GHz were fitted into each of these equation sets to compute the S-parameters. These new values were compared to the measured S-parameters as explained in Section 5.6.1 at 2 GHz. Table 29 lists the maximum errors obtained between the measured S_{12} parameter (does not change) and the computed values for variations in the reflection coefficient in the open and short termination standards. As shown in the table, a 10% variation in any of the termination standards has no considerable effect on the performance of the checker. The same was the case for all the other S-parameters too, since the variations in the standards will cause similar effects on the computed set of S-parameters.

The performance of the checker could be further improved by performing a one-time calibration of these termination standards. Once these dummy ICs are calibrated, their reflection coefficients could be used to derive the checker equations instead of the ideal ones. This would provide near-perfect results for the fabricated standards.

Table 29. Checker tool performance for a 'no-fault' case.

Max error in S_{12} computation	Open	Short
Magnitude(dB)	0.6197	0.5550
Phase(degrees)	9.4	9.39

Chapter 6

ADVANCED TEST SIGNAL PROCESSING ALGORITHMS: ACCURATE CAPTURE OF THE SYSTEM RESPONSE USING LOW-PERFORMANCE ATE RESOURCES

Chapter 3 of this thesis presents a spectral signature-based CAD framework for efficient production testing of RF systems using low-cost ATE. The proposed framework uses baseband resources of the low-cost, mixed-signal ATE to process the test signals. Also, the CAD framework involves co-simulation of test resources along with the RF systems for reliable test generation purposes. Development and deployment of such a framework would involve a clear understanding of the performance of the test resources in the mixed-signal ATE. Typically, low-cost ATE use older generation devices that do not permit accurate measurement of these signals. The nonlinearity and noise in the digitizer of the ATE limits the accuracy of measurement. Hence, the possibility of linearity/resolution improvement of the test resources needs to be considered for accurate testing purposes.

In modern cellular phone systems, the handset transmitters are power controlled, so almost the same amount of power is received for each channel at the base station. The receivers used in cable tuners, DSL solutions, repeaters and satellite communications also must operate properly in the presence of a multitude of large carriers. For example, asymmetric digital subscriber line (ADSL) technology employs quadrature amplitude modulation (QAM). Hence, the dynamic ranges of discrete multi tones in the modulated signal and their linearities through

all the transmission paths need to be large enough to guarantee the required data throughput. Also, multiple channels are simultaneously used for transmission and reception, which makes it necessary to check for the inter-modulation distortion in these multi-carrier systems.

In the scenario of single tone carrier systems, the linearity/distortion performance is normally measured by calculating specifications like spurious-free dynamic range (SFDR), two-tone inter-modulation distortion (IMD) and three-tone IMD (triple beats). If there are a large number of equally spaced and sized carriers, similar to the case of discrete multi-tone signals, then two-tone IMD is constant over the band while triple-beat distortion peaks fall in the middle of the band [64]. In addition, there are many more triple-beat products than two-tone products. These, combined with the triple beats being twice as large as the two-tone products, result in triple-beat IMD limiting the dynamic range of multi-channel systems more than two-tone IMD, particularly in the center of the band.

In multi-carrier systems, multi-tone power ratio (MTPR) specification is often referred to as the figure-of-merit as this specification more accurately represents the multi-carrier distortion performance in communication devices. When performing the MTPR test, the discrete multi-tones with some missing tones are input to the DUT as shown in Figure 96. The missing tones are specified by the communication standard. The amplitudes of all existing tones are determined by the power spectral density specifications of the specific technology. Due to the nonlinearity of the DUT, distortion components will show up in the output spectrum and raise the energy of missing frequency bins. MTPR is then obtained by calculating the ratio between average power of existing tones and the maximum power in the missing tones and is expressed in dB.

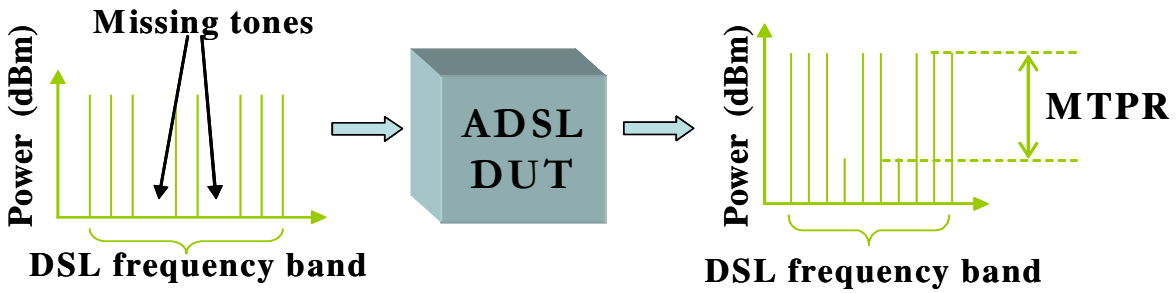


Figure 96. MTPR test procedure.

Typically low-cost ATE use older generation devices (low-resolution) that do not permit accurate measurement of the MTPR specification [92]. Figure 97 shows the FFT plot of a signal captured at the transmit chain output of a central office (central office) ADSL coder-decoder (CODEC) device to a 16 dB peak-to-average (PAR) discrete multi-tone signal using a low-cost ATE. This plot was obtained by capturing 65K samples of the time domain signal at the transmitter output port and computing the FFT on the average of ten such captured signals. From the plot, it can be observed that MTPR of this signal is about -63 dB. These CODEC devices typically exhibit about -75 dB MTPR performance, when measured using high-performance bench equipment. The problem addressed in this chapter is as follows: The nonlinearity of the digitizer in the low-cost ATE is limiting the MTPR measurement. Additional nonlinearity components are added by the digitizer in the missing bins of the MTPR test. Hence, it is not possible to measure MTPR to the required level of accuracy using a low-cost ATE.

In this work, a novel test architecture that enables reliable and robust production test of MTPR on ADSL devices using low-cost ATE is presented. In this approach, an optimally derived multi-tone noise signal is added along with the DUT output signal to be digitized so as to randomize or smoothen the nonlinear static errors of the ADC in the ATE digitizer that limit the linearity measurement. The multi-tone noise is a new form of dither noise proposed in this work

to reduce the distortion contributed by the digitizer in the missing bins of the MTPR test. Initial validation of the proposed approach was performed using modeled blocks of typical low-cost test equipment in MATLAB simulation environment. The improvement in the range of possible MTPR measurements in the simulation experiments resulted in experimental validation of proposed architecture on a low-cost ATE platform. In one of the case studies, ADSL central office CODEC devices were used as the test vehicle for the validation experiments. Results presented in Section 6.12 show that an improvement of approximately 7dB in linearity of MTPR measurement could be achieved using the proposed architecture. The experimental results also include statistical analysis performed on low-cost ATE to evaluate the repeatability and robustness of the proposed architecture.

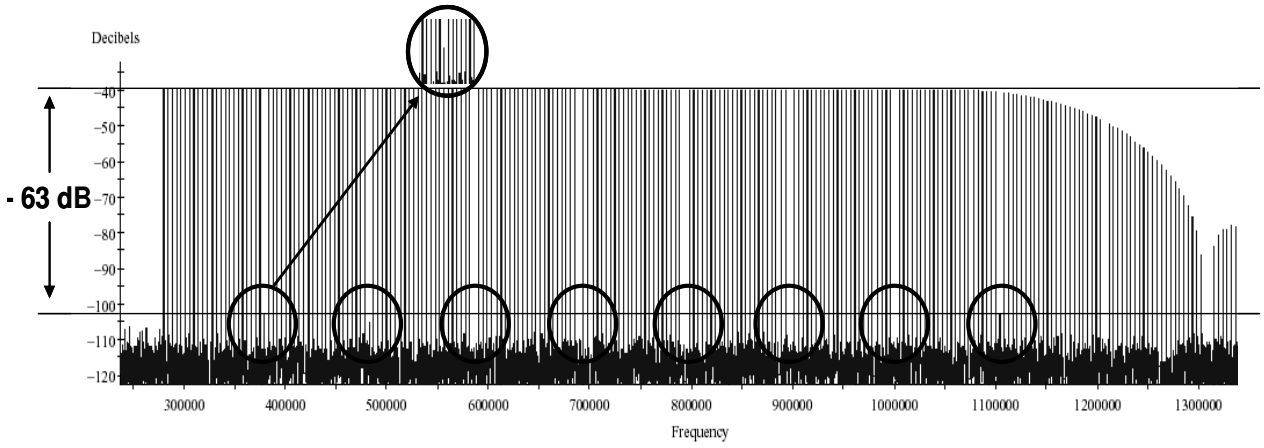


Figure 97. TX MTPR for ADSL CODEC DUT measured on low cost ATE.

6.1 ADSL TECHNOLOGY: BASICS

ADSL technology delivers high-speed internet access on existing twisted copper wire pair cables used by plain old telephone service (POTS) [85][86][87]. The twisted copper wire pair can support a frequency bandwidth beyond the useful frequency range of POTS. The lower 20 KHz is used by POTS to provide telephony services while ADSL technology uses the bandwidth from 26 KHz to 2.2 MHz to provide broadband internet services. The ADSL bandwidth is subdivided into up-stream and down-stream channels [86]. The upstream channel is within a lower frequency range and is used to carry data from the subscriber to the central office; while the downstream channel, in higher frequency range, is used to carry the data from the central office to the subscriber. The spectral usage of the copper wire pair based communication channel is shown in Figure 98. Due to the different average data throughput requirements for these upstream and downstream channels, the channels have much fewer bins than the downstream channel [86].

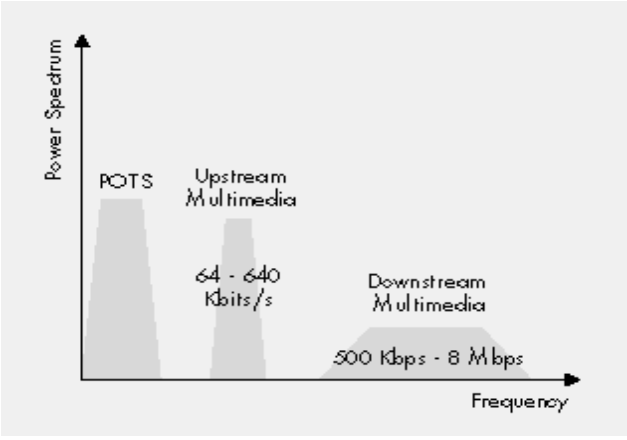


Figure 98. Spectral usage of the twisted copper wire pair.

ADSL technology employs discrete multi-tone modulation in which the frequency range is divided into 256 sub-frequencies or sub-carriers from 26 KHz up to 2.2 MHz [84][88][89]. A discrete multi-tone modulation appears in the frequency domain as power constrained signals in several individual sub-frequency bands [89]. Each sub-frequency band acts as an independent channel and has its own stream of data. Each channel in the ADSL spectrum has a bandwidth of 4.3125 KHz. The channel frequency is usually specified in terms of its bin number. The bin number multiplied by the channel bandwidth determines the channel frequency (bin number x 4.3125 KHz). The ADSL bandwidth ranges from bin 6 (6 * 4.3125 KHz = 26 KHz) to bin 511 (511 * 4.3125 KHz = 2.204 MHz) as shown in Figure 99. The range of bins in the upstream and downstream channels depends on the mode of ADSL transmission. These modes are specified by the ADSL transmission standard [90]. Table 30 presents some of these modes and their corresponding bin arrangement scheme.

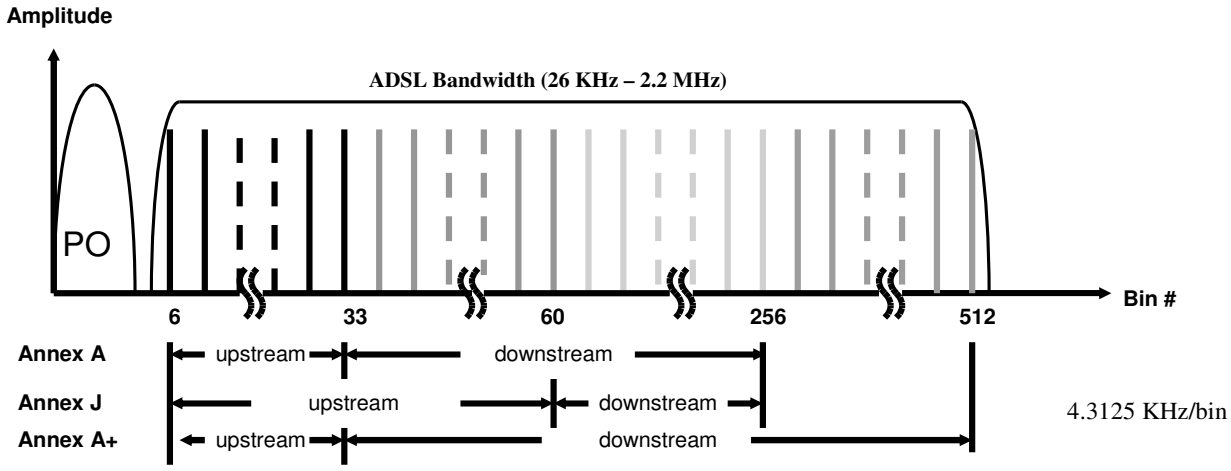


Figure 99. ADSL Discrete Multi-Tone Spectrum.

Table 30. ADSL Modes and Frequencies.

ADSL Modes	Upstream Bins	Downstream Bins
Annex A (ADSL over POTS)	6 - 31	33 - 255
Annex A+ (ADSL+ over POTS)	6 - 31	38 - 511
Annex J (EFM over POTS)	6 - 60	60 - 255

QAM is used to modulate carrier tones to carry digital data in each of the independent carrier bins. In QAM, two signals with 90 degrees phase difference (sine and cosine signals) are modulated in a specific ADSL carrier bin [4]. The amplitude of each modulated signal is set according to the digital code to be transferred (Figure 100(a)). In order to represent N bits by a sine or a cosine signal, it needs to have 2^N-1 amplitude levels across its positive and negative peaks. Upon addition of these two signals, the resulting ADSL tone has the capacity to carry a total of 2^N bits of information [4]. Since the tone amplitude is discretized to represent the digital data, ADSL tones are usually called discrete multi-tones. The capability of carrying N bits in one QAM tone is commonly referred to as 2^N-QAM. Figure 100(b) shows an example of 16-QAM constellation plot which can be used to carry 4 data bits in a single ADSL tone. Depending on the dynamic range of each signal path, the capacity of QAM can range anywhere from 4 (2 bits) to 32768 (15 bits) for ADSL transmission. The dynamic range of the discrete multi-tone is directly proportional to the number of bits that can transmitted by an ADSL tone.

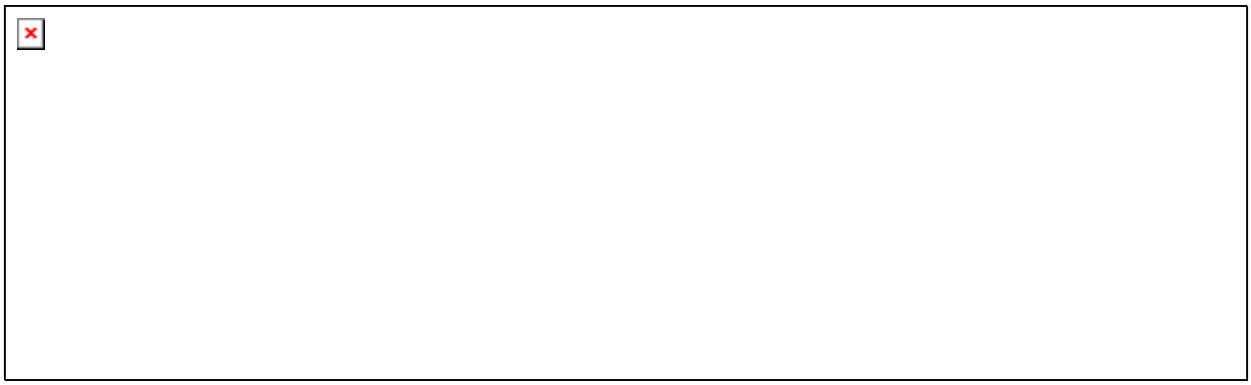


Figure 100. Quadrature amplitude modulation (QAM) (a) Amplitude coding for the two phases and (b) 16-QAM constellation plot.

6.2 MULTI-TONE POWER RATIO (MTPR) TEST

Since the tone amplitude is used to represent the binary data in DSL technology, the dynamic ranges of discrete multi-tones through all the transmission paths need to be large enough to guarantee the required minimum data throughput. Conventional specifications used to express dynamic range, such as SFDR, total harmonic distortion (THD), two-tone IMD have become less meaningful for testing densely modulated multi-carrier ADSL signals [84][88]. In ADSL technology, MTPR is the 'key test' for guaranteeing signal quality [84][86]. Figure 101 shows a typical ADSL communication setup. The DSP chipset generates the baseband digital data. This is followed by the ADSL CODEC, which is the converter interface with the front-end amplifiers. Since multiple channels are transmitted and received simultaneously, it becomes necessary to check for inter-modulation distortion introduced in these multi-carrier devices.

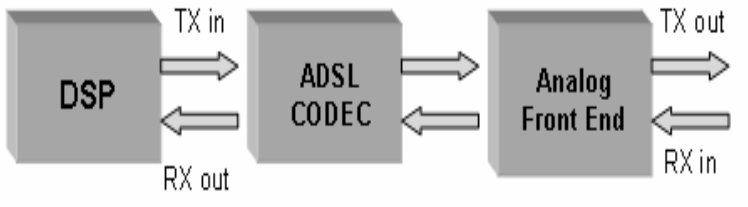


Figure 101. Block diagram of ADSL central office setup.

When performing the MTPR test, a set of discrete multi-tones with specific missing tones are input to the DUT [84][86][88][89]. The missing tones are specified by the ADSL standard. The amplitudes of all tones are determined by the power spectral density (PSD) specifications of the DSL technology. Due to nonlinearity of the DUT, distortion components raise the energy spectra in the missing frequency bins of the response spectrum. The MTPR specification value is determined as the ratio of the average power of existing tones to the maximum power in the missing tones. The ratio is often expressed in dB. The MTPR test is normally performed on the transmitted and received channels of the CODEC and analog front-end portions of the ADSL device. As shown in Table 30, the number of tones in the MTPR test of the DUT transmit channel of the DUT is significantly larger than the number of tones used to test the receive channel (due to the asymmetric data rates). Hence, it is much more demanding in terms of ATE instrumentation precision.

Depending on the phases of the discrete multi-tones, ADSL signals with the same power and amplitude might have different peak voltage (V_{pk}) values in the time domain [91]. Figure 102 and Figure 103 show the time domain waveforms of two upstream discrete multi-tone test stimuli with the same 16 dB peak-to-average ratio but different initial phases that result in different V_{pk} values at various time domain sampling instances. This is often the case in ADSL transmission as it involves streaming real-time random data. Hence, ADSL standard requires the MTPR test of these devices to be performed for different V_{pk} values. The parameter, peak-to-

average ratio (PAR) is used to differentiate the discrete multi-tone waveforms based on their V_{pk} values and can be defined as,

$$PAR = 20\ Log\left(V_{pk} \Big/ \sqrt{\frac{1}{T}\int_0^T f(t)^2\, dt} \right) (dB) \qquad \textbf{Equation 63}$$

where f(t) is the time domain discrete multi-tone waveform and T is the waveform period. The ADSL standard requires these MTPR tests to be performed for three different PAR values: 12 dB, 14 dB and 16 dB.

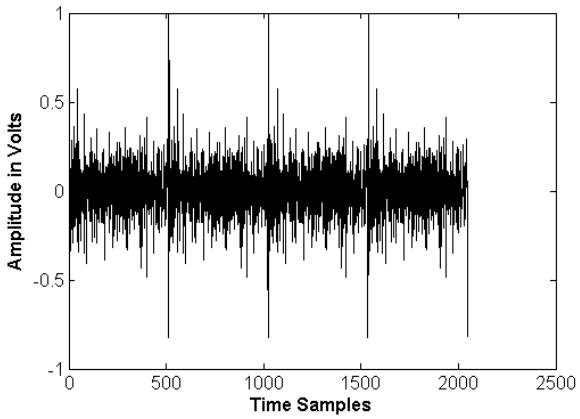


Figure 102. Upstream discrete multi-tone TX Annex A 16 dB PAR MTPR test stimulus.

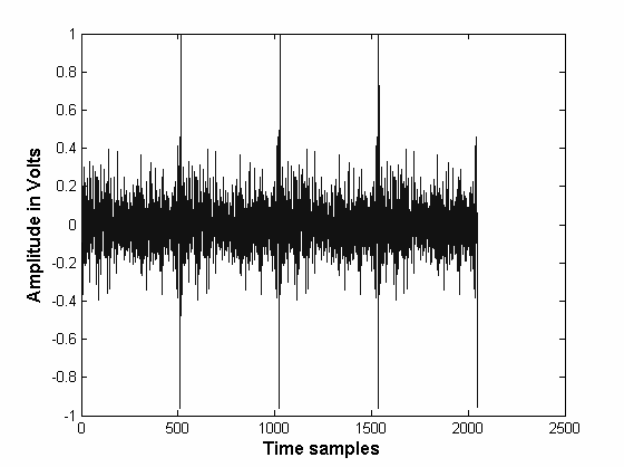


Figure 103. Another instance of the upstream discrete multi-tone TX Annex A 16 dB PAR MTPR test stimulus.

It is necessary for the test instrumentation employed in ADSL MTPR tests to have a high dynamic range in order to reduce the quantization distortion and hence accurately test the MTPR performance of these devices. The standard requires ADSL devices (up to 1.1 MHz) to have a minimum of - 65 dB MTPR performance for a 16 dB PAR discrete multi-tone signal, and ADSL+ devices (up to 2.2 MHz) to have a minimum of - 60 dB MTPR performances for the same. To robustly test these devices, the AC instrumentation needs to have a minimum bandwidth of 2.2 MHz as well as 70 db and 65 db MTPR for ADSL and ADSL+ devices respectively [84]. In general, the precision of the ATE instrumentation must be better than the ADSL DUT for accurate MTPR performance measurement.

6.3 STATE-OF-THE-ART MTPR PRODUCTION TEST APPROACH

In the past, accurate MTPR test of DSL devices required 12 bits of resolution, whereas currently these requirements have risen to 16 bits [84]. Also, the ATE needs to be electrically quiet and possess the ability to sample DUT signals with low-jitter. Advanced test platforms similar to Credence ASL 3000 [84] and certain configurations of Teradyne Catalyst have been developed in the past to support such highly sensitive measurements. Consequently, MTPR tests are usually performed on high-performance, high-cost ATE.

6.4 MTPR TEST IMPLEMENTATION CHALLENGES: PREMISE AND OBJECTIVES

Typically low-cost ATE use low-resolution devices that do not permit accurate measurement of the MTPR specification [92]. Figure 97 shows the FFT plot of 65K time domain samples of a signal with 16dB PAR value, captured at the transmitter output port of an ADSL device using a low-cost ATE. From the plot, it can be observed that MTPR of this signal is about -63 dB. These CODEC devices typically exhibit about -75 dB MTPR performance, when

measured using high-performance bench equipment. The problem addressed in this chapter is as follows: the nonlinearity of the digitizer in the low-cost ATE is limiting the MTPR measurement accuracy due to the fact that it induces spectral leakage into the frequency bins corresponding to the missing tones of the MTPR test. Hence, it is not possible to measure MTPR to the required level of accuracy using a low-cost ATE.

In this work, a novel test architecture that enables reliable and robust production test of MTPR production test of ADSL devices using low-cost ATE is presented. In this approach, "optimal" multi-tone noise signal is added to the DUT output signal to be digitized so as to randomize or smoothen the nonlinear static errors of the ADC in the ATE digitizer that limit the linearity measurement. The multi-tone noise is a new form of dither noise introduced in this work to reduce the distortion contributed by the digitizer to the missing bins of the MTPR test.

6.5 EFFECT OF DITHER SIGNAL ON THE LINEARITY PERFORMANCE OF DATA CONVERTERS

For periodic input signals such as, the MTPR test waveform, static quantization errors (INL and DNL) are coherent due to re-use of ADC codes during quantization of the periodic signal [92][93]. These coherent quantization errors add up to produce harmonic distortion components in the output spectrum of the quantized signal. Since this is a nonlinear device, these distortion components appear at integer multiples of the input frequency [92][93]. In digital audio applications, it has been demonstrated that addition of a noise signal (hereafter referred to as 'dither signal') with certain PDF along with the signal to be quantized (hereafter referred to as 'input signal') reduces or mitigates the harmonic distortion components in single carrier tone applications [94][95][96][97][98]. The reduction in harmonic distortion is due to the fact that the

signal to be quantized satisfies Widrow's requirement [99]. When this happens, the quantization errors have a typical white noise characteristic and the probability density of this white noise is no longer correlated to the input stimulus [99]. The modified PDF $\bar{f}_x$ of the signal to be quantized can be expressed as, $\bar{f}_x = f_x * f_d$, where f_x is the actual PDF and f_d is the PDF of dither noise.

In [100], impact of the use of dither signals with different noise PDFs (Uniform, Gaussian) for reduction of harmonic distortion components introduced by data converter nonlinearity is presented. From [100], it can be concluded that the performance of dither signal has less dependence on the specific noise statistics and relies more on the choice of optimum f_d to meet Widrow's requirements. In this chapter, multi-tone dither noise with a Gaussian PDF is proposed for reduction of harmonic distortion in MTPR tests. The dither noise modifies the transfer characteristic of the ADC in the digitizer of the ATE by modifying the PDF of the input signal [101]. The static errors in the transfer function are smoothened by the convolving effect of the PDF of dither noise [101]. The modified transfer characteristic and static errors can be expressed as:

$$\overline{Q}(x) = Q(x) * f_d(x)$$
$$\bar{q}_e(x) = q_e(x) * f_d(x) \qquad \textbf{Equation 64}$$

where Q(x) is the actual transfer characteristic and $q_e(x)$ are the actual static errors.

The effect of dither signal on the linearity improvement of data converters has been demonstrated on a 7-bit ADC (0-3V) with suitable DNL quantization errors in their codes. This study was performed in MATLAB simulation environment. The DNL errors were random variables whose PDF was a Gaussian function with zero mean and a standard deviation of 0.5

LSB. The standard deviation of DNL errors in most ADCs employed in low-cost ATE does not exceed this value. The DNL error at each ADC code is shown in Figure 104(a). The x-axis of the plot represents 128 (7 bit ADC) codes of the ADC in LSBs. The y-axis represents the quantization error is LSBs for the corresponding input amplitude in x-axis. In this case, the absolute value of the quantization error does exceed 1 LSB, as the standard deviation of the DNL error was chosen to be 0.5 LSB. Mathematically, S can be expressed as,

$$S(x) = \sum_{i=1}^{n} [u(x - a_i) - u(x - b_i)] \qquad \textbf{Equation 65}$$

where n is the number of code edges (128 in this case), u is the unit step function, and a_i, b_i are the codes for the actual and ideal ADC characteristics.

$$\begin{aligned} b_i &= i - 1 + offset \quad error \\ a_i &= b_i + DNL \quad (i) \end{aligned} \qquad \textbf{Equation 66}$$

If the PDF of dither noise f_d is even, then the modified quantization error at the output of the ADC can be expressed as,

$$\overline{S}(x) = S(x) * f_d(x) = \sum_{i=1}^{n} \int_{x-b_i}^{x-a_i} f_d(u)\, du \qquad \textbf{Equation 67}$$

For a Gaussian PDF this can be expressed as,

$$\overline{S}(x) = 0.5 * \sum_{i=1}^{n} \left[erf\left(\frac{x - b_i}{\sqrt{2\sigma^2}} \right) - erf\left(\frac{x - a_i}{\sqrt{2\sigma^2}} \right) \right] \qquad \textbf{Equation 68}$$

where $erf\ (x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt$ and σ is the standard deviation of the noise PDF.

Figure 104 shows plots of the quantization errors for increasing standard deviation values of the injected noise signal. Since the PDF of the dither signal is Gaussian, increasing the standard deviation in turn increases the power of the signal. This progressive improvement saturates at a certain power level above which the improvement is negligible for all practical purposes. In Figure 105, the increasing values of standard deviation are plotted vs. the residual value of maximum quantization error among all codes. From this plot, it can be observed that the improvement is negligible above a standard deviation value of 1.5. It must also be noted that larger standard deviations result in large values of peak-to-peak dither noise. Hence, exceeding a certain limit will cause an increase in the noise floor, affecting the ADC performance. In certain cases, where expected improvement cannot be achieved due to the constraints in maximum peak-to-peak dither noise amplitudes, it becomes necessary to use subtractive dither [93][102][105][106]. It is also necessary that the dither signal is chosen in a manner that the sum of the dither signal and input signal does not to exceed the dynamic range of the ADC.

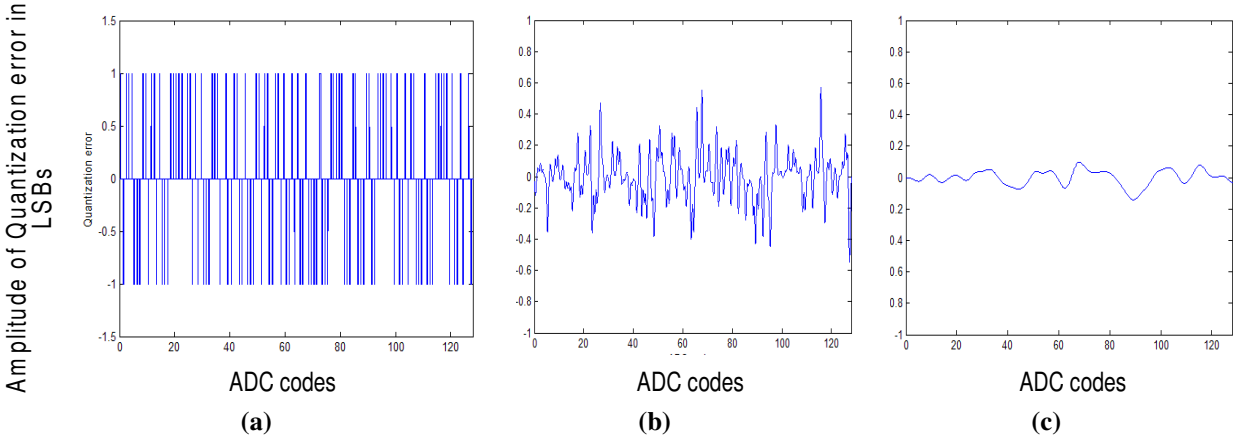


Figure 104. Quantization error convolved with (a) zero dither noise (b) dither noise with σ = 0.5 (c) dither noise of standard deviation σ = 2.

6.6 TYPES OF COMMONLY USED DITHER METHODOLOGIES

Two types of dither noise are commonly used. The first is the 'additive method' in which, dither noise is added to the signal to be digitized by the ADC such that, the spectrum of noise at the output does not overlap with that of the signal to be digitized. Hence, it is possible to place the dither noise band at DC or close to the Nyquist frequency. For most applications, several hundred kHz of bandwidth is available at these locations for the placement of dither noise. The effects of additive dither on quantization performance have been discussed in detail in [93] [100][102][103][104]. However, addition of wideband random noise can cause significant reduction of the SNR at the ADC output and may minimize harmonic distortion only for small-amplitude input signals.

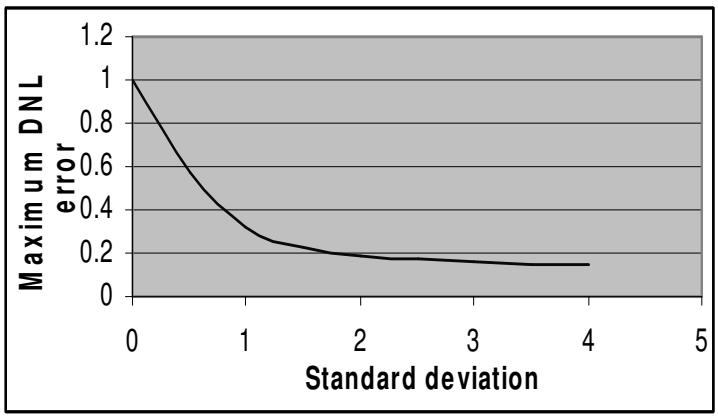


Figure 105. Maximum quantization error vs. Standard deviation.

The other dither technique is called the 'subtractive method' [93][102][105][106], in which a highly repeatable pseudorandom digital number generator is used to generate the dither signal. This dither signal is input to a DAC whose output is added to the signal to be digitized. On the output of the digitizer, the digital signal sent to the DAC is subtracted from the converter response. Figure 106 shows the methodology for subtractive dither. This method is often used for

large dither signals in order to compensate for the increase in noise floor during randomization of large nonlinear errors.

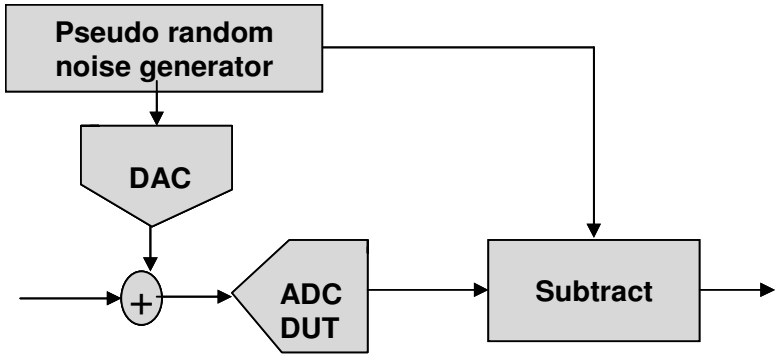


Figure 106. Subtractive dither methodology.

6.7 PROPOSED METHODOLOGY FOR LOW-COST HIGH-VOLUME MTPR TEST

The MTPR test is usually performed on the TX and RX outputs of each ADSL device. For a central office ADSL device the TX circuitry is used to source the downstream data signal to the subscriber and the RX circuitry is used to receive the upstream data signal from the subscriber. For an ADSL device operating in the subscriber's end, the TX circuitry is used to source the upstream data signal and the RX circuitry is used to receive the downstream data signal. As shown in Table 7 the downstream channel has far more frequency bins than the upstream channel for the ADSL Annex A, A+ and J modes. Hence, MTPR test performed on the downstream channel is much more demanding in terms of linearity and noise performance. The test stimulus for MTPR test on the downstream signal of an ADSL central office device contains 256 tones from 142 KHz to 1.1 MHz in steps of 4.3125 KHz. The amplitude of all these tones is set as specified by the standard, except for a few tones that are set intentionally to zero (missing bins) for the MTPR test. The phases of these tones are chosen such that the specified PAR for the

test is achieved. The time domain representation of one such MTPR test stimulus with 16 dB PAR is shown in Figure 102.

During test of the downstream channel, the MTPR stimulus is input to the ADSL DUT by the digital source of the ATE and the corresponding output of the DUT is captured by the ATE digitizer. Following this, the FFT is computed by baseband algorithms in the ATE mainframe and the corresponding MTPR is computed. As explained in Section 6.4, low-cost ATE cannot be used for accurate MTPR measurement due to the distortion components added in missing bins by the ATE digitizer. In order to improve their performance, a multi-tone dither signal with Gaussian PDF is added to the output signal form the DUT i.e. the input signal to be digitizer. This signal is added so as to randomize the static nonlinear errors in such a manner that they become uncorrelated to the input stimulus and improve the linearity performance of the digitizer.

6.7.1 Introduction to Multi-Tone Dither Noise

In the following, the use of multi-tone, out-of-band additive dither noise is proposed to improve the linearity of the ADC in the ATE digitizer. This dither noise N(t) can be mathematically expressed as:

$$N(t) = \sum_{n} A_n \sin\left(n\omega_n t + \phi_n\right) \qquad \textbf{Equation 69}$$

where A_n is the amplitude of the nth tone, ω_n is the angular frequency of the nth tone, and ϕ_n is the initial phase of the nth tone. The ϕ_n of each tone is a random variable whose PDF is a Gaussian function in order to meet the noise requirements of a dithering signal. It is essential to determine the optimum amplitude of the dither signal for linearity improvement, due to the tendency of large dither signals to increase the noise floor of MTPR measurements. In Section 6.5 it has been

shown that the performance of the dither signal is mainly dependant on the characteristics of its PDF. The PDF of multi-tone signals is mainly determined by the following parameters: n, A_n, ω_n, and ϕ_n.

The number of tones n, in the multi-tone signal is chosen based on the power requirements of the dither signal. An increase in n causes a corresponding increase in the power of the dither signal. The ω_n of the tones are selected based on the bandwidth availability. In MTPR test, the test stimulus occupies the bandwidth from 142 kHz to 1.1 MHz. Hence, the dither signals can be placed in the bandwidth from 100 Hz to 100 KHz to avoid spectral leakage into the MTPR test bandwidth. The frequency of each tone in the dither signal is chosen to be an integer multiple of a fundamental frequency to achieve coherent sampling. This sampling frequency for the dither signal is calculated from the formula:

$$\frac{f_{in}}{f_{sample}} = \frac{N_{window}}{N_{record}} \qquad \textbf{Equation 70}$$

where f_{in} is the fundamental frequency of the multi-tone signal, f_{sample} is the sampling/clock frequency employed during MTPR test of ADSL devices, N_{window} is an integer number of cycles within the sampling window, and N_{record} is the number of data points in the sampling window.

The proposed dither has a Gaussian PDF that is largely dependent on the amplitudes A_n of each individual tone that jointly determine the power (variance) of the dither signal due to its Gaussian nature and less dependence on the variance σ_{ϕ}^2 of the random function used to generate the ϕ_n for individual tones. This can be explained from the following expression of power (variance) of the multi-tone dither signal N(t):

$$Var\,(N(t)) = E(N^2(t)) \qquad \textbf{Equation 71}$$

$$N^2(t) = \sum_{n,m} A_n A_m \sin(n\omega t + \phi_n)\sin(m\omega t + \phi_m) \qquad \textbf{Equation 72}$$

Computing the left-hand side of Equation 72, the power (variance) of the dither signal can be expressed as:

$$\begin{aligned} \mathrm{Var}(N(t)) = &\left(\sum_n \frac{A_n{}^2}{2}\right)\left(1 - e^{-\sigma_\phi^2}\right) \\ &+ e^{-\sigma_\phi^2}\left(1 - e^{-\sigma_\phi^2}\right)\left[\sum_n A_n{}^2 \cos(2n\omega t + 2\phi_n)\right] \end{aligned}$$

Equation 73

where σ_φ^2 is the variance of the Gaussian PDF used to generate the random phase distribution. If the value of $e^{-\sigma^2}$ is small, then it is clear from Equation 73 that the power (variance) of dither signal has negligible dependence on the variance of the phase distribution. In this case, the power of the dither signal is essentially the sum of the squares of amplitudes of the individual tones. Also, using a variance value of less than 3 square radians reduces the noise characteristics of the multi-tone signal due to insufficient variance of their phase values.

From Equation 73, it can be concluded that the best dither signal can be generated by selecting optimum amplitudes of individual tones of the dither signal. It is important to note that the dither signal is independent of DUT performance and only improves ATE digitizer performance for MTPR tests. However, the dither signal needs to be generated in an ATE specific manner as different ATEs suffer from different nonlinearities.

6.8 DITHER SIGNAL GENERATION BASED ON EXTRACTED NONLINEARITIES

In this approach, nonlinear static errors of the ADC in the ATE digitizer i.e. the INL and DNL errors, are obtained by simple ramp tests and are used to determine the dither signal. A slow and accurate ramp signal generated by the AWG is input to the digitizer in the ATE loopback mode. As the AWGs employed in low-cost ATEs normally have better resolution performance that their source and digitizer counterparts, they can be used to generate accurate ramp signals. Based on the transfer function computed from the digitizer capture, the nonlinear errors are computed by the conventional histogram method [107][108]. These nonlinear errors are then used to calibrate a MATLAB based low-cost digitizer ADC model. The amplitudes of all the tones are linearly increased and the optimal level above which the MATLAB based simulation gives negligible incremental improvement of MTPR is determined. This amplitude level determines the dither signal used during MTPR testing on the low cost tester.

This algorithm though effective for certain test cases is not the most suitable approach for high-volume tests due to the following reasons:

- Significant effort is expended in developing MATLAB based ADC models incorporating measure nonlinearity metrics. It is difficult to incorporate tester-specific noise sources into this model. Hence, the generated MTPR tests may not be optimal across different test platforms and test conditions.
- This method can suffer from low MTPR test repeatability due to the fact that the actual phase noise injection statistics and that modeled in MATLAB may not be exactly the same.

In order to overcome these limitations and to provide a robust test solution for production deployment of MTPR tests on low-cost ATE an 'on-the-fly' alternate dither generation algorithm is proposed as follows.

6.9 'ON-THE-FLY' ALTERNATE DITHER GENERATION ALGORITHM

As opposed to the above presented approach, this algorithm computes the optimal dither noise on-the-fly in the high-volume test site during production test. The algorithm is included in the main production test routine of ADSL devices and is executed ahead of the high-volume tests. This algorithm helps to reduce the dither signal computation time and also improves the accuracy of computation of the dither signal. This algorithm determines the optimal amplitude and phases of the multi-tones for improved MTPR performance with a high degree of repeatability. Since the MTPR test stimulus occupies a bandwidth from 142 kHz to 1.1 MHz, the dither signals are placed in a bandwidth lower than 100 KHz. A hundred tones were used in the multi-tone signal as this was found to be a good number in some preliminary experiments conducted on low-cost ATE. Also, a reduced number of tones can be compensated by increasing the amplitudes of the existing tones as seen from Equation 73.

Table 31. On-the-fly alternate dither generation algorithm.

RAND_GAUSS (m, v, n): This function creates a Gaussian random variable vector with mean 'm', variance 'v' and size 'n'.
MTPR_test_routine: Sub-routine to compute MTPR specification of the DUT based on suitable ATE resources.
Multi_tone_gen (n, A, ω_n, ϕ_n): This function creates a multi-tone signal as given by Equation 73 with 'n' tones of equal amplitude 'A', frequency corresponding to n^{th} element of vector 'ω_n' and phase corresponding to n^{th} element of vector ϕ_n.

Main (MTPRB, A_o, A_{step}, ω_n)

1. m = 0
2. v = п
3. n = 100
4. $A_i = A_o$
5. **While** $MTPR_i < MTPR_B$
6. ϕ_n = RAND_GAUSS(m, v, n)
7. $dither\_noise_i$ = Multi_tone_gen (n, A_i, ω_n, ϕ_n)
8. Run MTPR_test_routine for golden die
9. **If** $MTPR_i < MTPR_{i-1}$
10. **While** j < 100
11. ϕ_n = RAND_GAUSS(m, v, n)
12. dither_noise_opt = Multi_tone_gen (n, A_{i-1}, ω_n, ϕ_n)
13. **While** k < 10
14. Run MTPR_test_routine for golden die
15. **End while**
16. Compute mean and variance of above obtained ten MTPR values
17. Store dither_noise_opt and corresponding MTPR value with the best repeatability and go to Step 22
18. **End while**
19. **End if**
20. $A_i = A_i + A_{step}$
21. **End while**

Proceed with Production_Test_Routine

Output: (Optimized multi-tone dither signal)

The 'on-the-fly' approach helps to optimize dither signals in an ATE specific manner. The generated dither signal enables MTPR measurements with an improved degree of repeatability and accuracy on the low-cost ATE. The computation of MTPR using the MTPR_test_routine is performed on the average of ten captured test responses to further improve repeatability. Compared to the overall test time required for each production lot, the additional

time required to run this algorithm is negligible. Also, the golden dies are easily available at production sites as these are used form time-to-time for calibration purposes.

The optimal dither signal obtained from the above mentioned algorithm is stored in the mainframe of the ATE for MTPR specification measurement purposes. During MTPR test in the production test routine, this dither noise is applied to the digitizer along with the ADSL device test response in a cheap and reliable manner using AWG resource already existent in the ATE and unused in the conventional approach of this test. As the generated multi-tone dither signal is a noise-like signal, it is not required that the dither signal be synchronized to the MTPR input stimulus. The dither signal could be a free-running signal and due to its out-of-signal bandwidth, multi-tone characteristics it can be reconstructed at the output of the ADSL device accurately without any signal leakage. Figure 107 shows the block diagram of the proposed test architecture. The dither signal is added along with the transmitted output of the ADSL DUT on the device interface board (DiB). Suitable adder circuitry is designed and placed on the loadboard to enable this test. This adder circuitry poses negligible overhead in the real estate requirements of the DiB.

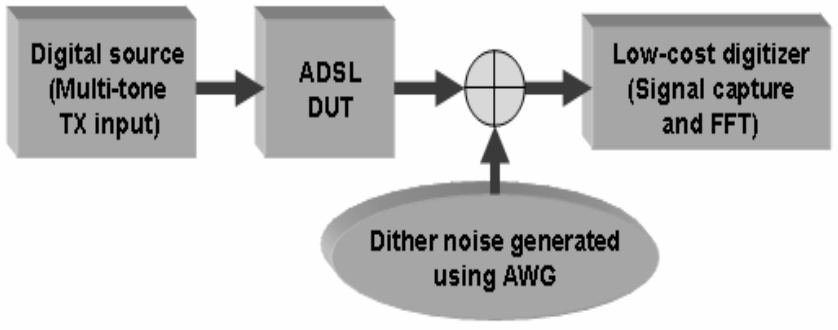


Figure 107. Block diagram of the proposed architecture for implementation of the dithering technique.

The proposed multi-tone form of dither signal has the following inherent advantages over previously proposed forms of dither signals in [93][94][100] for production test purposes:

- This signal can be easily sourced using the AWG of the ATE without any robustness issues.
- They have the characteristics of random noise but that they can be accurately repeated.
- These signals are coherent and out-of-signal bandwidth. Hence, these signals will not cause any spectral leakage in the ADSL signal bandwidth during reconstruction.
- Large amplitude dither signals can be produced to randomize large nonlinear errors.

These advantages specifically facilitate the use of such multi-tone signals for linearity improvement purposes.

6.10 VALIDATION BY SIMULATION OF MODELED LOW-COST ATE DIGITIZER

Initial validation of the proposed methodology was performed through the simulation of a developed low-cost digitizer model in MATLAB. The block diagram of the model is shown in Figure 108. The input signal is this case was the sum of the ADSL TX MTPR input stimulus and the dither noise (generated as explained in Section 6.9). This signal was applied to the digitizer block that was modeled by a 14-bit nonlinear ADC and an ideal 14-bit DAC. The DAC was implemented to covert the digitized output to their corresponding analog values, due to ease of FFT computation in the analog domain. The signal capture and FFT computation was performed using suitable baseband signal processing algorithms implemented in MATLAB. A sampling frequency of 2.208 MHz and 65K samples of data length were used for each test stimulus source and corresponding response capture. A 32K-point FFT computation was used for all spectral

measurements. The ADSL DUT was not included in this model since the goal of the experiment was to generate and evaluate the effect of dither noise on the ATE digitizer performance for high-volume MTPR tests.

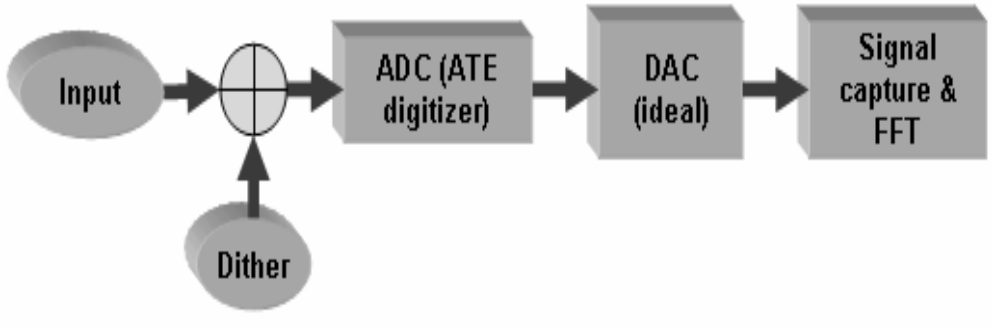


Figure 108. Simulation model used to validate the dithering technique.

6.11 NONLINEAR LOW-COST ATE DIGITIZER MODEL

The 14-bit ADC in the digitizer was modeled using a similar model as presented in Chapter 3 with suitable gain, offset, INL and DNL errors in their code edges. The plots of the static INL and DNL errors injected in the code edges of the ADC are shown in Figure 109. These static nonlinearities were incorporated in the model by altering the quantization code edges accordingly. Since the output of the ADC is a digital signal, this was converted to the corresponding analog signal through an ideal DAC also implemented in MATLAB.

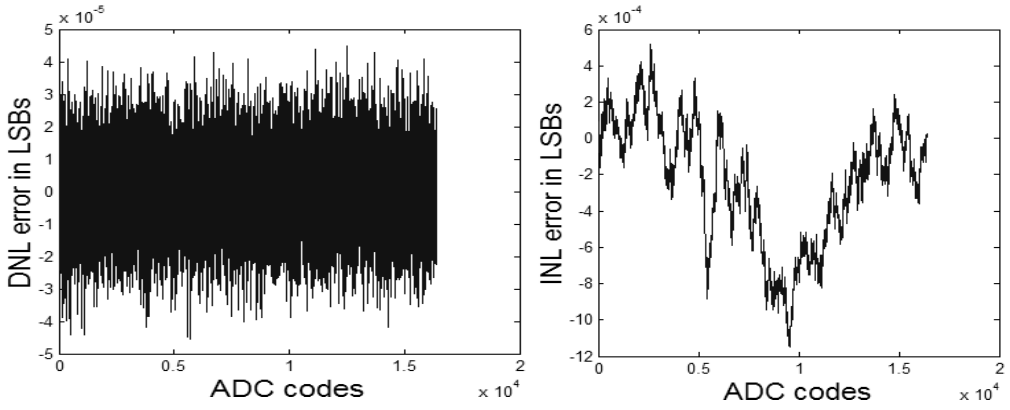


Figure 109. INL and DNL errors injected in the ADC digitizer model in LSBs.

The time domain response of the digitizer model to an Annex A 16 dB PAR MTPR test stimulus similar to the one shown in Figure 103 is shown in Figure 110. The corresponding 32K FFT plot of this waveform is shown in Figure 111. The distortion components added in the eight missing FFT bins of the MTPR due to the nonlinearity in the ATE digitizer are highlighted by circles. Their values are also listed in Table 32. In this experiment, the bin with maximum distortion was found to be the fifth bin that is specially highlighted in the plot. From Figure 111, it can be noted that the nonlinear static errors in the ADC cause harmonic distortions in the missing bins of the output spectrum. These distortion components dominate the MTPR measurement rather than the distortion caused by the DUT itself. The MTPR for this case was computed to be -49.8 dB.

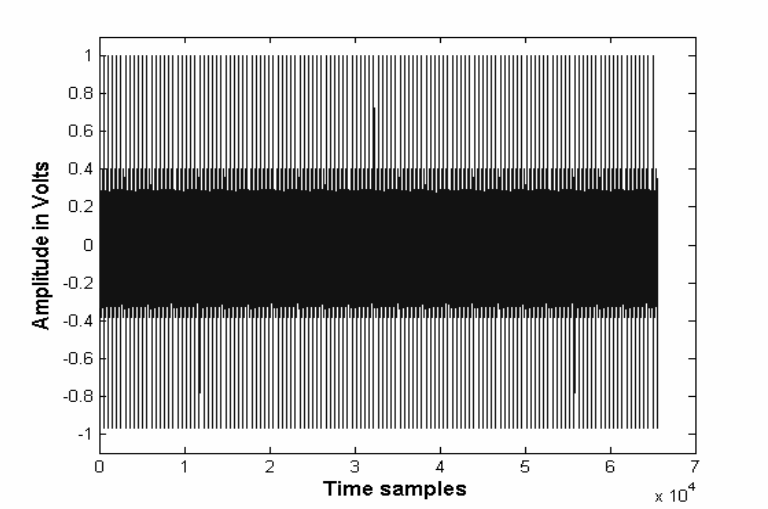


Figure 110. Time domain response of ATE digitizer model.

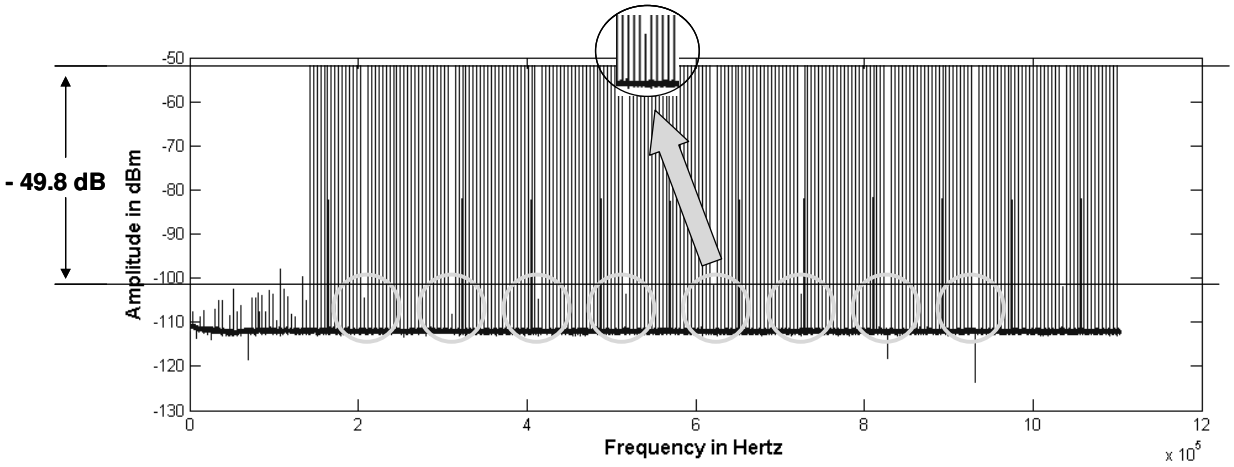


Figure 111. 32K FFT plot of the response of ATE digitizer model for a TX Annex A MTPR test stimulus.

In order to improve the linearity performance of the digitizer for multi-tone tests and thus enable accurate MTPR measurements, optimum dither noise (generated as explained in Section 6.9) was added to randomize the static errors in the ADC. The generated optimum dither signal is shown in Figure 112. The x-axis represents the time samples and the y-axis represents the amplitude of the dither signal in volts. The optimum dither signal generated for this case had a

variance (power) of 0.245 W. This dither signal was added to the MTPR test stimulus and the resultant signal was applied to the digitizer model. The corresponding FFT plot computed from the response at the output of the digitizer model is shown in Figure 113.

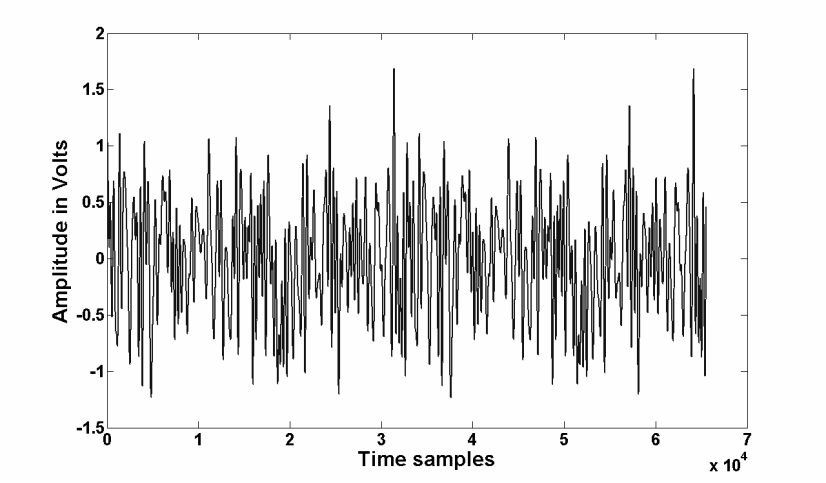


Figure 112. Time domain representation of multi-tone dither signal.

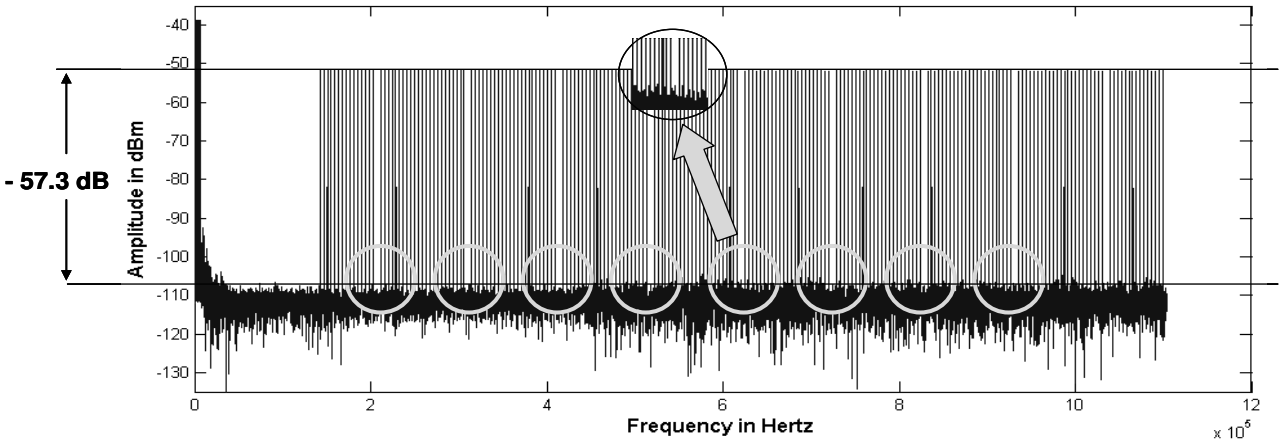


Figure 113. 32K FFT plot of the response of ATE digitizer model for the sum of the TX Annex A MTPR test stimulus and the dither noise as test stimulus.

It can be observed from Figure 113 that the distortion components in the missing bins of the MTPR test have been reduced to the noise floor of the digitizer. Also, Figure 113 highlights the MTPR computed from this FFT plot, which was -57.3 dB. Hence, an improvement of approximately 7.5 dB was achieved by the addition of the dither noise. Table 32 compares the maximum distortion components in the eight missing bins of the MTPR test performed with and without dither noise. From the table, it can be observed that the maximum distortion component that was observed in the fifth missing FFT bin without the addition of dither signal was improved by the addition of the dither noise to increase the possible range of MTPR measurements with the low-cost digitizer. Improvements can also be observed in other missing FFT bins from the same table.

Figure 114 shows the plot of MTPR values computed from the test responses obtained by sweeping the power (variance) of the dither signal. Since the power of the dither signal tends to the summation of the square of amplitudes of the individual tones as the variance of the Gaussian increases, the amplitude of individual tones was swept from 0.01 V to 0.1 V in steps of 0.01 V. This sweep was performed as a part of the on-the-fly alternate dither generation algorithm. It can be observed from the plot that maximum range of MTPR measurements were possible for a dither power of 0.245 W. Further increase in variance (above optimum) resulted in an increase in the noise floor, following the dither noise theory. Also, there is practically no use of increasing the standard deviation further, since all the distortion components have already been reduced to the noise floor.

Table 32. Summary of maximum distortion components in the missing bins of the MTPR test performed with and without dither noise.

Maximum distortion in missing bin	Without Dither	With Dither
1	-104.40	-112.18
2	-108.13	-114.77
3	-104.88	-108.16
4	-103.53	-107.12
5	-101.65	-108.11
6	-103.60	-108.64
7	-118.10	-107.86
8	-123.60	-108.48

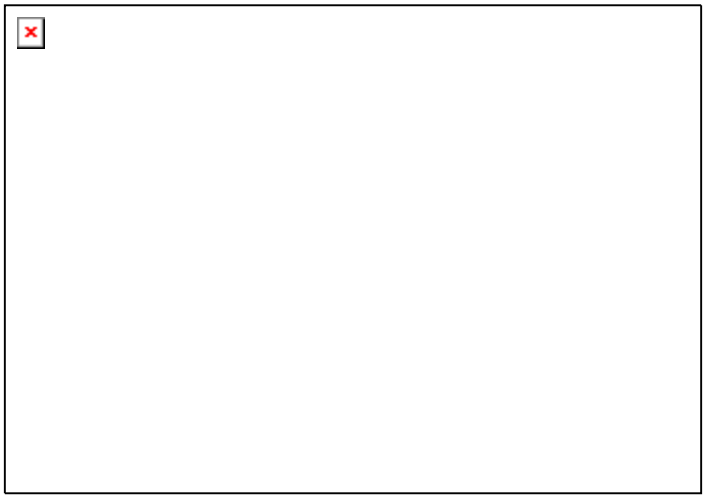


Figure 114. Plot of MTPR values observed while sweeping the power(variance) of the dither signal.

6.12 VALIDATION RESULTS OBTAINED FROM DEPLOYMENT OF PROPOSED TEST ARCHITECTURE ON LOW-COST ATE

The proposed test architecture was validated on a low-cost ATE platform to evaluate its production worthiness. The goal of the performed experiment was to enable MTPR test of ADSL devices on this low-cost platform in a specification compliant manner. Two case studies were conducted to validate the proposed architecture. In the first case study, a loopback approach of the ATE AWG source to the digitizer was used to evaluate the performance. In the second case study, the proposed test architecture was used to test a TI ADSL CODEC device on the low-cost platform.

6.12.1 Case Study I: Validation through Internal Loopback of ATE Resources

In this case study the proposed approach was validated for two different MTPR test stimuli cases, (1) TX Annex A upstream discrete multi-tone stimuli with 16 dB PAR and (2) RX annex A upstream Annex A with 10 dB PAR. These signals were stored in the mainframe of the ATE and sourced using the AWG. The signal was internally looped back to the digitizer in the ATE through a special mode. The response signal was captured using the digitizer in the ATE, upon which the FFT was computed and the MTPR specification was calculated. Since the goal of this case study was to evaluate the performance of dither on low-cost ATE and not to check specification compliance of MTPR, a reduced sample set (32 K samples) of the response signal was used to compute the FFT. Also the averaging function, which is normally employed in these tests, was not used in this case study. The evaluation results obtained with and without dither noise for each type of MTPR test stimulus employed are summarized below:

TX Annex A MTPR Test Stimulus with 16 dB PAR

As explained in Section 6.7, the MTPR test for ANNEX A test on the downstream channel of a central office device is the most demanding test in terms of linearity requirements. This test stimulus contains 256 tones from 142 KHz to 1.1 MHz in steps of 4.3125 KHz. The amplitude values of all these tones are set according to the requirements of the ADSL standard, except for a few tones that are set intentionally to zero (missing bins) for the MTPR test. The phases of these tones were chosen such that a 16 dB PAR was achieved. This signal was sourced using the AWG and captured by the digitizer using an internal loopback operation. 32K samples of this signal were captured by the digitizer and a 1024-point FFT was computed on this signal. At first, the experiment was conducted without the dither signal to evaluate the performance of the ATE. The observed FFT plot in this case is shown in Figure 115. In order to improve the linearity performance of the digitizer, suitable dither noise (generated as explained in Section 6.9) was added along with the MTPR signal and sourced using the AWG. The corresponding FFT plot for the response signal captured by the digitizer is shown in Figure 116. Comparing the performance of the ATE with and without the dither signal, it can be observed that an improvement of ~7 dB can be achieved using the proposed architecture. This improvement was due to the randomization of the nonlinear quantization errors in the ATE digitizer. The corresponding spurious tones caused by these nonlinear errors in the missing bins of the MTPR test were lowered to the noise floor. It can also be observed from Figure 116 that the MTPR measurements are now limited by the noise floor and not by the linearity of the digitizer.

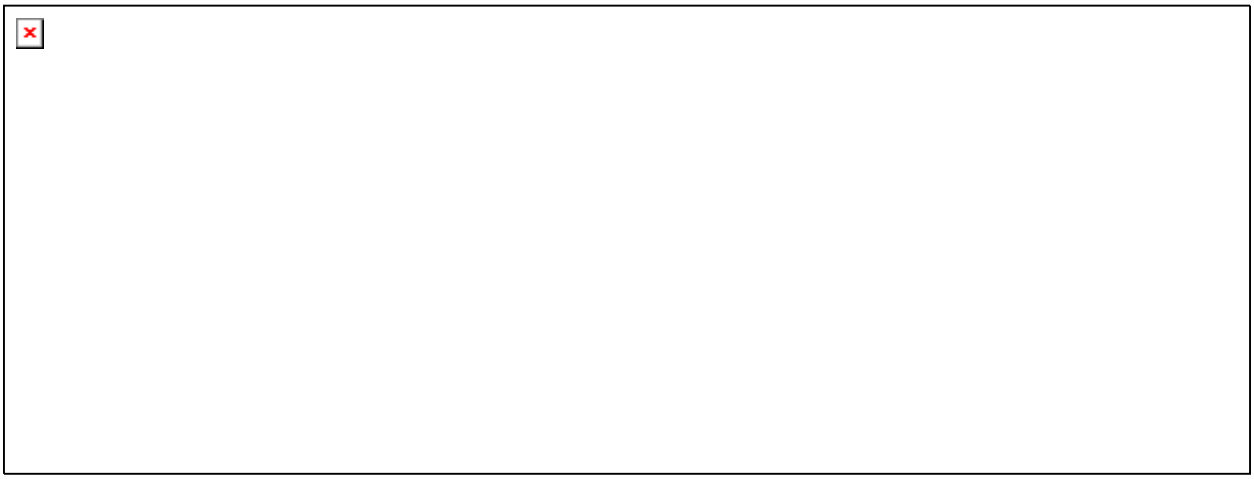


Figure 115 FFT plot of the low-cost ATE digitizer response to a TX Annex A MTPR test stimulus captured without dither noise.[1]

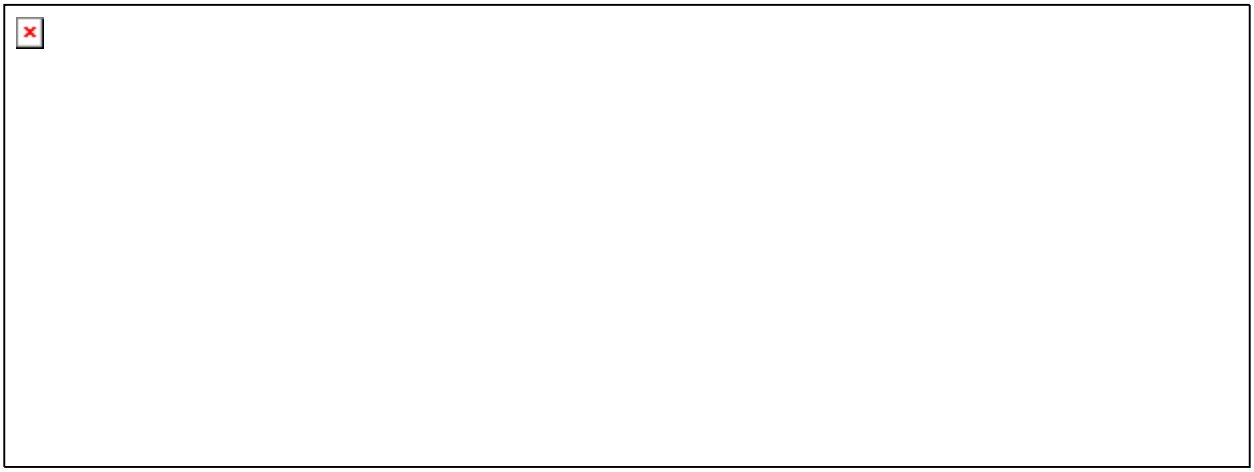


Figure 116 FFT plot of the low-cost ATE digitizer response to a TX Annex A MTPR test stimulus captured with dither noise.

RX Annex A MTPR test stimulus with 10 dB PAR

The loopback approach was also evaluated for the Annex A MTPR test stimulus applied to the upstream channel of a central office device. These signals typically exhibit a higher dynamic range compared to the downstream MTPR tests, as they have fewer carrier tones. These

[1] In all these FFT plots the X-axis represents the frequency in Hertz and the Y-axis represents the corresponding amplitude in dBm.

tests are less demanding in terms of linearity of the ATE, but nevertheless difficult to perform on low-cost ATE platforms. As in the case of the TX Annex A test, the performance of the ATE was evaluated by the loopback operation with and without the dither signal. Similar settings as in the previous experiment were used for the signal capture and FFT computation purposes.

The FFT plot of the test response captured using the digitizer without the dither signal is shown in Figure 117. The same dither noise from the previous experiment was used in this case also, since the dither noise was optimized for the nonlinearity in the ATE and not for the MTPR test signal. The FFT plot of the signal captured upon addition of this dither signal to the MTPR test signal is shown in Figure 118. In this experiment, it was found that the MTPR performance of the ATE for the RX Annex A standard could be improved form -62 dB MTPR to -74 dB using the proposed approach. As in the previous experiment, further improvements were limited by the noise floor and not by the linearity of the digitizer.

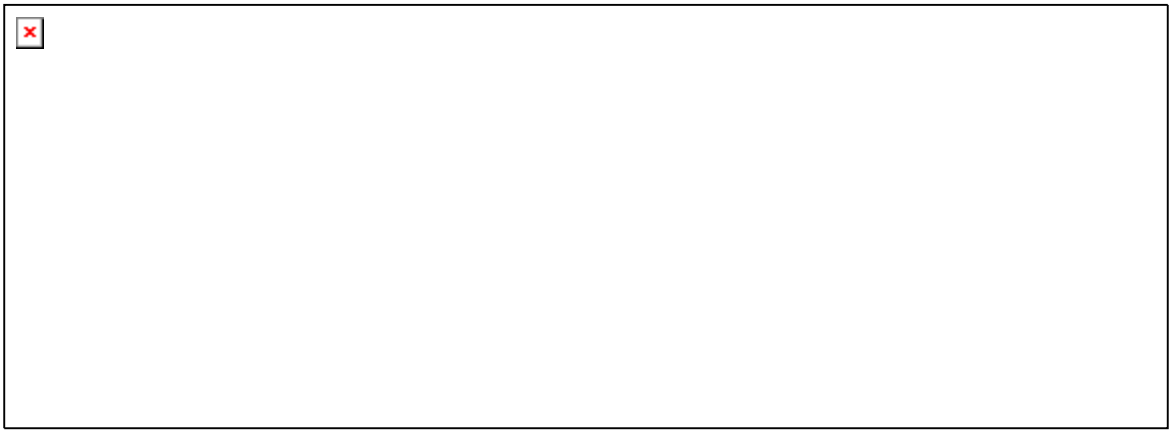


Figure 117 FFT plot of the low-cost ATE digitizer response to a RX Annex A MTPR test stimulus captured without dither noise.

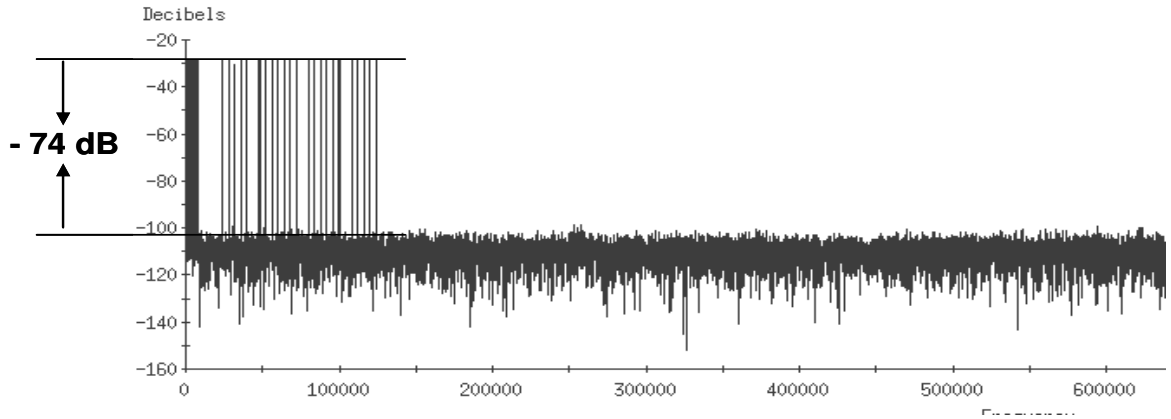


Figure 118. FFT plot of the low-cost ATE digitizer response to a RX Annex A MTPR test stimulus captured with dither noise.

6.12.2 Case Study II: Validation on ADSL central office CODEC Device

In this case study, the proposed test architecture was used to perform specification compliant MTPR test of ADSL central office CODEC devices on the same low-cost ATE platform employed in the previous case study. The DiB also known as the loadboard was re-designed to accommodate the summer circuitry as proposed in Section 6.7, along with the other standard DfT circuitry.

The configuration of the differential active summer circuitry added on the DiB to enable the proposed architecture is shown in Figure 119. In this experiment, TI's THS 4503 was used as the summer amplifier, since its harmonic distortion components was less than -100 dBc at 1.1 MHz (largest frequency component in the ADSL TX input spectrum) [109]. The harmonic performance plot of this device is shown in Figure 120.

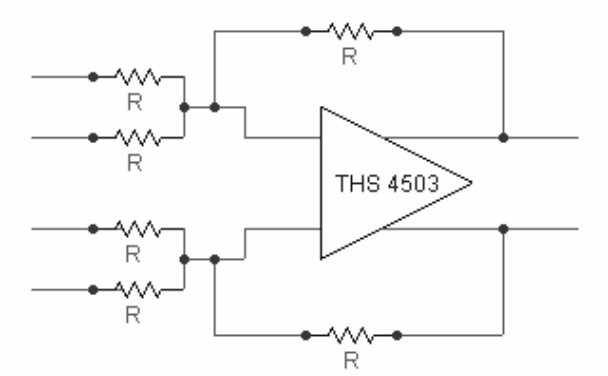


Figure 119. Schematic of differential summer circuitry.

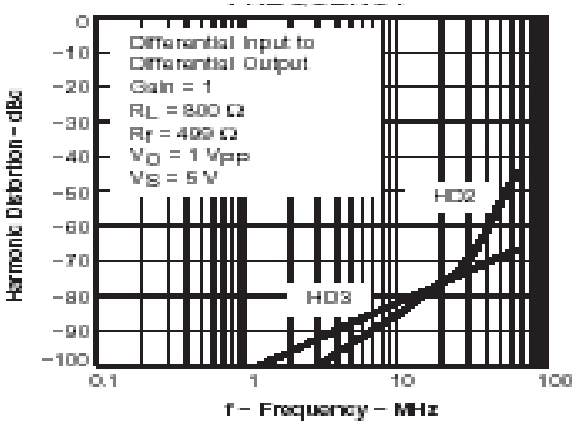


Figure 120. Harmonic performance of THS 4503 [109].

In this case study, a downstream Annex A MTPR input stimulus with 16 dB PAR was applied to the DUT. The digital source of the ATE was used to source this signal to the TX channel of the CODEC device as in the conventional approach. The ATE digitizer was used to capture the analog response of this device at a sampling frequency of 16 MHz. 65K samples of the time domain signal at the transmitter output port of the CODEC device was captured and the FFT was computed on the average of ten such captured signals. This FFT plot is presented in Figure 97. The MTPR computed from this FFT plot was limited to –63 dB due to the nonlinearities in the digitizer. These devices typically measure about -75 dB MTPR on bench.

Also, the ADSL standard requires these devices to pass the MTPR specification test of at least -65 dB to be employed for ADSL data transmission purposes.

To improve the performance of the digitizer and hence enable accurate MTPR tests, optimum dither signal (as explained in section 6.9) was generated. This dither waveform is displayed in Figure 121. 2048 samples of the dither signal were generated and sourced using the AWG of the ATE. This signal need not be synchronized to the MTPR waveform as this is a noise signal and its efficiency is optimized for the nonlinearities in the digitizer and is independent of the input waveform. This signal was added to the output of the DUT on the DiB and captured using the digitizer of the ATE. Figure 122 shows the corresponding FFT plot of the captured signal along with the dither signal. Comparing the FFT plots in Figure 97 and Figure 122, an improvement of 7dB in MTPR performance can be observed. Also from Figure 122, it can be observed that distortion components have been reduced to the noise floor and no further reduction is possible as we have already reached the noise floor of the device.

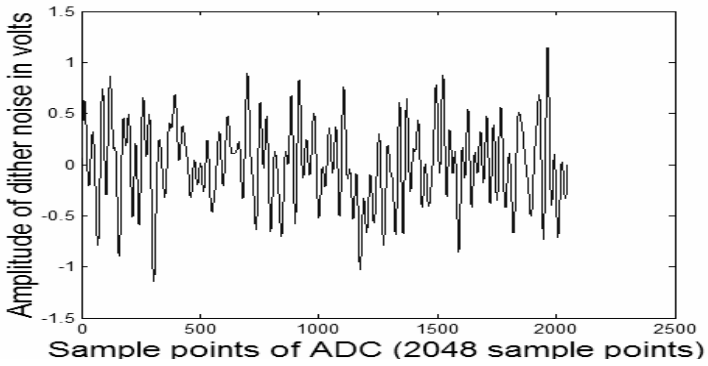


Figure 121. Dither signal for improving MTPR.

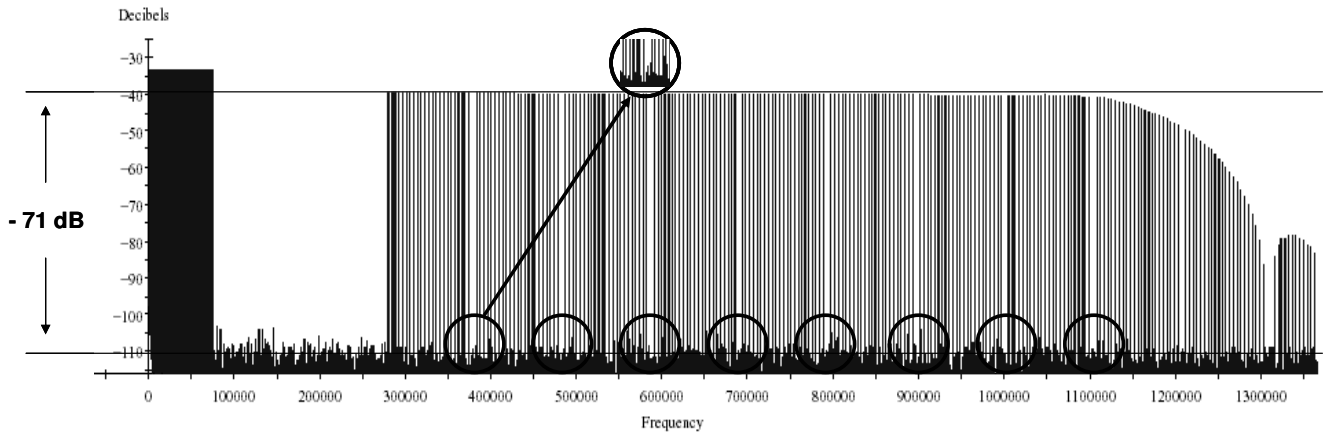


Figure 122. FFT plot of the low-cost ATE digitizer response to a RX Annex A MTPR test stimulus captured with dither noise.

6.12.3 Repeatability analysis of MTPR tests performed using proposed test architecture on the same die

Repeatability analysis of the proposed test architecture was performed on same device as part of the optimization algorithm to select the optimal dither signal and also to present the results in a statistical manner. Table 33 summarizes the repeatability results of MTPR measurements made on the device with and without the dither noise signal. From the table, an improvement of more than 7 dB can be observed in the mean value of measured MTPR, using the proposed test architecture. Figure 123 presents the histogram plot of these measurements. In Figure 123, the MTPR values on the left hand side refer to those measured with the optimal dither noise and the values on the right hand side refer to those measured without the dither noise.

Table 33.Summary of repeatability results.

	Mean	Standard deviation
Without dither	-63.796	0.541554
With dither	-70.9893	1.158994

The standard deviation (repeatability) of the MTPR value measured without the dither noise was ~ 0.5 dB, which was achieved through averaging of ten signal captures. The standard deviation value for the MTPR measurement with dither was ~1.1 dB. This variation is due the fact that we have reduced all the distortion components in the digitizer to the noise floor. Hence the variations are due to the random nature of the noise floor which adds additional vigor to the proposed architecture.

6.12.4 Repeatability analysis of MTPR tests performed using proposed test architecture over different dies

The proposed test architecture for MTPR test was repeated for another set of eight devices to evaluate its robustness across different devices that exhibit different MTPR values due to inherent process variations. The MTPR specification computed for these devices using high-end bench equipment was ~-75 dB. Table 34 presents the MPTR measurements made on these devices with and without the optimal dither noise. In all these MTPR measurements, the ATE digitizer was used to capture the DUT response at a sampling frequency of 16 MHz. 65K samples of the time domain signal at the transmitter output port of the CODEC device was captured and the FFT was computed on the average of ten such captured signals. From the table, it can be observed that an improvement of ~7 dB in MTPR performance can be achieved for each of these devices.

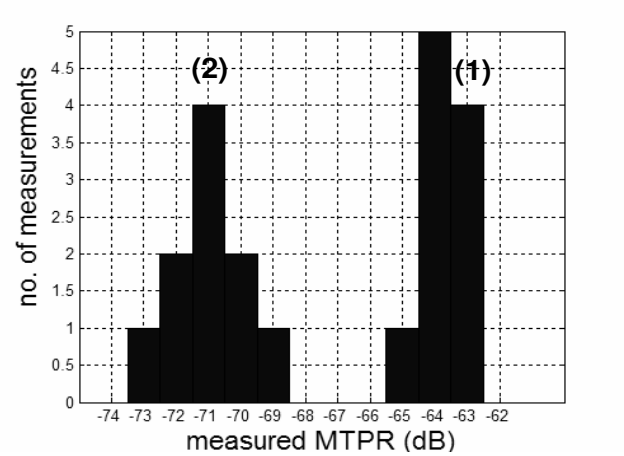


Figure 123. Repeatability results of MTPR measurements performed on same die (1) without and (2) with dither noise.

Under normal circumstances, i.e. without the addition of dither noise, all these devices would have failed the MTPR specification test in the high-volume production routine as the ADSL standard requires a minimum of -65 dB MTPR for the downstream Annex A waveform; Although these devices exhibit -75 dB MTPR performances when tested with high-end bench equipment. Hence, it can be concluded from these experiments that the addition of suitable multi-tone dither helps to perform more accurate MTPR tests on ADSL devices in a specification compliant manner over a high-volume of devices using low-cost ATE.

Table 34.Summary of repeatability results for MTPR tests performed over different dies.

Die ID	Without Dither	With Dither
1	-63.89	-70.34
2	-63.52	-70.26
3	-63.67	-71.90
4	-64.19	-70.96
5	-64.01	-70.62
6	-63.62	-69.65
7	-63.83	-70.38
8	-63.35	-71.80

6.12.5 Verification of proposed test architecture on 'Failed' IC

In order to verify that the proposed multi-tone dither noise only reduces the distortion added by the digitizer and not that of the device, the proposed approach was implemented on a device that had failed the MTPR specification during bench measurements. Table 35 summarizes the repeatability results obtained for this device with and without the addition of dither noise. The mean and standard deviation values with the dither noise show very good resemblance to the respective values without dither. Hence, it can be concluded that the dither only reduces the distortion added by the digitizer (i.e. only forward randomization).

Table 35. Summary of repeatability results for 'failed' device.

	Mean	Standard deviation
Without dither	-62.6823	0.549424
With dither	-62.2979	0.621273

6.13 IMPACT OF PROPOSED TEST ARCHITECTURE ON TEST COST/TIME

Due to shrinking IC geometries and ever-increasing performance requirements, the test cost of mixed-signal devices has become the fastest growing portion of the total IC manufacturing cost [110]. A simple expression commonly used to estimate Cost of Test (CoT) is presented in Chapter 1. As observed form Chapter 1, the CoT is highly sensitive to the cost of the ATE used to test the devices. Hence, if the total test time spent to test a particular lot of devices remains constant across ATE platforms then the CoT is directly proportional to the ATE capital cost. State-of-the-art mixed-signal ATEs typically used for MTPR tests are projected to cost one to two million dollars each based on their configuration [84][110]. This boils down to around three to five cents-per-second of test time [110]. The proposed architecture enables deployment of MTPR tests on standard low-cost digital testers that are projected to cost one to two hundred thousand dollars. This boils down to about one cent-per-second of test time. Hence, a possible 5X reduction in test cost of ADSL devices could be achieved using the proposed architecture, while maintaining the same throughput.

The only overhead required to implement the proposed test architecture is the real estate requirement of the summer amplifier on the DiB. The proposed circuitry occupies very little area and moreover this cost is negligible compared to the potential test cost savings of the proposed architecture. In future, the summer amplifier for the multi-tone dithering option could be integrated along with the ATE hardware to improve the range of possible linearity measurements using the low-cost ATE.

Chapter 7

ADVANCED TEST SIGNAL PROCESSING ALGORITHMS: ACCURATE CAPTURE OF THE SYSTEM RESPONSE USING LOW-PERFORMANCE ATE RESOURCES (CONT.)

As explained in Chapter 6, current generation RF/mixed-signal communication devices have very good linearity, superb noise performance and precise frequency characteristics. These constraints have made design and testing of these devices very challenging and expensive. Part of the testing dilemma arises from the fact that the low-cost automatic test equipments (ATE) use older generation devices, which lag behind the current devices in performance. Low-cost ATE usually limits the accuracy of measurement of these specifications due to the following reasons:

(a) The static nonlinearities (INL and DNL) in the ATE digitizer ADC causes distortion components in the output spectrum of the DUT which limit the SFDR and MTPR measurements

(b) The jitter in the sampling clock of the digitizer causes the noise floor of the ATE to dominate the noise floor of the device

In Chapter 6, it has been shown that the addition of out-of-band multi-tone dither noise along with the DUT output to be digitized reduces the distortion components of the low-cost ATE digitizer for accurate multi-tone power ratio (MTPR) tests. In this Chapter, the multi-tone dither technique is combined with a power spectral subtraction filter to enable accurate measurement of dynamic specifications viz. SNR, SINAD, ENOB along with the SFDR and the

THD specification of RF/mixed-signal devices. Since the ATE noise due to the jitter in the sampling clock is independent and additive to the device noise, the ATE noise power could be spectrally subtracted from the measured noisy signal to accurately determine the device noise power. In this work, power spectral subtraction is used to restore of the power spectrum of the device noise observed in additive ATE noise, through subtraction of an estimate of the average ATE noise spectrum from the measured noisy spectrum. Calibration techniques are employed to get an estimate of the ATE noise spectrum. The proposed approach is computationally simple and requires addition of little circuitry on the loadboard.

Power spectral subtraction is commonly used in speech enhancement in the past decades to suppress the additive background noise [111][112][113]. The greatest asset of spectral subtraction is its ease in implementation, as all it needs is an estimate of the mean additive noise power of the noisy signal spectrum. Due to the bursty nature of speech, it is possible to observe the noise by itself during frames when the signal is absent [112][113]. Also, it has to be noted that such techniques are less susceptible to the increase in the variance of the spectrum resulting from random fluctuations of the noise. These random fluctuations cannot be cancelled out and occasionally cause negative estimates of the power spectrum.

7.1 THEORY OF POWER SPECTRAL SUBTRACTION

The measurement noise in the low-cost ATE dominates the device noise during the SNR and SINAD measurements. Since the device noise and ATE noise are independent and uncorrelated, the total noise power is the sum of the individual noise powers. Hence, power spectral subtraction is used to restore the power spectrum of the device observed in noisy ATE environments. The assumptions in proposed approach are:

- N_{dev}, N_{ATE} are independent, wide-sense stationary random noise processes
- N_{dev}, N_{ATE} are both ergodic in variance and mean

The effect of additive noise on the power spectrum of a signal is to increase the mean and variance of the signal spectrum. The increase in the mean of the signal spectrum can be removed by subtraction of an estimate of the mean of the noise spectrum. In this work, the measured noisy signal in the time domain can be expressed as

$$y(t) = S(t) + N_{dev}(t) + N_{ATE}(t) \qquad \textbf{Equation 74}$$

where S(t) is the carrier signal, (N_{dev}) is the device noise, and (N_{ATE}) is the ATE noise. In the frequency domain, the noisy observed signal can be expressed as

$$y(f) = S(f) + N_{dev}(f) + N_{ATE}(f) \qquad \textbf{Equation 75}$$

where S(f), $N_{dev}(f)$, $N_{ATE}(f)$ are the Fourier transforms of S(t), $N_{dev}(t)$ and $N_{ATE}(t)$ respectively. The signal of interest to be measured is the sum of the carrier signal and device noise (N_{dev}). This can be represented as,

$$S_{dev(f)} = S(f) + N_{dev}(f) \qquad \textbf{Equation 76}$$

Substituting Equation 76 in Equation 75 yields,

$$y(f) = S_{dev}(f) + N_{ATE}(f) \qquad \textbf{Equation 77}$$

In power spectral subtraction, the mean of the ATE noise power is subtracted from the power of the instantaneous signal to restore the signal of interest. This can be expressed as,

$$\left|\hat{S}_{dev}(f)\right|^2 = \left|y(f)\right|^2 - \left|\hat{N}(f)\right|^2 \qquad \textbf{Equation 78}$$

where $\left|\hat{S}_{dev}(f)\right|^2$ is the spectral power of the estimated signal and $\left|\hat{N}(f)\right|^2 = \frac{1}{N}\sum_{N}\left|N(f)\right|^2$ is the ensemble mean of the ATE spectral noise power. Substituting Equation 77 in Equation 78 yields,

$$\left|\hat{S}_{dev}(f)\right|^2 = \left|S_{dev}(f)\right|^2 + \left[\left|N_{ATE}(f)\right|^2 - \left|\hat{N}_{ATE}(f)\right|^2\right] + \text{crossproduct} \qquad \textbf{Equation 79}$$

Under the assumption that the ATE noise and the device noise are uncorrelated ergodic processes, calculation of expected values on either side of Equation 79 yields,

$$E\left(\left|\hat{S}_{dev}(f)\right|^2\right) = E\left(\left|S_{dev}(f)\right|^2\right) \qquad \textbf{Equation 80}$$

Thus from Equation 80, it can be concluded that the estimate of the instantaneous power spectrum converges to the power spectrum of the noise free signal under the mentioned assumptions.

Complex statistical filters like Wiener and Kalman filters [114] could be used for the above purpose. The most commonly used least mean square error linear filter for noise removal is the Wiener filter. The transfer function of a Wiener statistical filter is of the form,

$$W(f) = \frac{E\left(\left|S(f)\right|^2\right) - E\left(\left|N(f)\right|^2\right)}{E\left(\left|S(f)\right|^2\right)} \qquad \textbf{Equation 81}$$

The corresponding transfer function of the spectral subtraction filter can be expressed as

$$\left|\hat{S}(f)\right|^2 = H(f)\left|S(f)\right|^2 \qquad \textbf{Equation 82}$$

where H(f) is the transfer function of the spectral subtraction filter. Since $\left|\hat{S}(f)\right|^2 = \left|S(f)\right|^2 - \left|\hat{N}(f)\right|^2$,

$$H(f) = 1 - \frac{\left|\hat{N}(f)\right|^2}{\left|S(f)\right|^2}$$ **Equation 83**

$$H(f) = \frac{\left|S(f)\right|^2 - \left|\hat{N}(f)\right|^2}{\left|S(f)\right|^2}$$ **Equation 84**

Comparing Equation 81 and Equation 84 it can be observed that the spectral subtraction filters converge to wiener filters for ergodic, uncorrelated noise processes. In this work, power spectral subtraction filters are used for the following reasons:

- They are easy to implement in the high-volume production environment,
- They are computationally less expensive
- They serve the purpose it terms of specification measurement accuracy.

7.2 PROPOSED APPROACH FOR ACCURATE DYNAMIC SPECIFICATION MEASUREMENT USING LOW-COST ATE

In order to improve the SFDR and lower the THD of the ATE digitizer, a multi-tone dither signal (generated as explained in Chapter 6) is added to the output of the DUT to be digitized by the ADC. This addition is done on the loadboard using suitable active adder circuitry. The dither noise can be cheaply generated using the arbitrary waveform generator (AWG) of the ATE. The computation of the dither signal requires the non-linear static errors i.e. the INL and DNL errors of the digitizer ADC. These can be obtained by applying a ramp signal using the AWG to the digitizer in the ATE loopback mode. The transfer function of the digitizer

can be used to compute these non-linearity errors. The optimum standard deviation value for the Gaussian PDF of the dither noise is chosen to randomize these quantization errors.

In order to apply the method of spectral subtraction, it is necessary to estimate the ensemble average of the ATE spectral noise power. Figure 124 shows the block diagram of the proposed approach. For the purpose of estimation, the DUT output to a sinusoidal input at the required test frequency is captured 'N' times (where N >=1000) using a digitizer whose performance is better than the device. The ensemble average of these measurements yields an estimate of the power spectrum of the device (N_{dev}). As the size of N increases, the accuracy of estimation also increases since the mean of the variance will tend to the actual variance of the noise signal (the signal power). The same number of data captures is repeated using the low-cost ATE, and the ensemble average of these measurements yields the estimate of the total measured noise (N_{dev}+ N_{ATE}). By the principle of spectral subtraction the difference in these two power spectrum measurements yields an estimate of the spectral noise of the ATE. From every subsequent measurement the estimated ATE noise power is subtracted from the noisy signal to estimate the signal of interest.

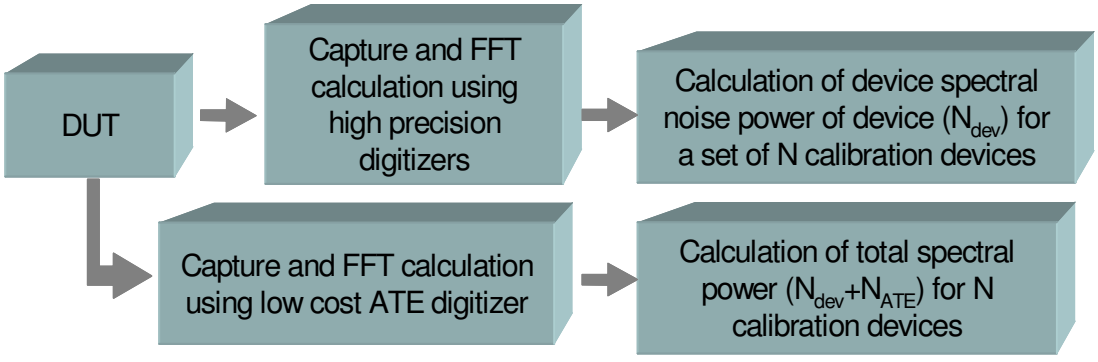


Figure 124. Block diagram of the calibration routine used for estimation of the ATE noise power.

The block diagram for production deployment of the proposed approach is presented in Figure 125. The tests stimulus is applied using the ATE source at the required test frequency. The output of the DUT to this test stimulus is added along with the 'optimum dither noise' sourced using the tester AWG. The sum of these signals is captured using the ATE digitizer. The dither noise helps to reduce the harmonic distortion components of the ATE for these tests. This is followed by a spectral subtraction filter, which estimates the power spectrum of the device noise from the observed noisy spectrum. The spectral powers are calculated from the respective FFT plots.

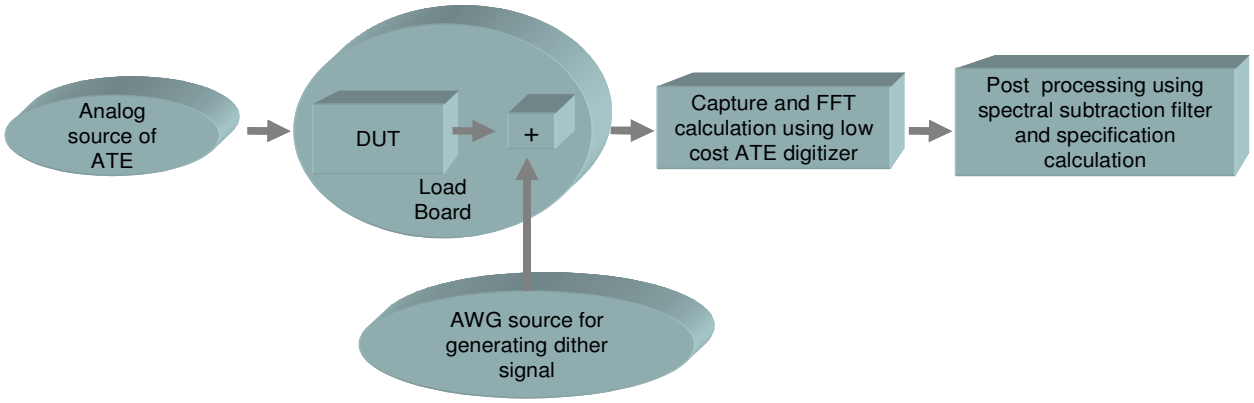


Figure 125. Block diagram of the production deployment methodology of the power spectral subtraction approach in combination with the dithering approach.

7.3 VALIDATION OF THE PROPOSED APPROACH

The proposed methodology was evaluated using simulation models built in the MATLAB environment. This section describes the model used for simulation and the validation results obtained using the proposed methodology.

7.3.1 ATE digitizer model

The ATE digitizer was modeled using an approach similar to the one presented in Chapter 3. The ATE digitizer is a 14-bit ADC with suitable INL and DNL errors in the code edges followed by a noise source which emulates the jitter noise in the sampling clock. The INL and DNL errors in LSBs of the 14-bit ADC are shown in Figure 126 and Figure 127 respectively.

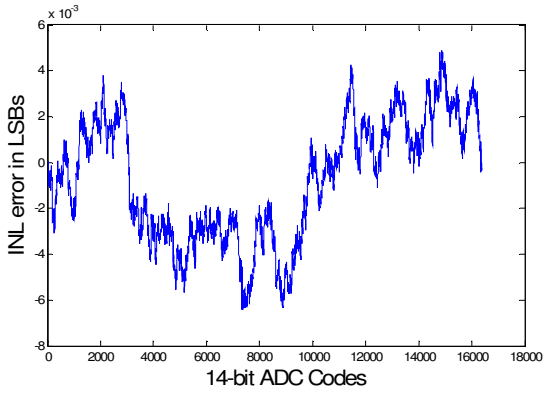


Figure 126. INL errors in the code edges of the ATE digitizer model in LSBs.

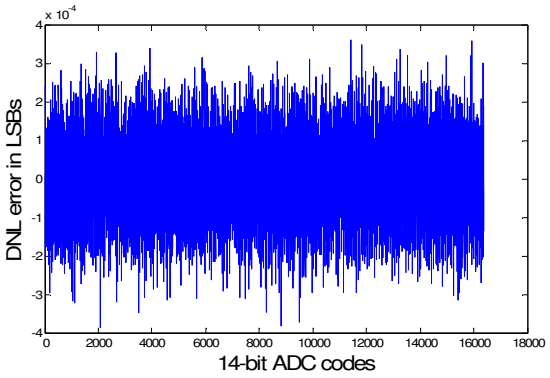


Figure 127. DNL errors in the code edges of the ATE digitizer model in LSBs.

7.3.2 Validation of the proposed approach

The DUT employed in this experiment was a 14-bit CODEC device with better performance than the 14-bit ADC in the ATE digitizer. A pure 1 MHz sine wave was input to the DUT using an analog source. The input stimulus has 4096 sample points and the sampling

frequency employed was 40.96 MHz. The output 2048-point FFT plot of the DUT for this stimulus is shown in Figure 128. This contains the carrier signal at 1 MHz and the corresponding first second and third non-linear harmonic components. The amplitude of the carrier signal and the harmonic components are highlighted in Figure 129.

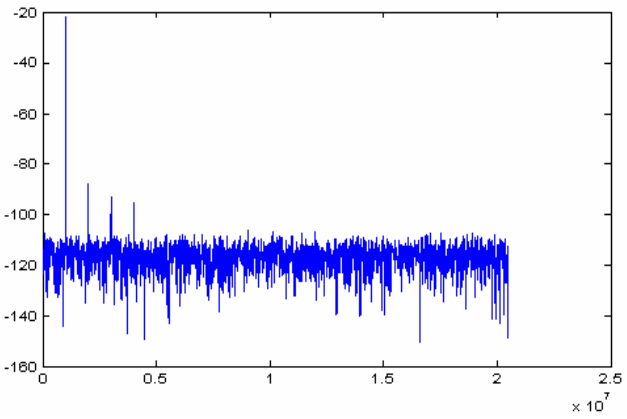


Figure 128. Output FFT plot of the DUT to the sinusoidal input stimulus.

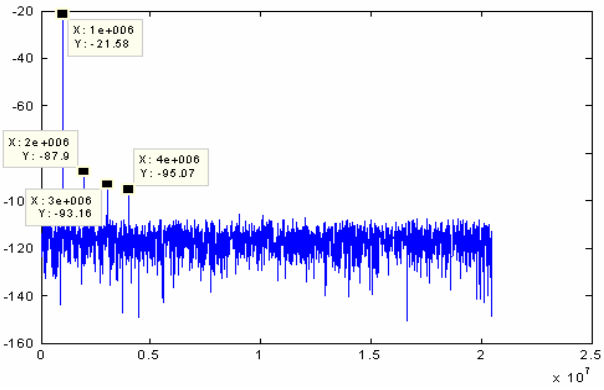


Figure 129. Output FFT plot of the DUT highlighting the amplitudes of carrier signal and the harmonic components.

Figure 130 shows the FFT plot of the output signal captured using the modeled low-cost ATE digitizer. This FFT plot presents the increase in noise floor and harmonic distortion components added by the low-cost digitizer. The 'optimum dither signal' used to reduce the distortion components, derived as described in Chapter 6 is shown in Figure 131. The derived

multi-tone dither noise was an out-of-signal band signal having a frequency span of 490 KHz from 10 KHz to 500 KHz.

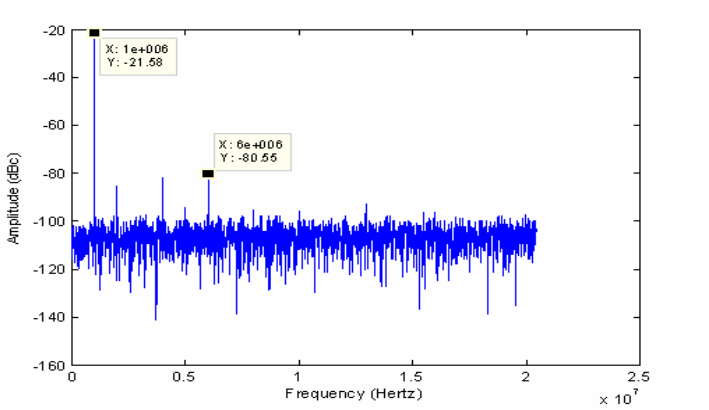


Figure 130. Output FFT plot of the DUT response captured using the low-cost ATE.

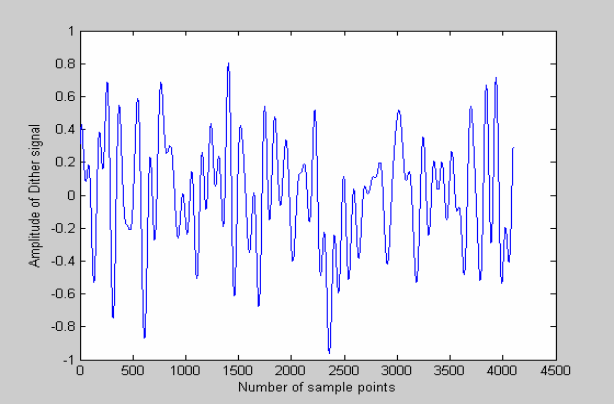


Figure 131. Time domain plot of the multi-tone dither signal derived to reduce the distortion components.

The derived multi-tone dither signal is added to the signal to be digitized and the resultant captured signal is shown in Figure 132. As observed from the figure, the non-harmonic components in the FFT spectrum due to the nonlinearities in the ATE digitizer have been lowered and the amplitudes of the harmonic components of the DUT have been restored. The amplitudes of the restored harmonic components are highlighted Figure 132.

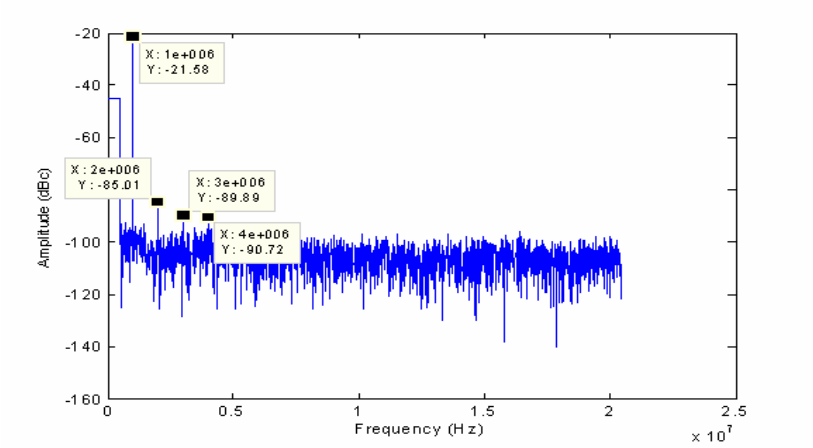


Figure 132. Output of DUT captured using low cost ATE with dither signal.

The proposed spectral subtraction filter combined with the dithering technique was validated for the SFDR and the SNR specifications in this work. The mean estimate of the ATE additive noise was measured as described earlier. A set of 1000 devices was used for the purpose of this calibration. The proposed approach was validated over a set of 200 validation devices. The FFT plots of these 200 devices for the pure sine wave test stimulus were captured using the low-cost digitizer model along with the dither signal. From the 2048-point FFT plots of each of the devices the SFDR and SNR specifications were calculated. The SDFR and SNR specifications were calculated as follows:

Signal-to-Noise Ratio (SNR): SNR characterizes the ratio of the fundamental signal to the noise spectrum. The noise spectrum includes all non-fundamental spectral components in the Nyquist frequency range (sampling frequency / 2) without the DC component, the fundamental and the first six harmonics.

Spurious Free Dynamic Range (SFDR): SDFR (sometimes also called only dynamic range) characterizes the ratio between the fundamental signal and the highest spurious in the spectrum.

Table 36 summarizes the mean and standard deviation values for the SFDR specification values measured using (a) an ideal digitizer (actual values), (b) the low-cost digitizer model without dither and (c) the low-cost digitizer model with dither. An improvement of ~5 dB can be observed in the mean values of the SDFR measurements with less than 1 dB standard deviation value. Figure 133 presents the histogram plot of the SFDR specification values measured using an ideal digitizer (right) and the SFDR values measured using the low-cost digitizer model without the addition of dither (left). Figure 134 presents the histogram plot of the SFDR specification values measured using the low-cost digitizer model with the multi-tone dither signal.

Table 36. Summary of results for the SFDR case study.

	Mean (dB)	Standard deviation (dB)
Actual device SFDR	65.9374	0.2609
ATE measured SDFR: without dither	59.2595	0.5690
ATE measured SDFR: with dither	64.2355	0.9774

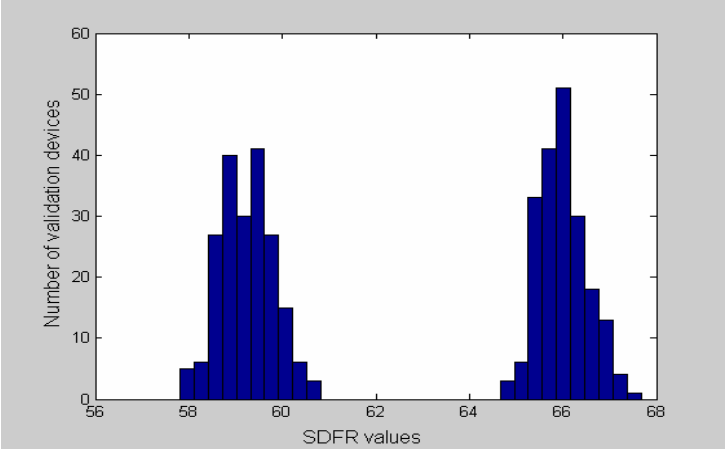


Figure 133. Histogram plot of the SFDR specification values results measured using (a) an ideal digitizer (right) and (b) the low-cost digitizer model (left).

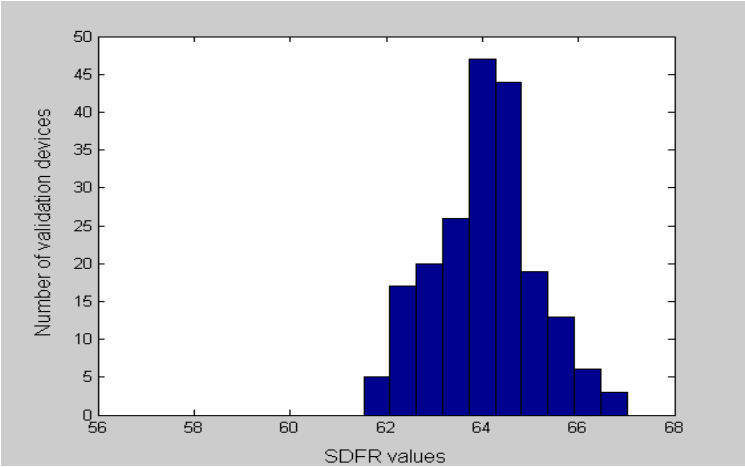


Figure 134. Histogram plot of the SFDR specification values measured using the low-cost digitizer model upon addition of the derived multi-tone dither signal.

Table 37 summarizes the mean and standard deviation values for the SNR specification values measured using (a) an ideal digitizer, (b) the low-cost digitizer without spectral subtraction and (c) the low-cost digitizer with spectral subtraction. An improvement of ~7 dB can be observed in the mean values of the SNR measurements with less than 3 dB standard deviation value. Figure 135 presents the histogram plot of the SNR values measured using an ideal digitizer (right) and the SNR values measured using the low-cost digitizer model without the spectral subtraction filter (left). Figure 136 presents the histogram plot of the SNR specification values measured using the low-cost digitizer model with the spectral subtraction filter.

Table 37. Summary of results for the SNR case study.

	Mean (dB)	Standard deviation (dB)
Actual device SNR	52.1214	0.0106
ATE measured SNR: without spectral subtraction	43.8788	0.8788
ATE measured SNR: with spectral subtraction	51.0288	2.8730

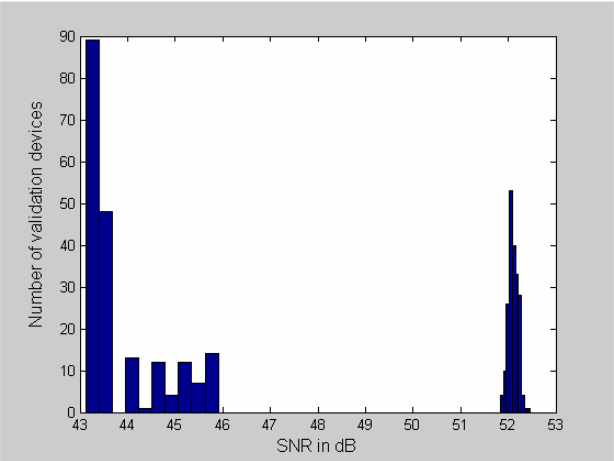


Figure 135 Histogram plot of the SNR specification values measured using (a) an ideal digitizer (right) and (b) the low-cost digitizer model (left).

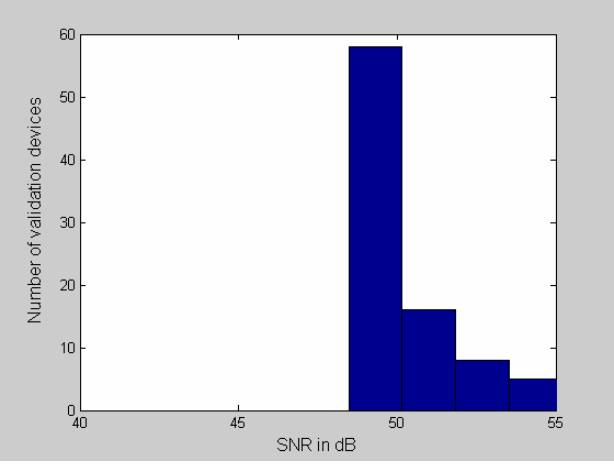


Figure 136. Histogram plot of the SNR specification values measured using the low-cost digitizer model with the spectral subtraction filter.

SCOPE OF THIS THESIS IN FUTURE DIRECTIONS

At the present time coordinated EDA tools for RF/mixed-signal pin test do not exist. An RF test engineer works with a variety of separate programs and physical test circuits to create a custom test solution for each RF production part. Significant effort is spent in optimizing and debugging the test program with no systematic tools available to optimally trade off test instrumentation accuracy with test complexity for a customer-generated specification list. Also, there is a significant gap that needs to be filled in terms of the fault modeling/simulation techniques in the IC production flow from the design stage to the test development stage. For complexity reasons, it is very difficult in the current circumstances, to co-optimize the tester resources, loadboard test resources, RF testing and test calibration procedures and the accuracy of the resulting test measurements while minimizing test costs and maximizing test coverage.

The main contribution of this thesis is a Genetic ATPG optimization engine to enable low-cost testability of RF devices. In addition, DfT approaches that co-exist with loadboard calibration (checker)/advanced test signal processing software tools for low-cost testability are presented. In the future, it is envisioned that a higher level of integration be performed to develop an 'RF virtual test laboratory'. This could include hierarchical simulation techniques (Cadence/HP-ADS/MATLAB) performed on well-characterized, scalable models of the SUT combined with scalable low-cost test approaches (sensors, loadboard DfT, loopback) to optimize the type of measurements employed by the alternate test framework to achieve the required test quality at the lowest possible cost. In addition, the use of loadboard vs. tester based resources can be considered to develop specialized test cards for multi-site parallel testing of RF systems on a range of "plug-and-play" ATE architectures available today. This kind of a test laboratory

presents a varied scope in terms of the research/need for accurate modeling techniques, fast simulation techniques, test stimuli optimization engines and low-cost ATE architectures.

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