# Design of High-Speed SiGe HBT Circuits for Wideband Transceivers

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# Design of High-Speed SiGe HBT Circuits for Wideband Transceivers

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*To my beloved family*

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# SUMMARY

The objective of this work was to design high-speed circuits using silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) and complementary SiGe (C-SiGe) HBTs, as well as silicon (Si) complementary metal oxide semiconductor (CMOS) devices, for next-generation ultra-wideband (UWB) transceivers. The demand for wideband circuits is driven by many newly introduced military and commercial applications, such as short-range high data rate communication systems, precision geolocation systems, intrusion detection radar, and software-defined radios. The advantages of using UWB systems over conventional narrowband transceivers include their lower power requirements, higher data rate, more efficient spectrum usage, precise positioning capability, lower complexity, and lower cost. The various components in a UWB system design include UWB communication channel and architecture design, UWB antenna design, and UWB transceiver integrated circuit (IC) implementation. The two major components in a UWB transceiver IC are the radio frequency (RF) circuit and the analog-to-digital converter (ADC). In this proposal, circuit-level solutions to improve the speed and performance of critical building blocks in both the RF front-end and the ADC are presented. Device-related issues affecting SiGe HBTs for potential applications in UWB systems intended for use in extreme environments will also be investigated.

Details of this dissertation can be found in the following refereed publications:

1. The design of 3-10 GHz UWB low noise amplifiers (LNAs) in both 120 GHz and 200 GHz SiGe HBT technologies (Chapter II, also published as [59]).

2. The design of an 8-bit 12 GSample/sec SiGe BiCMOS track-and-hold amplifier (THA) in 200 GHz SiGe HBT technology (Chapter III, also published as [72]).

3. The design of a 70 MHz - 4.1 GHz fifth-order elliptic $g_m$-$C$ low-pass filter in C-SiGe HBT technology (Chapter IV, also published as [79]).

4. An investigation of proton radiation effects in third-generation SiGe HBTs (Chapter V, also published as [84]).

# CHAPTER I

# INTRODUCTION

## *1.1 Applications of UWB Transceivers*

UWB communications systems are generally characterized in terms of their impulse response in the time domain, in contrast to the frequency domain analysis used in the characterization of their narrowband counterparts [1]. The concept of UWB was pioneered by Ross in 1963 [2]. Since then, UWB has inspired decades of innovations in theory and implementation, and numerous military and commercial applications have emerged that demonstrate the feasibly and viability of UWB technology.

Among all the applications of UWB technologies, the newly introduced commercial UWB communication technology is currently drawing the greatest attention as it exhibits the greatest potential for implementation in next generation wireless communication systems. In 2002, the Federal Communication Commission (FCC) approved UWB for use in commercial communication and imaging systems [3]. UWB systems are now permitted to operate in the 3.1–10.6 GHz range with a minimum signal bandwidth of 500 MHz and maximum power spectral density of -41.3 dBm/MHz [3]. Even though the UWB standard (IEEE 802.15.3a) for wireless personal area network (WPAN) communications has not yet been finalized [4], [5], it is envisioned that these systems will be capable of transmitting extremely high data rates (up to 500 Mb/s) at much lower digital power (less than 1 mW) [6] than the Wi-Fi technology (IEEE 802.11b) currently used for wireless local-area networks (WLAN), which typically delivers a 11 Mb/s data rate with a transmitted power of 200 mW. As a result, not only will UWB technology greatly improve the performance of wireless computer networks, but it will also revolutionize home multimedia by connecting virtually all home electronics such as the computer, camcoder, digital camera, and

high-definition TV with wireless UWB devices [6], [7]. In other words, UWB devices are expected to replace every data cable with a high-speed wireless connection [6].

**Table 1:** Key Specifications of Wireless Technologies (after[6]).

| Technology | Data Rate (Mb/s) | Output Power (mW) | Range (m) | Frequency |
|---|---|---|---|---|
| IrDA | 4 | 100 mW/sr | 1-2 | Infrared |
| Bluetooth | 1-2 | 100 | 100 | 2.4 GHz |
| IEEE 802.11a | 54 | 40-800 | 20 | 5 GHz |
| IEEE 802.11b | 11 | 200 | 100 | 2.4 GHz |
| IEEE 802.11g | 54 | 65 | 50 | 2.4 GHz |
| UWB | 100-500 | 1 | 10 | 3.1-10.6 GHz |

An interesting imaging applications of UWB technology is portable intrusion detection radar, or wall-penetrating radar. With this radar, military targets inside a building can be detected and precisely located through walls [8]. Even though some conventional radars, for example the L-band synthetic aperture radar (SAR), can "see through" the wall, several disadvantages, including its large size, heavy weight, high cost, low resolution, high power consumption, and high RF power (unsafe), make it impossible to deploy them widely as portable intrusion-detection radars [8]. However, with the development of UWB technology and the improvement in the performance of digital signal processing (DSP) circuits, low-power and high-resolution portable radars have become possible [8]. Several prototypes of the intrusion-detection radar have been developed in industrial research labs for defence and security applications based on this technology [9], [10].

Another application of UWB technology is in automobile collision-avoidance radar. In 2002, the FCC also approved a second 7 GHz UWB band, 22-29 GHz, for vehicular radar systems [3]. The wide bandwidth of the UWB vehicular radar makes it possible to precisely measure the movement of objects, and thus avoid collisions by triggering safety devices [11]. Even though 77/79 GHz frequencies are considered by the Conference of European Posts and Telegraphs (CEPT) to be a better band for automotive radars, the technology

required to develop a radar working at such high frequencies is still neither mature nor cost effective [11], [12]. consequently, 22-29 GHz radars (24 GHz narrowband radars and 24 GHz UWB radars) are expected to become the preferred solution for low-cost automobile radar in the the next few years [11].

Other applications of UWB technology include radio frequency identification (RFID), precision geolocation systems, surveillance systems, and military short-pulse communication systems [13].

**Table 2:** Military and Commercial Applications of UWB Technology (after [13]).

| Military/Government | Commercial |
|---|---|
| Tactical Handheld and Network LPI/D Radios | High-Speed LAN/WANs |
| Non-LOS LPI/D Groundwave Communications | Industrial RF Monitoring Systems |
| LPI/D Altimeter/Obstacle Avoidance Radar | Collision Avoidance Sensors |
| Tags (RFID) | Tags (RFID) |
| Intrusion Detection Radars | Intrusion Detection Radars |
| Precision Geolocation Systems | Precision Geolocation Systems |
| Unmanned Aerial Vehicles (UAV) | Altimeter/Obstacle Avoidance Radars |
| Unmanned Ground Vehicles (UGV) Datalinks | Medical Imaging Systems |
| LPI/D Wireless Intercom Systems | |

## *1.2 Motivations For Developing UWB Transceivers*

A typical a narrowband transceiver, in this case a super-heterodyne transceiver for 802.11b (Wi-Fi), is shown in Fig. 1 [14]. The super-heterodyne architecture, which was invented by E.H. Armstrong in 1918, is one of the oldest transceiver architectures, and is still the most widely used architecture in wireless communication systems. The benefits of super-heterodyne transceivers include their easy implementation and reliable operation. A quick glance at Fig. 1 shows that the system is fairly complicated, however, consisting of many RF components and involving several frequency up- and down-conversions. As a result, large power consumption, large chip area, and high cost are involved. In addition,

it takes a long time to design and debug a complicated system such as this, and once it is designed for a particular frequency and standard, the system cannot be reconfigured for operation at another frequency. Another important issue is that for some narrowband communication systems, such as super-heterodyne transceivers, off-chip high-Q channel-selection or image-rejection filters are required [15]. These filters, for example surface acoustic wave (SAW) filters, are kept off-chip in order to meet the high-Q and high linearity requirements. Off-chip components make the super-heterodyne architecture less favorable in terms of cost reduction and system-on-a-chip integration.

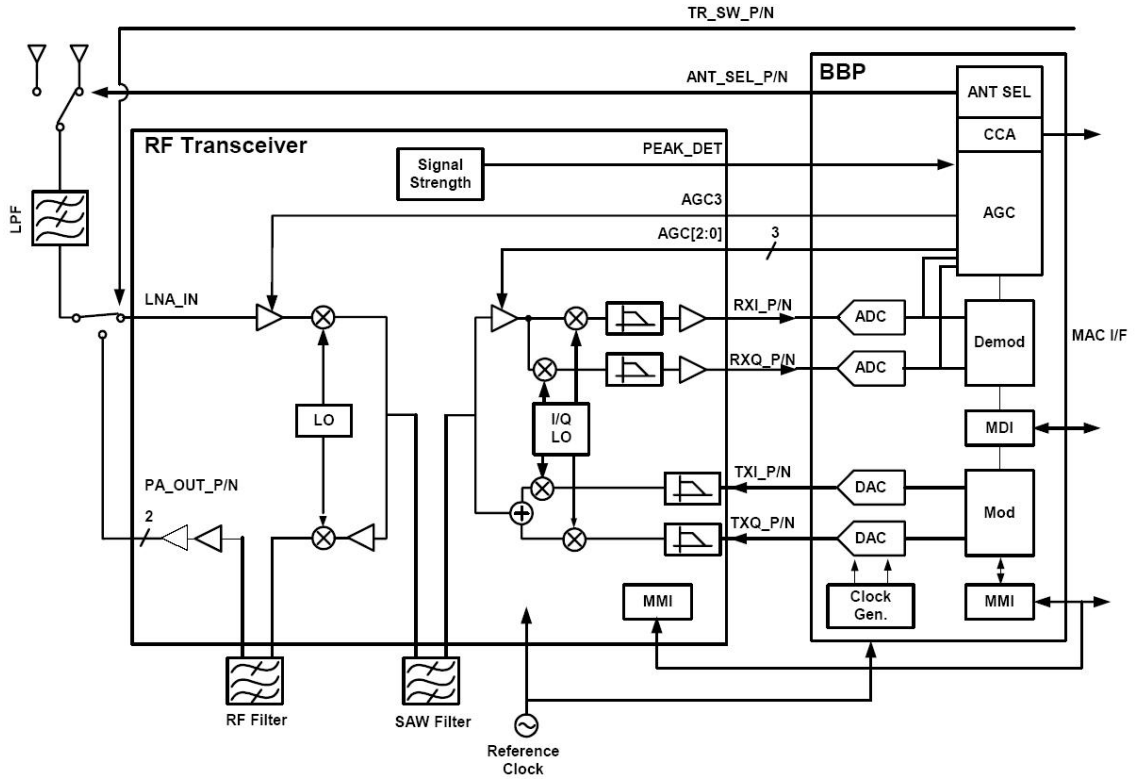


**Figure 1:** Block diagram of a super-heterodyne transceiver for IEEE 802.11b (after [14]).

According to Shannon's channel capacity theorem [16], channel capacity $C$ is given by

$$C = B \log_2(1 + \frac{S}{N}) \tag{1}$$

where $B$ is the bandwidth, $S$ is the total signal power, and $N$ is the total noise power. It is clear that the channel capacity (data rate) increases linearly with the bandwidth and

logarithmically (and hence weakly) with the signal-to-noise ratio (SNR). Thus, the large bandwidth of a UWB system not only helps achieve high data rates, but also allows operation at a significantly lower signal power than narrowband systems, with only a minor effect on channel capacity [17]. Figure 2 shows an ideal UWB transceiver architecture used in an impulse-radio transceiver [18]. Many components, including frequency synthesizers, down-conversion mixers, up-conversion mixers, image-rejection filters, and channel-selection filters, that are used in narrowband transceivers can be eliminated from a UWB transceiver [18]. Signal processing tasks such as modulation, demodulation, channel selection, and filtering that were previously performed by the RF and analog circuits in narrowband transceivers can now be executed in the digital domain by the baseband digital signal processing (DSP) circuits [18]. Many advantages can be achieved by using fewer RF circuits, including reduction in the hardware, power, cost, and number of design cycles, as well as high integration and more flexibility [18]. Also, the low RF signal power of the UWB system further reduces the transceiver's power consumption [1]. The ability of a UWB communication system using modulated short pulses to operate without a carrier signal allows a very efficient use of the signal spectrum [1], [6]. The PSD of UWB systems is so low (lower than -41.3 dBm/MHz) that it does not cause any interference with existing narrowband communication systems in the same frequency band. For instance, a 802.11.a (5 GHz) system would not be affected at all by UWB signals [19]. The large bandwidth of UWB technology can also be exploited by designing UWB radar systems to achieve higher resolution (as resolution is inversely proportional to the signal bandwidth) than that possible using narrowband radar operating in the same frequency band [11].

The direct implementation of the impulse-radio architecture shown in Fig. 2 for the entire 3.1–10.6 GHz band is very difficult, mainly because of the unavailability of ultra-high-speed ADCs. To relax the requirement on ADC operating speed, a less aggressive version of the UWB system, namely a direct conversion UWB system utilizing orthogonal frequency-division multiplexing (OFDM), has been proposed [20], [21]. The OFDM

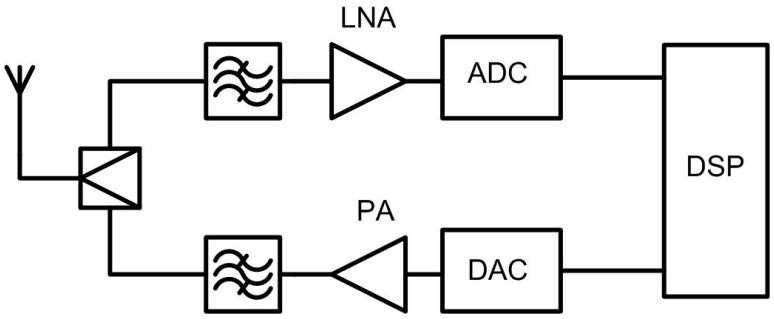


**Figure 2:** Block diagram of the impulse-radio transceiver (after [18]).

architecture evenly divides the entire UWB band into many sub-bands, each of which has a bandwidth of 528 MHz. An example of a direct conversion UWB transceivers is shown in Fig. 3 [21], which includes a frequency down-conversion stage for digitizing the low-frequency sub-band signals. However, in contrast to the original architecture shown in Fig. 2, this approach requires the addition of several mixers and frequency synthesizers, inevitably increasing the system complexity and power consumption.

## *1.3 Design Challenges of UWB transceivers*

From a signal and system perspective, UWB systems, especially the 3.1-10.6 GHz systems, are a relatively new technology, and standards for these systems have not yet been finalized, and the communication channels fully understood. Interference from the high-power signals generated by narrowband communication systems in the UWB band may cause UWB radio equipment to function improperly [19]. In addition, the design of efficient, wideband matched antennas for UWB systems is challenging, and a wideband antenna needs a constant group delay in order to operate reliably [19].

The two major components in UWB transceivers that pose significant challenges for the integrated circuit (IC) designers are the RF front-end block and analog-to-digital converter (ADC). In the RF front-end block, LNA is one of the more critical circuits, as it forms the first stage of the receiver. It has to not only provide wideband impedance matching to the antenna or external filters, but also achieve low noise, high and constant gain, and high

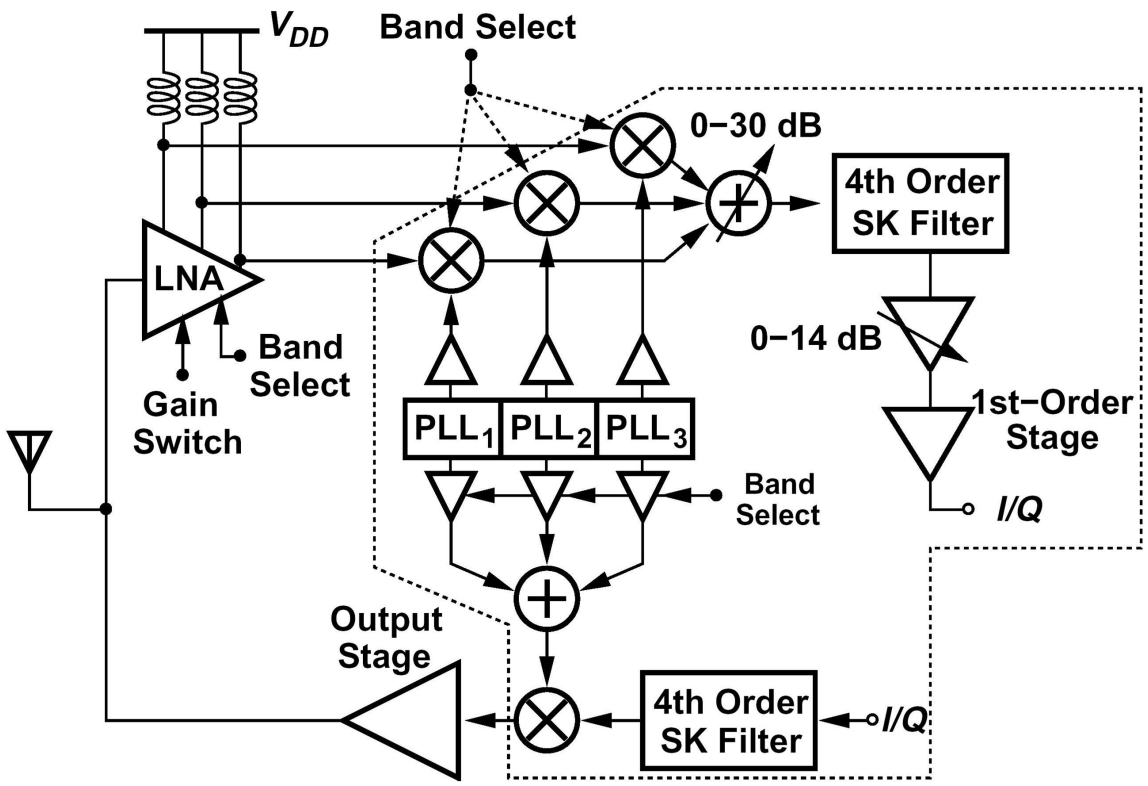


**Figure 3:** Block diagram of a direct conversion transceiver for OFDM UWB systems (after [21]).

linearity over the entire UWB frequency range [22]-[24]. Conventional narrowband LNAs are composed of a cascode amplifier with inductive degeneration and base inductance and are not adequate to simultaneously achieve all the requirements for a UWB receiver. Other LNA topologies, such as the distributed amplifier and common base amplifier, suffer from high noise figures. Feedback, on the other hand, is a powerful technique that can be used to improve both impedance matching and linearity. However, it also decreases the gain, increases the noise figure, and could lead to stability issues.

Achieving high linearity in UWB LNAs is of paramount importance. As discussed earlier, strong interference from existing narrowband communication systems, whose signal power density could be 1000 times higher than that of the UWB signals, may cause serious problems if the LNA linearity is too low given that only limited filtering can be achieved in a practical system [19]. The power consumption of UWB LNAs tends to be higher than

that of narrowband LNAs in the same band because of their more stringent requirements, such as higher gain, wider bandwidth, low noise, and higher linearity, and thus does not favor low-power operation [19].

In RF receivers, in order to relax the dynamic range requirement of the baseband ADCs, analog signals are generally amplified by variable gain amplifiers (VGAs) before being fed to the ADCs. However, because of the extremely large bandwidth of UWB signals, the design of the VGA becomes challenging at high frequencies [24]. In addition, OFDM systems need a 14-band (3.1–10.6 GHz) frequency synthesizer, which can switch rapidly between frequency bands, with less than 9.5 ns switching time available. The conventional closed loop approach using a single phase lock loop (PLL) is not able to meet these stringent settling time and tuning range requirements [24]-[26].

The overall performance of the UWB system (Fig. 2) depends heavily on the performance of the ADC, which needs sufficient sampling rate, bandwidth, and resolution. For instance, according to Nyquist-Shannon sampling theorem, to be able to directly sample the 3–10 GHz UWB signals, the sampling rate must be at least twice the highest signal frequency, or 20 Gsample/s, in order to avoid aliasing [27], and the bandwidth of the ADC must be greater than 10 GHz. Only a few high-speed ADCs can work well at full Nyquist speed, i.e., with a sampling rate two times that of the input frequency, but in practice, an ADC's sampling rate should be at least four times the highest signal frequency for reliable digitization. Therefore, to directly digitize the entire 3–10 GHz UWB band, a 40 Gsample/s ADC with at least 10 GHz bandwidth is required. Unfortunately, the difficulties associated with designing such a high-speed ADC, even for low resolution, are so formidable that a direct implementation of Fig. 2 for the entire 3-10 GHz band (not to mention for 22-29 GHz band) is widely considered impossible in CMOS and not power efficient in other technologies [31]. Some of the world's fastest ADCs reported in [28]-[30] operate at the limits of the technologies they are realized in and all have very high power consumptions of several watts. For the less aggressive version of UWB systems, namely the direct conversion

architecture, the sampling rate of the ADC must still be faster than 528 Msample/s in order to sample a 528 MHz sub-band, which remains a serious challenge for low-power UWB systems.

The receiver path in Fig. 2 is also often referred to as software-defined-radio (SDR), a concept for a far more powerful radio system that can theoretically receive and demodulate any signal falling within the receiver bandwidth, irrespective of whether it is a narrowband or wideband signal. SDR has even more stringent requirements for the ADC. Besides a high speed, the ADC now also needs a higher dynamic range or higher resolution than that needed in a standard UWB system in order to capture some weak narrowband RF signals in the presence of undesired strong in-band signals [31]. Thus, it is clear that the ADC plays an extremely important role in UWB system design. In fact, not only will the UWB system benefit from an improved ADC, but a faster ADC will also be useful in conventional narrowband systems, thus permitting the ADC to be pushed closer to the antenna, and reducing power and hardware requirements. Many high-end measurement instruments, for example ultra-wideband digital oscilloscopes, also require high-sampling rate, high-resolution ADCs.

## *1.4 SiGe HBT / BiCMOS Technology*

Bandgap-engineered SiGe HBTs are of increasing interest for wireless communication IC applications [32] because of their remarkable transistor-level performance combined with their ability to simultaneously maintain strict compatibility with conventional low-cost, high-integration, and high-volume Si CMOS manufacturing [33]. SiGe HBT technologies with 50 GHz (first-generation) [34] and 120 GHz (second-generation) [35] peak cutoff frequency are currently in commercial production worldwide from multiple sources, and are being deployed in both the commercial and defense sectors.

The recent announcement of a third-generation SiGe HBT technology with 200 GHz peak cutoff frequency [36]-[37], and a fourth-generation SiGe HBT technology with over

300 GHz peak cutoff frequency [38]-[39], along with the complementary (*npn* and *pnp*) SiGe HBTs with peak $f_T$ values above 180 GHz and 80 GHz, respectively [40], has pushed the upper bound on the speeds achievable in these devices considerably higher than previously believed possible, thus vastly increasing the application options for SiGe HBT technology to encompass a wide variety of analog and RF through millimeter-wave systems [41].

While it might be argued that a peak cutoff frequency in excess of 200 GHz is not needed to support most IC applications, which are currently clustered in the 1-40 GHz range, such extreme levels of performance create a much broader circuit design space, where, for instance, a designer has the option to trade frequency response for dramatic reductions in power consumption (10x reduction in bias current in the third-generation devices over second-generation technology for similar operating speeds), as indicated in Fig. 4. Third-generation SiGe HBTs are in fact quite competitive now with the best-of-breed commercial InP HBTs, and out-perform these devices when thermal effects are also considered [33].

**Table 3:** Key Specifications of SiGe BiCMOS Technologies Used in this Research.

| SiGe Technology | 7HP [35] | 8HP [36] | sg25c [37] | sg25h2 [40] |
|---|---|---|---|---|
| Company | IBM | IBM | IHP | IHP |
| HBT | npn | npn | npn | npn/pnp |
| $f_T$ (GHz) | 120 | 200 | 190 | 170/90 |
| $f_{max}$ (GHz) | 100 | 280 | 190 | 170/120 |
| $BV_{CEO}$ (V) | 1.8 | 1.7 | 1.7 | 1.9/3.1 |
| $W_{E,eff}$ ($\mu$m) | 0.18 | 0.13 | 0.25 | 0.25/0.25 |
| CMOS $L_g$ ($\mu$m) | 0.14 | 0.092 | 0.25 | 0.25 |
| CMOS Supply (V) | 1.8 | 1.3 | 2.5 | 2.5 |

## *1.5 Organization of Dissertation*

Chapter II (also published in [59]) presents the design and implementation of SiGe LNAs for use in UWB systems. The use of a shunt base-emitter capacitor and weak shunt

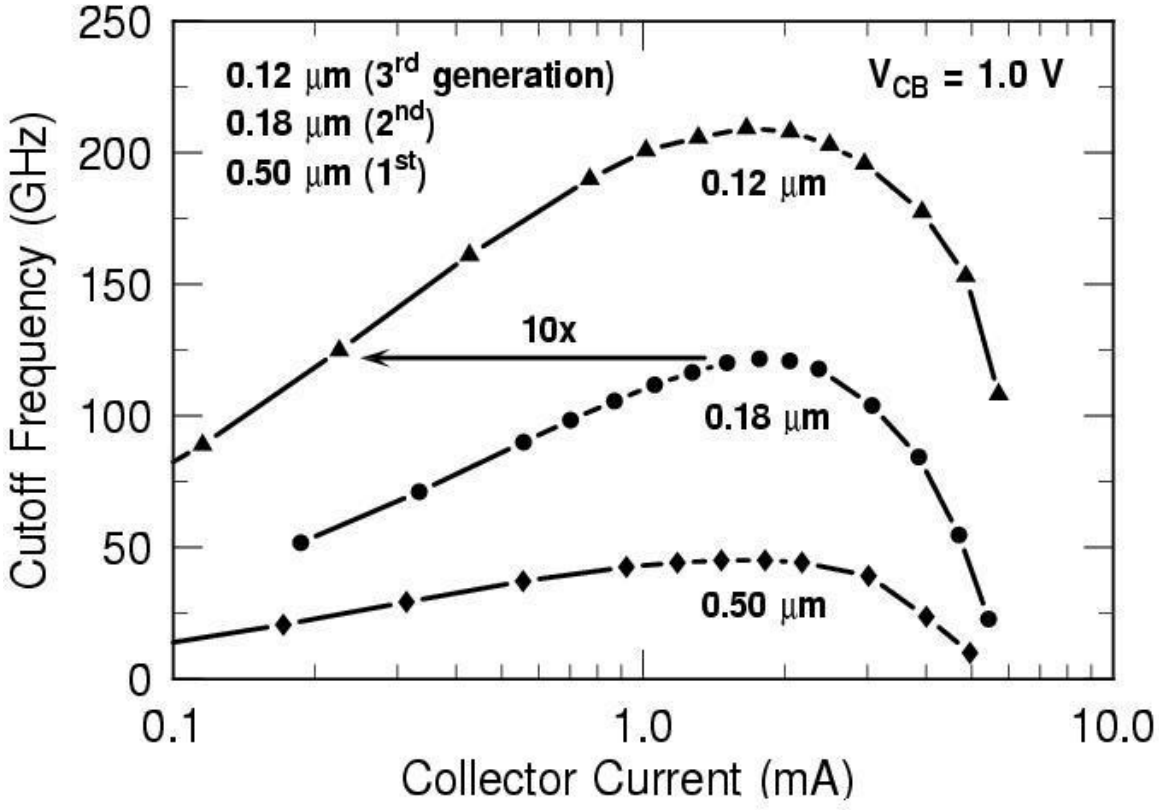


**Figure 4:** Measured $f_T$ as a function of bias current for three SiGe technology generations.

resistive feedback in a cascode amplifier with inductive degeneration significantly improves the input bandwidth of the LNA, and simultaneously allows a very low noise figure to be achieved. LNA 1 and 2 were fabricated using a commercially-available 0.18 $\mu$m 120 GHz SiGe HBT BiCMOS process technology. LNA 1 occupies an area of 0.80 × 0.90 mm$^2$, exhibits a noise figure (NF) of 1.8–3.1 dB, and attains a maximum gain of 20.3 dB across 3.0–10.0 GHz. LNA 2 occupies an area of 0.94 × 0.96 mm$^2$, exhibits an NF of 1.61–2.38 dB, and attains a maximum gain of 20.6 dB across 3.0–10.0 GHz. Both LNAs operate off a 3.3 V supply with a total power consumption of 26 mW. LNA 3 was fabricated in a 0.13 $\mu$m 200 GHz SiGe HBT BiCMOS process technology. It occupies an area of 0.86 × 0.95 mm$^2$, exhibits an NF of 1.17–1.75 dB (simulated), and attains a maximum gain of 23.3 dB across 3.0–10.0 GHz. LNA 3 operates off a 3.3 V supply with a total power consumption of 32 mW.

Chapter III (also published in [72]) presents the design and implementation of an ultra-high-speed SiGe BiCMOS track-and-hold amplifier (THA) for use in high-speed analog-to-digital converters. The use of a degeneration inductor in the input buffer was found to significantly improve the performance of the THA. The THA was fabricated using a commercially-available 0.25 $\mu$m 200 GHz SiGe HBT BiCMOS process technology. The circuit occupies an area of 1.0×1.2 mm$^2$, and exhibits -49.5 dBc of total harmonic distortion (THD) when operated at a sampling frequency of 12.5 GHz with an input frequency of 3.0 GHz. Operating from a 3.5 V supply, the total power consumption is 0.7 W.

Chapter IV (also published in [79]) presents the first demonstration of a continuous-time, fifth-order, elliptic, $g_m$-$C$ low-pass active filter in 0.25 $\mu$m complementary (*npn* + *pnp*) silicon-germanium (C-SiGe) HBT technology. This C-SiGe technology features *npn* SiGe HBTs with peak $f_T$ and $f_{max}$ of 170 GHz and 170 GHz, respectively, as well as *pnp* SiGe HBTs having $f_T$ and $f_{max}$ of 90 GHz and 120 GHz, respectively. This C-SiGe active filter was implemented with Voorman transconductors [73] to fully exploit the complementary high-speed *npn* and *pnp* SiGe HBTs. The circuit occupies an area of 0.90 × 0.91 mm$^2$, and exhibits a filter cut-off frequency of 4.1 GHz. This C-SiGe $g_m$-$C$ filter achieves a record continuous tuning range between 70 MHz and 4.1 GHz, attains an output noise power spectrum density (PSD) of -143 dBm/Hz, and operates off a 3.5 V supply, with a total power consumption of 100 mW at the maximum bandwidth of 4.1 GHz.

Chapter V (also published in [84]) presents results for the impact of proton irradiation on the *dc* and *ac* characteristics of third-generation, 0.12 $\mu$m 185 GHz SiGe HBTs. Comparisons with prior technology generations are used to assess how the structural changes needed to enhance performance between second- and third-generation technology affect the observed proton response. The results demonstrate that SiGe HBT technologies can successfully maintain their Mrad-level total dose hardness without intentional hardening, even when vertically-scaled in order to achieve unprecedented levels of transistor performance.

Chapter VI concludes the dissertation with a discussion of possible future research

directions.

# CHAPTER II

# UWB LOW NOISE AMPLIFIER

## *2.1 Introduction*

The low-noise amplifier (LNA) is a critical building block in UWB radios and is one of the most difficult components to realize because it must simultaneously achieve both broad impedance matching and low noise performance.

Distributed amplifiers can achieve the widest bandwidth, but their noise figures (NF) are typically very high [42]-[44]. The same problem exists in common-base input LNAs [45] and conventional shunt resistive feedback LNAs [46], [47]. Cascode LNAs with inductive degeneration, on the other hand, achieve the lowest noise figure compared to other architectures. However, they can only be matched to 50 Ω over a narrowband [50]-[52]. In previous research, an on-chip LC-ladder filter has been employed at the input of the LNA to broaden the bandwidth [22], [23]. However, this technique has several disadvantages, including enlarged chip size, increased circuit complexity, and enhanced noise figure, mainly due to the extra noise contributed by the lossy inductors present in the LC-filter network. Another way to broaden the bandwidth of a reactively matched LNA is to use weak resistive feedback between the input and the output [53]. In this case, however, matching the input to 50 Ω over the entire 3-10 GHz bandwidth is still a serious challenge.

The UWB LNA designs reported in the present work are implemented in IBM's second-generation (7HP) and third-generation (8HP) SiGe HBT BiCMOS technologies. 7HP is a commercially available SiGe technology platform featuring 180 nm lithography, 120/100 GHz ($f_T$ / $f_{max}$), and 1.8 V $BV_{CEO}$, and is integrated with aggressively scaled 0.11 $\mu$m $L_{eff}$, 1.8 V Si CMOS. This SiGe technology features shallow- and deep-trench isolation, along with a thermodynamically stable, 25% peak Ge content, graded UHV/CVD epitaxial

SiGe base [35]. Figure 5 shows the cross-section of the 7HP SiGe HBT.

8HP features 130 nm lithography, 200/280 GHz ($f_T$ / $f_{max}$), and 1.7 V $BV_{CEO}$, and is provided with 0.09 $\mu$m $L_{eff}$, 1.3 V Si CMOS. 8HP technology employs a novel, reduced thermal cycle, "raised extrinsic base" structure, and utilizes conventional deep and shallow trench isolation, an *in-situ* doped polysilicon emitter, and an unconditionally stable, 25% peak Ge, C-doped, graded UHV/CVD epitaxial SiGe base [36].

Both technologies come with a full suite of passive elements and seven levels of metallization.

In this chapter, the design and demonstration of LNAs for use in UWB systems is presented. Section 2.2 and Section 2.3 review noise theory and BJT noise model, respectively. Section 2.4, and Section 2.5 review the narrow band LNA and the resistive feedback LNA, respectively. Details of LNA 1 are described in Section 2.6. Measurement results of LNA1 are presented in Section 2.7. Details of LNA 2 and LNA 3 are described in Section 2.8. Measurement results of LNA 2 and LNA 3 are presented in Section 2.9 and Section 2.10, respectively. This work is also published as [59].

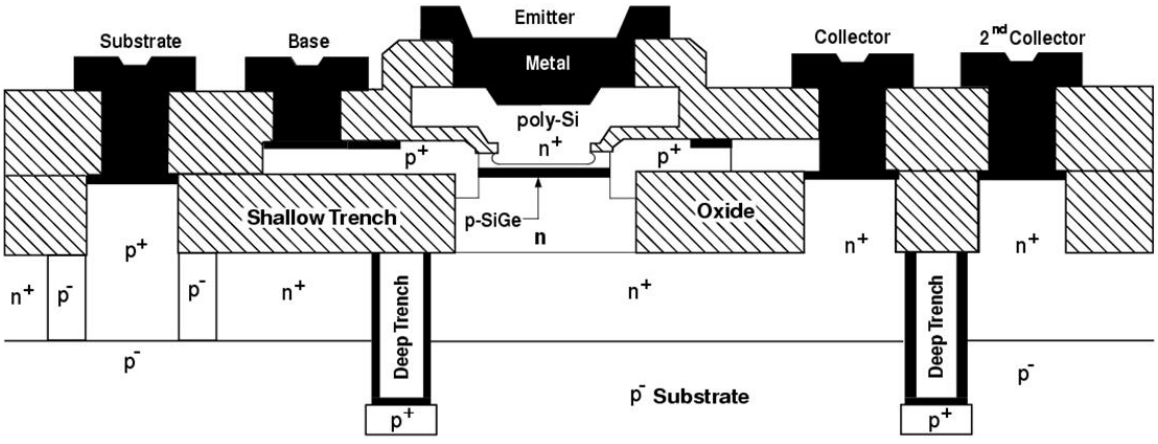


**Figure 5:** Schematic cross-section of the 7HP SiGe HBT.

## 2.2 Noise Factor of a Linear Two-Port Network

A noisy amplifier can be modeled as a noiseless amplifier with a noise voltage source ($v_n$) and a noise current source ($i_n$) at the input [48], as shown in Fig. 6. The noise factor is given as [48]

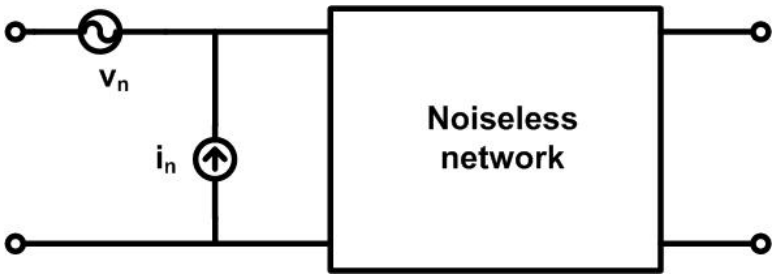


**Figure 6:** Two-port network with input-referred noise voltage source and current source.

$$F = 1 + \frac{(i_n + v_n Y_s)(i_n^* + v_n^* Y_s^*)}{i_{ns}^2} \tag{2}$$

$$= 1 + \frac{i_n^2 + 2\Re(i_n v_n^* Y_s^*) + v_n^2 Y_s^2}{i_{ns}^2}, \tag{3}$$

where $Y_s$ is the source admittance made out of a real part of $G_s$ and an imaginary part of $B_s$ [48]

$$Y_s = G_s + jB_s, \tag{4}$$

$i_{ns}^2$ is the mean-square value of the source noise current and is given by [48]

$$i_{ns}^2 = 4kTG_s, \tag{5}$$

where $k$ is the Boltzmann constant and $T$ the absolute temperature. The correlation admittance $Y_c$ is defined as [48]

$$Y_c = \frac{v_n i_n^*}{v_n^2} = G_c + jB_c. \tag{6}$$

The noise resistance $R_n$ and conductance $G_n$ can be defined as [48]

$$R_n = \frac{v_n^2}{4kT}, \tag{7}$$

$$G_n = \frac{i_n^2}{4kT}. \tag{8}$$

The noise factor can be written as [48]

$$F = 1 + \frac{i_n^2 + 2v_n^2\Re(Y_c Y_s^*) + v_n^2 Y_s^2}{i_{ns}^2} \tag{9}$$

$$= 1 + \frac{G_n + 2R_n\Re(Y_c Y_s^*) + R_n Y_s^2}{G_s}. \tag{10}$$

The minimum noise factor is achieved when the following conditions are satisfied [48]:

$$\frac{\partial F}{\partial G_s} = 0, \tag{11}$$

$$\frac{\partial F}{\partial B_s} = 0, \tag{12}$$

solving for optimum source admittance $Y_{s,opt}$ and impedance $Z_{s,opt}$ [48]

$$B_{s,opt} = -B_c, \tag{13}$$

$$G_{s,opt} = \sqrt{\frac{G_n}{R_n} - B_c^2}, \tag{14}$$

$$Y_{s,opt} = G_{s,opt} + jB_{s,opt}, \tag{15}$$

$$Z_{s,opt} = R_{s,opt} + jX_{s,opt} = 1/Y_{s,opt}, \tag{16}$$

$$R_{s,opt} = \frac{G_{s,opt}}{G_{s,opt}^2 + B_{s,opt}^2}, \tag{17}$$

$$X_{s,opt} = -\frac{B_{s,opt}}{G_{s,opt}^2 + B_{s,opt}^2}. \tag{18}$$

Thus, the minimum noise factor is [48]

$$F_{min} = 1 + 2R_n(G_c + G_{s,opt}). \tag{19}$$

The noise factor can be re-written as [48]

$$F = F_{mim} + \frac{R_n}{G_s}[(G_s - G_{s,opt})^2 + (B_s - B_{s,opt})^2]. \tag{20}$$

## 2.3 BJT Noise Model

The noise model for the bipolar transistor is shown in Fig. 7 [33]. The mean-square values of input-referred noise voltage and current of the bipolar transistor are [33]

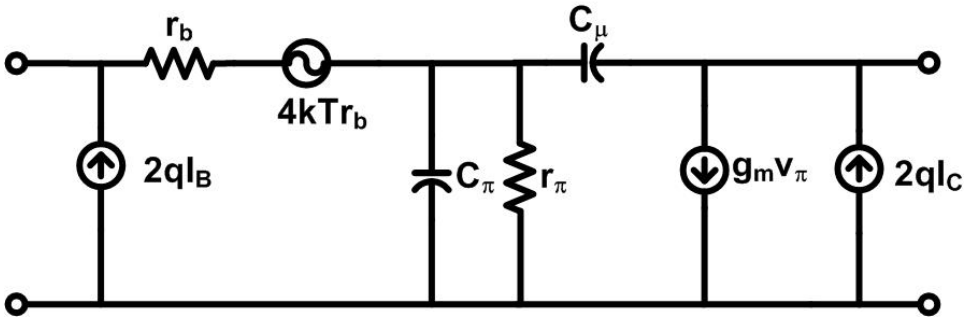


**Figure 7:** Noise model of the bipolar transistor.

$$v_n^2 = \frac{2qI_C}{g_m^2} + 4kTr_b, \tag{21}$$

$$i_n^2 = 2qI_B + \frac{2qI_C Y_{in}^2}{g_m^2}, \tag{22}$$

where $2qI_B$ and $2qI_C$ are the base and collector shot noise, respectively; $4kTr_b$ is the thermal noise because of the base resistance; $Y_{in}$, the input admittance of the transistor, is given as [33]

$$Y_{in} = \frac{1}{r_\pi} + j\omega C_\pi. \tag{23}$$

Thus, $R_n$, $G_n$, $Y_c$, $G_c$ and $B_c$ can be calculated as [33]

$$R_n = \frac{v_n^2}{4kT} \tag{24}$$

$$= \frac{\frac{2qI_C}{g_m^2} + 4kTr_b}{4kT} \tag{25}$$

$$= \frac{1}{2g_m} + r_b, \tag{26}$$

$$G_n = \frac{i_n^2}{4kT} \tag{27}$$

$$= \frac{2qI_B + \frac{2qI_C Y_{in}^2}{g_m^2}}{4kT} \tag{28}$$

$$= \frac{g_m}{2}(\frac{1}{\beta} + \frac{1}{\beta^2} + \frac{\omega^2 C_\pi^2}{g_m^2}), \tag{29}$$

$$Y_c = \frac{v_n i_n^*}{v_n^2} \tag{30}$$

$$= \frac{\frac{2qI_C}{g_m^2}(\frac{1}{r_\pi} + j\omega C_\pi)}{\frac{2qI_C}{g_m^2} + 4kTr_b} \tag{31}$$

$$= \frac{\frac{1}{\beta} + j\frac{\omega C_\pi}{g_m}}{\frac{1}{g_m^2} + 2r_b}, \tag{32}$$

$$G_c = \frac{1}{\beta}\frac{1}{\frac{1}{g_m} + 2r_b}, \tag{33}$$

$$B_c = \frac{\frac{\omega C_\pi}{g_m}}{\frac{1}{g_m} + 2r_b}. \tag{34}$$

$G_{s,opt}$, $B_{s,opt}$, $R_{s,opt}$, $X_{s,opt}$, and $F_{min}$ can also be calculated [33]

$$G_{s,opt} = \sqrt{\frac{G_n}{R_n} - B_c^2} \tag{35}$$

$$= \sqrt{\frac{\frac{g_m}{2}(\frac{1}{\beta} + \frac{1}{\beta^2} + \frac{\omega^2 C_\pi^2}{g_m^2})}{\frac{1}{2g_m} + r_b} - (\frac{\frac{\omega C_\pi}{g_m}}{\frac{1}{g_m} + 2r_b})^2}, \tag{36}$$

$$B_{s,opt} = -B_c = -\frac{\frac{\omega C_\pi}{g_m}}{\frac{1}{g_m} + 2r_b}, \tag{37}$$

$$R_{s,opt} = \frac{G_{s,opt}}{G_{s,opt}^2 + B_{s,opt}^2} \tag{38}$$

$$= \frac{\sqrt{\frac{\frac{g_m}{2}(\frac{1}{\beta} + \frac{1}{\beta^2} + \frac{\omega^2 C_\pi^2}{g_m^2})}{\frac{1}{2g_m} + r_b} - (\frac{\frac{\omega C_\pi}{g_m}}{\frac{1}{g_m} + 2r_b})^2}}{\frac{\frac{g_m}{2}(\frac{1}{\beta} + \frac{1}{\beta^2} + \frac{\omega^2 C_\pi^2}{g_m^2})}{\frac{1}{2g_m} + r_b}}, \tag{39}$$

$$X_{s,opt} = -\frac{B_{s,opt}}{G_{s,opt}^2 + B_{s,opt}^2} \tag{40}$$

$$= \frac{\frac{\frac{\omega C_\pi}{g_m}}{\frac{1}{g_m}+2r_b}}{\frac{\frac{g_m}{2}(\frac{1}{\beta}+\frac{1}{\beta^2}+\frac{\omega^2 C_\pi^2}{g_m^2})}{\frac{1}{2g_m}+r_b}}, \tag{41}$$

$$F_{min} = 1 + 2R_n(G_c + G_{s,opt}) \tag{42}$$

$$= 1 + 2(\frac{1}{2g_m} + r_b)[\frac{1}{\beta}\frac{1}{\frac{1}{g_m}+2r_b} + \sqrt{\frac{\frac{g_m}{2}(\frac{1}{\beta}+\frac{1}{\beta^2}+\frac{\omega^2 C_\pi^2}{g_m^2})}{\frac{1}{2g_m}+r_b} - (\frac{\frac{\omega C_\pi}{g_m}}{\frac{1}{g_m}+2r_b})^2}]. \tag{43}$$

By scaling the device size and adding reactive components, noise matching can be achieved [33]

$$Z_{s,opt} = R_{s,opt} + jX_{s,opt} = Z_s. \tag{44}$$

The design of LNA with simultaneous impedance and noise matching will be discussed in the next section [51].

## *2.4 Narrow Band LNA*

From the previous section, for a given collector current density, the minimum noise factor can be achieved if

$$Z_s = Z_{s,opt}. \tag{45}$$

In most RF systems, $Z_s$=50 Ω. Thus, in order to achieve noise matching and power matching, both input impedance and optimum noise source impedance should be 50Ω. In [51], an elegant solution that achieves simultaneous impedance and noise matching has been given. An optimum current density, which gives the lowest minimum noise figure can first be chosen based on the device minimum noise figure vs. the current density curve [51], which is available from the device model for a given process technology. By changing the emitter length of the device, $R_{s,opt}$ of 50 Ω can be realized, thus also determining the device size

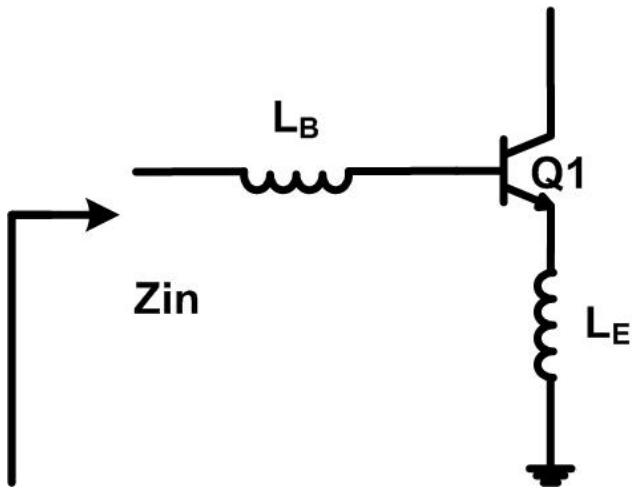


**Figure 8:** Common emitter amplifier with emitter and base inductors.

and bias current [51]. Then a degeneration inductance ($L_E$) and a base inductance ($L_B$) can be added (Fig. 8) [51].

The impedance looking into the input of LNA is given by [51]

$$Z_{in} = j\omega(L_E + L_B) + \frac{1}{j\omega C_\pi} + \frac{g_m}{C_\pi}L_E, \tag{46}$$

where $L_E$ is the emitter degeneration inductance, $L_B$ is the base series inductance, $C_\pi$ is the base-emitter capacitance of $Q_1$, and $g_m$ is the transconductance. The real part of the input impedance is equal to 50Ω [51]

$$\frac{g_m}{C_\pi}L_E = 50\Omega, \tag{47}$$

solving for $L_E$ [51]

$$L_E = \frac{C_\pi 50\Omega}{g_m}. \tag{48}$$

The value of $L_B$ is chosen so that the circuit resonances at the center frequency $\omega$ [51]. The imaginary part of the input impedance is equal to 0 [51]

$$j\omega(L_E + L_B) + \frac{1}{j\omega C_\pi} = 0, \tag{49}$$

solving for $L_B$ [51]

$$L_B = \frac{1}{\omega^2 C_\pi} - L_E. \tag{50}$$

Simultaneous impedance and noise matching has now been achieved [51]. This technique can be directly appled into cascode topology, as shown in Fig. 9. The cascode LNA has been widely used because of its higher gain, better isolation, and with only slightly higher noise figure compared to a simple common-emitter amplifier. However, this method only

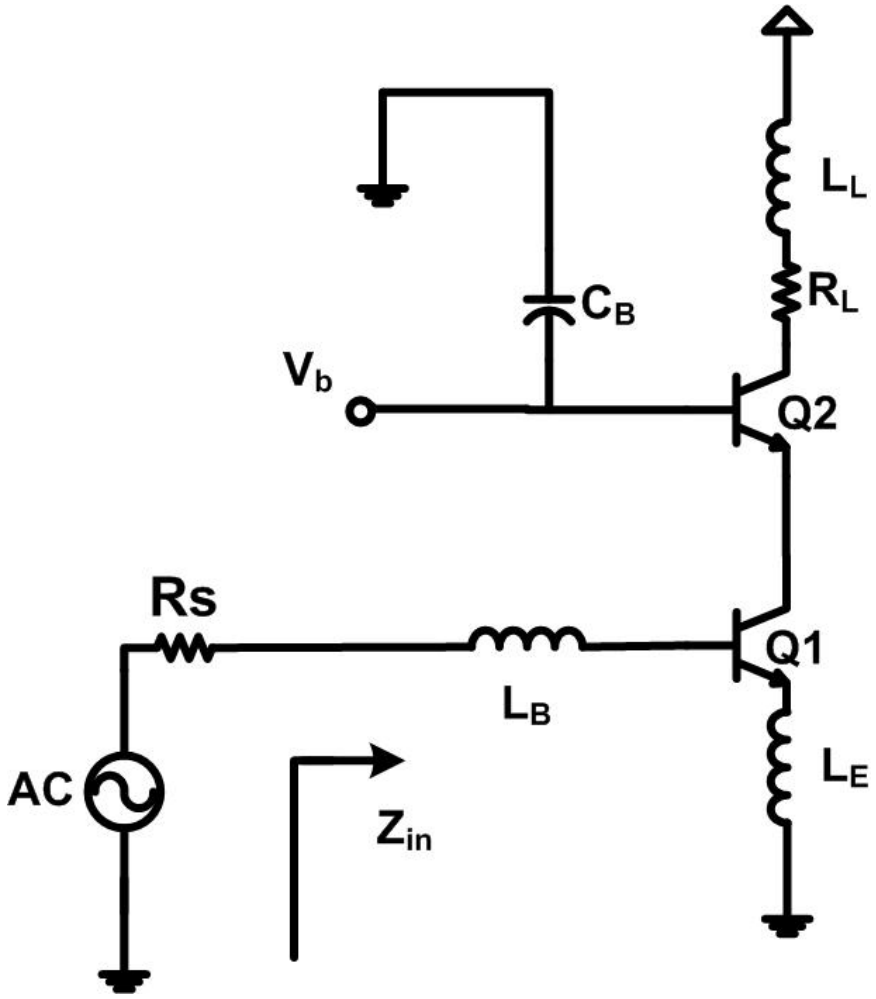


**Figure 9:** Schematic of the cascode LNA with inductive degeneration.

takes into account the noise and impedance matching. Other important specifications of the LNA, especially its linearity, power consumption and bandwidth also need to be addressed in order to suit different applications. For UWB applications, special techniques need to be adopted to widen the input bandwidth.

## 2.5 *Resistive Feedback LNA*

Adding a shunt 50 Ω resistor at the input is the simplest way to achieve wideband impedance matching to 50 Ω. However, the 3 dB noise figure increasement added by this resistor is unacceptable for LNA in most applications [49]. Shunt-shunt feedback (Fig. 10) is generally preferred as it combines wideband impedance matching with a reasonably low noise figure [49].

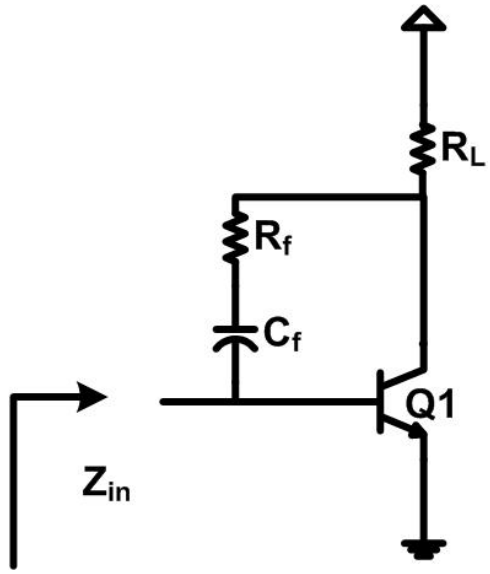


**Figure 10:** Schematic of the LNA with shunt-shunt feedback.

$$a = \frac{v_o}{i_i} = -g_m \frac{R_f R_\pi}{R_f + R_\pi} \frac{R_f R_L}{R_f + R_L}, \tag{51}$$

$$f = \frac{v_o}{i_i} = -\frac{1}{R_f}. \tag{52}$$

The loop gain ($T$) is

$$T = af = g_m \frac{R_\pi}{R_f + R_\pi} \frac{R_f R_L}{R_f + R_L}, \tag{53}$$

$$A_v = \frac{v_o}{v_i} = -g_m \frac{R_f R_\pi}{R_f + R_\pi}. \tag{54}$$

The input impedance of the basic amplifier is

$$Z_{ia} = \frac{R_f R_\pi}{R_f + R_\pi}, \tag{55}$$

Taking into account feedback, the input impedance becomes [49]

$$Z_{in} = \frac{Z_{ia}}{1+T} = \frac{\frac{R_f R_\pi}{R_f + R_\pi}}{1 + g_m \frac{R_\pi}{R_f + R_\pi} \frac{R_f R_L}{R_f + R_L}}, \tag{56}$$

assuming $T >> 1$

$$Z_{in} = \frac{Z_{ia}}{1+T} \approx \frac{R_f + R_L}{g_m R_L}. \tag{57}$$

An emitter follower buffer can also be added to to the feedback loop, as shown in Fig. 11 [49]. The input impedance of the amplifier becomes [49]

$$Z_{in} = \frac{R_f}{g_m R_L}. \tag{58}$$

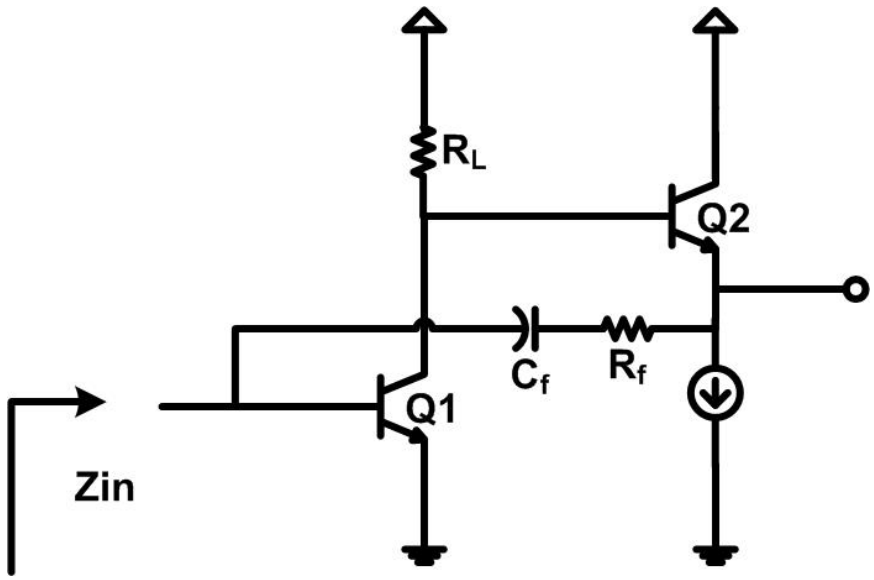


**Figure 11:** Schematic of the LNA with shunt-shunt feedback and emitter follower.

## *2.6 UWB LNA 1*

A conventional narrow-band cascode LNA with inductive degeneration is shown in Fig. 9. The expression for its input bandwidth as a function of the quality factor ($Q_{in}$) of

the input network is [25]

$$BW_{in} = \frac{\omega_0}{Q_{in}}, \tag{59}$$

where $\omega_0$, the center frequency, is given by

$$\omega_0 = \frac{1}{\sqrt{C_\pi(L_B + L_E)}}, \tag{60}$$

and $Q_{in}$ is given by [25]

$$Q_{in} = \frac{\sqrt{\frac{(L_B+L_E)}{C_\pi}}}{\frac{g_m L_E}{C_\pi} + R_s} = \frac{1}{C_\pi \omega_0 (\frac{g_m L_E}{C_\pi} + R_s)}, \tag{61}$$

where $R_S$ is the source resistance.

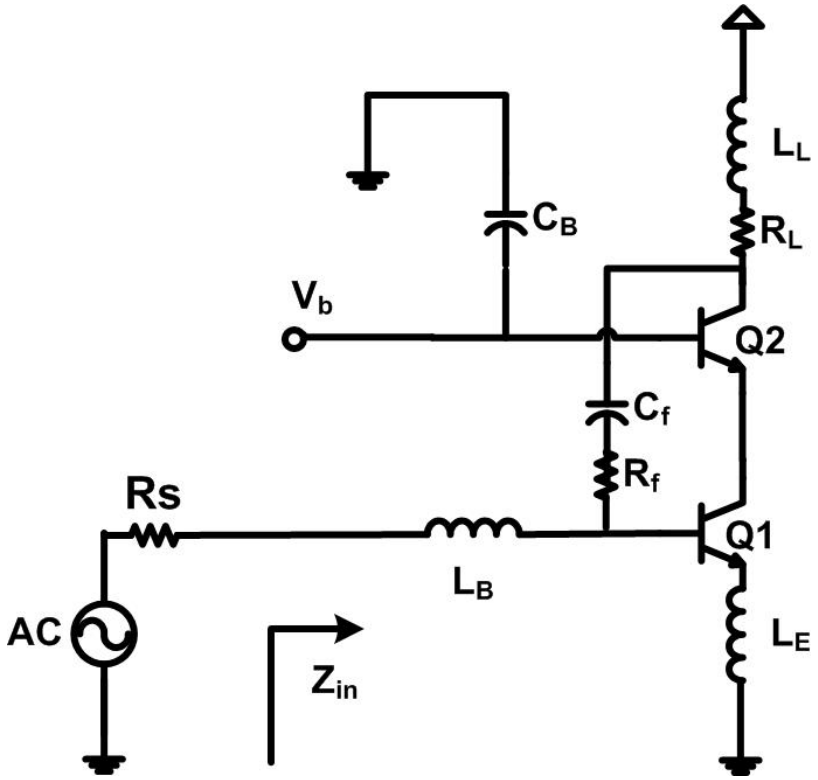


**Figure 12:** Schematic of the broadband LNA with weak resistive feedback.

Typically, in a cascode LNA, $Q_{in}$ is high and the bandwidth is very narrow [25]. To

broaden the bandwidth, a large resistor ($R_f$) is added between the base of the input transistor and the cascode output (Fig. 12). $Q_{in}$ then becomes [53]

$$Q_{in} \approx \frac{1}{C_\pi \omega_0 (\frac{g_m L_E}{C_\pi} + R_s + \frac{(\omega_0 L_B)^2}{R_f})}. \tag{62}$$

Observe that this is not a conventional resistive feedback LNA because the resistor does not directly provide the 50 Ω impedance match. Instead, it uses a much larger resistor that broadens the input bandwidth of the LNA by decreasing the $Q_{in}$ of the network, while causing only a marginal degradation in the noise performance [53]. However, the bandwidth covering the 3-5 GHz range obtained in [53] is still insufficient to cover the 3-10 GHz range required for UWB applications.

Assuming $\omega_0$ and $R_s$ are fixed in the input impedance expression for the original input network (61), the parameters that can be tweaked to obtain the desired wideband response are $L_E$, $g_m$, and $C_\pi$. $L_E$ must be very small in order to achieve high gain and low noise and hence offers little room for adjustment. The effective value of $C_\pi$ (base-emitter capacitance) can, however, be increased by adding a shunt capacitor $C_m$ between the base and emitter of the input transistor (Fig. 13).

The effective base-emitter capacitance ($C_{eff}$) is now given by

$$C_{eff} = C_\pi + C_m, \tag{63}$$

This increase in effective base-emitter capacitance causes the $Q_{in}$ of the input network to decrease. In addition, the transconductance ($g_m$) needs to be increased so that $g_m L_E / C_{eff} + r_b$ is still matched to 50 Ω. $Q_{in}$ for this modified network is now given by

$$Q_{in} = \frac{1}{C_{eff} \omega_0 (\frac{g_m L_E}{C_{eff}} + R_s)}, \tag{64}$$

The expression for $\omega_0$ can be modified as follows to include $C_{eff}$.

$$\omega_0 = \frac{1}{\sqrt{C_{eff}(L_B + L_E)}}, \tag{65}$$

Contrary to the initial assumption that $\omega_0$ is fixed, (65) suggests that $\omega_0$ decreases as $C_{eff}$

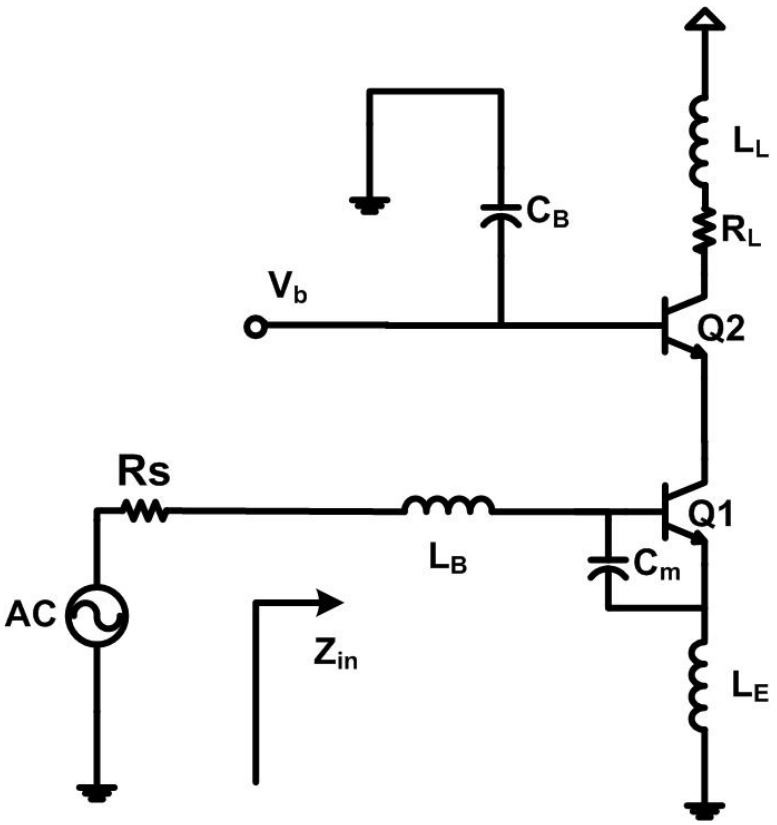


**Figure 13:** Schematic of the broadband LNA with shunt base-emitter capacitor.

increases. However, the shift in center frequency caused by the increase in $C_{eff}$ can be offset by decreasing $L_B$. This suggests that the $L_B$ required is much smaller than that used in a traditional narrow-band LNA. For the present design, an $L_B$ of 300 pH was chosen compared to a 1 nH or larger $L_B$ required in a conventional narrow-band LNA. In addition, a smaller $L_B$ can help reduce the noise figure by introducing a smaller series resistance at the input of the LNA.

It is well known that an increased base-emitter capacitance (decreased $f_T$) degrades the gain and noise figure at high frequencies. However, if the value of this extra capacitance is carefully chosen, the degradation in performance over the frequency band of interest can be minimized.

Similar techniques can be found in [55] and [22]. The LNA presented in [55] achieves multi-band matching centered at frequencies of 2.45 GHz and 5.25 GHz, whereas that

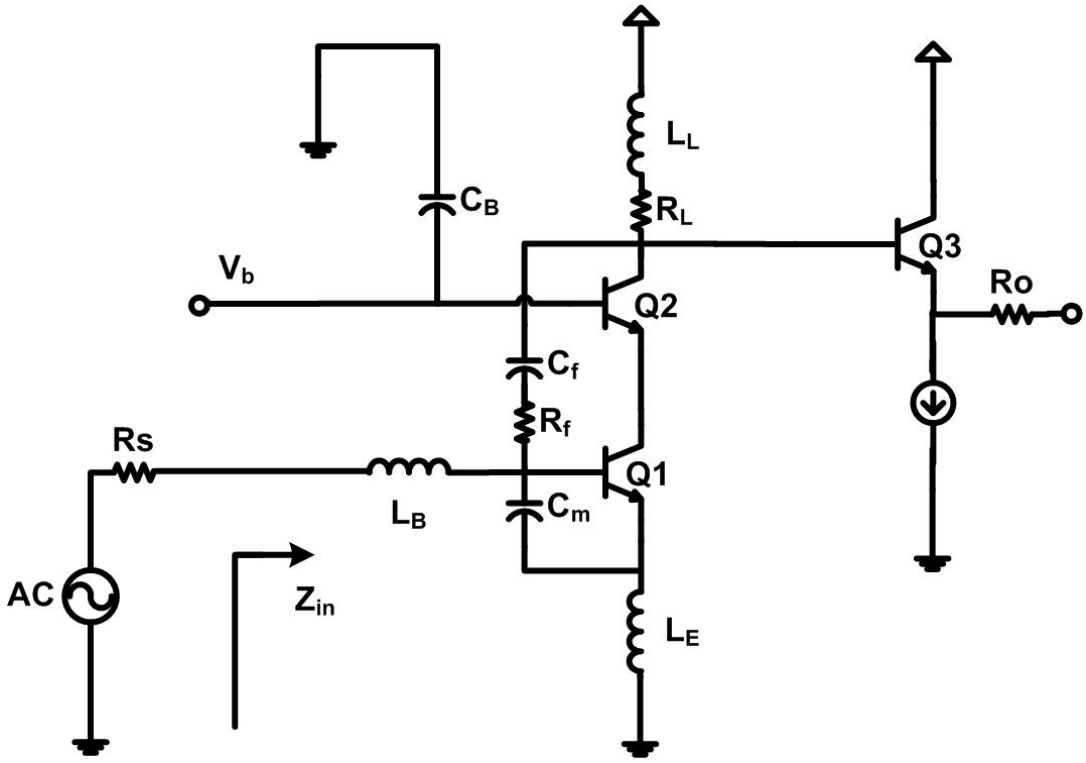


**Figure 14:** Schematic of the present SiGe UWB LNA with weak resistive feedback and shunt base-emitter capacitor.

described in [22], relies primarily on an LC filter at the input to achieve an input match. These designs, however, are not adequate to achieve matching over the entire 3-10 GHz UWB range without a filter.

It is clear from the preceding analysis that the bandwidth of the LNA ($\propto 1/Q_{in}$) is very sensitive to the base-emitter capacitance and the feedback resistance. In contrast, the other electrical parameters such as gain, noise, isolation, input impedance, and linearity are not very sensitive to $C_m$ and $R_f$. Thus, a broadband input match can be achieved by using a very small $C_m$ and a very large $R_f$ with only a minimal effect on the other parameters.

The LNA realized in the present work incorporates both a shunt base-emitter capacitance and weak resistive feedback in a cascode architecture with inductive degeneration, as shown in Fig. 14. The load inductor $L_L$ widens the bandwidth at high frequency by causing inductive peaking, which offsets the gain roll-off introduced by a capacitive load. The

output buffer is a simple emitter-follower, providing broadband 50 Ω match at the output.

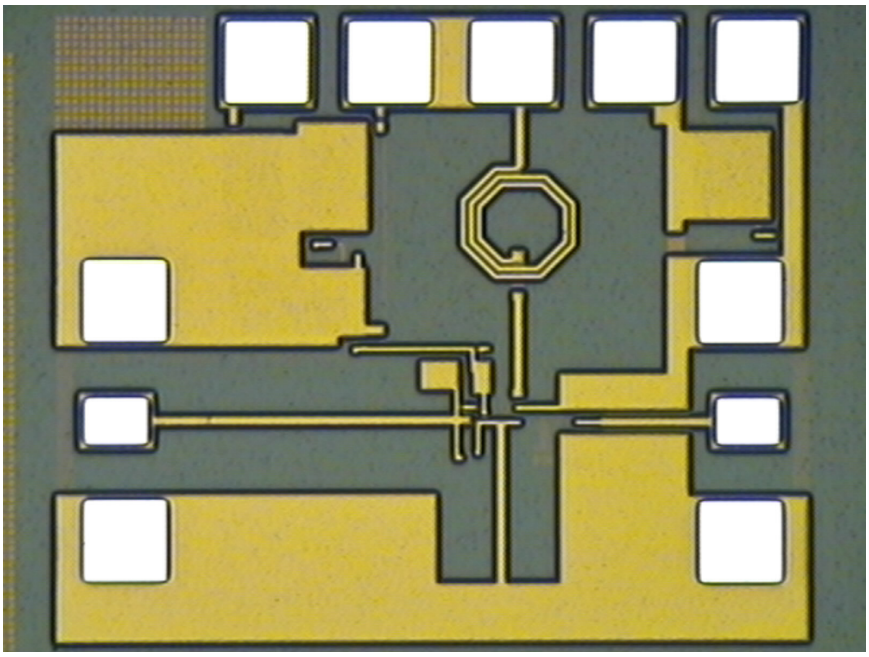

**Figure 15:** Die micrograph of the SiGe UWB LNA 1.

## *2.7 Measurement Results of LNA 1*

The LNA 1 was implemented in a commercially available 0.18 $\mu$m 120 GHz SiGe HBT BiCMOS technology [35] and occupies a total area of 0.8×0.9 mm$^2$, including the probe pads. The chip micrograph is shown in Fig. 15. The base and emitter inductors ($L_B$ and $L_E$, respectively), both of which are very small, can be best implemented using line inductors, which have higher $Q$ and lower parasitic resistance compared to spiral inductors. The load inductor $L_L$ is a spiral inductor. The output is connected to the probe pad through a side-shielded 50 Ω micro-strip transmission line. The LNA was tested on-wafer using 50 GHz probes and cables.

The LNA 1 operates off a 3.3 V power supply and has 7.8 mA of bias current flowing through the core circuit. Figure 16 shows its two-port measured S-parameters from 0.1 GHz to 20 GHz. The measured values $S_{11}$ and $S_{22}$ are lower than -7.2 dB across the

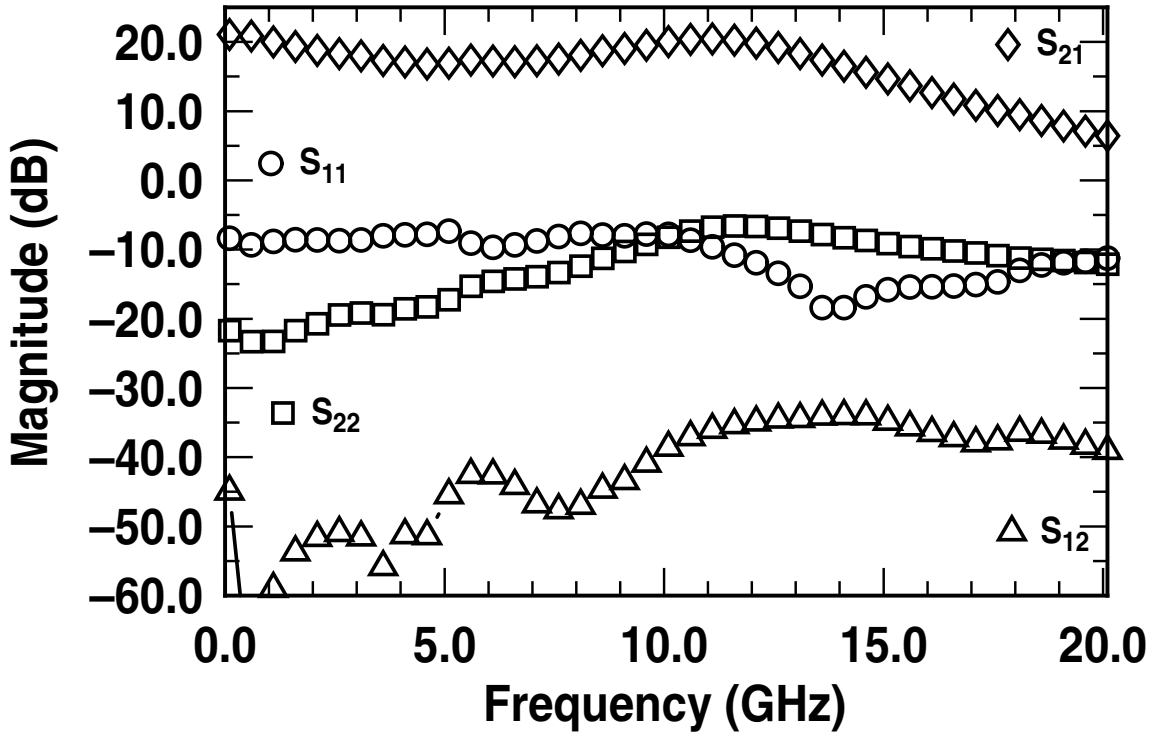


**Figure 16:** Measured S-parameters of the SiGe UWB LNA 1.

frequency band of 3–10 GHz, which is higher than the -12 dB and -16 dB, respectively, predicted by simulations. The $S_{21}$ displays a maximum gain of 20.3 dB and shows a variation of 3.5 dB over the band of interest. The reverse isolation $S_{12}$ is lower than -37 dB. Figure 17 shows the measured and simulated noise figures across the frequency range. The measured minimum NF is 1.8 dB at 3.0 GHz compared to 1.38 dB in the simulation. At high frequencies the measured NF reaches as high as 3.1 dB at 10.0 GHz, compared to the 2.03 dB in the simulation. The achieved noise figure is better than that of other UWB LNAs published in the literature and is in fact comparable to a well-designed narrow-band LNA. The key to achieving both low noise and wide bandwidth lies in the simultaneous use of shunt base-emitter capacitance and shunt-resistive feedback in a cascode LNA with inductive degeneration.

Figure 18 shows the linearity data for the LNA 1. The third-order input intercept point (IIP3) is 2.1 dBm for a two-tone input signal containing 6.00 GHz and 6.02 GHz frequency

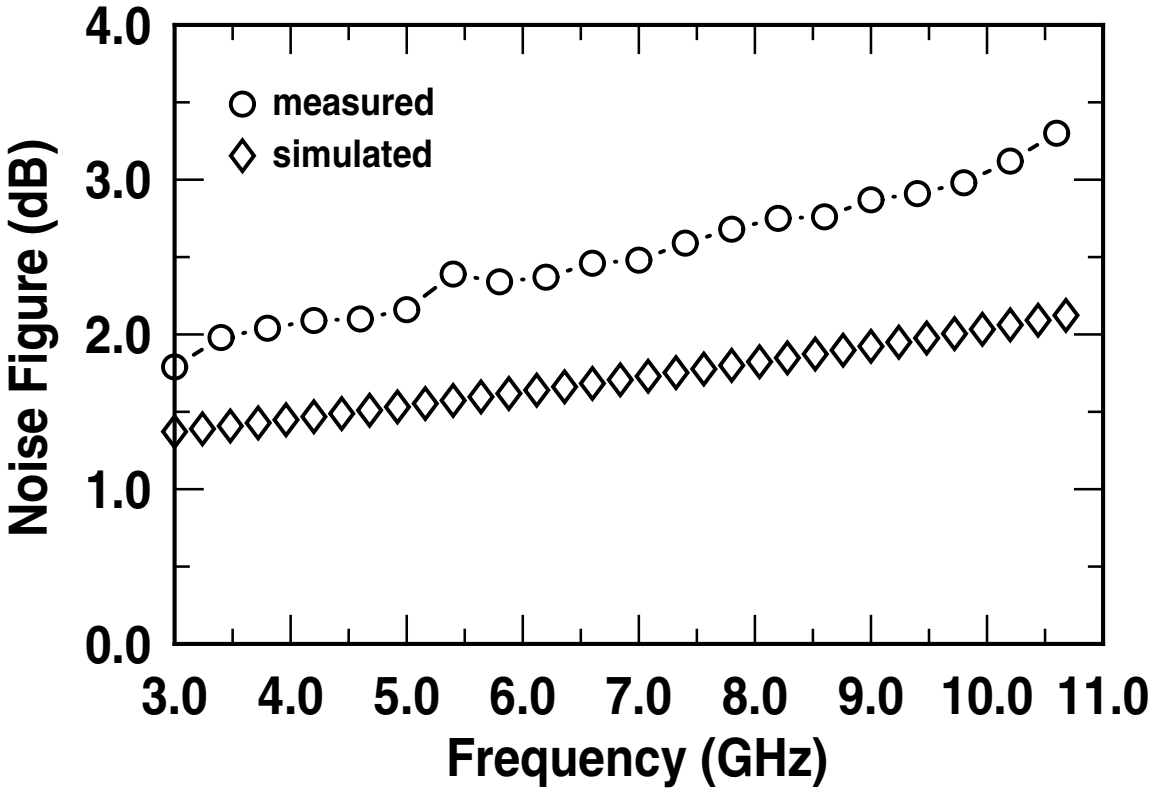


**Figure 17:** Measured and simulated noise figure of the SiGe UWB LNA 1.

components, and the 1-dB compression point ($P_{1dB}$) is -12.5 dBm for a 6.0 GHz input signal. The measurement and simulation results of the UWB LNA 1 are summarized in Table 4.

## *2.8 UWB LNA 2 and 3*

The LNA 1 data revealed significant differences between the simulation results and the measured results, with measured results showing worse return losses, lower gain, and a higher noise figure, but better linearity than those simulated. The parasitic inductance at the ground of the degeneration inductor ($L_E$) appears to be responsible these discrepancies. To address this problem, in the LNA 2 and LNA3 design, a better ground was achieved by using all seven metal layers in parallel and as many substrate contacts as possible between the ground pads and the $L_E$. Also, the parasitic inductance at the base of the common-base

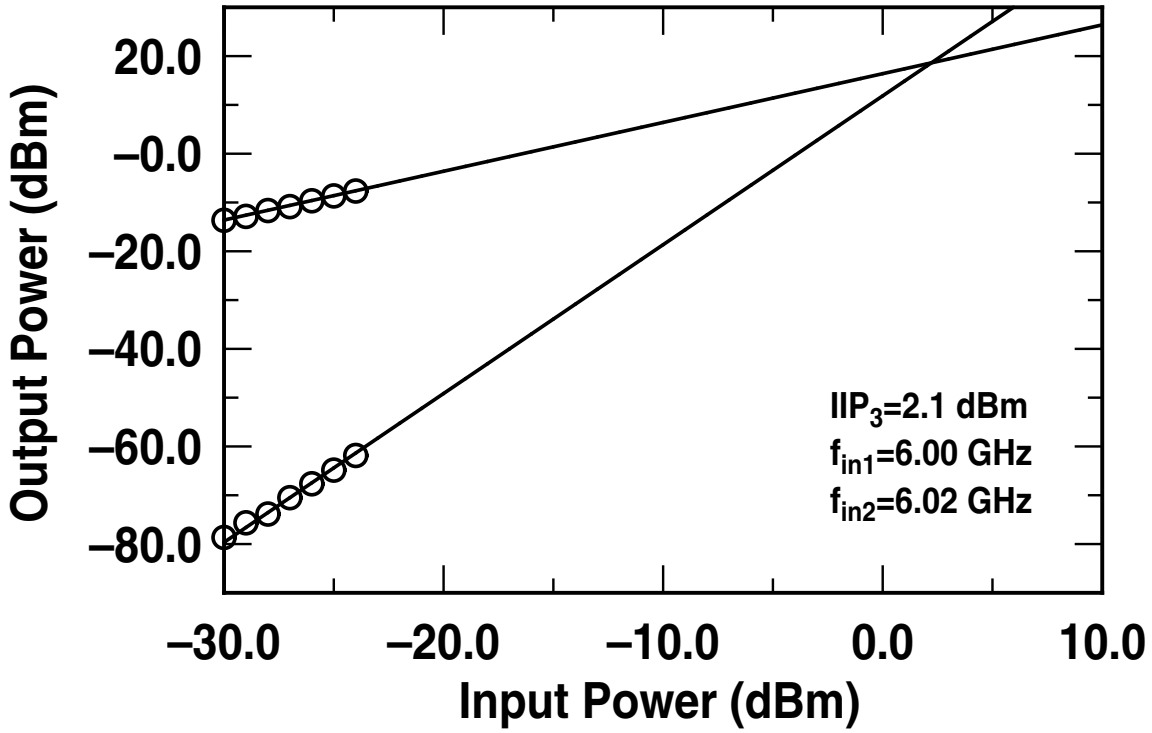


**Figure 18:** Measured IIP3 of the SiGe UWB LNA 1.

**Table 4:** Summary of the SiGe UWB LNA 1 Characteristics.

| | Measured | Simulated |
|---|---|---|
| Bandwidth | 0.1-13.6 GHz | 0.1-13.7 GHz |
| $NF_{min}$- $NF_{max}$ | 1.8 - 3.1 dB | 1.38 - 2.03 dB |
| $Gain_{min}$ - $Gain_{max}$ | 16.8 - 20.3 dB | 19.7 - 21.8 dB |
| $S_{11}$ | < -7.2 dB | < -12.2 dB |
| $S_{22}$ | < -7.4 dB | < -16 dB |
| $S_{12}$ | < -37 dB | < -48.3 dB |
| IIP3(at 6 GHz) | 2.1 dBm | -4 dBm |
| $P_{1dB}$(at 6 GHz) | -12.5 dBm | -14.6 dBm |
| Power supply | 3.3 V | 3.3 V |
| Power consumption (without output buffer) | 26 mW | 26 mW |
| Die size | 0.80 × 0.90 mm$^2$ | 0.80 × 0.90 mm$^2$ |

transistor (non-ideal ground) may have degraded the S-parameters. A by-pass capacitor was therefore used to achieve a better ground, but the return path to ground may still introduce non-negligible parasitic inductance. Similar methods that incorporated the use of

wider and multiple layer of metals have also been used to alleviate this problem. Instead of using a parallel capacitor $C_M$ between the base and emitter, the new design simply uses a very large transistor size to increase the $C_{BE}$. The larger transistor also has a smaller $r_b$, and thus a lower noise figure. LNA 2 was implemented in 7HP technology, as with the LNA 1, but LNA 3 was implemented in 8HP technology, which features 130 nm lithography, 200/280 GHz ($f_T$ / $f_{max}$), and 1.7 V $BV_{CEO}$ [36]. Therefore, a lower noise figure is expected from LNA 3.

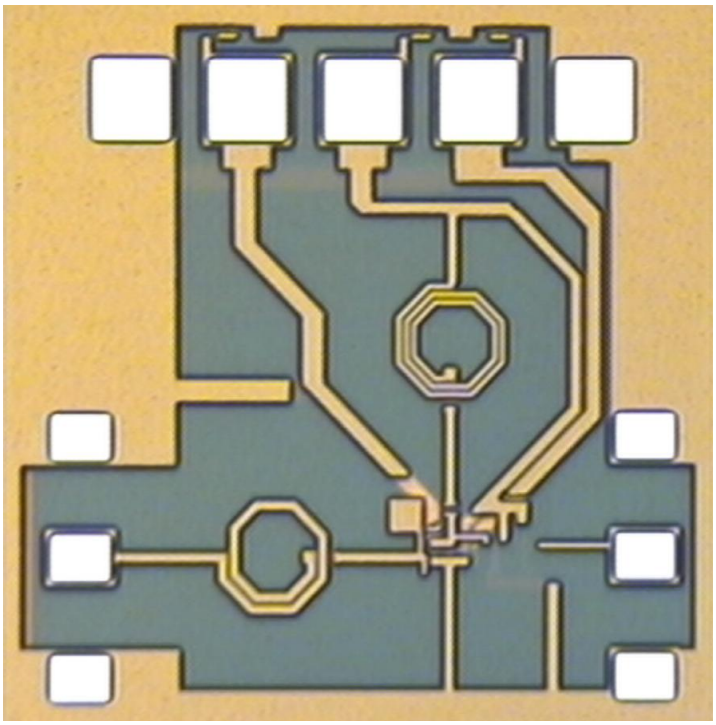

**Figure 19:** Die micrograph of the SiGe UWB LNA 2.

## *2.9 Measurement Results of UWB LNA 2*

The chip micrograph of LNA 2 is shown in Fig. 19. This LNA operates off a 3.3 V power supply and has 7.95 mA of bias current flowing through its core circuit.

Figures 20- 23 show the two-port measured S-parameters from 1.0 GHz to 15.0 GHz. The measured $S_{11}$ and $S_{22}$ are lower than -13.4 dB and -8.7 dB, respectively, across the

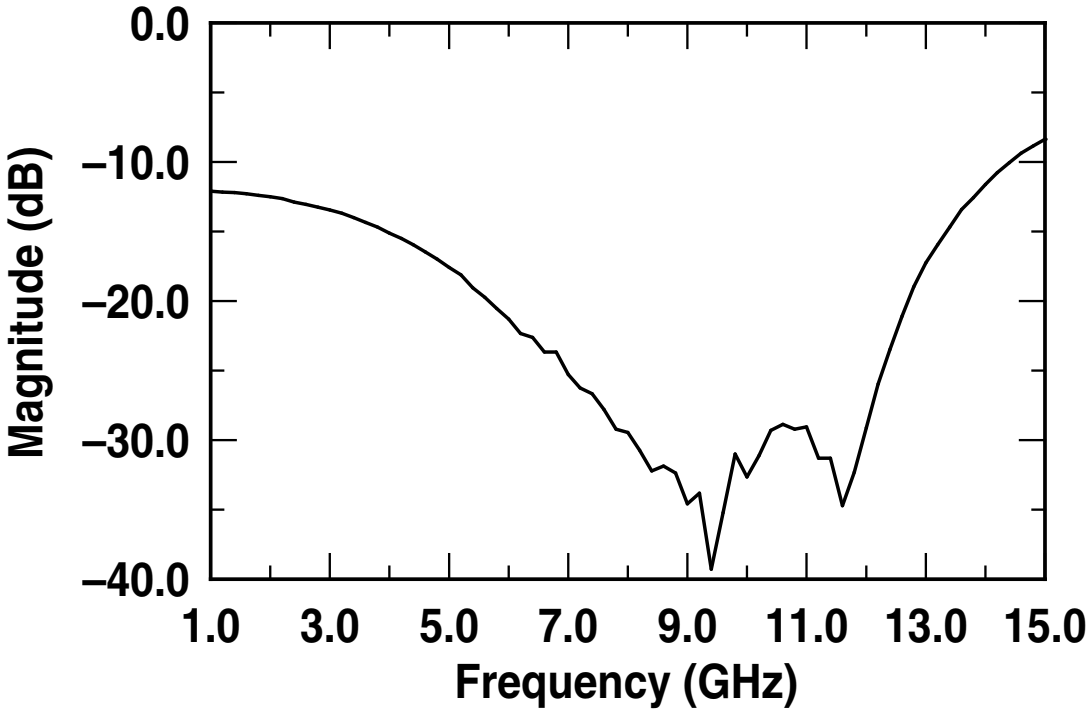


**Figure 20:** Measured $S_{11}$ of the SiGe UWB LNA 2.

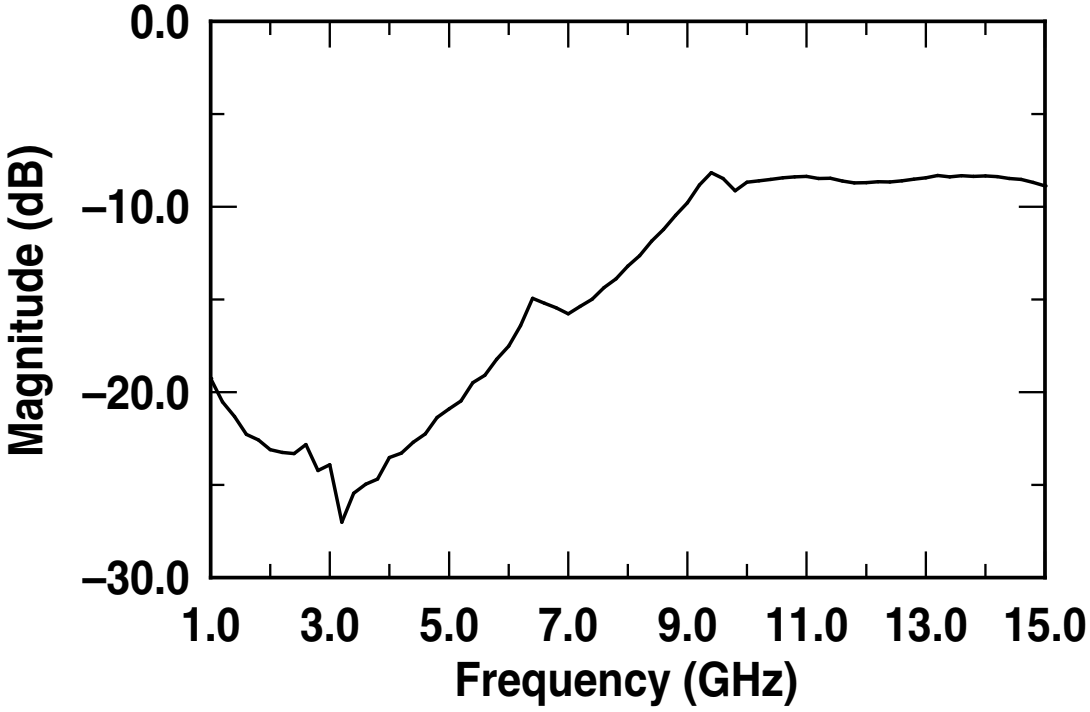


**Figure 21:** Measured $S_{22}$ of the SiGe UWB LNA 2.

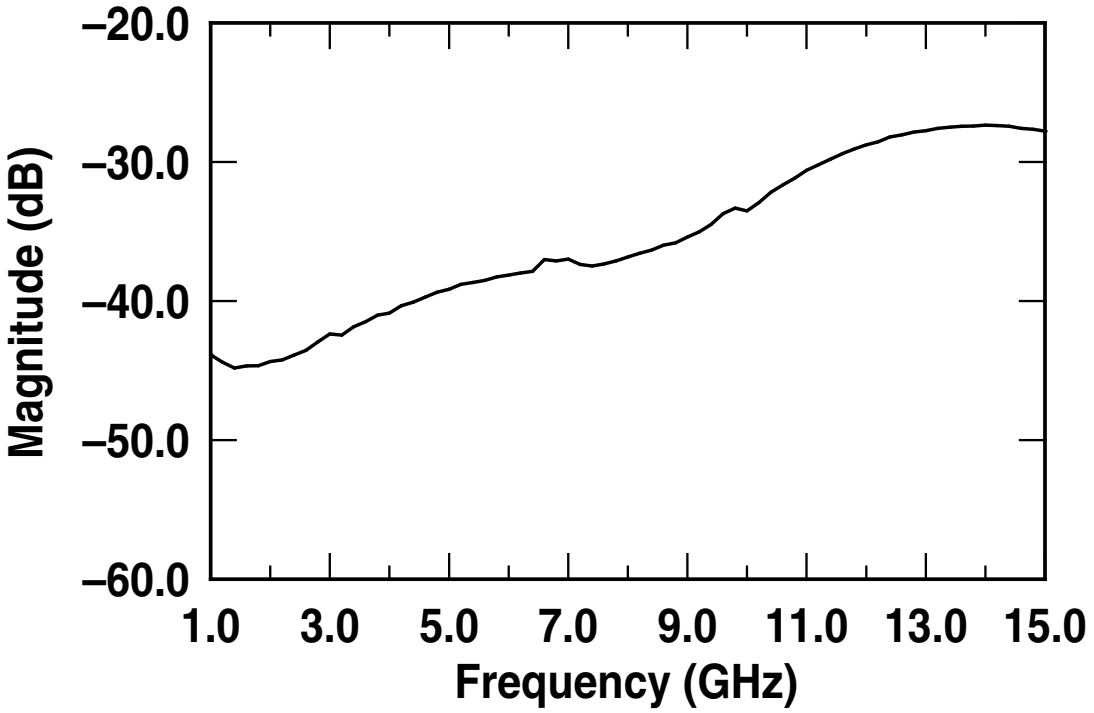


**Figure 22:** Measured $S_{12}$ of the SiGe UWB LNA 2.

frequency band of 3-10 GHz, compared with the -12.7 dB and -21.9 dB, respectively, predicted by simulations. The $S_{21}$ displays a maximum gain of 20.0 dB and shows a variation of 1.1 dB over the band of interest. The reverse isolation $S_{12}$ is lower than -33 dB. Figure 24 shows the measured and simulated noise figures across the frequency range. The measured minimum NF is 1.61 dB, compared to 1.46 dB in the simulation. At high frequencies the measured NF reached as high as 2.38 dB, compared to 2.32 dB in the simulation. The achieved noise figure is better than that of LNA 1 because of the improvements discussed in the previous section.

Figure 25 shows the linearity data for the LNA 2. The third-order input intercept point (IIP3) is -4.0 dBm for a two-tone input signal containing 6.00 GHz and 6.02 GHz frequency components.

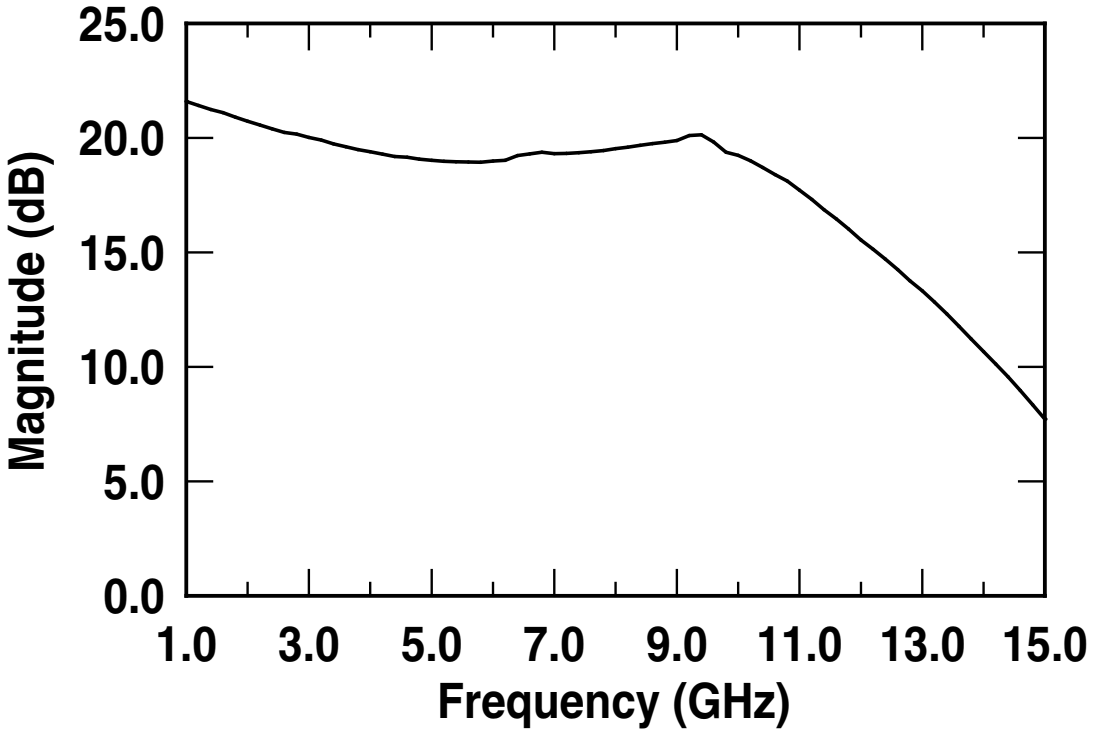


**Figure 23:** Measured $S_{21}$ of the SiGe UWB LNA 2.

**Table 5:** Summary of the SiGe UWB LNA 2 Characteristics.

| | Measured | Simulated |
|---|---|---|
| Bandwidth | 0.1-11.2 GHz | 0.1-11.6 GHz |
| $NF_{min}$- $NF_{max}$ | 1.61 - 2.38 dB | 1.46 - 2.32 dB |
| $Gain_{min}$ - $Gain_{max}$ | 18.9 - 20.0 dB | 19.0 - 20.6 dB |
| $S_{11}$ | < -13.4 dB | < -12.7 dB |
| $S_{22}$ | < -8.7 dB | < -21.9 dB |
| $S_{12}$ | < -33 dB | < -52.4 dB |
| IIP3(at 6 GHz) | -4 dBm | -6.5 dBm |
| Power supply | 3.3 V | 3.3 V |
| Power consumption (without output buffer) | 26.2 mW | 26.2 mW |
| Die size | 0.96 × 0.94 mm$^2$ | 0.96 × 0.94 mm$^2$ |

## *2.10 Measurement Results of UWB LNA 3*

The chip micrograph of LNA 3 is shown in Figure 26. This LNA operates off a 3.3 V power supply and has 9.7 mA of bias current flowing through its core circuit.

Figures 27- 30 show the two-port measured S-parameters from 1.0 GHz to 15.0 GHz.

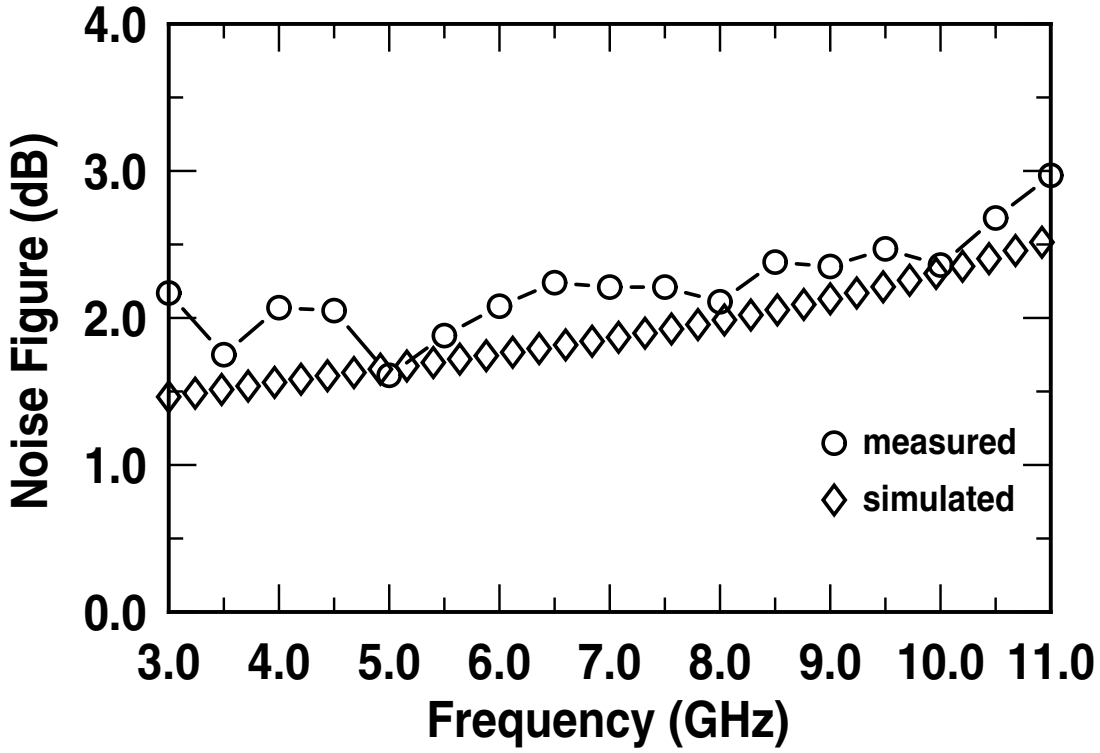


**Figure 24:** Measured and simulated noise figure of the SiGe UWB LNA 2.

The measured $S_{11}$ and $S_{22}$ are lower than -12.6 dB and -16.6 dB, respectively, across the frequency band of 3-10 GHz, compared with the -12.8 dB and -29.2 dB, respectively, predicted by simulations. The $S_{21}$ displays a maximum gain of 23.6 dB with a variation of 2.9 dB over the band of interest. The reverse isolation $S_{12}$ is lower than -58 dB. Fig. 31 shows the measured and simulated noise figures across the frequency range. The measured minimum NF is 1.17 dB, compared to 0.96 dB predicted by the simulation. At high frequencies the measured NF reached as high as 1.75 dB, compared to 1.39 dB in the simulation. The achieved noise figure is again better than that of LNA 1 or LNA 2 because of the improvements discussed in the previous section and the more advanced process technology.

Figure 32 shows the linearity data of the LNA 3. The third-order input intercept point (IIP3) is -3.6 dBm for a two-tone input signal containing 6.00 GHz and 6.02 GHz frequency components.

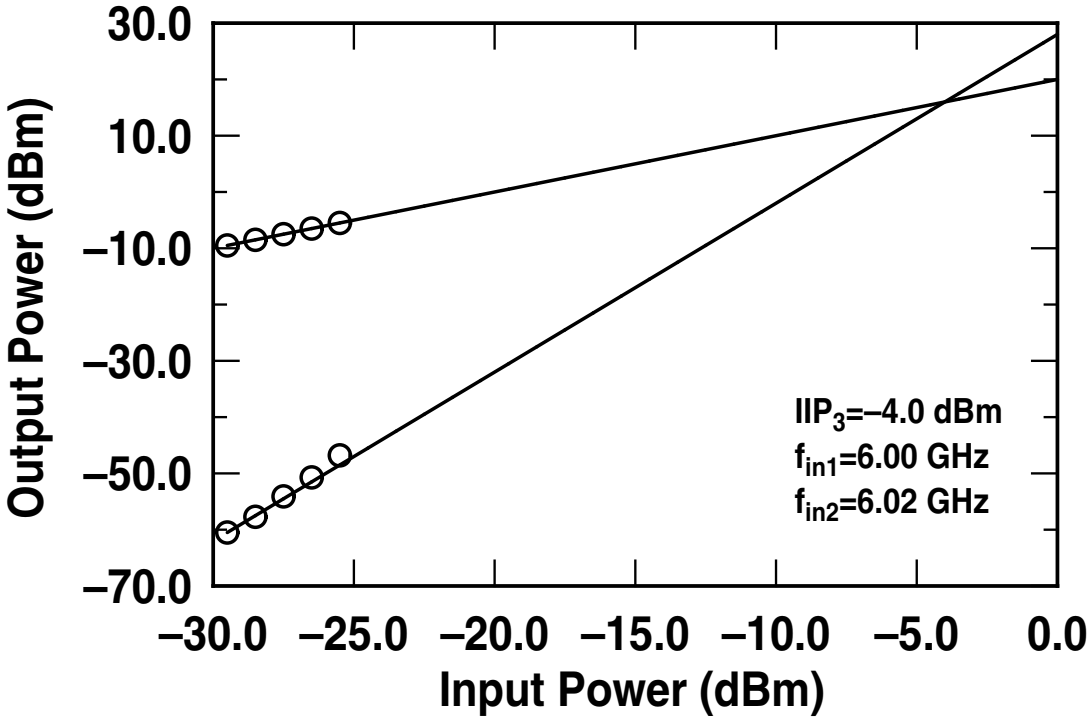


**Figure 25:** Measured IIP3 of the SiGe UWB LNA 2.

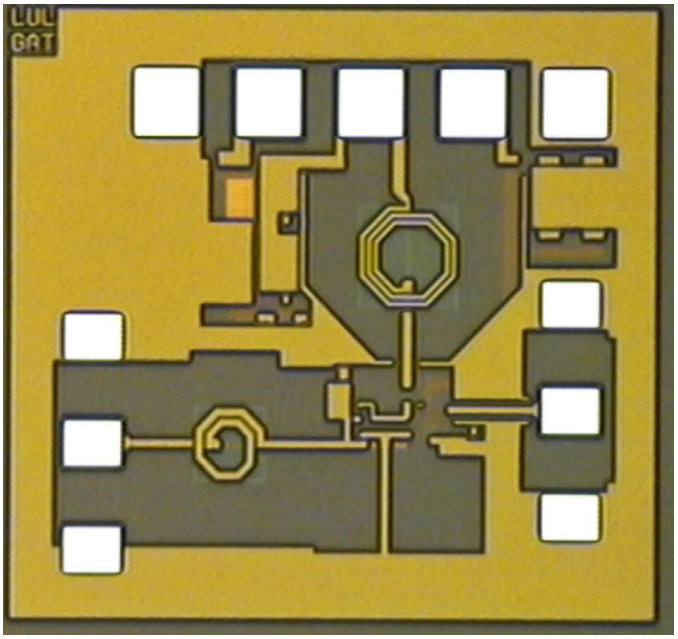

**Figure 26:** Die micrograph of the SiGe UWB LNA 3.

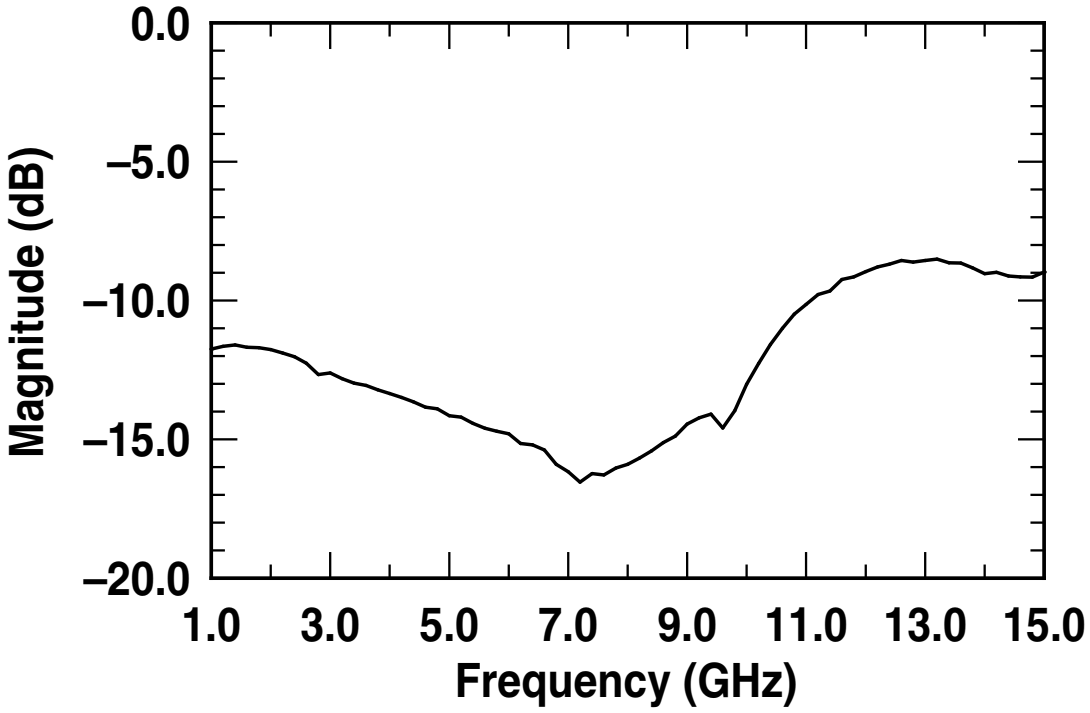


**Figure 27:** Measured $S_{11}$ of the SiGe UWB LNA 3.

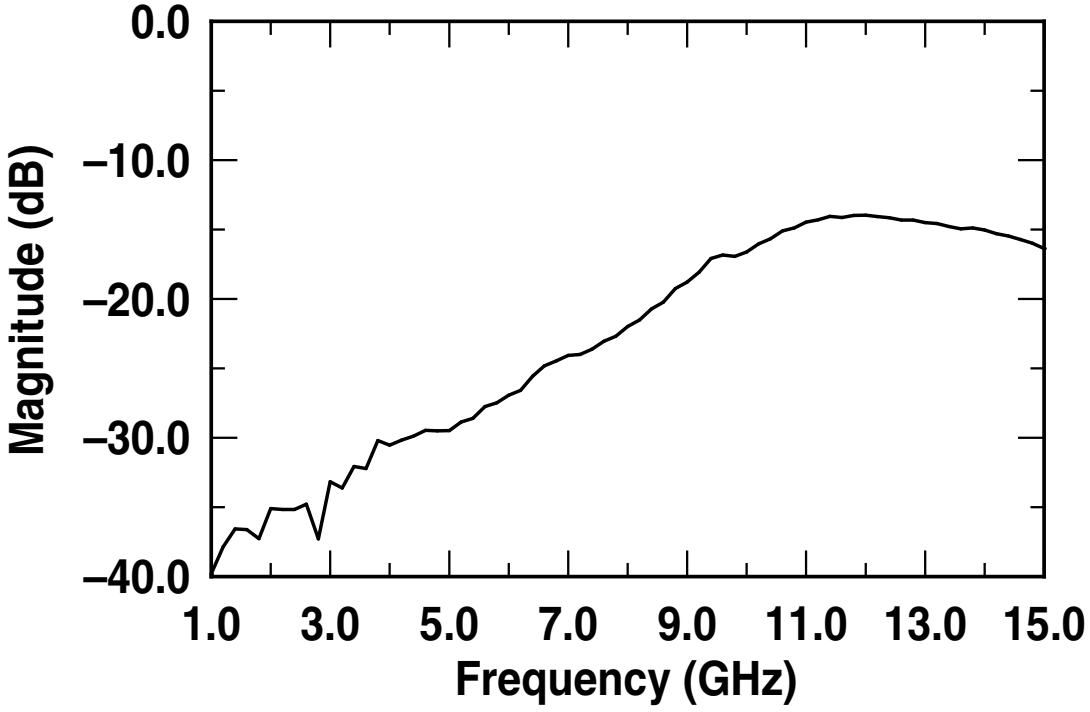


**Figure 28:** Measured $S_{22}$ of the SiGe UWB LNA 3.

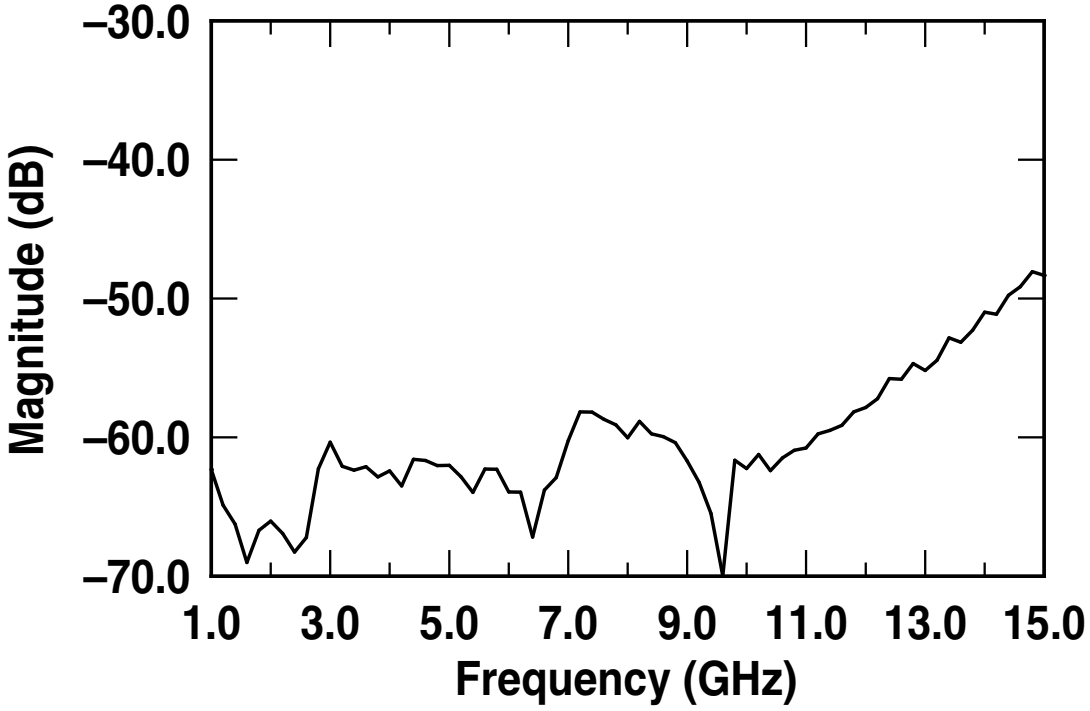


**Figure 29:** Measured $S_{12}$ of the SiGe UWB LNA 3.

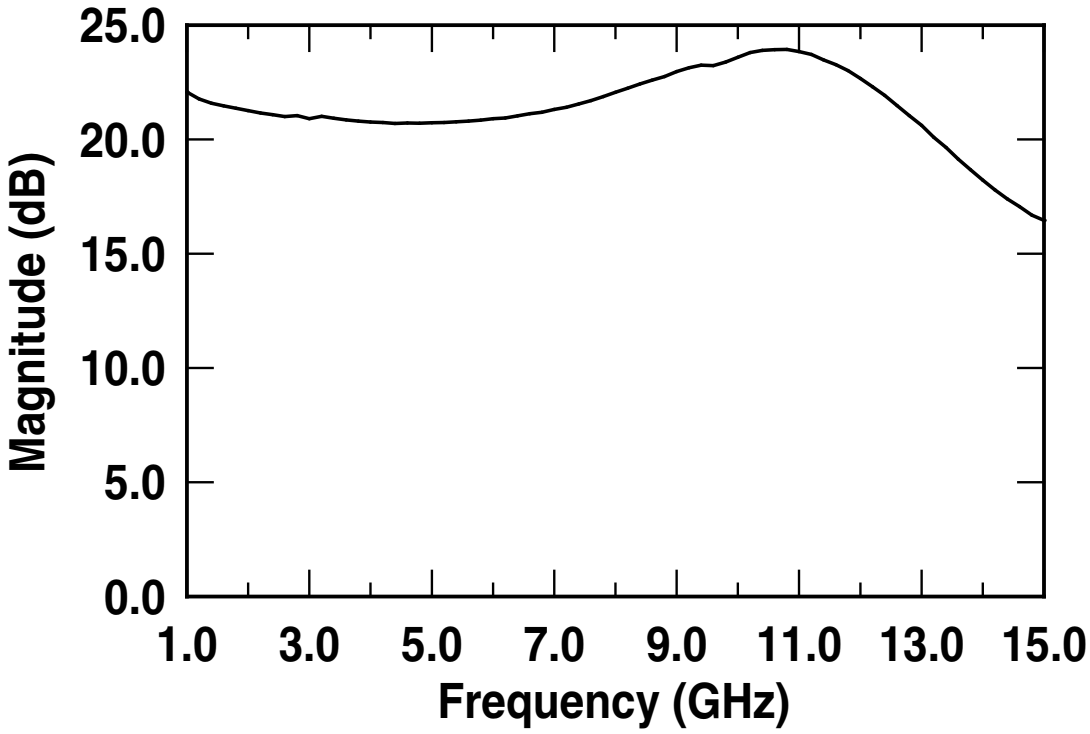


**Figure 30:** Measured $S_{21}$ of the SiGe UWB LNA 3.

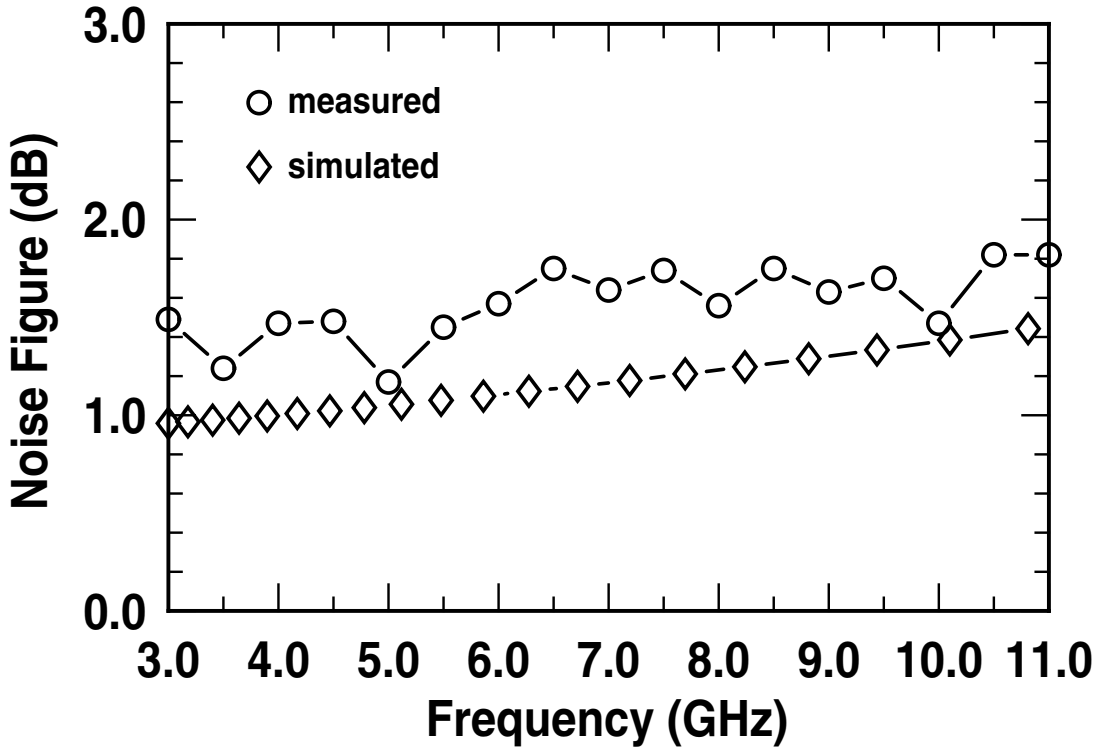


**Figure 31:** Measured and simulated noise figure of the SiGe UWB LNA 3.

The measurement and simulation results for the UWB LNA 3 are summarized in Table 6.

**Table 6:** Summary of the SiGe UWB LNA 3 Characteristics.

| | Measured | Simulated |
|---|---|---|
| Bandwidth | 0.1-14.2 GHz | 0.1-16.3 GHz |
| $NF_{min}$- $NF_{max}$ | 1.17 - 1.75 dB | 0.96 - 1.39 dB |
| $Gain_{min}$ - $Gain_{max}$ | 20.7 - 23.6 dB | 21.6 - 23.3 dB |
| $S_{11}$ | < -12.6 dB | < -12.8 dB |
| $S_{22}$ | < -16.6 dB | < -29.2 dB |
| $S_{12}$ | < -58 dB | < -51.0 dB |
| IIP3(at 6 GHz) | -3.6 dBm | -7.5 dBm |
| Power supply | 3.3 V | 3.3 V |
| Power consumption (without output buffer) | 32 mW | 32 mW |
| Die size | 0.86 × 0.95 mm$^2$ | 0.86 × 0.95 mm$^2$ |

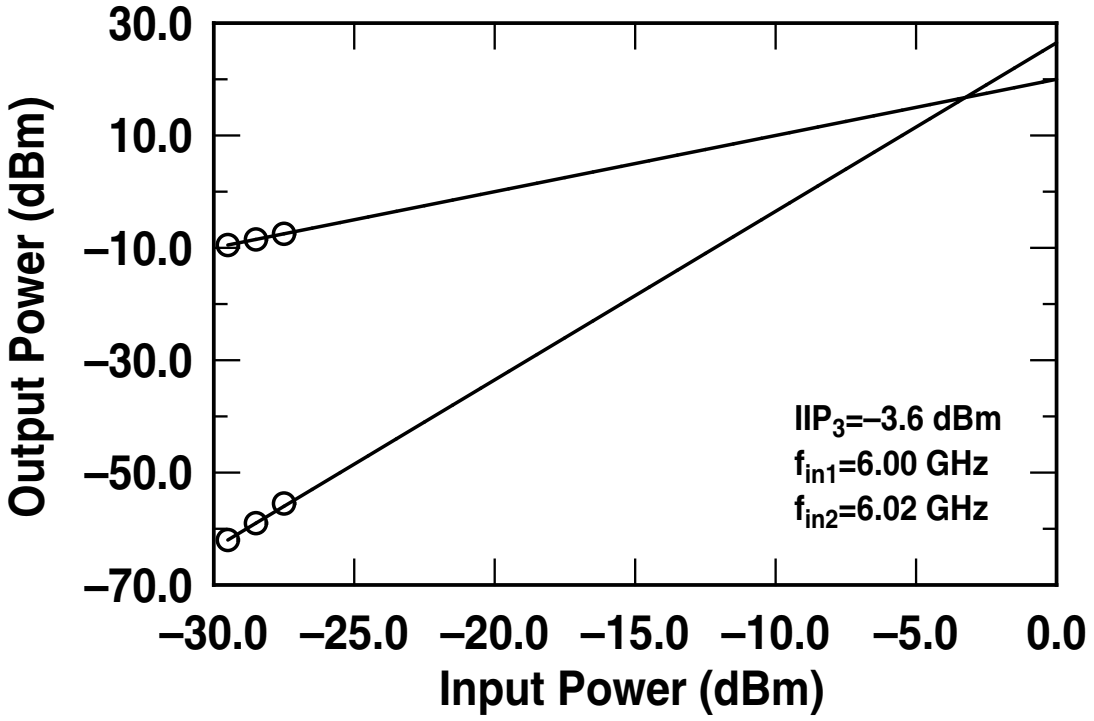


**Figure 32:** Measured IIP3 of the SiGe UWB LNA 3.

Table 7 draws a comparison between the characteristics of the three UWB LNAs reported in this work and those of other published Si/SiGe UWB LNAs. Based on this comparison, the proposed UWB LNAs have the lowest noise figure achieved to date in Si technology.

## *2.11 Summary*

High-performance wideband SiGe HBT LNAs for use in UWB systems have been presented here. The use of increased base-emitter capacitance and weak shunt resistive feedback in a cascode amplifier with inductive degeneration significantly improves the bandwidth of the LNA, and simultaneously achieves a very low noise figure. Design strategies for this UWB LNA and comparisons to other topologies have been discussed. The proposed UWB LNAs have the best wideband noise performance of all reported other state-of-the-art UWB LNAs, exhibiting the lowest noise figures across the entire 3-10 GHz bandwidth.

**Table 7:** Comparison with Published Si/SiGe UWB LNAs.

| Reference | BW [GHz] | NF [dB] | $S_{11}$ [dB] | $Gain_{max}$ [dB] | $IIP_3$ [dBm] | Power [mW] | Process |
|---|---|---|---|---|---|---|---|
| [43] | 0.5-14 | 3.4-5.4[2] | <-11.0 | 10.6 | 10 | 52 | 0.18 $\mu$m CMOS |
| [44] | 0.6-22 | 4.3-6.1[3] | <-8.0 | 8.1 | - | 52 | 0.18 $\mu$m CMOS |
| [57] | 3.1-10.6 | 4.5-5.5[1] | <-7 | 10 | -4 | 5.4 | 0.35 $\mu$m CMOS |
| [45] | 3.1-14.5 | 2.7-3.9[1] | <-1.0 | 22 | -32.5 | 13.2 | 0.25 $\mu$m SOI SiGe |
| [22] | 2.3-9.2 | 4.0-9.2[1] | <-9.9 | 9.3 | -6.7 | 9 | 0.18 $\mu$m CMOS |
| [23] | 3-10 | 2.5-4.2[1] | <-9 | 21 | -1 | 30 | 0.18 $\mu$m SiGe |
| [54] | 3-10 | 3.05-4.5[1] | <-10 | 20 | -11.75 | 42.5 | 0.18 $\mu$m SiGe |
| [56] | 0.5-10 | 2.9-3.3[1] | <-7 | 13 | -7.5 | 9.6 | 0.18 $\mu$m SiGe |
| [53] | 2-4.6 | 2.3-5.2[4] | <-9 | 9.8 | -7 | 12.6 | 0.18 $\mu$m CMOS |
| [58] | 3.1-10.6 | 2.07-2.93 | <-9.9 | 16.5 | -8.5 - -5.1 | 9 | 0.13 $\mu$m CMOS |
| [60] | 1.3-12.3 | 4.6-5.5 | <-10 | 8.2 | 7.6-9.1 | 4.5 | 0.18 $\mu$m CMOS |
| [61] | 3.1-10.6 | 4.7-5.6 | <-11.2 | 12.02 | -12.0 - -10.6 | 10.57 | 0.18 $\mu$m CMOS |
| [62] | 3.1-10.6 | 2.8-4.7 | <-12 | 21 | -8 | 29.7 | 0.25 $\mu$m SiGe |
| LNA 1 [59] | 0.1-13.6 | 1.8-3.1[1] | <-7.2 | 20.3 | 2.1[5] | 25.7 | 0.18 $\mu$m SiGe |
| LNA 2 | 0.1-11.2 | 1.61-2.38[1] | <-13.4 | 20.6 | -4.0[5] | 26.2 | 0.18 $\mu$m SiGe |
| LNA 3 | 0.1-14.2 | 1.17-1.75[1] | <-12.6 | 23.6 | -3.6[5] | 32 | 0.13 $\mu$m SiGe |

[1]*3-10 GHz,* [2]*0.5-14 GHz,* [3]*0.6-18 GHz,* [4]*3-5 GHz,* [5]*with 6.0 and 6.02 GHz input frequencies*

# CHAPTER III

# TRACK-AND-HOLD AMPLIFIER

## *3.1 Introduction*

The demand for high-speed and high-resolution analog-to-digital converters (ADC) is driven by the continuing evolution of wireless communications systems. With the increase in the performance of DSP circuits, numerous advantages can be achieved by digitizing RF analog signals early-on in the transceiver path [18]. Substantial cost savings and power reductions can then be realized as more functions are processed in the digital domain [18]. Thus, high-speed ADCs that also possess high resolution are essential to enable this paradigm-shift in design methodology [18]. The track-and-hold amplifier (THA) is a crucial circuit block in ADCs and is usually a bottleneck of in high-performance ADCs because the errors introduced by the THA cannot be corrected by subsequent stages [63].

The design of a track-and-hold amplifier is challenging because it is necessary to consider sampling rate, bandwidth, linearity, noise, droop rate, hold-mode feed-through, voltage swing, power supply voltage, and power consumption. Obviously, the highest performance for all of these targets cannot be achieved simultaneously. For instance, a wide bandwidth requires small hold capacitance and high current; a low droop rate requires a large hold capacitor; high linearity requires a small hold capacitor, while a low kT/C noise requires a large hold capacitor; a high slew rate requires a small hold capacitor and high current. Clearly many of these requirements work against each other and trade-offs have to be made to achieve the highest possible performance for a given ADC application. This chapter reports the design of an 8-bit THA with the highest possible sampling rate and bandwidth that operates off a reasonably low power supply voltage for SDR and UWB applications.

To achieve high-speed operation, an open-loop architecture is preferred over a closed-loop architecture because the latter has a global feedback that will inevitably decrease the speed in order to meet the stability and settling requirements [63]. One popular open-loop THA architecture employs a (bipolar-based) switched-emitter-follower (SEF) that can operate at very high speeds while maintaining good linearity because of the high $g_m$, high $f_T$, low leakage, and good matching properties of bipolar transistors compared with their CMOS counterparts. In this research, the design and implementation of an ultra-high-speed (> 12 GSample/sec) THA using SEF is presented. This THA was fabricated in the 0.25 $\mu$m 200 GHz SiGe HBT BiCMOS process technology from IHP. Figure 33 shows a schematic cross-section of the *npn* SiGe HBT.

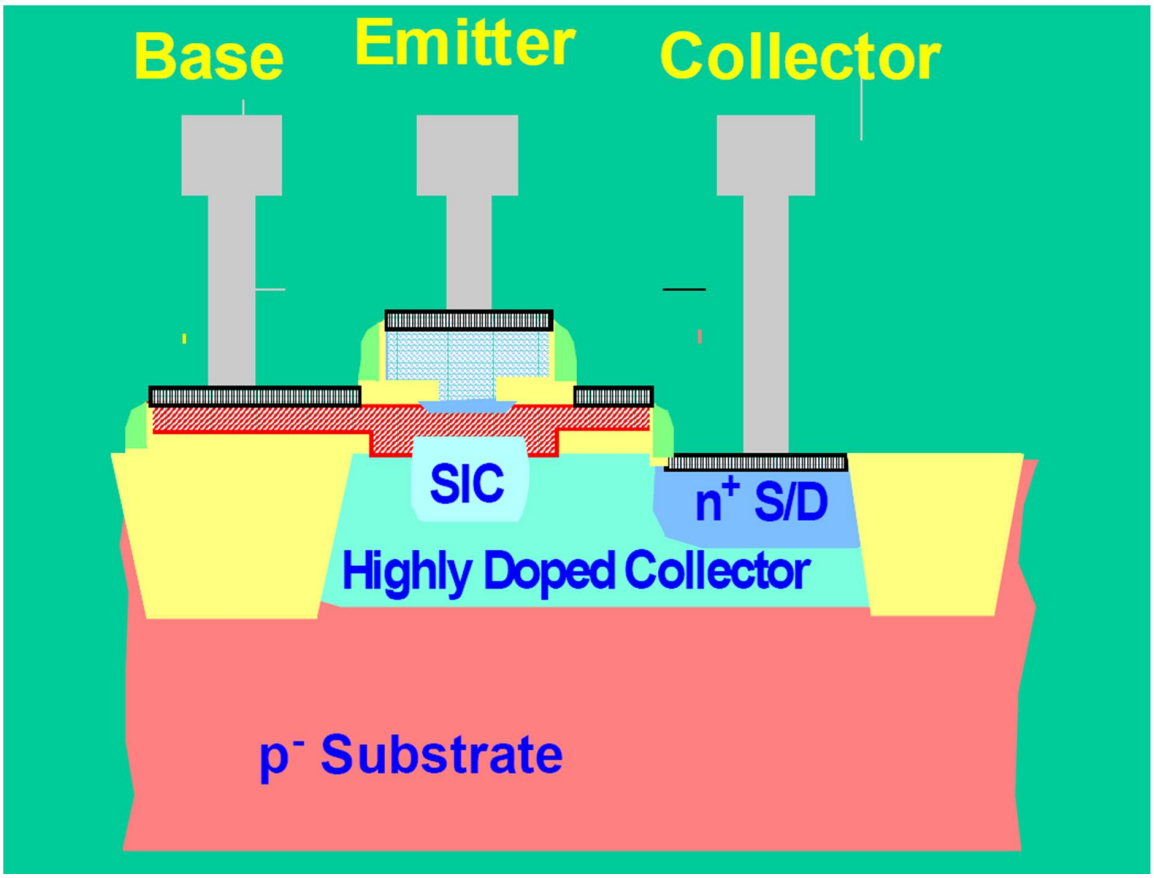


**Figure 33:** Schematic cross-section of the 200 GHz *npn* SiGe HBT.

A key feature of this SiGe HBT technology is the formation of the entire HBT structure

in a single active area with no shallow trench isolation between the active emitter and the collector contact region. This provides both low-capacitance isolation from the substrate and low collector resistances [37]. The current THA design makes use of six different geometrical variations of the SiGe HBT, ranging from the minimum emitter size (0.21×0.84 $\mu$m$^2$) to eight times the minimum emitter size. The following transistor parameters have been determined on an array of four minimum emitter size SiGe HBTs, from the same individual wafer that the THA test chips have been fabricated: peak $f_T$=190 GHz, peak $f_{max}$=190 GHz (with $V_{CE}$=1.5 V); and $BV_{CEO}$ = 2.0 V. The $f_T$ and $f_{max}$ are extrapolated from $h_{21}$ and unilateral gain ($U$), respectively, at 30 GHz using a -20 dB/decade slope at room temperature. In addition to SiGe HBTs, ASIC-compatible 2.5 V CMOS devices and a full suite of passives (including metal-insulator-metal (MIM) capacitors, polysilicon resistors, and spiral inductors) are also available.

In this chapter, the design and demonstration of an ultra-high-speed THA is presented. Section 3.2 and Section 3.3 review Volrenkamp THA and Fiocchi THA, respectively. Details of improved Fiocchi THA are described in Section 3.4. Measurement results are presented in Section 3.5, followed by a summary. This work is also published as [72].

## *3.2 Volrenkamp THA*

In a THA, the input buffer is one of the most important sub-blocks because it directly affects the overall performance of the THA. In [65], an input buffer with an emitter-degenerated differential pair and a resistor in series with a diode-connected BJT as the load, was used to improve the linearity Fig. 34.

The large-signal relationships between the input voltage and the current in the input transistor pair are given by [65]

$$\frac{V_{in}}{2} = V_T \ln \frac{\alpha I/2 + I_{out}}{\alpha I/2} + I_{out} R_1, \tag{66}$$

$$-\frac{V_{in}}{2} = V_T \ln \frac{\alpha I/2 - I_{out}}{\alpha I/2} - I_{out} R_1, \tag{67}$$

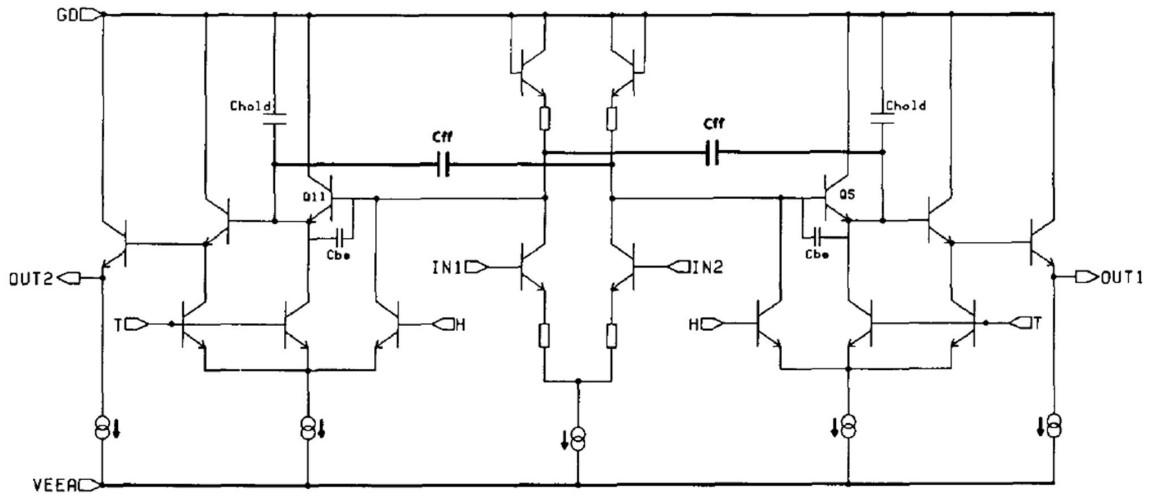


**Figure 34:** Schematic of the Vorenkamp THA (after [65]).

$$\alpha = \frac{\beta}{1+\beta}, \tag{68}$$

where $I$ is the tail current; $V_{in}$ is the input voltage; where $I$ is the output current; $\beta$ is the current gain and $V_T$ is the thermal voltage ($kT/q$), solving for $V_{in}$ [65]

$$\begin{aligned} V_{in} &= V_T \ln \frac{\alpha I/2 + I_{out}}{\alpha I/2} + I_{out} R_1 - V_T \ln \frac{\alpha I/2 - I_{out}}{\alpha I/2} - I_{out} R_1 & (69) \\ &= V_T \ln \frac{\alpha I/2 + I_{out}}{\alpha I/2 - I_{out}} + 2 I_{out} R_1. & (70) \end{aligned}$$

At the output, the load is a resistor in series with a diode [65]

$$\frac{V_{out}}{2} = V_T \ln \frac{\alpha I/2 + I_{out}}{\alpha I/2} + I_{out} R_2, \tag{71}$$

$$-\frac{V_{in}}{2} = V_T \ln \frac{\alpha I/2 - I_{out}}{\alpha I/2} - I_{out} R_1, \tag{72}$$

Hence [65]

$$V_{out} = V_T \ln \frac{\alpha I/2 + I_{out}}{\alpha I/2 - I_{out}} + 2 I_{out} R_2. \tag{73}$$

If $R_1$=$R_2$

$$V_{in} = V_{out}. \tag{74}$$

Thus the input buffer has a linear transfer function [65]. However, in a practical circuit mismatches and device second-order effects, eg., Early effects, and parasitic capacitance, will introduce distortions [65].

The hold-mode feedthrough is given by [65]

$$A_{feedthrough} = \frac{C_{be,Q5}}{C_{hold} + C_{be,Q5}}(1 - \frac{C_{FF}}{C_{be,Q5}}), \tag{75}$$

where $C_{be,Q5}$ is the base-emitter capacitance of Q5; $C_{hold}$ is the hold capacitor; $C_{FF}$ is the feed-forward capacitor. If $C_{FF} = C_{be,Q5}$, $A_{feedthrough} = 0$ [65]. Figure 35 shows the implementation of $C_{FF}$.

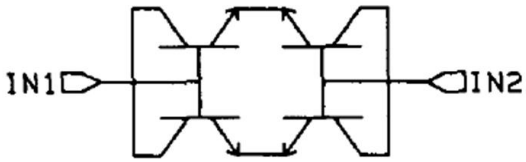


**Figure 35:** Schematics of the feed-forward capacitor $C_{FF}$ (after [65]).

This architecture, however, requires a rather high power supply voltage due to the *dc* voltage drop across the diode and resistor [66]. The operation voltage can be reduced by removing the series diode, but as a result, the linearity is significantly worse [66]. To alleviate this effect, a large current is needed, which results in higher power consumption [66].

Another drawback of [65] is that the large output impedance (time constant) of the input buffer limits the bandwidth and degrades the settling time [66]. For the above reasons, the design in [65] is not favorable for low-voltage, high-speed ADCs [66].

## *3.3 Fiocchi THA*

Fiocchi, *et al.* [66], proposed a novel THA implemented in standard Si BiCMOS technology was proposed, which is shown in Fig. 36.

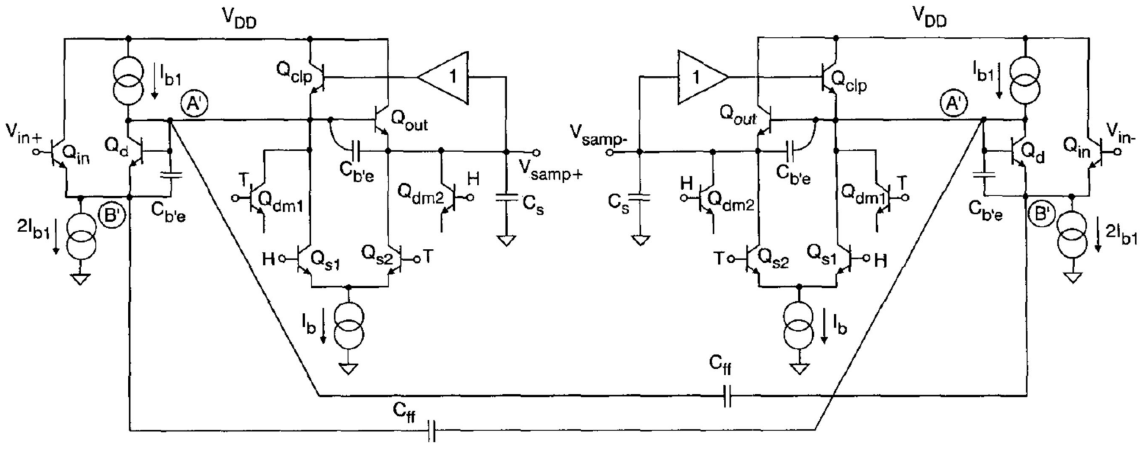


**Figure 36:** Schematics of the Fiocchi THA (after [66]).

The input buffer of this THA features a *npn* BJT differential amplifier with a pMOS current source load in a unit feedback configuration [66]. Because of the high open-loop gain due to the high transconductance of the BJT, this THA design can achieve high linearity with a lower voltage supply [67]. On the other hand, because the output resistance is only $1/g_m$, which is much smaller than in [65], the time constant is reduced so that the bandwidth of the input buffer is improved [67]. Because of the parasitic capacitance of the pMOS transistor, however, the effective output impedance of the pMOS current source decreases as the frequency increases [67]. As a result, both the linearity and the bandwidth are degraded. To address this problem, an adaptive-biased input buffer was proposed in [67], but the input signal is still limited to relatively low frequencies of around several hundred MHz [67].

## *3.4 Improved Fiocchi THA*

Based on [66] and [67], an improved version of the pseudo-differential track-and-hold amplifier is implemented in the present work in 0.25 $\mu$m 200 GHz SiGe HBT BiCMOS technology. Figure 37 shows the block diagram for this THA design.

Two input buffers are used in the present THA design [67]. The main input buffer,

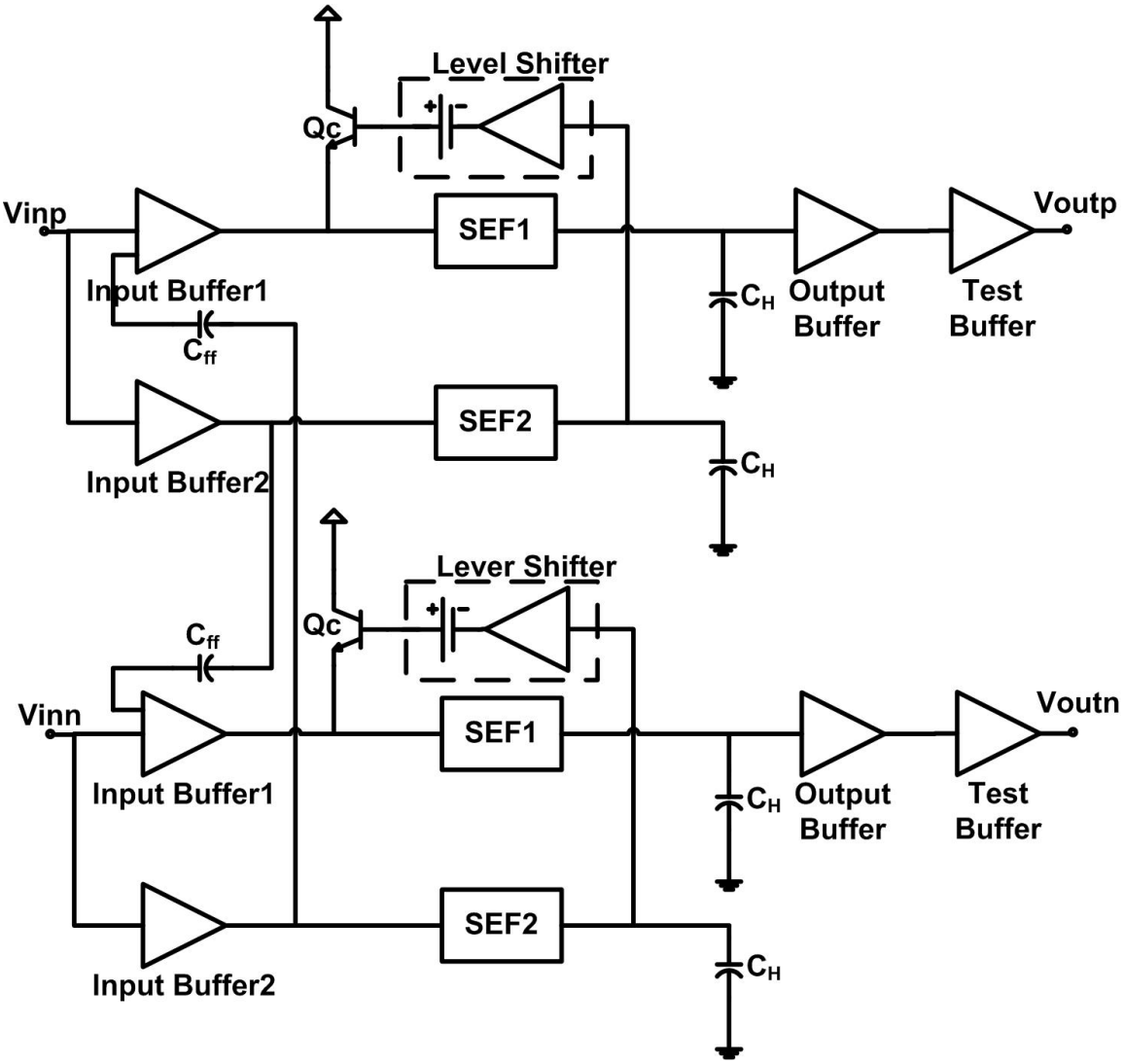


**Figure 37:** Block diagram of the 8-b 12-GSample/sec THA.

*Buffer1* in Fig. 37, provides the analog signal for the main switch *SEF1*, while *Buffer2* provides a replica signal for the auxiliary switch *SEF2* in order to prevent capacitively loading the output of *Buffer1* [67]. To improve the output impedance of the pMOS current source at high frequency, a degeneration inductor is used [68]. Figure 38 shows the schematic of the proposed input buffer.

The output impedance of the input buffer with inductor degeneration is

$$r_{out} = \frac{r_d + j\omega L_s(1 + r_d g_m)}{1 - \omega^2 L_s C_p - \omega^2 L_s C_p r_d g_m + j\omega C_p r_d}, \tag{76}$$

while the normal input buffer in [66] is

$$r_{out} = \frac{r_d}{1 + j\omega C_p r_d}, \tag{77}$$

where $L_s$ is the degeneration inductance, $C_p$ is the parasitic capacitance at the output, and $g_m$ and $r_d$ are the transconductance and output resistance of M2, respectively. Figure 39 shows the calculated output impedance as a function of input frequency. It is clear that at frequencies higher than 0.6 GHz, the output impedance of the current source is significantly improved by the degeneration inductor.

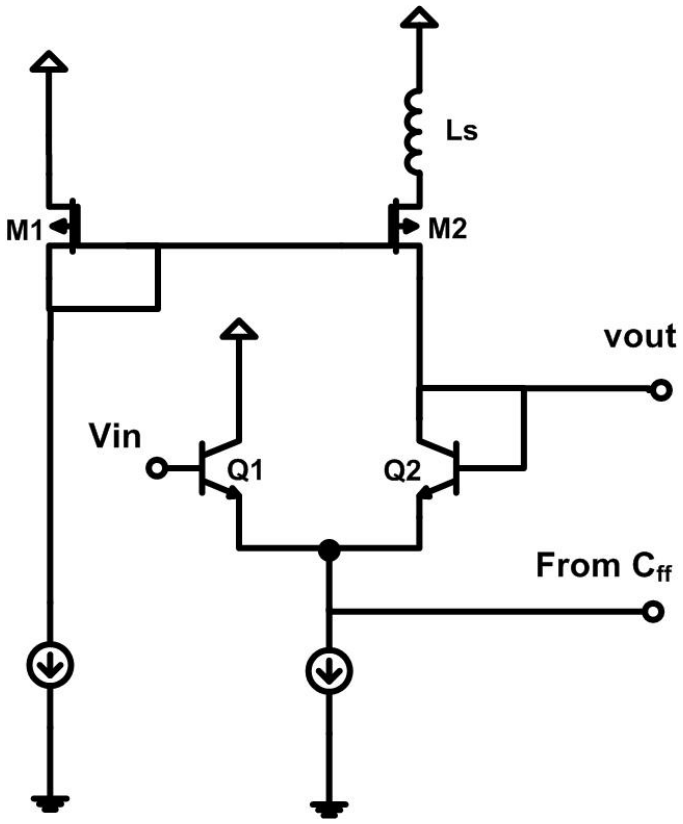


**Figure 38:** Schematic of the proposed high-performance input buffer .

Figure 40 shows a schematic of the SEF and the level shifter. When the clock at node $T$ is high, the THA is in track mode. When the clock at node $H$ is high, the transistor Q2 is off and the THA is in hold mode, during which the capacitor $C_H$ maintains the sampled voltage. Transistor $Q_c$ functions as a clamp to prevent transistor Q2 of the input buffer

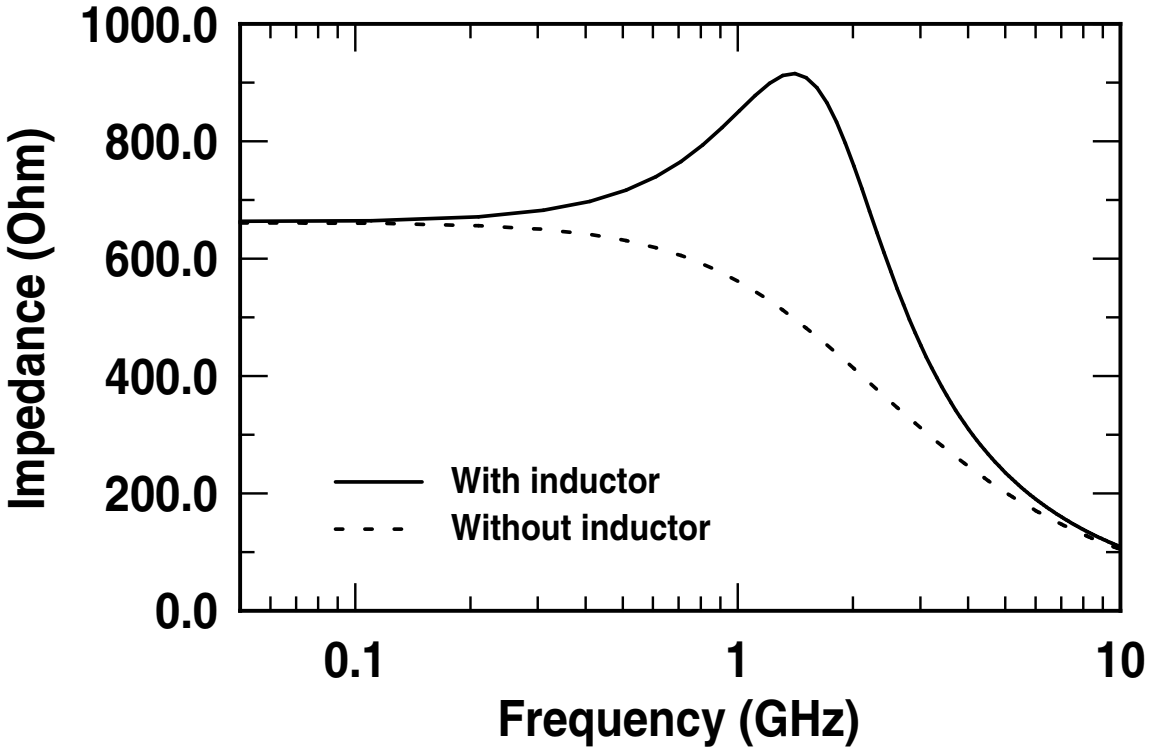


**Figure 39:** Calculated output impedance of the input buffer as a function of frequency.

in Fig. 38 from entering into saturation during hold mode. Transistor $Q_c$ is biased by a replica signal generated from the auxiliary switch *SEF2* and level shifted by a $V_{BE}$ [66]. In track mode, the transistor $Q_c$ is off because the $V_{BE}$ is very small. In hold mode, the base voltage is a constant voltage provided by the hold capacitor $C_H$ in the auxiliary *SEF2* [66]. Thus, this architecture provides good isolation between input and output, resulting in a reduction in the hold-mode feedthrough [66]. To further suppress hold-mode feedthrough, a compensation capacitor $C_{ff}$ is also included [65]. Two dummy transistors, Q5 and Q6, are used to minimize the pedestal error caused by charge injection [66]. Figure 41 shows the schematic of the clock buffer.

As shown in Fig. 42, the output buffer uses a pMOS current mirror to improve the droop rate by compensating for the base current [66]. The test buffer is matched to 50 Ω. In order to achieve higher linearity, the 50 Ω testing buffer is operated with a larger supply voltage.

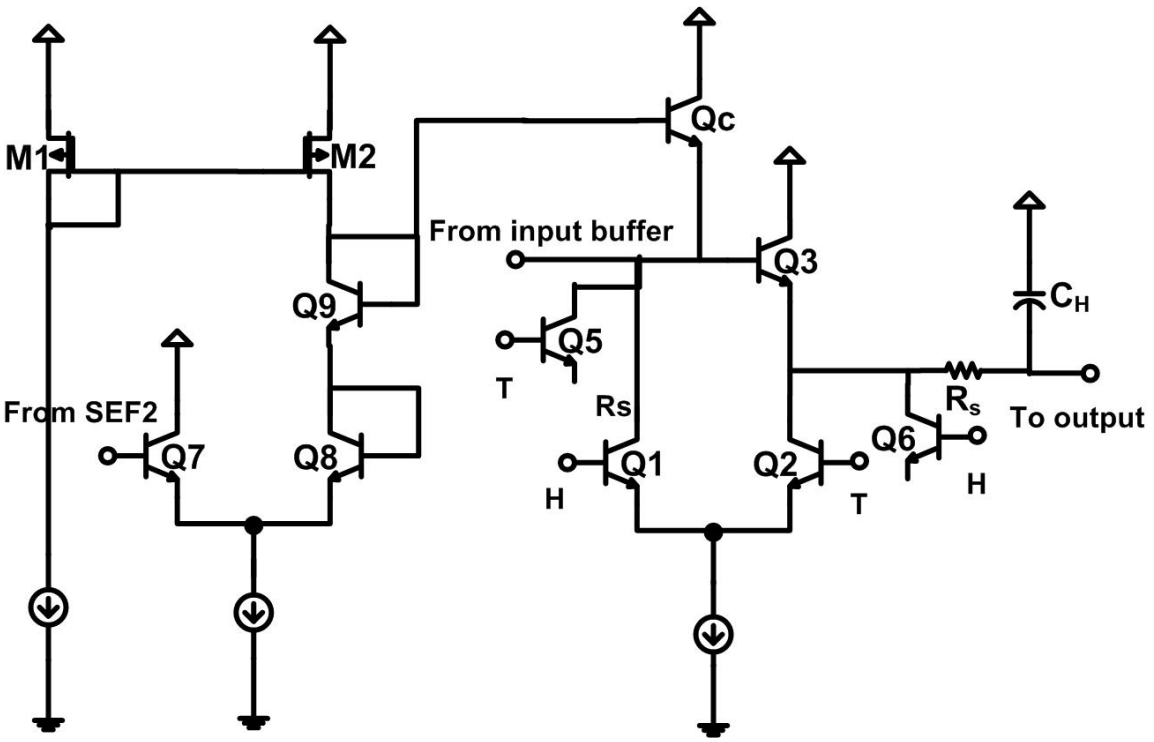


**Figure 40:** Schematic of the switched-emitter-follower and the level shifter.

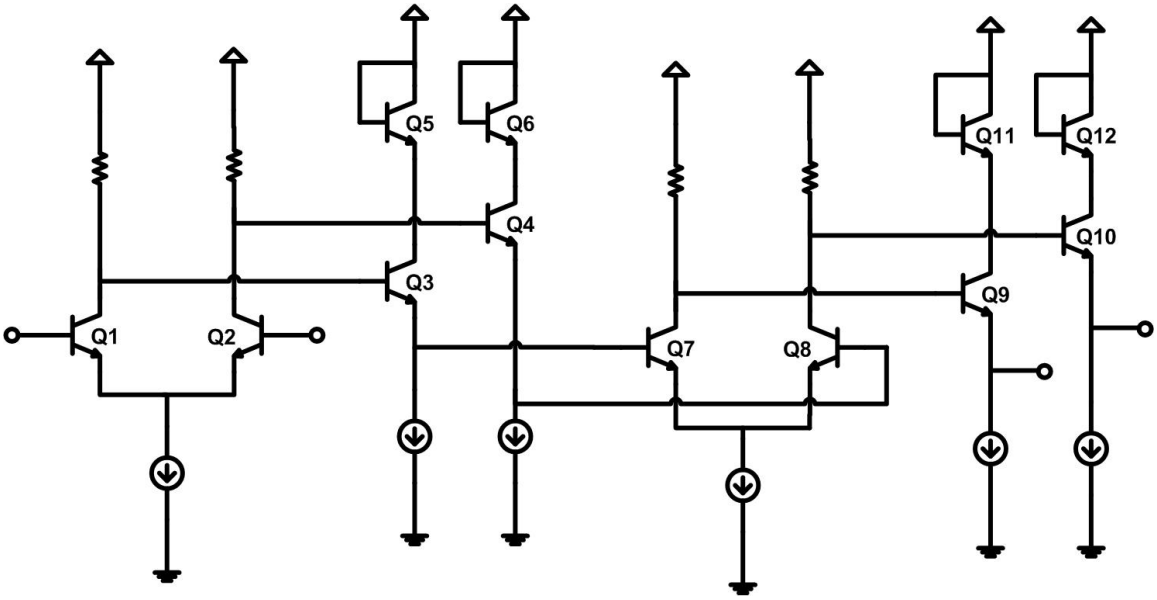


**Figure 41:** Schematic of the clock buffer.

## *3.5 Measurement Results*

The THA was implemented in a commercially available 0.25 $\mu$m 200 GHz SiGe HBT BiCMOS technology [37] and occupies an area of 1.0×1.2 mm$^2$, including bondpads. The

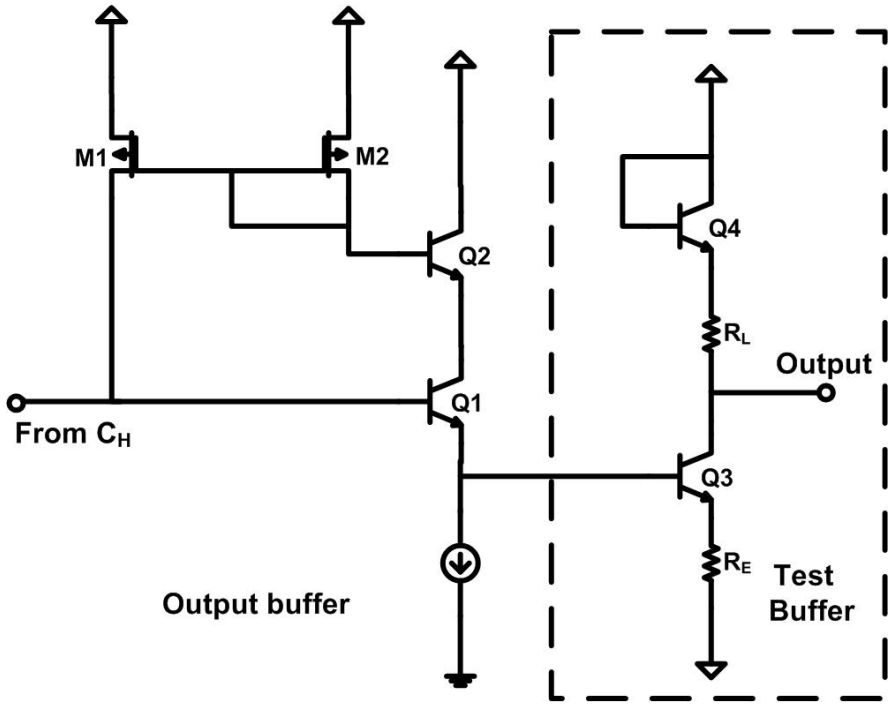


**Figure 42:** Schematic of the output buffer and 50 Ω test buffer.

chip micrograph is shown in Fig. 43. The THA was tested on-wafer using 40 GHz probes and cables. Special attention was paid to maintaining symmetrical signal paths because any asymmetry caused by the external testing components (e.g., hybrids, cables, and probes) introduces parasitic non-linearity and degrades the performance of the THA dramatically at high frequencies. In the current setup, well-matched components were chosen and adjustable phase adapters used to compensate for the different signal lengths.

Figure 44 shows the time-domain measurement results at $f_s$ of 12.0 GHz with $f_{in}$ of 1.5 GHz. With $f_{in}$ of 1.5 GHz, the total harmonic distortion (THD) as a function of the sampling frequency is shown in Fig. 47. Based on the results shown in Fig. 47, this THA is capable of an 8-bit resolution operating above 12-GSample/sec with $f_{in}$ of 1.5 GHz and 1 $V_{pp}$ input signal.

Figure 45 shows the spectrum of the output signal with $f_s$ of 12.5 GHz and $f_{in}$ of 1.5 GHz. The third harmonic distortion is -54.0 dBc. Figure 46 shows the spectrum of the output signal with $f_s$ of 12.5 GHz and $f_{in}$ of 3.0 GHz. The second, third, and total

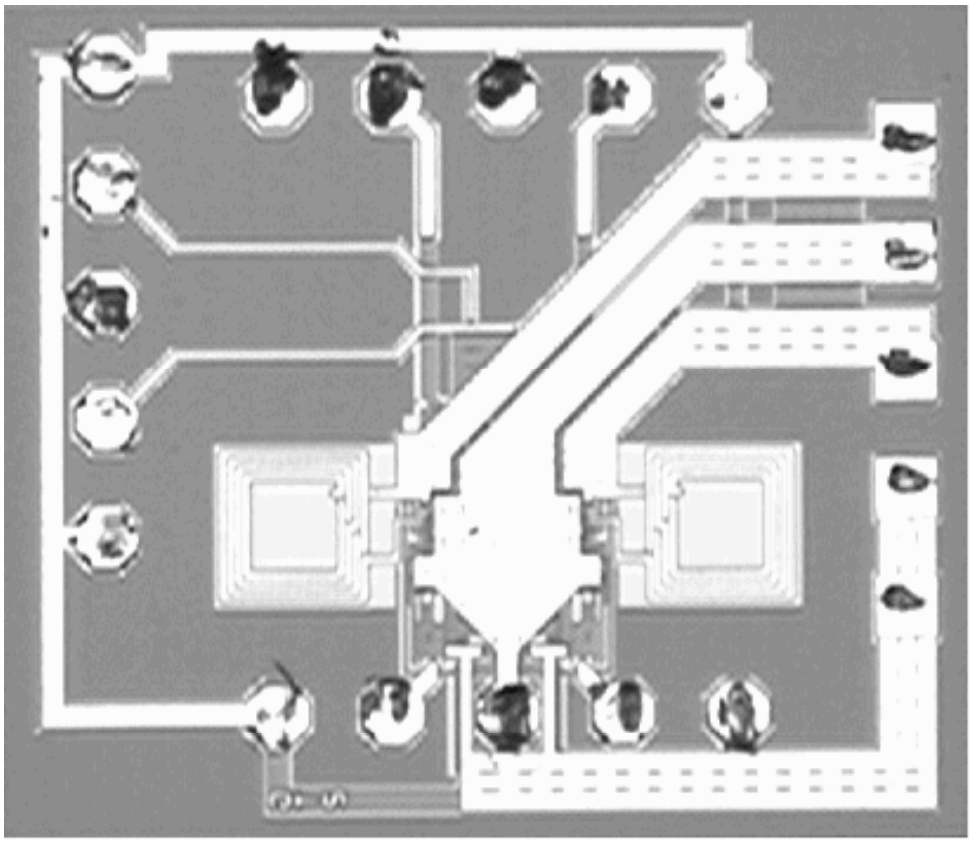

**Figure 43:** Chip micrograph of the 8-b 12-GSample/s SiGe THA.

harmonic distortion are -52.0 dBc, -53.1dBc, and -49.5 dBc, respectively, resulting in an ENOB of 7.93 bits. The measurement results of the THA are summarized in Table 8.

The highest sampling rate is limited by the settling time and the slew rate (charging and discharging capacitors). The droop current limits the lowest sampling rate, and thus determines the longest time the capacitor can hold the signal voltage below a certain error. Thus, there is an optimum sampling rate that maximizes th THA performance. From Fig. 47, the THA has its lowest 3rd order harmonic distortion, -61.0 dBc, around 4 Gsample/sec.

In addition to the parasitic non-linearity introduced by the imperfections of the external test components, the non-linearity during the transition from hold-mode to track-mode is also inherently included in the THD data, while for real ADC applications only the accuracy of the hold value is of interest. Thus, the measured performance of the SiGe THA may actually be underestimated. On the other hand, additional sources of error such as clock

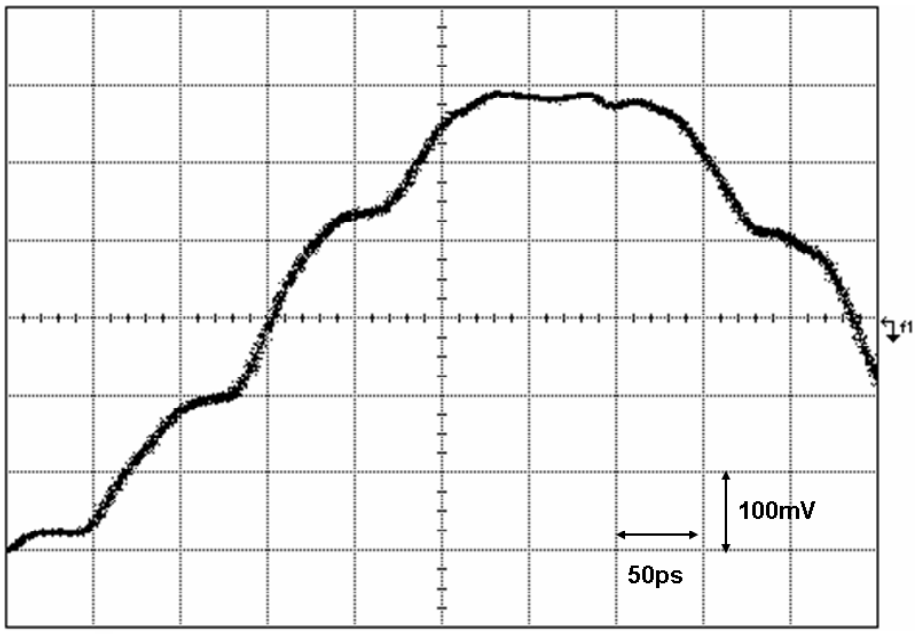


**Figure 44:** Measured output waveform at 12-GSample/sec with a 1.5 GHz input frequency.

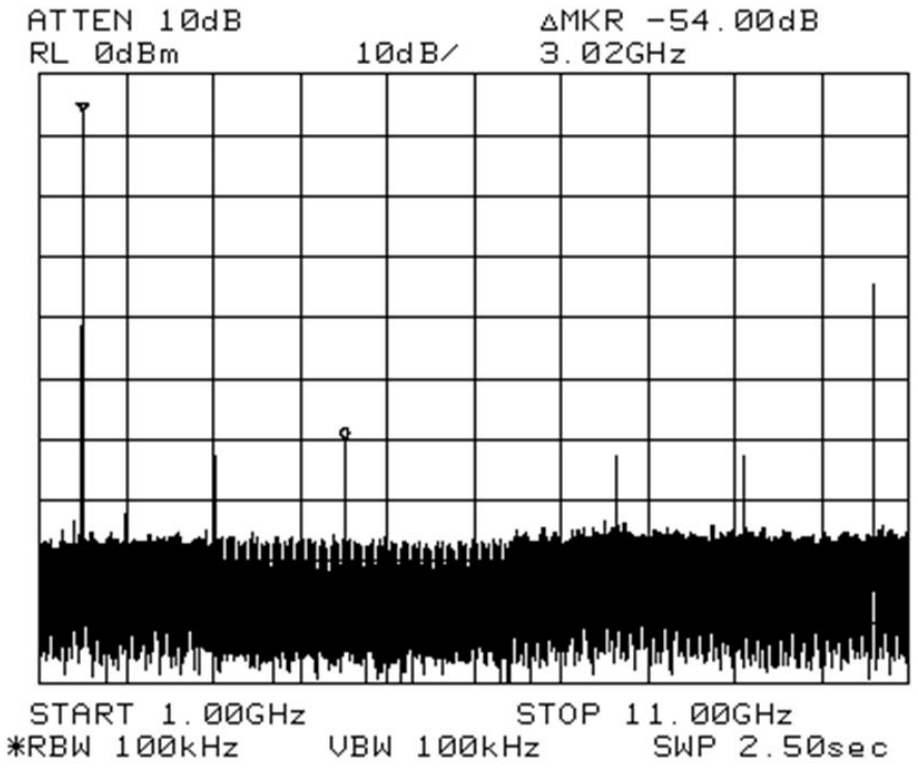


**Figure 45:** Measured output spectrum with 12.5-GSample/sec and a 1.5 GHz input frequency.

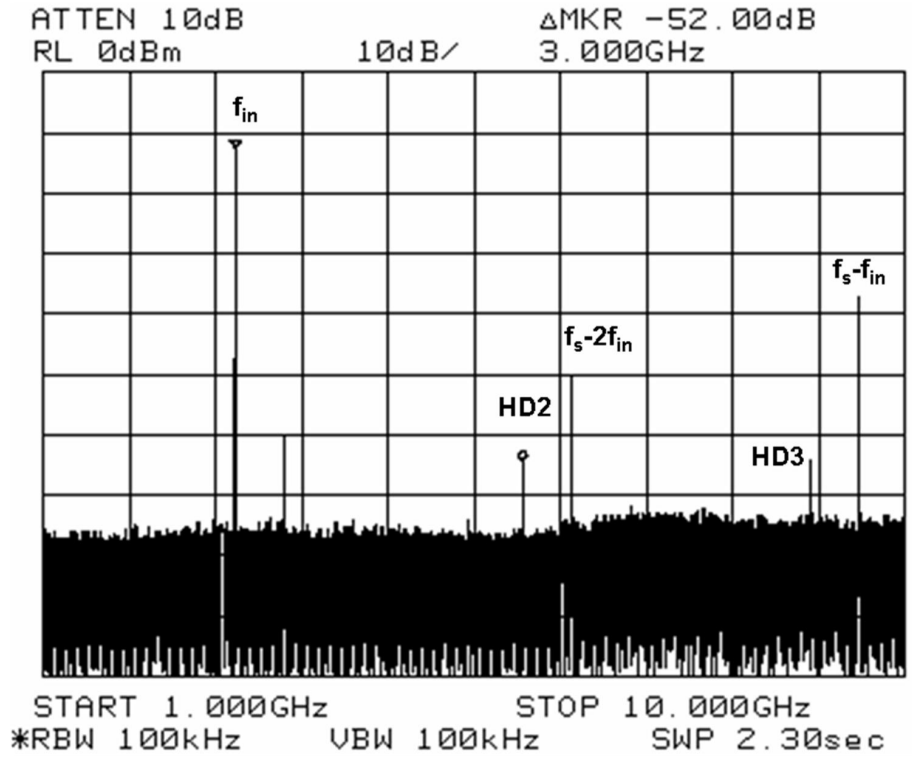


**Figure 46:** Measured output spectrum with 12.5-GSample/sec and a 3.0 GHz input frequency.

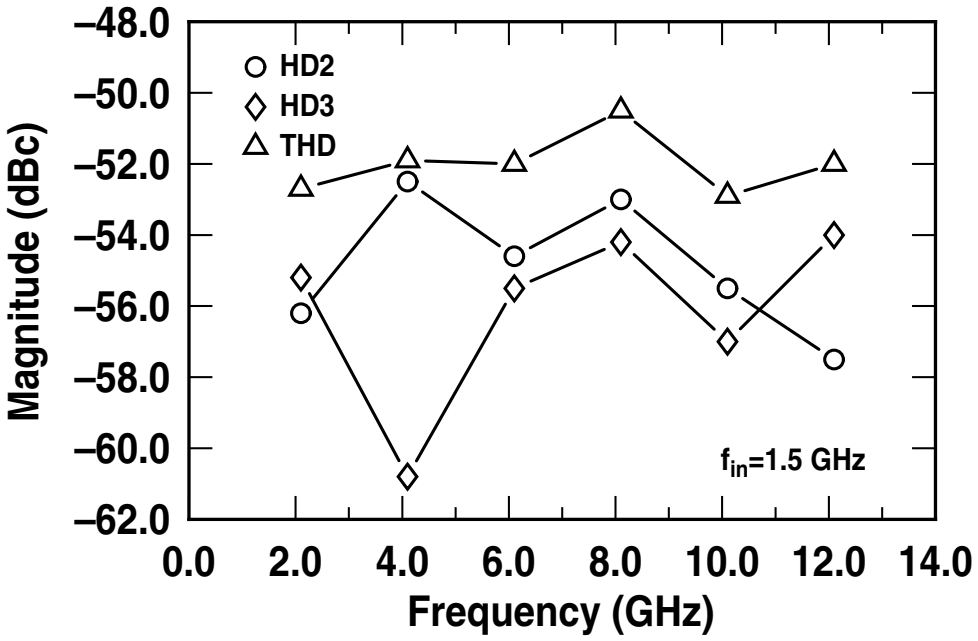


**Figure 47:** Output harmonic distortion as a function of sampling frequency.

jitter may further limit the THA performance. Furthermore, according to the simulation results, the 50 Ω buffer degrades the overall performance of the THA, while in ADCs the THA is an internal building block and need not be matched to 50 Ω. A comparison of this THA to other published Si/SiGe THAs is given in Table 9. Based on this comparison, the present THA is the fastest 8-bit Si-based THA achieved to date.

**Table 8:** Summary of the SiGe THA Characteristics.

| | |
|---|---|
| THD at $f_s$= 12.1 GHz, $f_{in}$= 1.5 GHz | -52.4 dBc |
| THD at $f_s$= 12.5 GHz, $f_{in}$= 3.0 GHz | -49.5 dBc |
| Bandwidth (3dB) | 5.5 GHz |
| Pedestal error | < 5 mV |
| Droop rate (differential) | < 5 mV/ns |
| Power supply | 3.5 V |
| Power consumption (with clock and test buffer) | 0.7 W |
| Die size | 1.2 $mm^2$ |

**Table 9:** Comparison with Published Si/SiGe High-Speed Track-and-Hold Amplifiers.

| Reference | $f_{sample}$ [GHz] | $f_{in}$ [GHz] | Input [$V_{pp}$] | ENOB [bit] | BW [GHz] | Supply [V] | $P_{diss}$ [W] | Process/$f_T$ [/GHz] |
|---|---|---|---|---|---|---|---|---|
| [30] | 10.0 | 10.0 | 1.0 | 5 | 16.0 | -3.7 | - | SiGe/120 |
| [68] | 4.0 | 8.0 | 0.6 | 6 | 10.0 | 5.2 | 0.55 | SiGe/45 |
| [70] | 1.2 | 0.6 | 1.0 | 8 | 2.0 | +2.0/-5.0 | 0.46 | Si/25 |
| [71] | 2.0 | 0.9 | 0.8 | 8 | 0.9 | -3.3 | 0.55 | SiGe/65 |
| [69] | 1.0 | 0.5 | 1.0 | 10 | - | -5.2 | 0.35 | Si/25 |
| This work | 12.1 | 1.5 | 1.0 | 8 | 5.5 | 3.5 | 0.70 | SiGe/200 |

## *3.6 Summary*

An ultra-high-speed SiGe HBT BiCMOS THA has been presented in this chapter that incorporates. a degeneration inductor in the input buffer and thus significantly improves the performance of the THA. Compared with other state-of-the-art THAs, the realized THA is the fastest 8-bit Si-based THA yet reported.

# CHAPTER IV

# TRANSCONDUCTANCE-C LOW-PASS FILTER

## *4.1 Introduction*

As the data transfer rates of recording devices (e.g., DVDs and hard-disk drives) continue to increase, very high-speed analog filters are required for the front-end electronics [73]. In addition, ultra-wideband (UWB) wireless technology that is capable of transmitting extremely low power signals at very high data rates requires high-frequency anti-alias filters before the signals can be digitized by analog-to-digital converters (ADCs) [77]. The integrated filters for such applications can be implemented with on-chip passives, (i.e., capacitors and inductors), but given the frequency range of interest, which extends from several hundred MHz to several GHz, excessively large chip areas would be required. Passive filters, while attractively linear in their response, unfortunately have a very limited tuning capability and often have significant pass-band loss due to low-Q inductors, especially in Si-based technologies. For recording devices and communication channel selection applications, integrated active filters thus become an obvious alternative. Operational amplifier based filters (e.g., op amp RC filters) have higher linearity than transconductor based filters (i.e., $g_m$-$C$ filters) [75]. However, it is very difficult to achieve very high-frequency operation (above 1 GHz) with op amp based filters, mainly because of their insufficient loop gain at high frequency, which is limited by the trade-off between the gain-bandwidth and phase-margin for a multi-stage op amp [75]. Thus, to achieve maximum speed, $g_m$-$C$ filters are preferred.

In this chapter, the design and demonstration of an ultra-high-speed (4.1 GHz) $g_m$-$C$ C-SiGe active filter using Voorman transconductors is presented. The 0.25 $\mu$m C-SiGe process technology used to implement this filter is discussed in Section 4.2. Section 4.3

reviews transconductor design. Details of gyrator design and filter design are described in Section 4.4 and Section 4.5, respectively. Measurement results are presented in Section 4.6, followed by a summary. Thsi work is also published as [79].

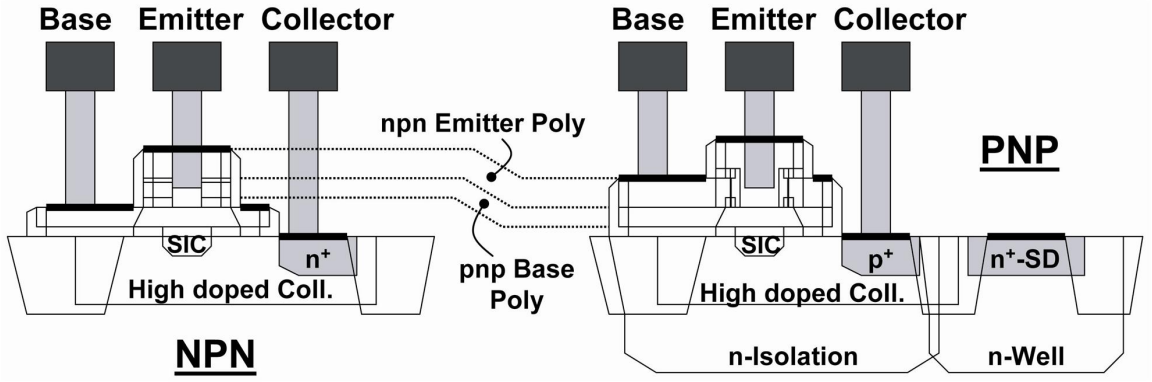


**Figure 48:** Schematic cross-section of the *npn* and *pnp* SiGe HBTs.

**Table 10:** Key Parameters of the C-SiGe Technology.

| | *npn* | *pnp* |
|---|---|---|
| $\beta$ | 200 | 100 |
| $A_{E,min}$ ($\mu$m$^2$) | 0.21×0.84 | 0.21×0.84 |
| $f_T$ (GHz) | 170 | 90 |
| $f_{max}$ (GHz) | 170 | 120 |
| $BV_{CEO}$ (V) | 1.9 | 3.1 |
| $BV_{CBO}$ (V) | 4.5 | 4.0 |
| CMOS $L_g$ ($\mu$m) | 0.25 | |
| Metal Layers | 4 | |

## *4.2 C-SiGe HBT Process Technology*

Bandgap-engineered SiGe HBTs are receiving significant attention for communications IC applications because they enable a dramatic improvement in transistor-level performance while simultaneously maintaining strict compatibility with conventional low-cost, high-integration level, high-volume CMOS manufacturing [33]. SiGe technology is evolving rapidly, and has today reached a point where SiGe HBT technology is of comparable

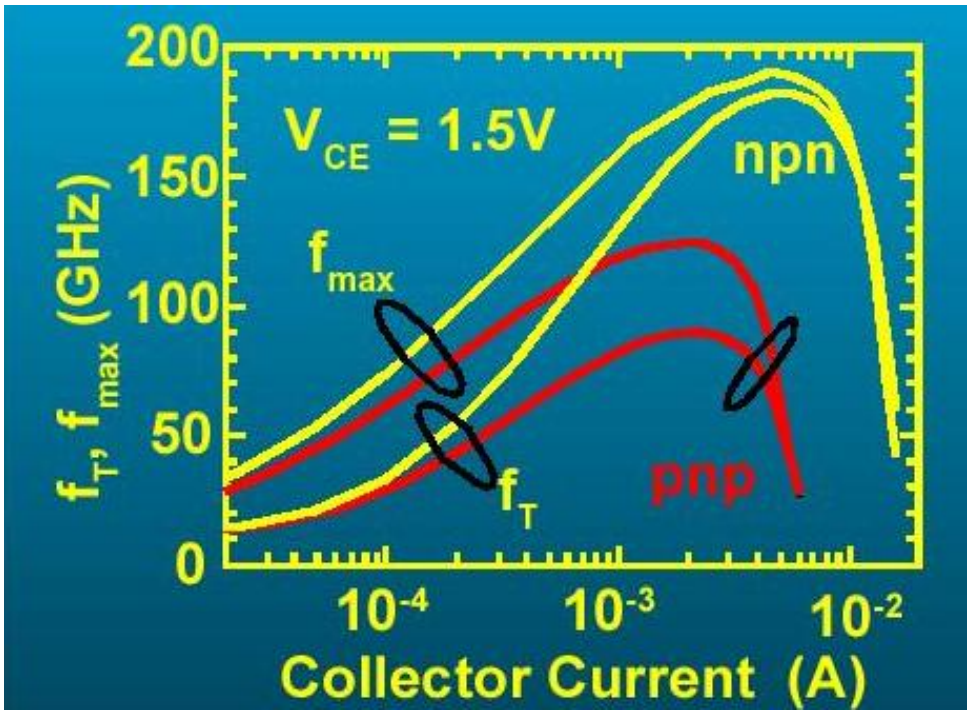


**Figure 49:** $f_T$ and $f_{max}$ vs. collector current of the *npn* and *pnp* SiGe HBTs.

performance with the best-of-breed III-V technologies. With the recent announcement of SiGe HBTs with peak cutoff frequency ($f_T$) above 300 GHz [39], and complementary (*npn* and *pnp*) SiGe HBTs with peak $f_T$ above 180 GHz and 80 GHz, respectively [40], the application space for SiGe HBT technology is now for a wide variety of analog and RF through mm-wave applications. A key feature of the present work is the use of complementary (*npn* and *pnp*) SiGe HBTs. The high performance of the *pnp* SiGe HBTs is mainly the result of a highly tuned vertical doping profile, taking full advantage of the reduced phosphorus diffusion in the carbon-doped base, combined with the special collector construction of previously reported 200 GHz *npn* transistors [40]. In this C-SiGe technology, the formation of the entire SiGe HBT structure is made in one active area, without shallow trench isolation between the active emitter and the collector contact regions. This provides low-capacitance isolation from the substrate and low collector resistances [37]. Figure 48 shows a schematic cross-section of these *npn* and *pnp* transistors.

The current filter design makes use of six different geometrical variations of SiGe

HBTs, ranging from the minimum emitter size (0.21×0.84 $\mu m^2$) to eight times of the minimum emitter size. The following transistor parameters have been determined on an array of four minimum emitter size SiGe HBTs from the same wafer the filter test chips are fabricated on: peak $f_T$=170 GHz and peak $f_{max}$=170 GHz (with $BV_{CEO}$=1.9 V), for the *npn* SiGe HBTs; peak $f_T$=90 GHz, and peak $f_{max}$=120 GHz (with $BV_{CEO}$=3.1 V), for the *pnp* SiGe HBTs. The $f_T$ and $f_{max}$ were extrapolated from $h_{21}$ and the unilateral gain ($U$), respectively, at 30 GHz using a -20 dB/decade slope at room temperature. In addition to the C-SiGe HBTs, ASIC compatible 2.5 V CMOS devices, and a full suite of passives (including metal-insulator-metal (MIM) capacitors, polysilicon resistors, and spiral inductors) are also available in this technology platform. Table 10 summarizes the key parameters of this C-SiGe technology.

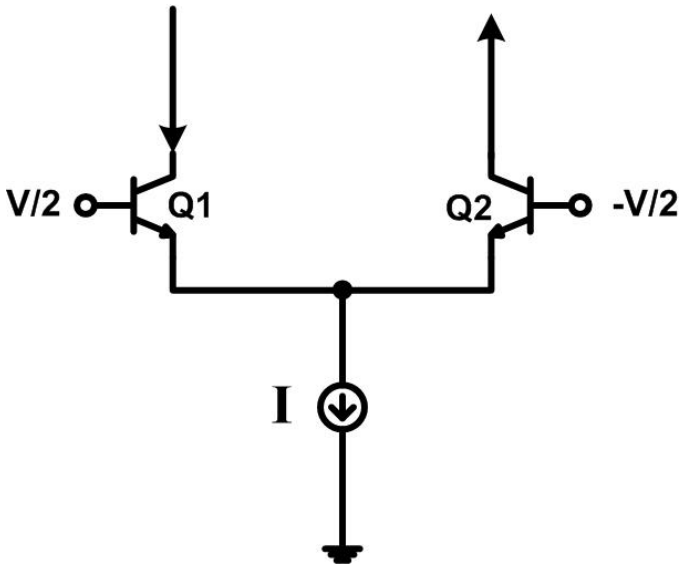


**Figure 50:** Schematic of the differential pair.

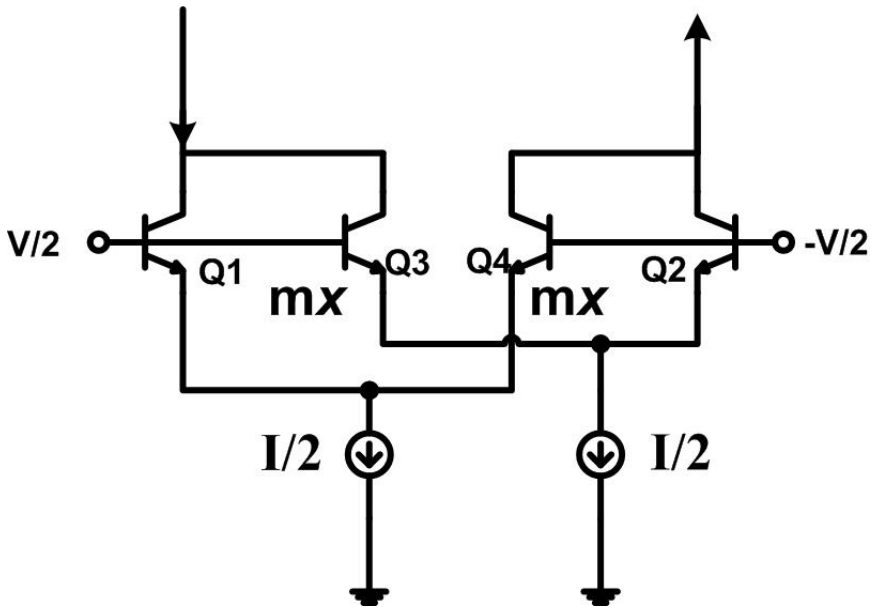


**Figure 51:** Schematic of the Schmoock transconductor.

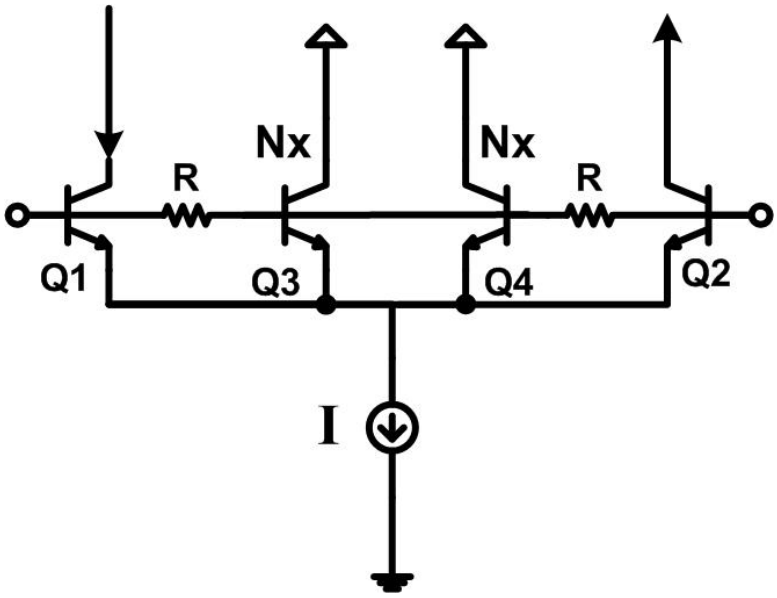


**Figure 52:** Schematic of the Voorman transconductor.

## *4.3 Transconductor Design*

### 4.3.1 Differential Pair

In a simple differential pair, shown in Fig. 50, the large-signal currents in Q1 and Q2 are [64]

$$I_{C1} = I_S \exp\left(\frac{V_{BE} + V/2}{63 \quad V_T}\right), \tag{78}$$

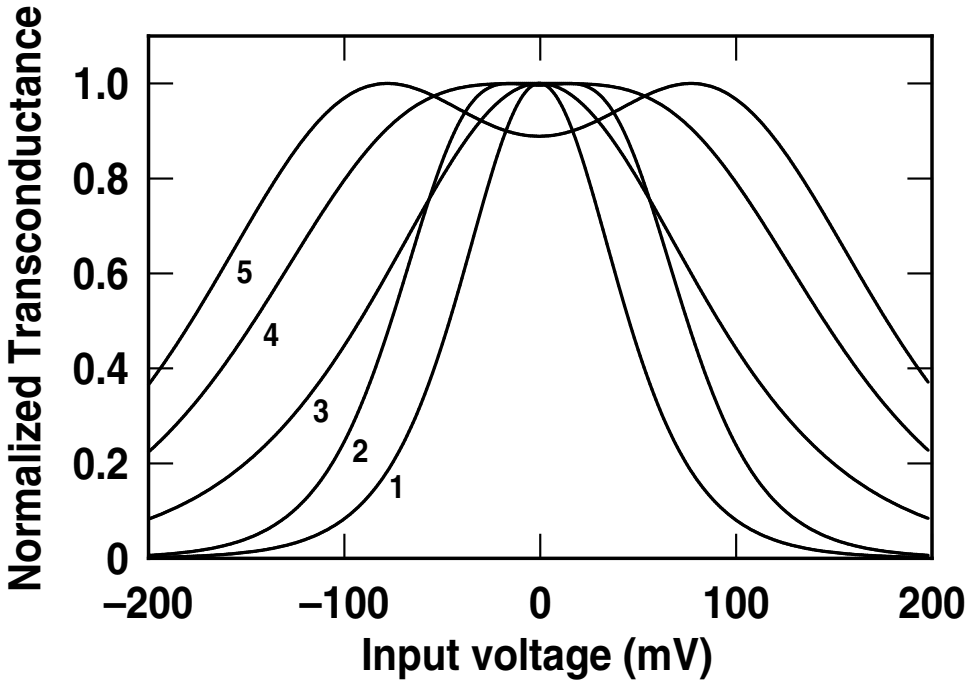


**Figure 53:** Theoretical normalized transconductance ($g_m/g_{m,max}$) as a function of the input voltage.

$$I_{C2} = I_S \exp\left(\frac{V_{BE} - V/2}{V_T}\right), \tag{79}$$

$$\alpha I = I_{C1} + I_{C2}, \tag{80}$$

$$\alpha = \frac{\beta}{1+\beta}, \tag{81}$$

where $I_{C1}$ and $I_{C2}$ are the collector currents of transistors $Q_1$ and $Q_2$, respectively; $I$ is the tail current; $V$ is the input voltage; $V_{BE}$ is the DC bias voltage; $I_S$ is a constant; $\beta$ is the current gain and $V_T$ is the thermal voltage ($kT/q$). Solving for $I_{C1}$ and $I_{C2}$

$$I_{C1} = \frac{\alpha I}{1 + \exp\left(-\frac{V}{V_T}\right)}, \tag{82}$$

$$I_{C2} = \frac{\alpha I}{1 + \exp\left(\frac{V}{V_T}\right)}. \tag{83}$$

The total output current $I_{out}$ can be found as [64]

$$I_{out} = \frac{I_{C1} - I_{C2}}{2} \tag{84}$$

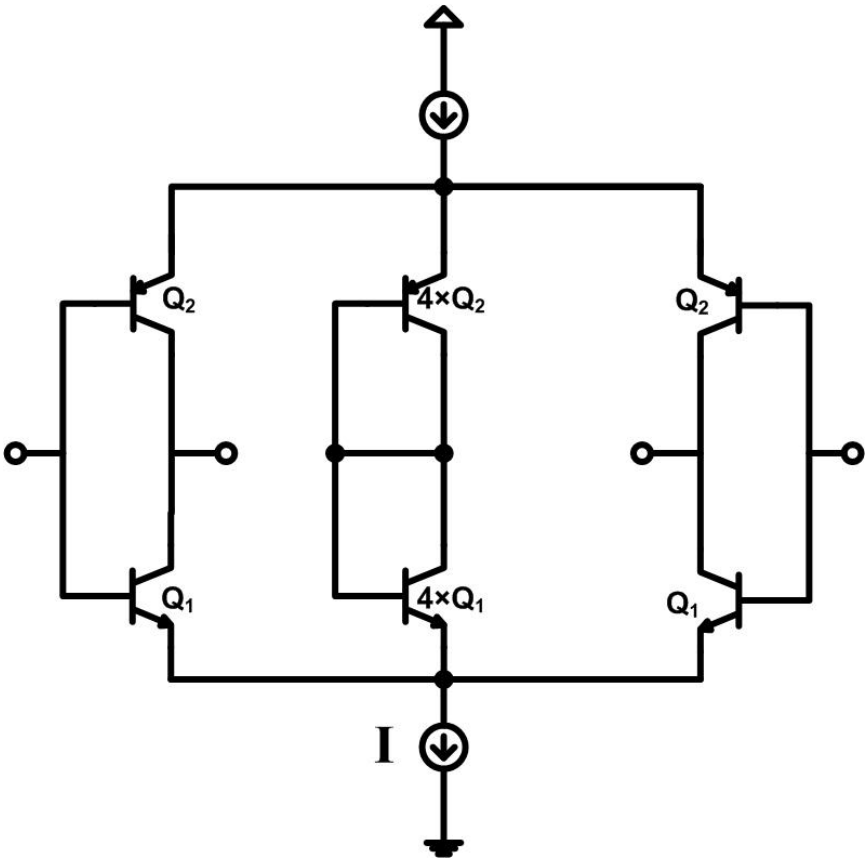


**Figure 54:** Schematic of the complementary Voorman transconductor used here.

$$= \frac{\alpha I}{2}[\frac{1}{1+\exp(-\frac{V}{V_T})} - \frac{1}{1+\exp(\frac{V}{V_T})}]. \tag{85}$$

$$= \frac{\alpha I}{2}\tanh(\frac{V}{2V_T}). \tag{86}$$

The simple differential pair has a very limited linear input range due to the exponential $V - I$ transfer function of the bipolar transistor. When the input voltage is larger than a few $V_T$, one of the transistors is turned off. The linear input range is limited to 32 mV $V_{PP}$ [64].

### 4.3.2 Schmoock Transconductor

For the Schmoock transconductor [74], shown in Fig. 51, the large-signal currents in $Q1$, $Q2$, $Q3$ and $Q4$ are [73]

$$I_{C1} = I_S \exp(\frac{V_{BE} + V/2}{V_T}), \tag{87}$$

$$I_{C4} = mI_S \exp\left(\frac{V_{BE} - V/2}{V_T}\right), \tag{88}$$

$$\frac{\alpha I}{2} = I_{C1} + I_{C4}, \tag{89}$$

$$\frac{I_{C1}}{I_{C4}} = \frac{1}{m} \exp\left(\frac{V}{V_T}\right), \tag{90}$$

solving for $I_{C1}$ and $I_{C4}$ [73]

$$I_{C1} = \frac{\alpha I/2}{1 + m \exp\left(-\frac{V}{V_T}\right)}, \tag{91}$$

$$I_{C4} = \frac{\alpha I/2}{1 + \frac{1}{m} \exp\left(\frac{V}{V_T}\right)}. \tag{92}$$

The output current of the differential pair $Q1$ and $Q4$ is [73]

$$\begin{aligned} I_{out1} &= \frac{I_{C1} - I_{C4}}{2} && (93)\\ &= \frac{\alpha I/4}{1 + m \exp\left(-\frac{V}{V_T}\right)} - \frac{\alpha I/4}{1 + \frac{1}{m} \exp\left(\frac{V}{V_T}\right)} && (94)\\ &= \frac{\alpha I/4}{1 + \exp\left(-\frac{V}{V_T} + \ln m\right)} - \frac{\alpha I/4}{1 + \exp\left(\frac{V}{V_T} - \ln m\right)} && (95)\\ &= \frac{\alpha I}{4} \tanh\left[\left(\frac{V}{V_T} - \ln m\right)/2\right]. && (96) \end{aligned}$$

Similarly, the output current from the differential pair $Q2$ and $Q3$ is [73]

$$I_{out2} = \frac{\alpha I}{4} \tanh\left[\left(\frac{V}{V_T} + \ln m\right)/2\right], \tag{97}$$

and the total output current of the two differential pairs in parallel is [73]

$$\begin{aligned} I_{out} &= I_{out1} + I_{out2} && (98)\\ &= \frac{\alpha I}{4} \tanh\left[\left(\frac{V}{V_T} - \ln m\right)/2\right] + \frac{\alpha I}{4} \tanh\left[\left(\frac{V}{V_T} + \ln m\right)/2\right]. && (99) \end{aligned}$$

Varying the emitter area ratio $m$ results in this transconductor having different linear input ranges [74]. When m=3.72 the maximum linear input range of 70 mV $V_{pp}$ is achieved [74].

In practical implementation, an integer of 4 is generally chosen for convenience [73]. The transconductance $g_m$ of the optimum Schmoock transconductor ($n = 4$) can be found as [73]

$$g_m = \frac{4\alpha I}{25V_T}. \tag{100}$$

Further increasing the number of parallel differential pairs improves the linearity modestly, but increases the complexity dramatically [76].

### 4.3.3 Voorman Transconductor

In the Voorman transconductor [73], shown in Fig. 54, the large-signal currents in $Q1$, $Q2$, $Q3$ and $Q4$ are

$$I_{C1} = I_S \exp\left(\frac{V_{BE} + V/2}{V_T}\right), \tag{101}$$

$$I_{C2} = I_S \exp\left(\frac{V_{BE} - V/2}{V_T}\right), \tag{102}$$

$$I_{C3} = mI_S \exp\left(\frac{V_{BE}}{V_T}\right), \tag{103}$$

$$I_{C4} = I_S \exp\left(\frac{V_{BE}}{V_T}\right), \tag{104}$$

The total current of for $Q1$, $Q2$, $Q3$ and $Q4$ is equal to the tail current $I$ [73]

$$I_{C1} + I_{C2} + I_{C3} + I_{C4} = \alpha I, \tag{105}$$

solving for $I_{C1}$ and $I_{C2}$ [73]

$$I_{C1} = \frac{\alpha I}{1 + 2n \exp\left(-\frac{V}{2V_T}\right) + \exp\left(-\frac{V}{V_T}\right)}, \tag{106}$$

$$I_{C2} = \frac{\alpha I \exp\left(-\frac{V}{V_T}\right)}{1 + 2n \exp\left(-\frac{V}{2V_T}\right) + \exp\left(-\frac{V}{V_T}\right)}. \tag{107}$$

and the large-signal differential signal current is [73]

$$I_{out} = \frac{1}{2}(I_{C1} - I_{C2}) \tag{108}$$

$$= \frac{1}{2}\left(\frac{\alpha I}{1 + 2n\exp(-\frac{V}{2V_T}) + \exp(-\frac{V}{V_T})} - \frac{\alpha I \exp(-\frac{V}{V_T})}{1 + 2n\exp(-\frac{V}{2V_T}) + \exp(-\frac{V}{V_T})}\right) \tag{109}$$

$$= \frac{\alpha I}{2}\frac{\exp(\frac{V}{2V_T}) - \exp(-\frac{V}{2V_T})}{2n + \exp(\frac{V}{2V_T}) + \exp(-\frac{V}{2V_T})}, \tag{110}$$

Varying the emitter area ratio, $n$, produces different linear input ranges in the transconductor [73]. Figure 53 shows the theoretical normalized transconductance ($g_m/g_{m,max}$) as a function of the input voltage. Curves 3, 4, and 5 correspond to the $g_m - V$ curves when $n = 1$, 2, and 3, respectively. Note that when $n = 2$, the circuit experiences its maximum linear input range of 140 mV $V_{pp}$ [73].

Curve 1 corresponds to a simple differential pair, while curve 2 represents the Schmoock transconductor [74]. The linear input range of a Voorman transconductor ($n = 2$) is significantly larger compared to either a simple differential pair or a Schmoock transconductor.

The transconductance, $g_m$, of the optimum Voorman transconductor ($n = 2$) can be found as [73]

$$g_m = \frac{\alpha I}{12V_T}. \tag{111}$$

Obviously Voorman is a better transconductor compared to the Schmoock transconductor; in addition to doubling the linear input range, it also has lower input capacitance due to the smaller transistor size, $1\times A_E$ on the signal path [73]. In the Schmoock transconductor, the signal is fed into parallel connected differential pairs, both of which have both $1\times A_E$ and $4\times A_E$ transistors [73]. Hence, a filter implemented with Voorman transconductors is expected to operate at higher operating frequencies [73]. The noise is also lower in Voorman transconductors [73]. The Schmoock transconductor has two tail current sources, and the noise current generated by each of these current sources is unequally delivered to the output because of their different transistor sizes [73]. Consequently, the differential noise current is not zero, and the noise generated by the two current sources is un-correlated

and their mean-square noise voltage can be added directly [73]. In contrast, in a Voorman transconductor the noise current generated by the tail current source is a common-mode signal and is therefore largely rejected by the differential pair at the output [73].

Since the center node of the resistors is at virtual ground, the transistor's base can be directly connected to its collector with no effect on the output current and, furthermore, the two center transistors can be combined [73]. Figure 54 shows the complementary Voorman transconductor used here [73]. The use of both *npn* and *pnp* transistors reduces the power consumption by effectively doubling the transconductance at the same current or, conversely, by maintaining the same transconductance with only half of the current [73].

In summary, complementary Voorman transconductors are very suitable for high-speed, low-noise, and low-power applications [73]. With the availability of very high speed C-SiGe HBTs, very attractive active filters can be achieved [73]. However, the performance of the $g_m$-$C$ filter remains limited by the speed of the pnp transistor, which unfortunately is not widely available, and is significantly slower than its *npn* counterpart [73].

As a result of recent breakthroughs in the complimentary SiGe HBT technology, the performance of the *pnp* transistor has now reached a level that is comparable to the state-of-the-art *npn* HBTs, and the speed of the $g_m$-$C$ filters can therefore be significantly improved.

## *4.4 Gyrator Design*

Figure 55 shows the tunable differential inductor (gyrator) used in this study. The effective inductance is given by

$$L = \frac{C}{{g_m}^2}. \tag{112}$$

Because this is a fully differential amplifier with an active load, the common-mode voltage at the output is not defined and a common-mode feedback circuit is needed, as shown in Fig. 56 [73], in order to correct the mismatch between the upper and lower tail current sources. If, for example, the collector current of Q13 is larger than I, the collector voltages of Q1, Q3, Q7 and Q9 all increase, as do the base and emitter voltages of Q10 and Q12

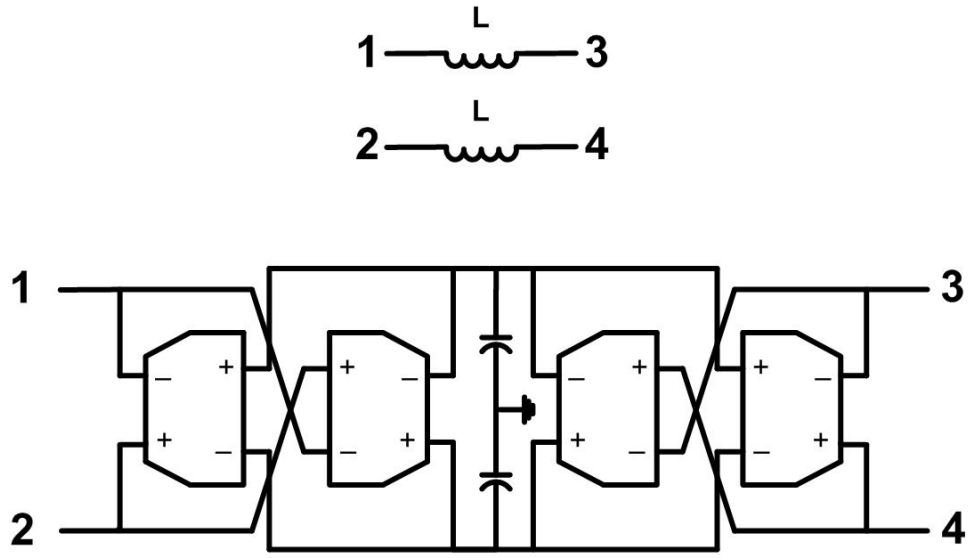


**Figure 55:** Schematic of the differential tunable inductor (gyrator).

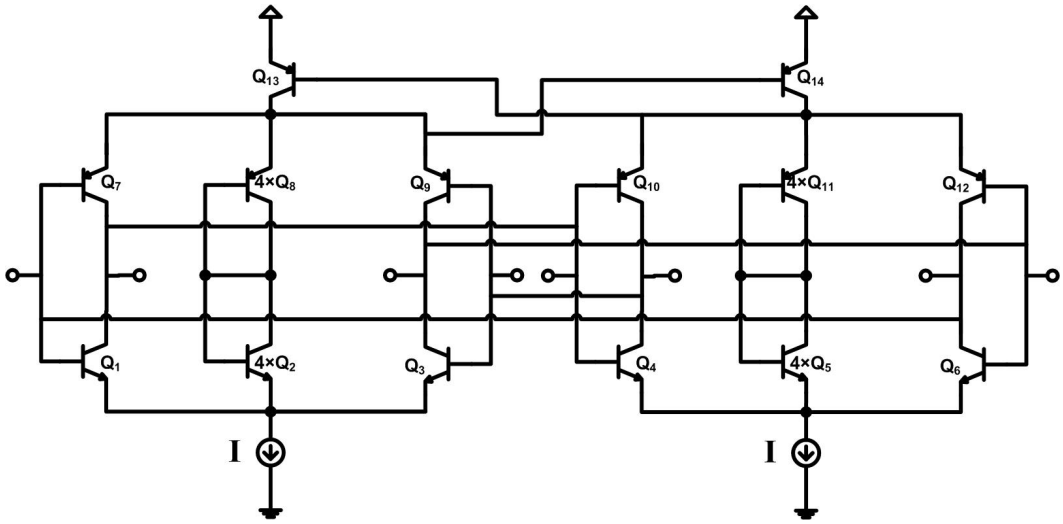


**Figure 56:** Schematic of the gyrator with common-mode feedback.

and, eventually, the base voltage of Q13 increases, and the current in Q13 decreases until it is equal to I.

## *4.5 Filter Design*

The block diagram of the core fifth-order elliptic low-pass filter is shown in Fig. 57, and the *RLC* equivalent circuit of this filter is shown in Fig. 58. All of the differential capacitors

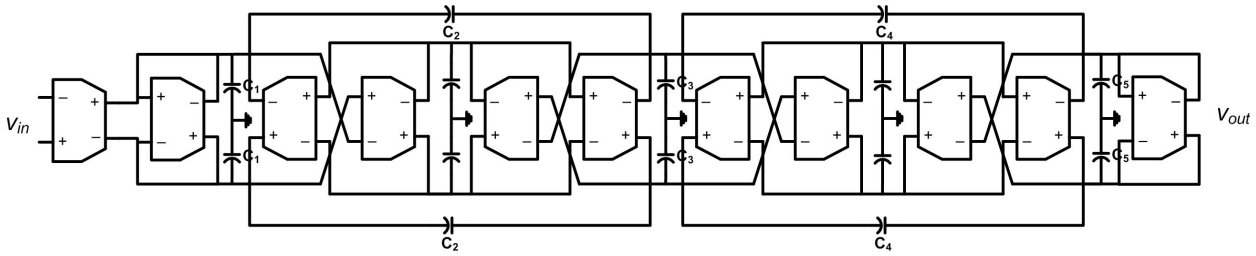


**Figure 57:** Block diagram of the fifth-order low-pass filter.

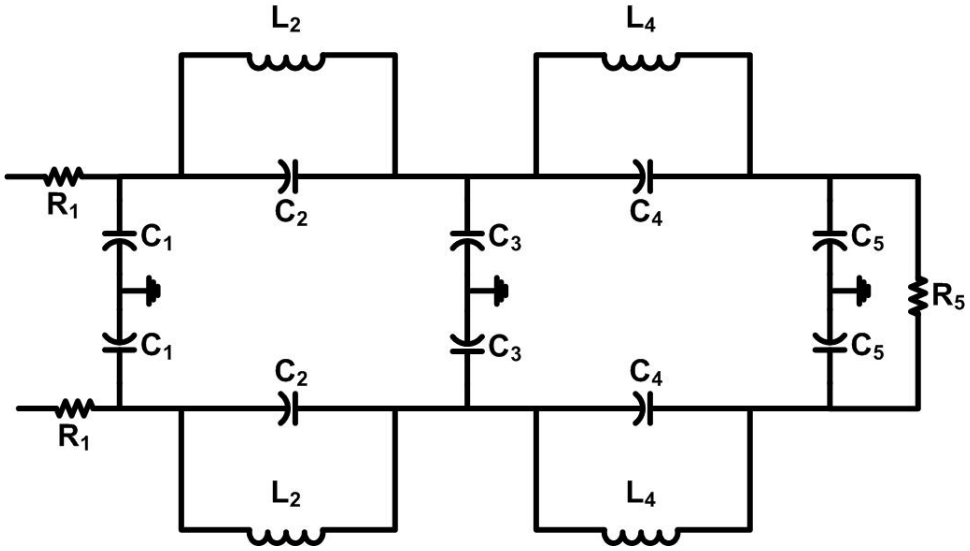


**Figure 58:** Equivalent *RLC* circuit of the fifth-order low-pass filter.

($C_1$, $C_3$ and $C_5$) were connected to the real ground in order to improve the common-mode stability at high frequency [73]. Two 50 Ω shunt input resistors and a 50 Ω output buffer were added (not shown in Figure 57) in order to achieve broadband impedance matching to the test equipment.

By changing the tail current of the transconductor, the tuning function is realized. From the simulation results, shown in Fig. 59, the filter has a maximum bandwidth of 4.2 GHz, a tuning range of 42 MHz–4.12 GHz and a pass-band gain of 0 dB.

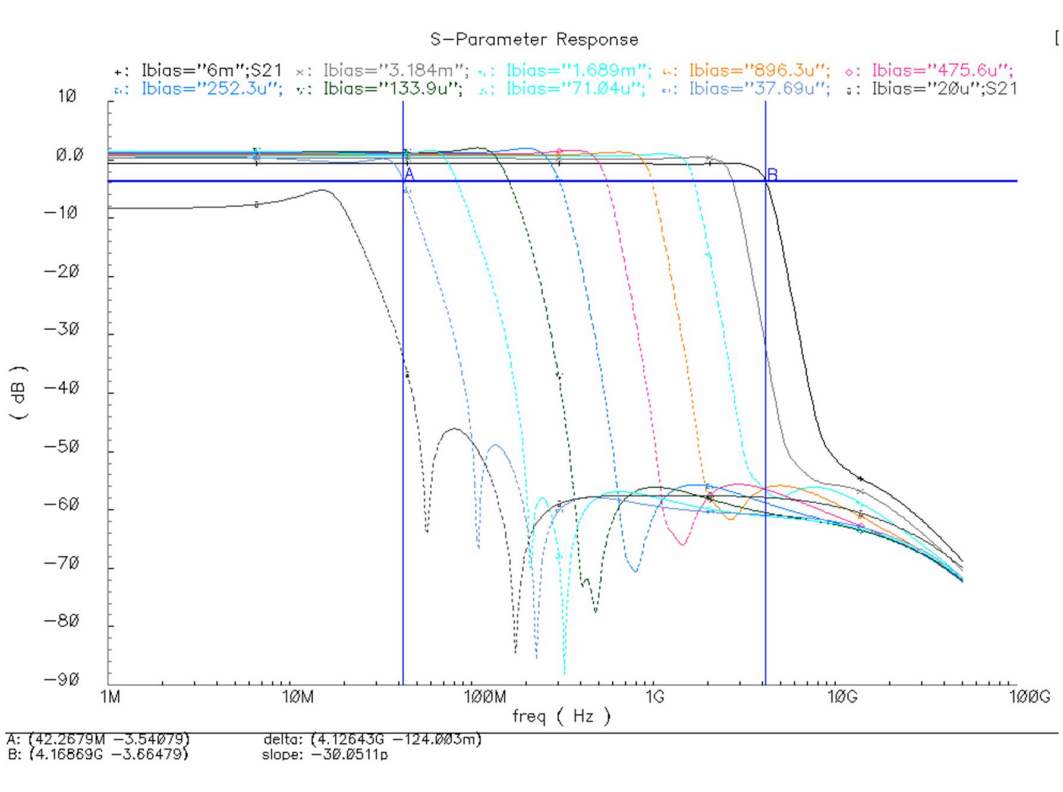


**Figure 59:** Simulated $S_{21}$ of the C-SiGe $g_m$-$C$ filter over its tuning range.

## *4.6 Measurement Results*

This C-SiGe filter was implemented in a commercially-available 0.25 $\mu$m 170/90 GHz C-SiGe HBT BiCMOS technology [40], and occupies a total area of 0.90×0.91 mm$^2$ including the probe pads. The chip micrograph is shown in Fig. 60. The filter was tested on-wafer using 40 GHz probes and cables.

The filter operates off a 3.5 V power supply and has 28.5 mA of bias current flowing through its core circuit when achieving a maximum bandwidth of 4.1 GHz. Fig. 61 shows a typical measured $S_{21}$ from 0.05 GHz to 5 GHz. The 3-dB bandwidth is 430 MHz, and the attenuation at 670 MHz is about 42 dB. The pass-band shows a loss of 6.8 dB (compared to 0 dB predicted by the simulation). Part of this loss is measurement-setup induced, originating from the lack of high-performance ultra-wideband (from 50 MHz to 10 GHz) differential signals for testing. A pair of back-to-back connected ultra-wideband baluns

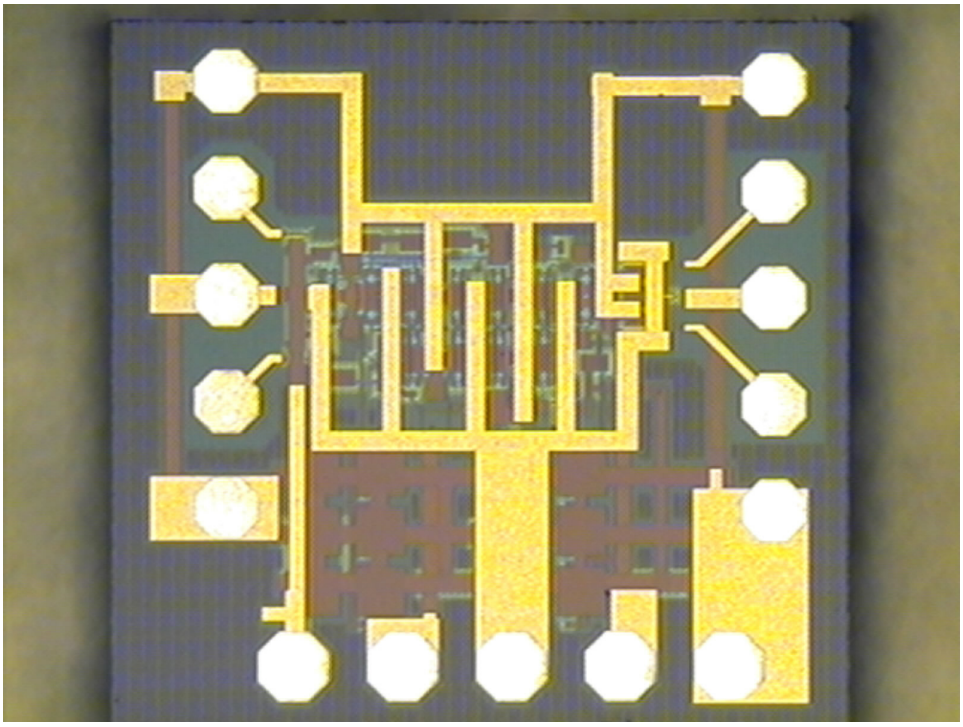

**Figure 60:** Die micrograph of the C-SiGe $g_m$-$C$ filter.

were used to achieve single-ended to differential and differential to single-ended conversions. However, large phase and amplitude mismatches were observed (and uncorrected for) at the output of the balun. In addition, it is possible to increase the transconductance (current) of the input $g_m$ cell to compensate for any pass-band loss. Fig. 62 shows the measured $S_{21}$ over the tuning range. The bandwidth can be continuously tuned over a very wide range, from 70 MHz to 4.1 GHz. Figure 63 shows the linearity data for the filter. The third-order input intercept point (IIP3) is -5.5 dBm for a two-tone input signal containing 1.50 GHz and 1.52 GHz frequency components, and the output noise power spectrum density (PSD) is -143 dBm/Hz. Table 11 shows a comparison between this C-SiGe filter and other reported low-pass active filters. To the best of our knowledge, the present C-SiGe filter has the widest bandwidth and achieves a record continuous tuning range between 70 MHz and 4.1 GHz compared with the previous state-of-the-art.

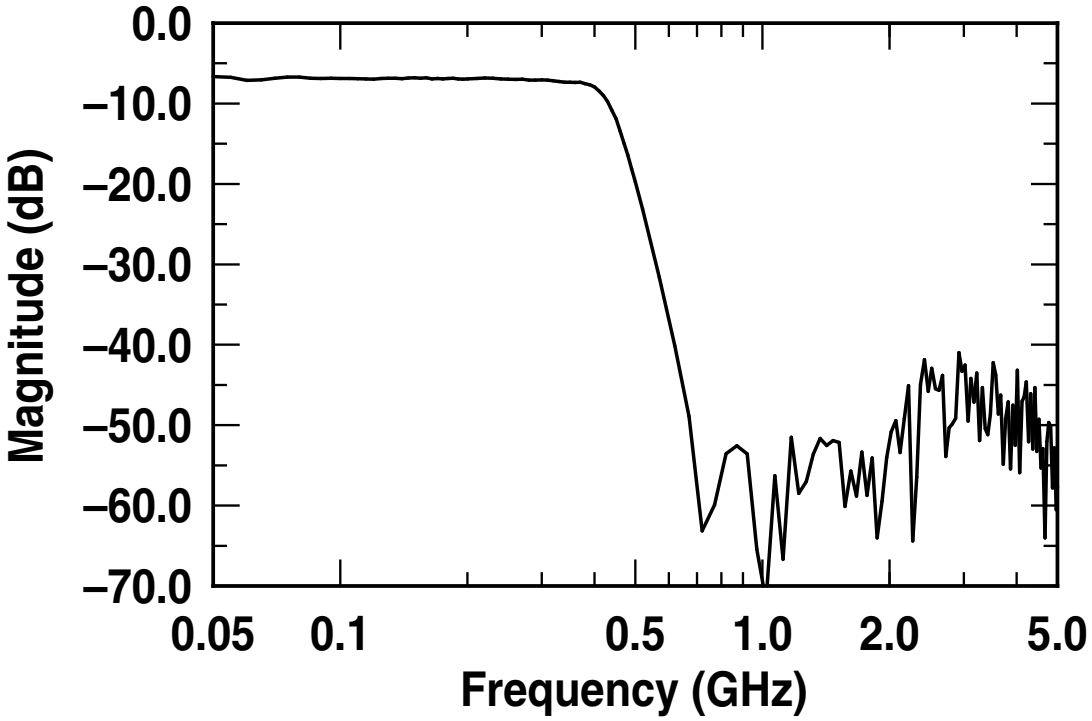


**Figure 61:** Measured $S_{21}$ of the C-SiGe $g_m$-$C$ filter.

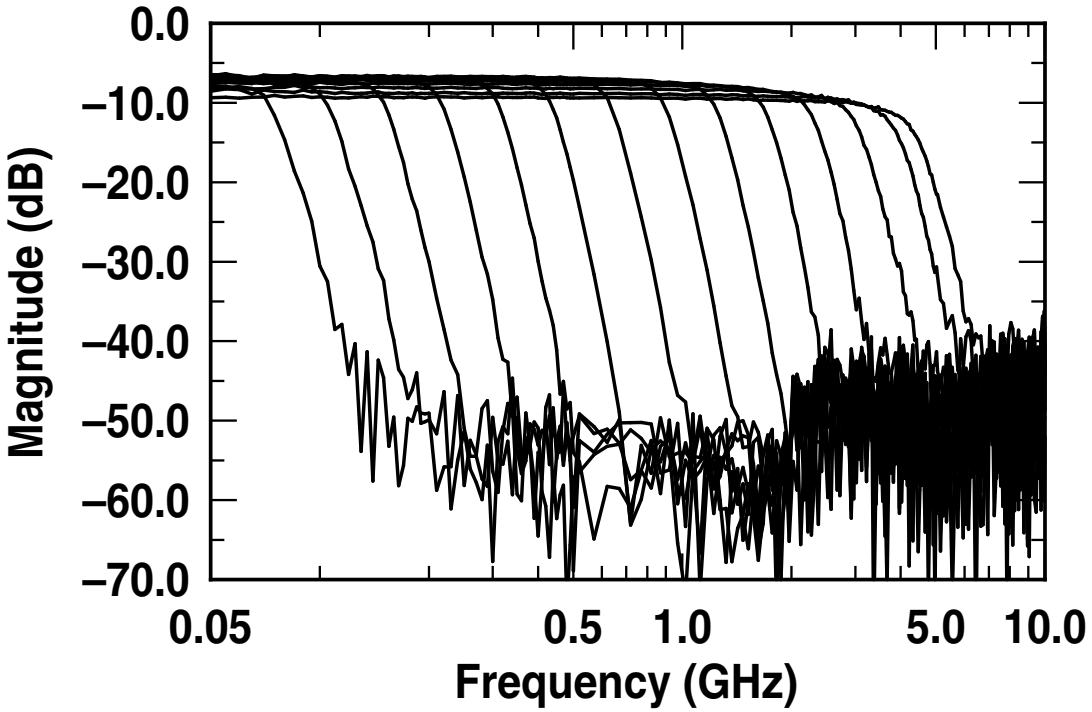


**Figure 62:** Measured $S_{21}$ of the C-SiGe $g_m$-$C$ filter over its tuning range.

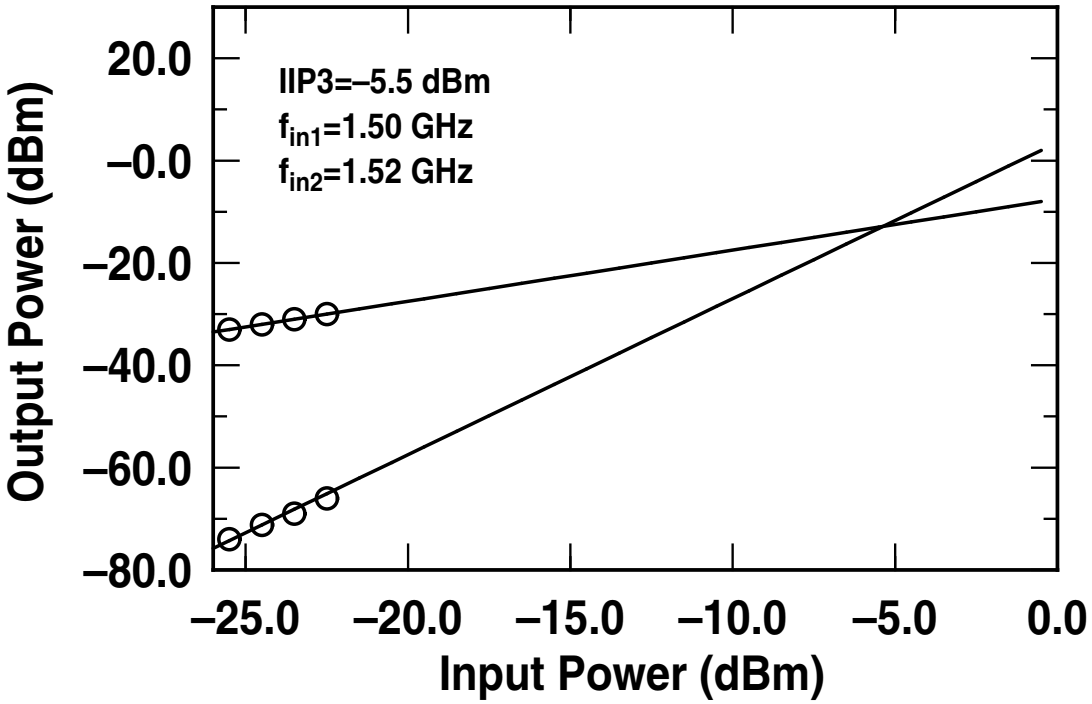


**Figure 63:** Measured IIP3 of the C-SiGe $g_m$-$C$ filter.

**Table 11:** Comparison with Published High-Frequency Active Low-Pass Filters.

| Reference | BW [MHz] | Power [mW] | VCC [V] | IIP3 | Order | Topology | Technology |
|---|---|---|---|---|---|---|---|
| [75] | 200-1000 | 90 | 1.8 | 13.5 dBV | 5 | op amp RC | 0.18 $\mu$m CMOS |
| [77] | 500 | 14 | 1.8 | 3.0 dBm | 5 | op amp RC | 0.18 $\mu$m CMOS |
| [78] | 80-200 | 270 | 3.0 | - | 7 | $g_m$-$C$ | 0.25 $\mu$m CMOS |
| This work | 70-4100 | 100 | 3.5 | -5.5 dBm | 5 | $g_m$-$C$ | 0.25 $\mu$m C-SiGe |

## *4.7 Summary*

A high-frequency, continuous-time, fifth-order, elliptic, $g_m$-$C$ filter based on Voorman transconductors has been presented in this chapter. The filter was fabricated in a high-performance complementary SiGe BiCMOS technology and achieved a 3-dB bandwidth of 4.1 GHz and a tuning range of 70 MHz to 4.1 GHz. This C-SiGe $g_m$-$C$ filter is well-suited for next-generation recording devices and UWB communications system applications.

# CHAPTER V

# RADIATION RESPONSE OF THE THIRD GENERATION SIGE HBTS

## *5.1 Introduction*

Bandgap-engineered SiGe HBTs are receiving increasing attention due to the potential they offer for terrestrial communications IC applications because they enable a dramatic improvement in transistor-level performance while simultaneously maintaining strict compatibility with conventional low-cost, high-integration level, high-volume Si CMOS manufacturing [33]. SiGe HBT technologies with 50 GHz (first-generation) and 120 GHz (second-generation) peak cutoff frequency are currently in commercial production worldwide from multiple sources, and are being widely deployed in both the commercial and defense sectors. SiGe HBT technology has also generated significant recent interest in the space community, because it offers substantial (multi-Mrad) total dose hardness without the need for costly radiation hardening, although SEU tolerance is still under active investigation [33].

This advance in the SiGe state-of-the-art to 200 GHz (third-generation) [36] performance has only been achieved by radically altering the structure of previous SiGe HBT design points. The third-generation SiGe HBT technology used in the present investigation (IBM's SiGe 8HP technology) employs a novel, reduced thermal cycle, "raised extrinsic base" structure, and utilizes conventional deep and shallow trench isolation, an *in-situ* doped polysilicon emitter, and an unconditionally stable, 25% peak Ge, C-doped, graded UHV/CVD epitaxial SiGe base (Fig. 64) [36]. The device structure has been scaled later-

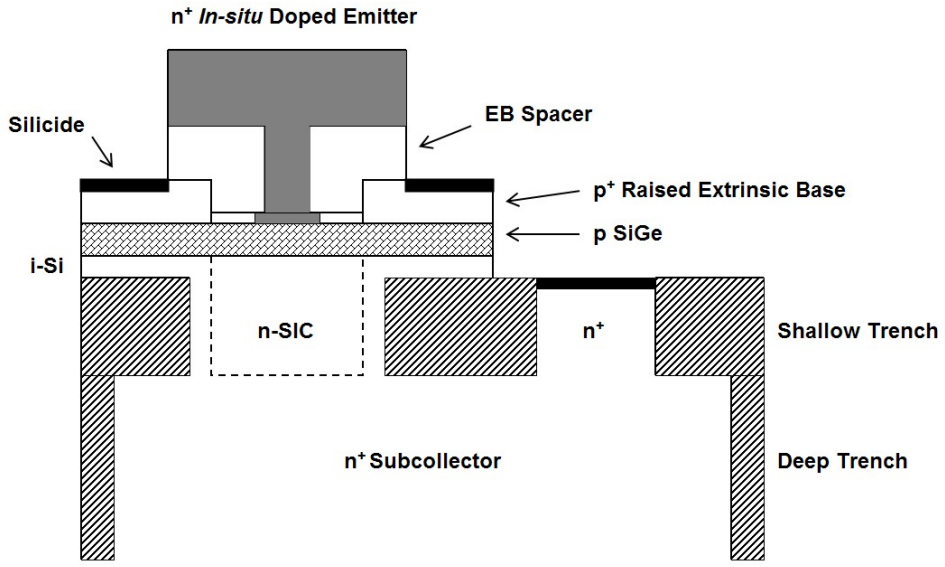


**Figure 64:** Schematic cross-section of the 185 GHz SiGe HBT.

ally to a 0.12 $\mu$m emitter stripe width to minimize base resistance and thus improve the frequency response and noise characteristics. Such a raised extrinsic base structure facilitates the elimination of any out-diffusion of the extrinsic base, thereby significantly lowering the collector-base junction capacitance [36]. From a radiation tolerance perspective, however, the emitter-base (EB) spacer and the shallow trench isolation (STI) of the new structure are both fundamentally different than those found in first- and second-generation (IBM SiGe 5HP and SiGe 7HP) technologies, and the composite films and processing/thermal cycles are significantly altered, raising a valid question as to the overall radiation tolerance of the new device structure with respect to previous SiGe technology generations. This question is particularly relevant given that the overall processing thermal cycles have also been significantly reduced, thus raising questions about the overall robustness of the oxide interfaces, the primary damage points in an ionizing radiation environment. In this work, the first results on the proton tolerance of a third-generation SiGe HBT technology are reported and compared with prior SiGe technology generations to quantify any differences. This work is also published as [84]).

## 5.2 Experiment

The third-generation SiGe HBT technology (IBM SiGe 8HP) examined in this work has a 0.12 $\mu$m emitter stripe width and 185 GHz peak $f_T$ (this was off a different fabrication lot than that reported in [36], but is essentially the same technology, with a slightly different vertical profile). Two earlier SiGe HBT technology generations were also measured to assess the impact of vertical scaling, lateral scaling, and structural changes on the radiation response and included a 0.50$\mu$m 50 GHz $f_T$ SiGe HBT (IBM SiGe 5HP) and a 0.20 $\mu$m 120 GHz $f_T$ SiGe HBT (IBM SiGe 7HP). In the case of 7HP SiGe technology, the effects of radiation on the *ac* performance are reported here for the first time.

The samples were irradiated with 62.5 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup [80], [81]. The radiation source (Ta scattering foils), located several meters upstream of the target, establish a beam spatial uniformity of about 15% over a 2.0 cm radius circular area [80], [81] Beam currents from about 5 pA to 50 nA allow testing with proton fluxes from $1 \times 10^6$ to $1 \times 10^{11}$ proton/cm$^2$sec [80], [81]. The dosimetry system has been previously described [80], [81] and is accurate to about 10%. At a proton fluence of $1 \times 10^{12}$ p/cm$^2$, the measured equivalent gamma dose was approximately 136 krad(Si). The SiGe HBTs were irradiated with all terminals grounded for the *dc* measurements and with all terminals floating for the *ac* measurements at proton fluences ranging from $1.0 \times 10^{12}$ p/cm$^2$ to $5.0 \times 10^{13}$ p/cm$^2$. It was previously shown that SiGe HBTs are not sensitive to applied bias during irradiation. Wirebonding of ac test structures is not compatible with robust broadband measurements, and hence on-wafer probing of S-parameters (with terminals floating) was used to characterize the high-frequency performance. The samples were measured at room temperature with an Agilent 4155 Semiconductor Parameter Analyzer (*dc*) and an Agilent 8510C Vector Network Analyzer (*ac*) using the techniques discussed in [82].

## 5.3 *dc* Results

The resultant 8HP forward-mode Gummel characteristics are shown in Fig. 65 and 66 as a function of proton fluence, and reveal a remarkably minor degradation in the base current at a few Mrad equivalent gamma dose. As has been previously discussed [83], this base current degradation is physically the result of proton-induced G/R center, physically located at the emitter-base spacer at the emitter periphery.

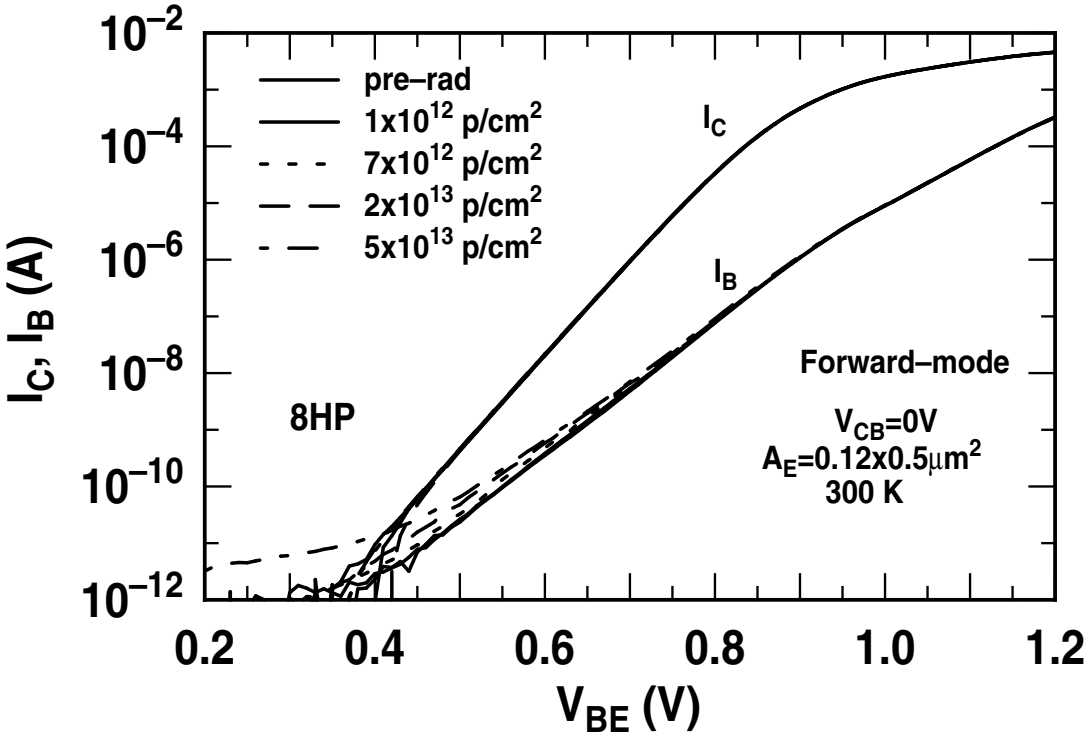


**Figure 65:** Forward-mode Gummel characteristics of the 8HP SiGe HBT.

A comparison of the normalized base current degradation of the 8HP transistor to that of the first- (5HP) and second- (7HP) generation SiGe devices shows that the 8HP devices experienced significantly *smaller* radiation-induced damage than the earlier technology generations (Fig. 67). This result is a pleasant surprise and would appear to be in direct contradiction with the results of SiGe HBT scaling presented in 2002 [83], in which vertical and lateral device scaling generally degraded the forward-mode proton response. It should be noted, however, that this result can be easily misinterpreted, since the base

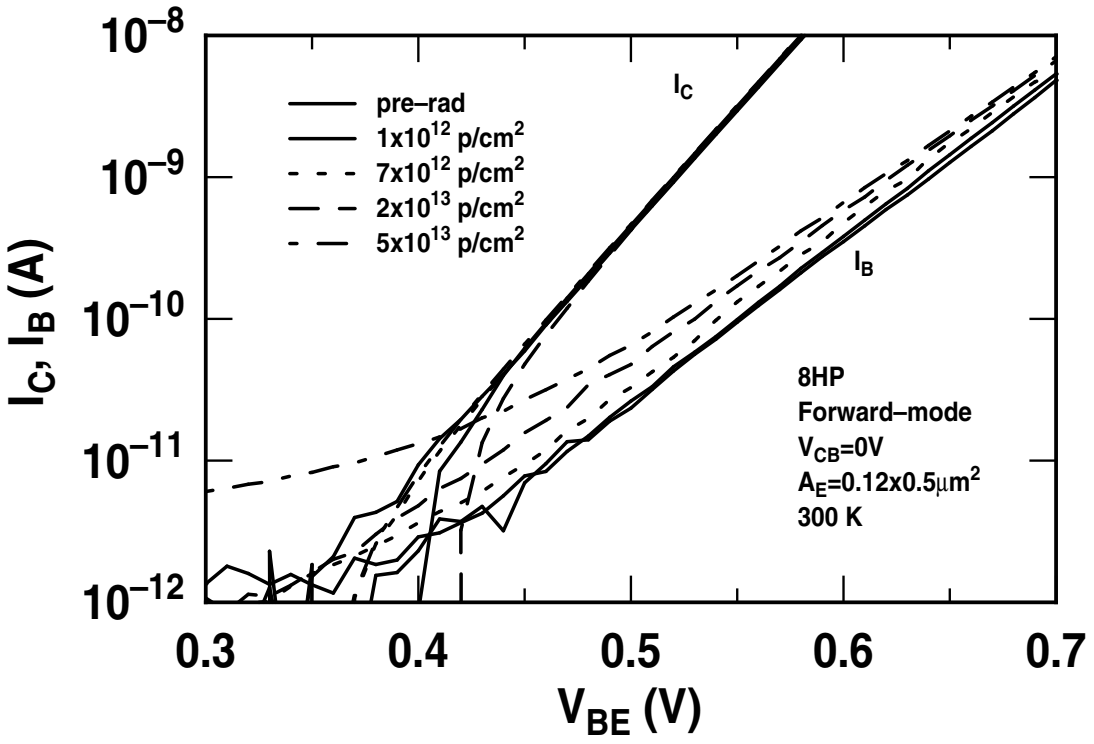


**Figure 66:** Forward-mode Gummel characteristics(Vbe=0.3-0.7V) of the 8HP SiGe HBT.

current ideality of the pre-radiation device influences the final base current change. That is, in the case of 8HP, there is clearly a pre-existing G/R center dominated base current leakage component, as evidenced by the non-ideal base current slope of about 120 mV/decade, which is consistent with classical G/R leakage. For the 5HP and 7HP devices, however, the starting base currents were significantly more ideal, and hence even a small absolute degradation of the base current resulting from proton exposure produced a larger damage ratio in these devices. In effect, the 8HP base current damage was still present but effectively "hidden" beneath the pre-radiation, non-ideal base leakage component. As the 8HP technology has matured, its pre-radiation, non-ideal base current has become more ideal, thus facilitating a more meaningful comparison with 5HP and 7HP devices; an experiment aimed at addressing this is underway and will be reported at a later date. Nevertheless, at the low end of the practical circuit operating currents (e.g., $I_C = 1.0\mu A$), the change in the current gain ($\beta$) for the 8HP device is less than 20% at $5 \times 10^{13} p/cm^2$, significantly better

than that achieved for either 5HP or 7HP (Fig. 68). This is clearly very good news and speaks well of the inherent tolerance of the various potentially sensitive interfaces in the modified, low-thermal budget, 8HP device structure, namely the EB spacer and STI edge.

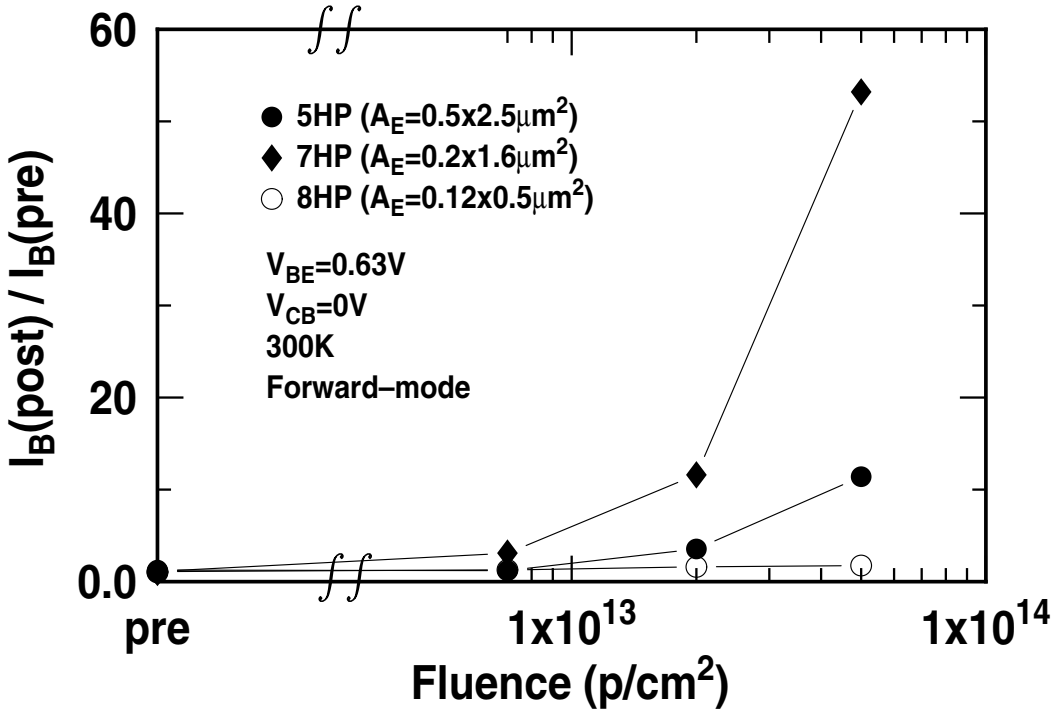


**Figure 67:** Comparison of the normalized base current in *forward*-mode as a function of proton fluence for the 5HP, 7HP, and 8HP SiGe HBT technology generations.

Measurements of the inverse-mode Gummel characteristics (Fig. 69 and 70) with the emitter and collector swapped, which effectively samples the physical collector-base junction, indicate that while the pre-radiation base current is less ideal than perhaps desired, the proton-induced change to the inverse-mode base current is minor at best, which is consistent with the fact that the STI is very thin in this generation (much less than 5HP, but similar to 7HP) and thus has less impact on the collector-base junction characteristics. This is significant, given that, unlike in the 5HP and 7HP devices, the overall thermal cycle of the 8HP process is substantially reduced, and hence no out-diffusion of the extrinsic base is available to "cover" the exposured corners of the STI with high doping, effectively containing any proton-induced damage. This result suggests that this "raised extrinsic base"

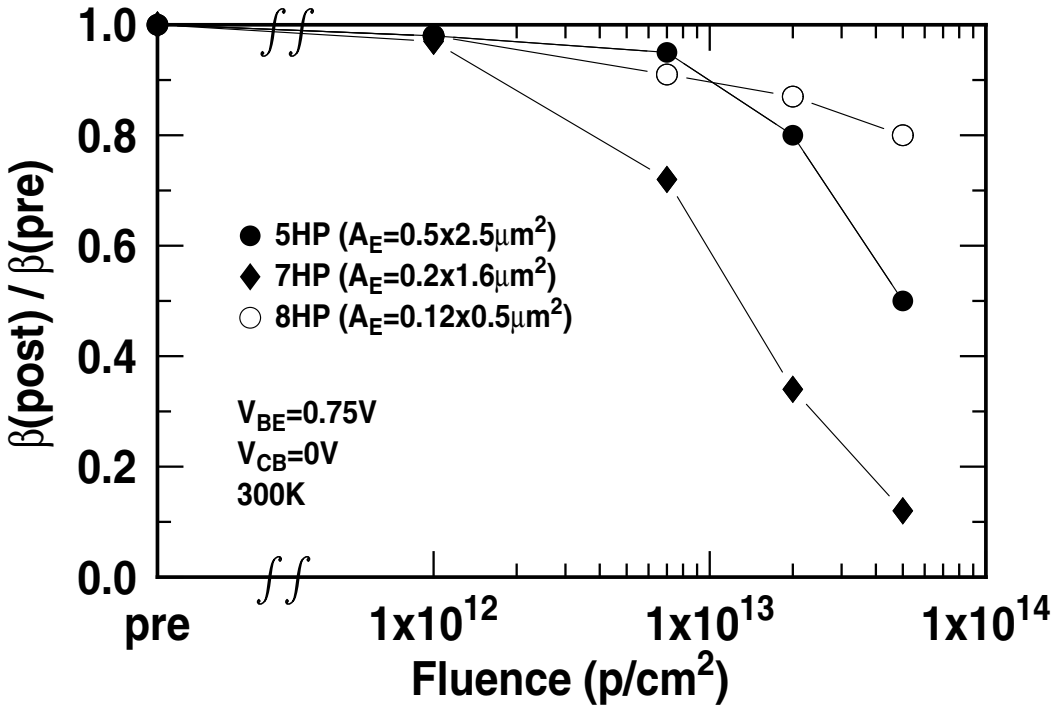


**Figure 68:** Comparison of the normalized current gain as a function of proton fluence for the 5HP, 7HP, and 8HP SiGe HBT technology generations.

8HP structure should continue to enjoy substantial proton tolerance even as the technology is further scaled for even higher performance, as has in fact been recently reported in a 350 GHz peak $f_T$ SiGe HBT [38].

## *5.4 ac Results*

The transistor scattering parameters (S-parameters) were fully characterized to 26 GHz, from which the cut-off frequency $f_T$ was extracted at each bias current point. The pre- and post-radiation cut-off frequencies versus collector current density for the 8HP devices are shown in Fig. 71, together with comparisons to the 7HP (at $7 \times 10^{12} p/cm^2$ fluence) and 5HP (at $5 \times 10^{13} p/cm^2$ fluence) SiGe technologies. As can be clearly seen, negligible degradation of $f_T$ is observed in the 8HP devices, which is well within the measurement error of about $\pm 5\%$.

The *ac* small signal model for SiGe HBTs is shown in Fig. 72. From the measured

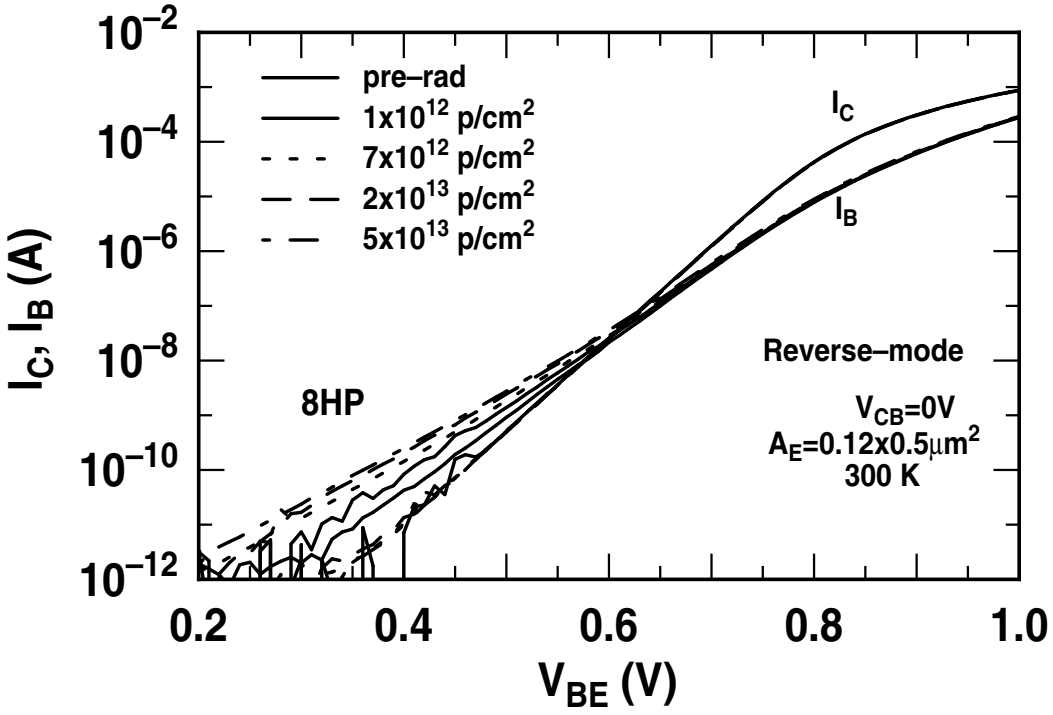


**Figure 69:** Inverse-mode Gummel characteristics of the 8HP SiGe HBT.

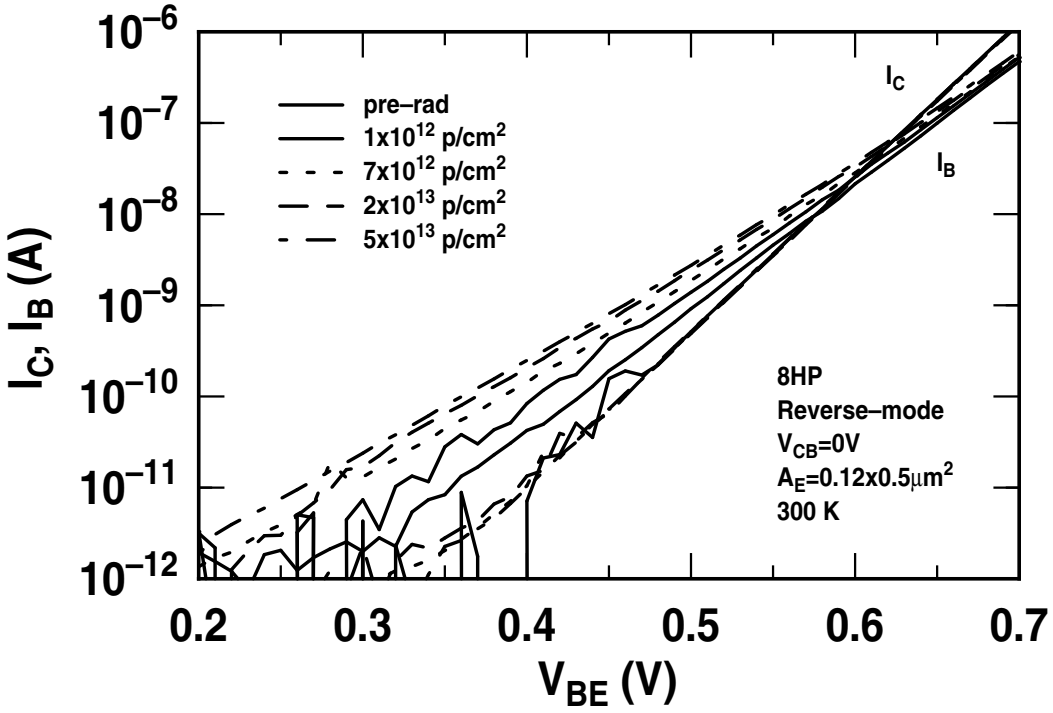


**Figure 70:** Inverse-mode Gummel characteristics (Vbe=0.3-0.7V) of the 8HP SiGe HBT.

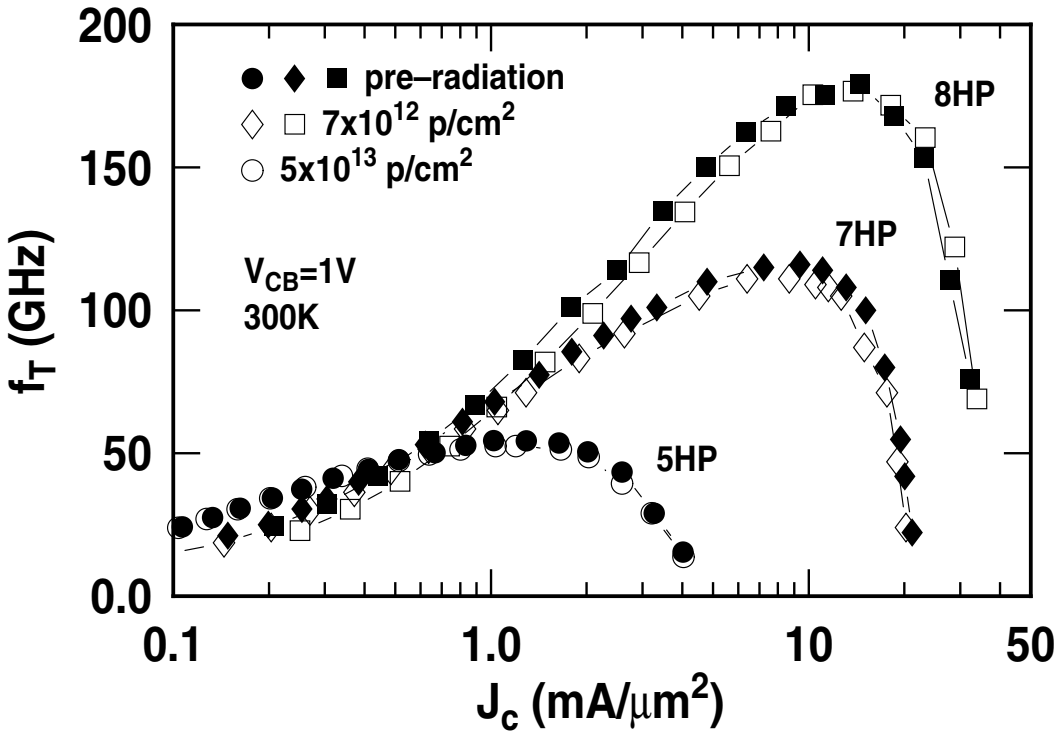


**Figure 71:** Pre-radiation and post-radiation cut-off frequency versus collector current density for 8HP, 7HP, and 5HP SiGe HBTs.

S-parameters, the dynamic base resistance ($r_{bb}$) can also be extracted, as shown in Fig. 73. The 8HP base doping level is higher than that for 7HP, and thus the base resistance is smaller. Note that the total base resistance increases slightly as the proton fluence increases above $1\times10^{13} p/cm^2$, presumably because of displacement effects in the neutral base region, and the deactivation of boron dopants. A similar trend can be seen in the 7HP. This effect is very minor, however, because the base profile is very thin (<30 nm) and it is very heavily doped ($> 1 \times 10^{19} cm^{-3}$), and should not therefore have a significant impact on either the maximum oscillation frequency or the broadband noise performance.

The total emitter-to-collector delay time ($\tau_{EC}$) and the total depletion capacitance ($C_{total}$) can be extracted from the measured cut-off frequency characteristics and are shown as a function of proton fluence in Fig. 74 and 75. Interestingly, it can be observed that the total transit time of the 7HP devices monotonically increases (degrades) with fluence, while the 8HP total transit time remains constant with fluence. This is clearly reflected in the

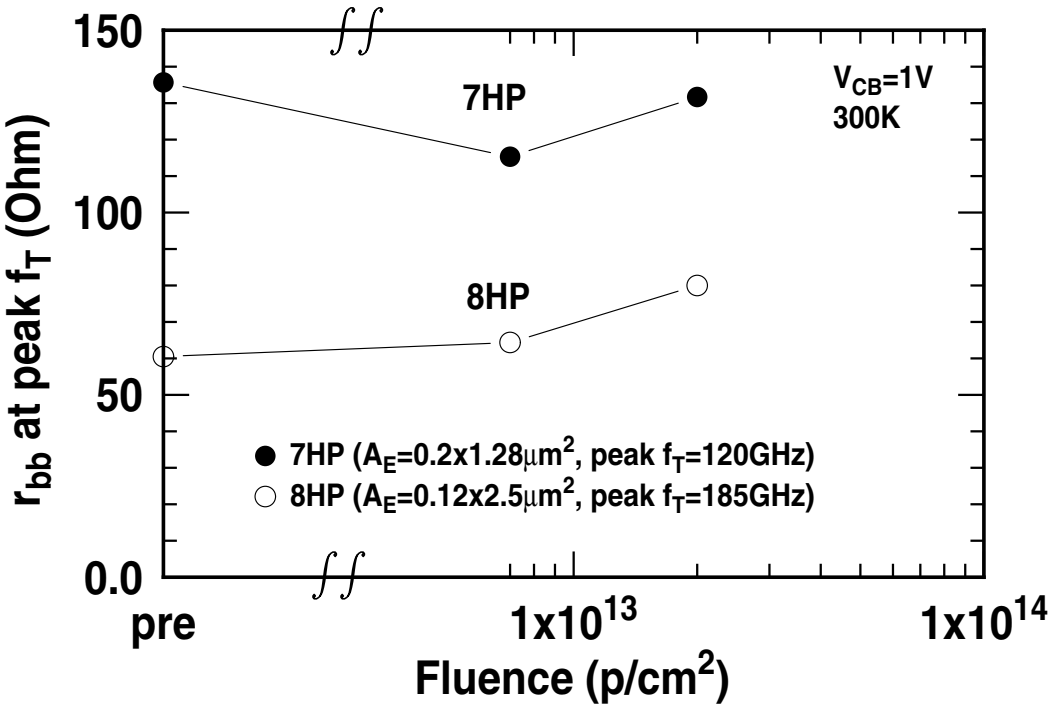


**Figure 72:** Dynamic base resistance dependence on proton fluence.

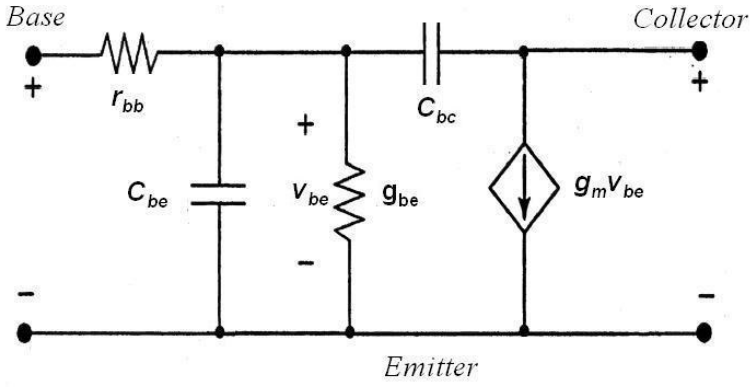


**Figure 73:** Small signal model for SiGe HBTs.

change in the peak cut-off frequency of the respective technologies (the 8HP peak $f_T$ does not change, while there is a small but observable decrease in peak $f_T$ in 7HP (Fig. 71). The small observable increase in base resistance at high fluence coincides with a slight decrease in the total depletion capacitance (Fig. 74) and is consistent with the above claims that small but finite displacement-induced acceptor de-ionization occurs in the base region

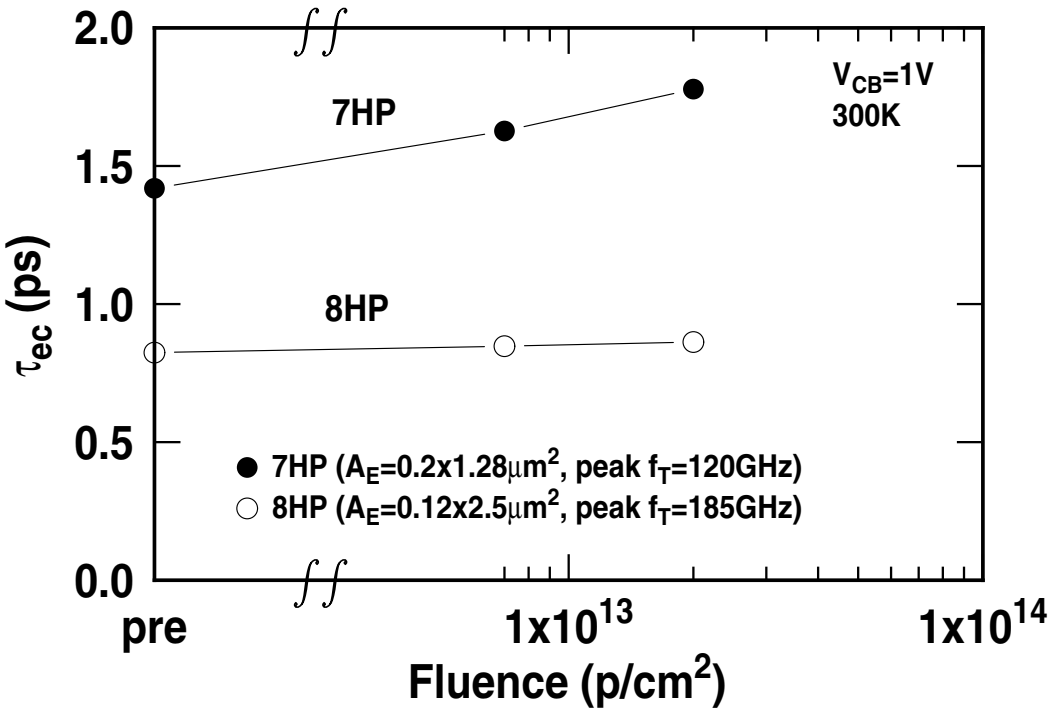


**Figure 74:** Extrapolated transit time dependence on proton fluence.

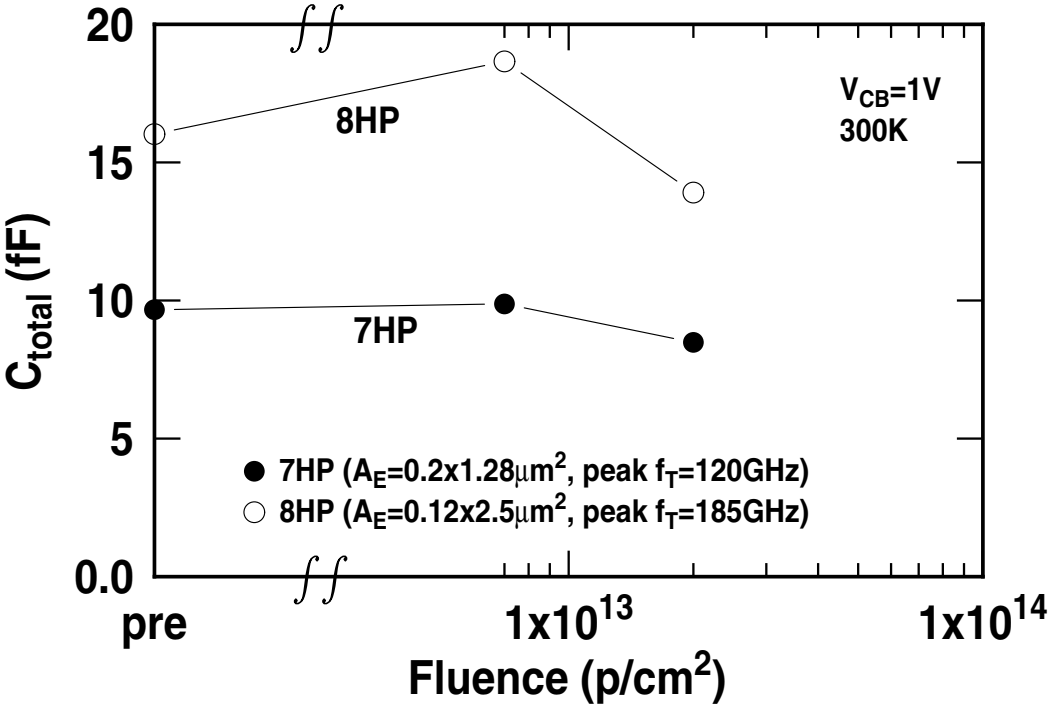


**Figure 75:** Total depletion capacitance dependence on proton fluence.

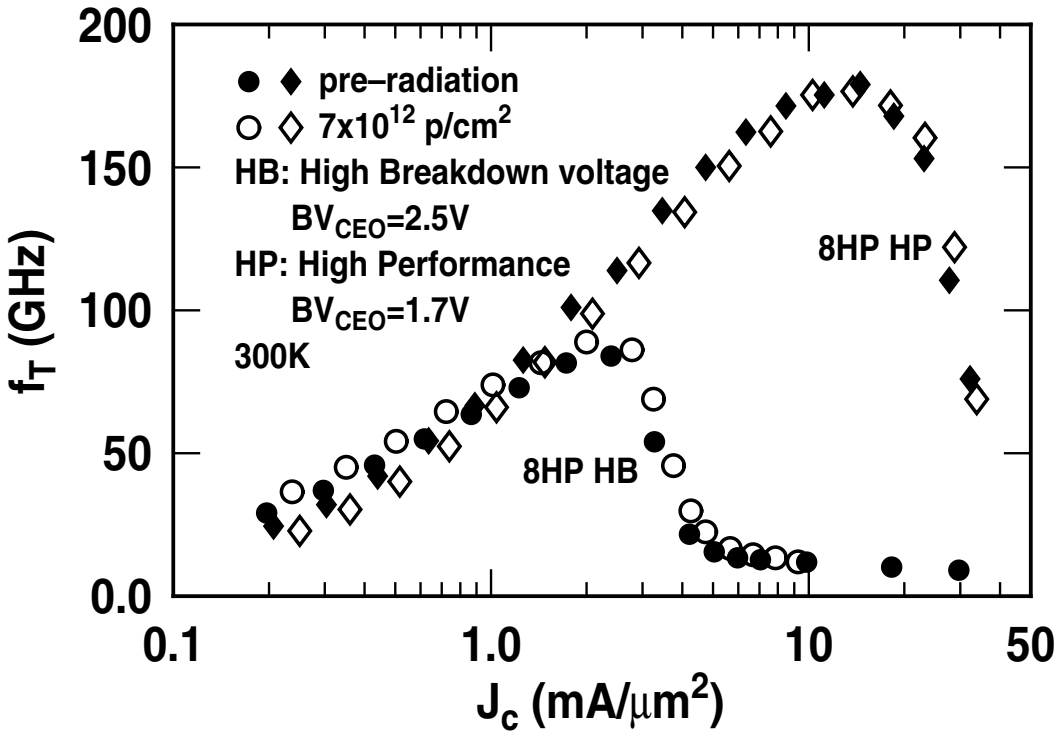


**Figure 76:** Pre- and post-radiation cut-off frequency versus collector current density for both high breakdown and low breakdown 8HP SiGe HBTs.

of the device.

Finally, the impact of proton exposure on the cut-off frequency characteristics of two different breakdown voltage 8HP transistors on the same wafer was examined (Fig. 76). One of the key advantages offered by SiGe technology is its ability to trivially integrate transistors with multiple breakdown voltages on the same wafer using only a collector implant blockout mask, thereby facilitating great flexibility for circuit designers. Clearly, the peak operating frequency does not depend strongly on proton fluence, which is good news. Note, however, that the roll-off in $f_T$ at high $J_C$ does not change significantly with proton exposure. This is significant since the $f_T$-$J_C$ roll-off is very sensitive to any changes in the effective doping level in the collector region and thus suggests that collector-region displacement damage is not a major concern in this generation of device technology, which is consistent with the above observations on base resistance. This can be quantified by plotting the current at which $f_T$ falls by 20% and normalizing to pre-radiation values (Fig. 77).

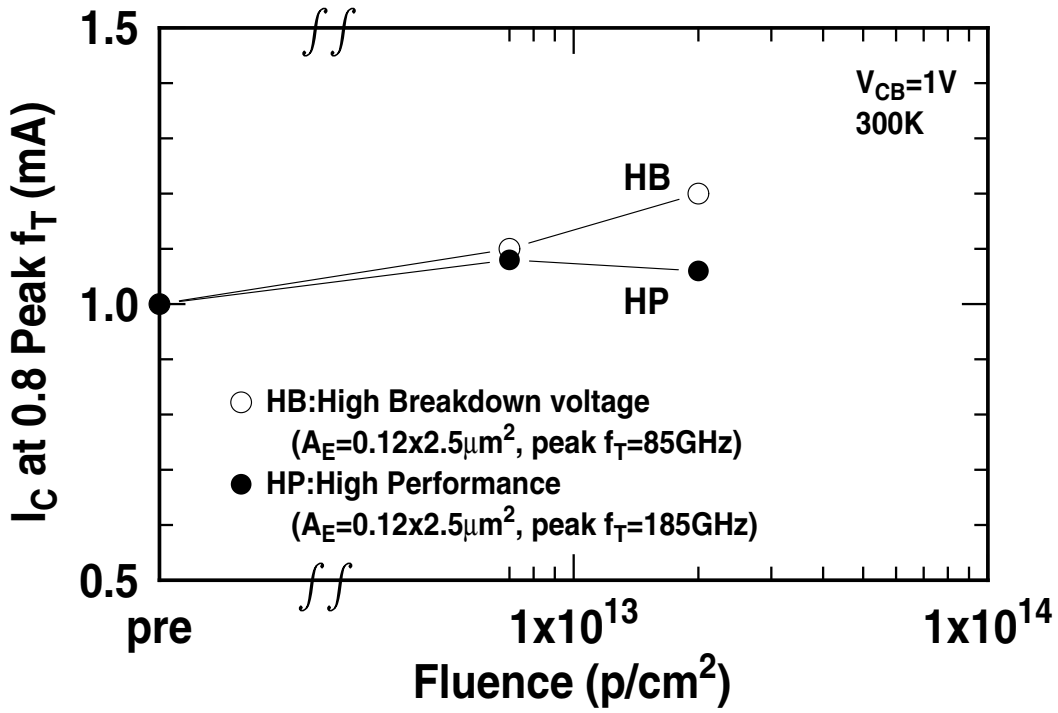


**Figure 77:** Normalized collector current roll-off point for both high breakdown and low breakdown 8HP SiGe HBTs.

The roll-off current density actually increases slightly with irradiation, and this manifests more strongly in the low breakdown device.

## *5.5 Summary*

The impact of proton irradiation on the *dc* and *ac* characteristics of third-generation, 185 GHz SiGe HBTs is reported here for the first time. The results demonstrate that the latest SiGe HBT technologies can successfully maintain their inherent Mrad-level total dose hardness, without intentional hardening, even when the device structure is fundamentally altered in order to achieve unprecedented levels of device performance.

# CHAPTER VI

# CONCLUSION AND FUTURE WORK

The contributions of this research are as follows:

1. Proposed and implemented a new 3-10 GHz SiGe HBT LNA for UWB applications. The use of a shunt base-emitter capacitor and weak shunt resistive feedback in a cascode amplifier with inductive degeneration significantly improves the input bandwidth of the LNA, and simultaneously allows a very low noise figure to be achieved. This LNA achieves the lowest reported *NF* of any LNA in Si-based technology in the UWB band to date (Chapter II, also published in [59]).

2. Proposed and implemented an 8-bit 12 GSample/sec SiGe BiCMOS track-and-hold amplifier for use in high-speed analog-to-digital converters. The use of a degeneration inductor in the input buffer significantly improves the performance of the THA. This circuit is the fastest 8-bit Si-based THA reported to date. (Chapter III, also published in [72]).

3. First demonstrated a continuous-time, fifth-order, elliptic, $g_m$-$C$ low-pass active filter in 0.25 $\mu$m complementary ($npn + pnp$) silicon-germanium (C-SiGe) HBT technology. This C-SiGe filter has the widest bandwidth reported to date achieving a record continuous tuning range between 70 MHz and 4.1 GHz. (Chapter IV, also published in [79]).

4. Studied the impact of proton irradiation on the *dc* and *ac* characteristics of third-generation, 0.12 $\mu$m 185 GHz SiGe HBTs. The results demonstrate that SiGe HBT technologies can successfully maintain their Mrad-level total dose hardness, without

intentional hardening, even when vertically-scaled in order to achieve unprecedented levels of transistor performance(Chapter VII, also published in [84]).

In the future, this work can be extended by:

1. Designing a new 3-10 GHz UWB receiver front-end that integrates the LNA, I/Q mixers, channel selection filters, and VGAs.
2. Designing a new 3-10 GHz UWB receiver that integrates the front-end, LO generation and ADCs.
3. Designing a new 8-bit 10 Gsample/sec ADC that integrates the proposed THA.
4. Designing a new automatic tuning circuitry to tune the gain, cut-off frequency, and Q of the elliptic low-pass $g_m$-$C$ filter to compensate for process variations.
5. Designing a new active-RC filter in the C-SiGe process.

# REFERENCES


[1] R.J. Fontana, "Recent system applications of short-pulse ultra-wideband (UWB) technology," *IEEE Transactions on Microwave Theory and Techniques*, 52, pp. 2087-2104, September 2004.

[2] G.F. Ross, "The transient analysis of multiple beam feed networks for array systems", Ph.D. dissertation, Polytechnic Institute of Brooklyn, Brooklyn, NY, 1963.

[3] "First report and order, revision of part 15 of the commissionªs rules regarding ultra wideband transmission systems," Federal Communications Commission, February 2002.

[4] "Multiband OFDM physical layer proposal for IEEE 802.15.3a," IEEE P802.15 Working Group for WPANs, September 2004.

[5] "IEEE 802.15.3a updated DS-UWB proposal specification," IEEE P802.15 Working Group for WPANs, July 2004.

[6] S. Stroth, "Ultra-wideband: multimedia unplugged," *IEEE Spectrum*, vol. 40, pp. 23-27, September 2003.

[7] G.R. Aiello and G.D. Rogerson, "Ultra-wideband wireless systems," *IEEE Microwave Magazine*, pp. 36-47, June 2003.

[8] W.D. Jones, "No place to hide," *IEEE Spectrum*, vol. 42, pp. 20-21, November 2005.

[9] "Introducing through-wall motion detection radar for military operations in urban terrain," Product Brochure, Time Domain Corporation, Huntsville, Alabama, USA 2004.

[10] "PRISM - portable radar interior space monitor," Product Data Sheet, Cambridge Consultants Ltd, Cambridge, UK 2004.

[11] I. Gresham, A. Jenkins, R. Egri, C. Eswarappa, N. Kinayman, N. Jain, R. Anderson, F. Kolak, R. Wohlert, S.P. Bawell, J. Bennett, and J.-P. Lanteri, "Ultra-wideband radar sensors for short-range vehicular applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 2105-2122, September 2004.

[12] "Road safety: A new push through new technologies," European Commission, September 2003.

[13] R.J. Fontana, "Recent applications of ultra wideband radar and communications system," *Ultra-Wideband, Short-Pulse Electromagnetics 5*, P.D. Smith and S.R. Cloude, eds., New York, NY: Kluwer Academic/Plenum Publ., 2002.

[14] G. Chien, W. Feng, Y.A Hsu, and L. Tse, "A 2.4 GHz CMOS transceiver and baseband processor chipset for 802.11b wireless LAN application," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 358-359, February 2003.

[15] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ: Prentice Hall, 1998.

[16] C.E. Shannon, "A mathematical theory of communications," *Proceedings of the IRE*, vol. 37, pp. 10-21, January 1949.

[17] P. Heydari, "A study of low-power ultra wideband radio transceiver architectures," in *Proceedings of Wireless Communications and Networking Conference*, vol. 2, pp. 758-763, March 2005.

[18] R. Schreier, "ADCs and DACs: marching towards the antenna," in *IEEE International Solid-State Circuits Conference GigaHertz-Radio Front Ends Workshop*, February 2003.

[19] D.D. Wentzloff, R. Blazquez, F.S. Lee, B.P. Ginsburge, J. Powell, and A.P. Chandrakasan, "System design considerations for ultra-wideband communication," *IEEE Communications Magazine*, vol. 43, pp. 114-121, August 2005.

[20] A. Batra *et al.*, "Multi-Band OFDM Physical Layer Proposal", IEEE 802.15-03/267r5, July 2003.

[21] B. Razavi, T. Aytur, F.-R. Yang, R.-H. Yan, H.-C. Kang, C.-C. Hsu, and C.-C. Lee, "A 0.13$\mu$m CMOS UWB transceiver," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 216-217, February 2005.

[22] A. Bevilacqua and A.M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2259-2268 December 2004.

[23] A. Ismail and A.A Abidi, "A 3-10 GHz low-Noise amplifier with wideband LC-ladder matching network," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2269-2277, December 2004.

[24] R. Gharpurey, "Design challenges in emerging broadband wireless systems ," in *Proceeding of IEEE Radio Frequency Integrated Circuits Symposium*, pp. 331-334, June 2005.

[25] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge, U.K.: Cambridge University Press, 1998.

[26] D. Leenaerts, R. van de Beek, G. van der Weide, J. Bergervoet, K.S. Harish, H. Waite, Y. Zhang, C. Razzell, and R. Roovers, "A SiGe BiCMOS 1ns fast hopping frequency synthesizer for UWB radio," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 202-203, February 2005.

[27] J.H McClellan, R.W. Schafer, and M.A. Yoder, *DSP First: A Multimedia Approach*, Upper Saddle River, NJ: Prentice Hall, 1998.

[28] K. Poulton, R. Neff, B. Setterberg, B. Wuppermann, T. Kopley, R. Jewett, J. Pernillo, C. Tan, and A. Montijo, "20GS/s 8 Bit ADC with a 1MB memory in 0.18$\mu$ m CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 318-319, February 2003.

[29] W. Cheng, W. Ali, M.-J. Choi, K. Liu, T. Tat, D. Devendorf, L. Linder, and R. Stevens, "A 3b 40GS/s ADC-DAC in 0.12$\mu$ m SiGe," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 262-263, February 2004.

[30] J. Lee, P. Roux, U.-V. Koc, T. Link, Y. Baeyens, and Y.-K. Chen, "A 5-b 10-GSample/s A/D converter for 10-Gb/s optical receivers," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1671-1678, October 2004.

[31] A.A. Abidi, "RF CMOS comes of age," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 549-561, April 2004.

[32] J.D. Cressler, "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 572-589, May 1998.

[33] J.D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Norwood, MA: Artech House, 2003.

[34] D.C. Ahlgren, G. Freeman, S. Subbanna, R. Groves, D. Greenberg, J. Malinowski, D. Nguyen-Ngoc, S.J. Jeng, K. Stein, K. Schonenberg, D. Kiesling, B. Martin, S. Wu, D.L. Harame, and B. Meyerson, "A SiGe HBT BiCMOS technology for mixed-signal RF applications," in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 195-197, September 1997.

[35] A. Joseph, D. Coolbaugh, M. Zierak, R. Wuthrich, P. Geiss, Z. He, X. Liu, B. Orner, J. Johnson, G. Freeman, D. Ahlgren, B. Jagannathan, L. Lanzerotti, V. Ramachandran, J. Malinowski, H. Chen, J. Chu, P. Gray, R. Johnson, J. Dunn, S. Subbanna, K. Schonenberg, D. Harame, R. Groves, K. Watson, D. Jadus, M. Meghelli, and A. Rylyakov, "A 0.18$\mu$m BiCMOS technology featuring 120/100 GHz ($f_T/f_{max}$) and ASIC-compatible CMOS using copper interconnect," in *Proceedings of the Bipolar/BiCMOS Circuits Circuit Tech. Meeting*, Minneapolis, pp. 143-146, October 2001.

[36] B.A. Orner, Q.Z. Liu, B. Rainey, A. Stricker, P. Geiss, P. Gray, M. Zierak, M. Gordon, D. Collins, V. Ramachandran, W. Hodge, C. Willets, A. Joseph, J. Dunn, J.-S. Rieh, S.-J. Jeng, E. Eld, G. Freeman, and D. Ahlgren, "A 0.13 $\mu$m BiCMOS technology featuring a 200/280 GHz $f_T/f_{max}$ SiGe HBT," in *Proceedings of the Bipolar/BiCMOS Circuit Tech. Meeting*, Toulouse, France, pp. 203-206, September 2003.

[37] B. Heinemann, H. Rücker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K.-E. Ehwald, T. Grabolla, U. Haak, W. Höppner, D. Knoll, D. Krüger, B. Kuck, R. Kurps,

M. Marschmeyer, H.H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, W. Winkler, D. Wolnsky, H.-E. Wulf, Y. Yamamoto, and P. Zaumseil, "Novel collector design for high-speed SiGe:C HBTs," in *IEEE International Electron Devevice Meeting Technical Digest*, pp. 775-778, December 2002.

[38] J.-S. Rieh, B. Jagannathan, H. Chen, K.T. Schonenberg, D. Angell, A. Chinthakindi, J. Florkey, F. Golan, D. Greenberg, S.-J. Jeng, M. Khater, F. Pagette, C. Schnabel, P. Smith, A. Stricker, K. Vaed, R. Volant, D. Ahlgren, G. Freeman, K. Stein, S. Subbanna, "SiGe HBTs with cut-off frequency of 350 GHz," in *IEEE International Electron Devevice Meeting Technical Digest*, pp. 771-774, December 2002.

[39] B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, T. Grabolla, U. Haak, W. Höppner, D. Knoll, K. Köpke, B. Kuck, R. Kurps, S. Marschmeyer, H.H. Richter, H. Rücker, P. Schley, D. Schmidt, W. Winkler, D. Wolansky, H.-E. Wulf, and Y. Yamamoto "A low-parasitic collector construction for high-speed SiGe:C HBTs," in *IEEE International Electron Devevice Meeting Technical Digest*, pp. 251-254, December 2004.

[40] B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, O. Fursenko, M. Glante, K. Glowatzki, A. Gregor, U. Haak, W. Höppner, D. Knoll, R. Kurps, S. Marschmeyer, S. Orlowski, H. Rücker, P. Schley, D. Schmidt, R. Scholz, W. Winkler, and Y. Yamamoto, "A complementary BiCMOS technology with high speed npn and pnp SiGe:C HBTs," in *IEEE International Electron Devevice Meeting Technical Digest*, pp. 117-120, December 2003.

[41] W.-M.L. Kuo, Y. Lu, B. Floyd, B. Haugerud, A. Sutton, R. Krithivasan, J.D. Cressler, B. Gaucher, P. Marshall, R. Reed, J.-S. Rieh, and G. Freeman, "Total dose tolerance of monolithic millimeter-wave transceiver building blocks in 200 GHz SiGe technology," *IEEE Transactions on Nuclear Science*, vol. 51, pp. 3781-3787, 2004.

[42] B.M. Ballweber, R. Gupta, and D.J. Allstot, "A fully integrated 0.5-5.5 GHz CMOS Distributed Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 231-239, Ferbruary 2000.

[43] R.-C. Liu, C.-S. Lin, K.-L. Deng, and H. Wang, "A 0.5-14G-Hz 10.6dB CMOS Cascode Distributed Amplifier," in *Symposium on VLSl Circuits Digest of Technical Papers*, pp. 382-383, June 2003.

[44] R.-C. Liu, K.-L. Deng, and H. Wang, "A 0.5-22G-Hz Broadband CMOS Distributed Amplifier," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*, pp. 103-106, June 2003.

[45] N. Shiramizu, T. Masuda, M. Tanabe, and K. Washio "A 3-10 GHz Bandwidth Low-noise and Low-power Amplifier for Full-band UWB Communications in 0.25-um SiGe BiCMOS Technology," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*. pp. 39-42, June 2005.

[46] F. Bruccoleri, E.A.M. Klumperink, and B. Nauta, "Noise canceling in CMOS LNA's," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 406-407, Ferbruary 2002

[47] M.C. Chiang, S.-S. Lu, C.-C. Meng, S.-A. Yu, S.-C. Yang, and Y.-J. Chan, "Analysis, Design, and Optimization of InGaP-GaAs HBT Matched-Impedance Wide-Band Amplifiers With Multiple Feedback Loops," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 6, pp. 694-701, June 2002.

[48] W.M. Leach, Jr., *ECE 6416 Low noise electronic design class notes*, Georgia Insitute of Technology, Fall 2004.

[49] J. Rogers and C. Plett, *Radio frequency integrated circuit Design*, Artech House Publishers, 2003.

[50] R.G. Meyer, and W.D. Mack, "A 1-GHz BiCMOS RF Front-end IC," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 350-355, March 1994.

[51] S.P. Voinigescu, M.C. Maliepaard, J.L. Showell, G.E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D.L. Harame, "A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1430-1439, September 1997.

[52] D.K. Shaefer, and T.H. Lee, "A 1.5V 1.5-GHz CMOS Low Noise Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 745-759, May 1997.

[53] C.W. Kim, M.-S. Kang, P.-T. Anh, H.-T. Kim, and S.-G. Lee, "An Ultra-Wideband CMOS Low Noise Amplifier for 2-5-GHz UWB system," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 544-547, Ferbruary 2005.

[54] J. Lee and J.D. Cressler, "A 3-10 GHz SiGe Resistive Feedback Low Noise Amplifier for UWB Applications," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*, pp. 545-548, June 2005.

[55] H. Hashemi, and A. Hajimiri, "Concurrent Multiband Low-Noise Amplifiers-Theory, Design, and Application," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 288-301, January 2002.

[56] J. Park, C.-H. Lee, J.D. Cressler, J. Laskar and A. Joseph "A Very Low Power SiGe LNA for UWB Application," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 1041-1044, June 2005.

[57] M.-D. Tsai, K.-Y. Lin, and H. Wang "A 5.4-mW LNA Using 0.35-$\mu$m SiGe BiCMOS Technology for 3.1-10.6-GHz UWB Wireless Receivers," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*. pp. 335-338, June 2005.

[58] M.T. Reiha, J.R. Long and J.J. Pekarik, "A 1.2 V reactive-feedback 3.1-10.6 GHz ultrawideband low-noise amplifier in 0.13 $\mu$m CMOS," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*. pp. 55-58, June 2006.

[59] Y. Lu, R. Krithivasan, W.-M.L. Kuo, and J.D. Cressler, "A 1.8-3.1 dB noise figure (3-10 GHz) SiGe HBT LNA for UWB applications," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*. pp. 59-62, June 2006.

[60] S. Shekhar, X. Li and D.J. Allstot, "A CMOS 3.1-10.6 GHz UWB LNA employing stagger-compensated series peaking," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*. pp. 63-66, June 2006.

[61] C.-T Fu and C.-N. Kuo, "3 11-GHz CMOS UWB LNA using dual feedback for broadband matching," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*. pp. 67-70, June 2006.

[62] B. Shi and Y.W. Chia, "A SiGe low-noise amplifier for 3.1-10.6 GHz ultra-wideband wireless receivers," in *Proceedings of the Radio Frequency Integrated Circuits Symposium*. pp. 71-74, June 2006.

[63] B. Razavi, *Principles of data conversion system design,* Piscataway, NJ: IEEE Press, 1995.

[64] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and design of analog integrated circuits,* Fourth Edition, John Wiley & Sons, Inc. 2001.

[65] P. Vorekamp, and J.P.M. Verdaasdonk, "Fully bipolar, 120-Msamples/s 10-b track-and-hold circuit," *IEEE Journal of Solid-State Circuits*, vol. 27, pp. 988-992, July 1992.

[66] C. Fiocchi, U. Gatti, and F. Maloberti, "Design issues on high-speed high-resolution track-and-holds in BiCOMS technology," *IEE Proceedings - Circuits, Devices and Systems*, vol. 147, pp. 100-106, April 2000.

[67] A. Razzaghi and M.C.F Chang, "A 10b, 1-GSample/s track-and-hold amplifier using SiGe BiCMOS technology," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 433-436, September 2003.

[68] J.C. Jensen, L.E. Larson, "A broadband 10-GHz track-and-hold in Si/SiGe HBT technology," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 325-330, March 2001.

[69] T. Baumheinrich, B. Prégardierr, and U. Langmann,, "A 1-Gsample/s 10-b full Nyquist silicon bipolar track hold IC," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1951-1960, December 1997.

[70] B. Prégardier, U. Langmann, and W.J. Hillery, "A 1.2-Gs/s 8-b silicon bipolar track hold IC," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1336-1339, Semptember 1996.

[71] F. Vessal and C.A.T Salama, "A bipolar 2-GSamples/s track-and-hold amplifier (THA) in 0.35 $\mu$m SiGe technology," in *Proceedings of the International Symposium on Circuits and Systems*, vol. 5, pp. 573-576, May 2002.

[72] Y. Lu, W.-M. L. Kuo, X. Li, R. Krithivasan, J.D. Cressler, Y. Borokhovych, H. Gustat, B. Tillack, and B. Heinemann, "An 8-bit 12 GSample/sec SiGe Track-and-Hold Amplifier," in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 148-151, October 2005.

[73] H. Voorman and H. Veenstra, "Tunable high-frequency gm-C filters," *IEEE Journal of Solid-State Circuits*, 35, pp. 1097-1108, August 2000.

[74] J.C. Schmoock, "An input stage transconductance reduction technique for high-slew rate operational amplifiers," *IEEE Journal of Solid-State Circuits*, 10, pp. 407-411, December 1975.

[75] J. Harrison and N. Weste, "A 500MHz CMOS anti-alias filter using feed-forward op-amps with local common-mode feedback," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 481-483, Ferbruary 2003.

[76] H. Tanimoto, M. Koyama, and Y. Yoshida, "Realization of a 1-V active filter using a linearization technique employing plurality of emitter-coupled pairs," *IEEE Journal of Solid-State Circuits*, 26, pp. 937-945, July 1991.

[77] S. Lida, K. Tanaka1, H. Suzuki, N. Yoshikawa, N. Shoji, B. Griffiths, D. Mellor, F. Hayden, I. Butler, and J. Chatwin, "A 3.1 to 5 GHz CMOS DSSS UWB transceiver for WPANs," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 214-215, Ferbruary 2005.

[78] S. Dosho, T. Morie, and H. Fujiyama, "A 200-MHz seventh-order equiripple continuous-time filter by design of nonlinearity suppression in 0.25-$\mu$m CMOS process," *IEEE Journal of Solid-State Circuits*, 37, pp. 559-565, May 2002.

[79] Y. Lu, R. Krithivasan, W.-M. L. Kuo, X. Li, J.D. Cressler, H. Gustat, and B. Heinemann, "A 70 MHz - 4.1 GHz 5th-order elliptic gm-C low-pass filter in complementary SiGe technology," in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 80-83, October 2006.

[80] K.M. Murray, W.J. Stapor, and C. Castenada, "Calibrated charge particle measurement system with precision dosimetric measurement and control," *Nuclear Instrument and Methods in Physics Research, Section A (Accelerators, Spectrometers, Detectors and Associated Equipment)*, vol. A281, pp. 616-621, September 1989.

[81] P.W. Marshall, C.J. Dale, M.A. Carts, and K.A. LaBel, "Particle-induced bit errors in high performance fiber optic data links for satellite data management," *IEEE Transactions on Nuclear Science*, vol. 41, pp. 1958-1965, December 1994.

[82] S. Zhang, G. Niu, S.D. Clark, J.D. Cressler, and M. Palmer, "The effects of proton irradiation on the RF performance of SiGeHBTs", *IEEE Transactions on Nuclear Science*, vol. 46, pp. 1716-1721, December 1999.

[83] J.D. Cressler, R. Krithivasan, G. Zhang, G. Niu, P. Marshall, H. Kim, R. Reed, M. Palmer, and A. Joseph, "An Investigation of the Origins of the Variable Proton Tolerance in Multiple SiGe HBT BiCMOS Technology Generations", *IEEE Transactions on Nuclear Science*, vol. 49, pp. 3203-3207, December 2002.

[84] Y. Lu, J.D. Cressler, R. Krithivasan, Y. Li, R.A. Reed, P.W. Marshall, C. Polar, G. Freeman, and D. Ahlgren, "A Proton tolerance of third-generation 0.12 $\mu$m 185 GHz SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol. 50, pp. 1811-1815, December 2003.

# VITA

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