MODELING OF INTEGRATED VOLTAGE REGULATOR POWER DELIVERY SYSTEMS

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Nihar Dasari

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MODELING OF INTEGRATED VOLTAGE REGULATOR POWER DELIVERY SYSTEMS

Thesis committee:

Dr. Saibal Mukhopadhyay
Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Tushar Krishna
Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Hyesoon Kim
College of Computing
Georgia Institute of Technology

Date approved: December 4, 2020

Objectivity consists in understanding that the only one who never makes a mistake is the one who never does anything.

Vladimir Kramnik

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SUMMARY

Distributed power delivery poses new power design challenges in modern ICs, requiring circuit level techniques to convert and regulate power at points-of-load (POL), methodological solutions for distributing on-chip power supplies, and automated design techniques to co-design distributed power supplies and decoupling capacitors. Integration of on chip inductive DC-DC voltage regulators has become a popular way to design SOCs with improved power efficiency and performance. Such distributed power systems are highly complex because of their multi parametric interactive behavior. The various parameters encompass the voltage sources (input and reference voltages), loads, power semiconductors, and control circuits. Behavioural analysis, prior to prototyping, of such complex is possible only by suitable simulations. This thesis aims to study the the design and construction of a combined IVR and LDO system model using Simulink and MATLAB.

CHAPTER 1
INTRODUCTION

1.1 Background and problem statement

In earlier generations of technology, off chip voltage convertors were used to deliver DC voltages and currents to on-chip load circuitry. However, in order to maintain sufficient quality of power under increasing current densities and parasitic impedance, the power distribution system needs to be have locally regulated with distributed on-chip voltage converters close to the load. This concept of distributed power delivery poses new power design challenges in modern ICs, requiring circuit level techniques to convert and regulate power at points-of-load (POL), methodological solutions for distributing on-chip power supplies, and automated design techniques to co-design distributed power supplies and decoupling capacitors [1]. The integration of inductive voltage regulators with onchip/on-package inductors on the same chip as the digital logic cores helps fast recovery from voltage droops (load transient) and a fast transition of the output voltage (reference transient) to support dynamic voltage and frequency scaling (DVFS) [2]. Also, DVFS is one of the most popular options to reduce CMOS power consumption [3, 4]. However, efficacy of traditional off chip Voltage Regulator Modules (VRM) for DVFS applications is limited due to their slow response time, low switching frequency and the presence of increased parasitics between the VRs and their loads [5]. Hence integrated voltage regulators have become popular in providing multicore systems with point of load regulation to multiple voltage domains, operating at high frequency with fast control loops and reduced parasitics [6, 7, 8, 9, 10].

Circuit designs trending towards using multiple cores on a chip, lead to a need to regulate of multiple power domains [6], while still providing quick response to load changes along with the the ability to perform DVFS. Point-of-load regulation using digital low

dropout (DLDO) regulators to provide post regulation in conjunctions with inductive voltage regulators present a suitable solution due to their fast transient response and the ability to create a new voltage domains[11]. This distributed power delivery architecture is shown in Figure 1.1, with the power being brought onto the chip by a single IVR and feeding multiple LDOs to different parts of the circuit. This thesis aims to study the the design and construction of a combined IVR and LDO system model using Simulink and MATLAB. The reasons for doing so are multifold. Firstly, it provides an avenue for design space exploration in the early phases of developing a power delivery system without the need for arduous SPICE simulations. Secondly, we can also study the interactions between the two systems and the need for them to be developed together in order to fine tune system performance.

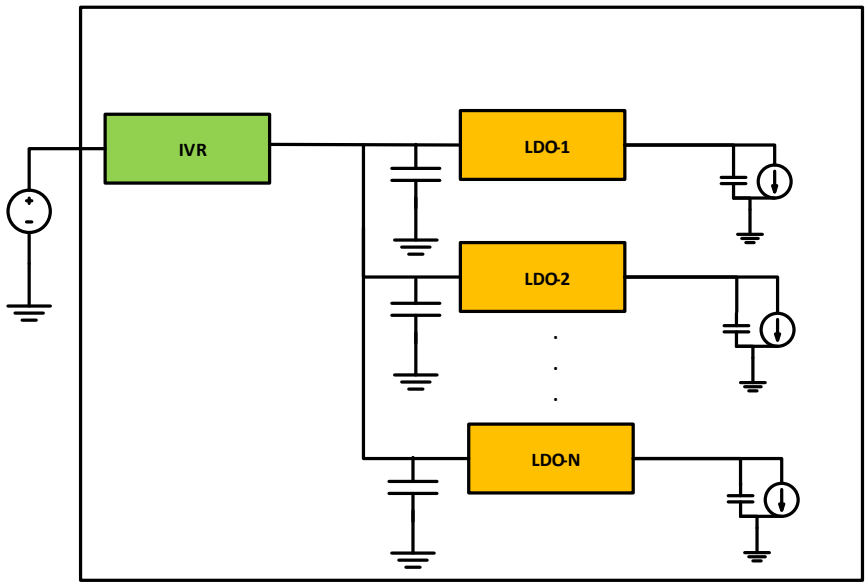

Figure 1.1: Distributed power delivery in an SoC

The work involved the following tasks:

1. IVR: Understanding the analytical model & development of simulation model

2. LDO: Understanding the analytical model & development of simulation model

3. Combined model: Understanding the analytical model & development of simulation model

4. Frame work development

1.2 Thesis outline

Chapter 2 presents the literature survey done. Chapter 3 discusses the mathematical models of IVR, LDO and combined IVR-LDO. Chapter 4 presents the simulation framework while chapter 5 details the evaluation results. Finally, chapter 6 discusses the conclusions with future work scope. In the next chapter, the detailed literature survey from the perspectives as depicted in Figure 1.2 are described.

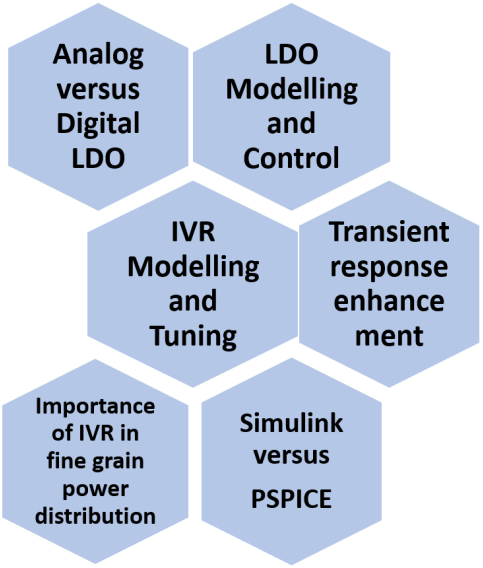

Figure 1.2: Perspectives of Literature Survey

CHAPTER 2

LITERATURE SURVEY

Literature survey findings are presented in this chapter. The take away points of this survey, from different perspectives as listed below, have motivated and formed the basis for the work presented in this thesis.

- Importance of IVR in fine grained power distribution circuits (as discussed in chapter 1)
- LDO modelling and control
- IVR modelling and tuning
- Analog versus digital LDOs comparison
- Digital LDO transient behaviour enhancement importance and techniques.
- The advantages of Simulink models over spice models

2.1 LDO modelling and control

The most common topologies used for implementing power delivery in SoCs are linear and switching regulators. Low dropout regulators (LDOs) are used to provide power, with quick transient response and low output ripple compared to switching regulators. Their small footprint makes them an attractive option for point of load regulation, especially in designs with multiple voltage domains [12, 13, 14]. In [12], the discussion is on an an active filter-based on-chip DC–DC voltage converter for application to distributed on-chip power supplies in multivoltage systems. The circuit proposed is as an alternative to classical LDO voltage regulators. Similarly, in [13], a fully-integrated low-dropout regulator (LDO) is proposed, which is realized using a tri-loop LDO architecture in a 65 nm CMOS process. [14] proposes a two sampling frequency circuit model using low sampling and high sampling in the same circuit. In this paper the advantages by controlling the sampling

frequency under different conditions were seen. [15] highlights the challenges involved in DLDO design for digital design with multiple voltage scenarios. The circuit here has been designed in 32nm CMOS for fine-grained power delivery to multi-Vcc digital circuits using a fully-digital voltage-scalable LDO based on a secondorder phase-locked loop. In [15], having realized the challenges of power delivery and voltage delivery in fine-grained voltage domains of power constrained digital circuits, a fully-digital phase-locked low dropout regulator (LDO) has been designed in 32nm CMOS for fine-grained power delivery to multi-Vcc digital circuits. The scenario considered was one in which high-speed local adjustments to the supply are required, wherein, the distribution of regulated supply and a local drop down by an embedded LDO is used in general. These scenarios have the requirements of compactness, high efficiency and large signal operation having higher priority over high supply voltage rejection. Usage of an analog feedback loop to suppress an error voltage, though accurate can result in incompatibilities with the digital design flow. This paper discusses a compact fully-digital voltage-scalable LDO based on a second order phase-locked loop.

[16] provides a comprehensive methodology, based on Mason's Gain Formula applied to hybrid control, for modeling and analyzing distributed linear regulators and their interaction with the PDN. It was shown that when multiple LDOs drive a common voltage grid, significant loss of phase margin can occur.

The stability and transient performance improvements of DLDOs are based on using a clock-based comparator as an error amplifier have been well addressed in literature. [17] aims to propose the use of sliding-mode control (SMC), as the controller of DLDO instead of the conventional clock-based comparator. In the proposed controller, the design is based on SMC-based DLDO, whose state-space model and sliding coefficients are extracted by considering the hitting and existence conditions. Further, a solution towards the chattering problem of sliding-mode control is also provided in the form of compensation by introducing additional control signal, named freeze control signal. The proposed SMC-based

DLDO is implemented and validated using Matlab/Simulink. In [18], a control model for discrete time LDOs and online adaptive control for consistent performance and high efficiency across the load current range, is presented in detail.

2.2 Analog versus digital LDOs

Low-dropout (LDO) regulators are widely used in analog, mixed-mode, and RF applications. While analog control of LDOs is a common solution, using digital control provides easier implementation and scalability of the design [19]. LDOs working in analog domain, in general use a large off-chip capacitor for stability requirements which is detrimental to SoC applications. On the other hand, there are some design challenges to obtain analog external capacitorless LDOs (CL-LDOs) including dynamic performance (i.e., load/line transient), and stability problems, especially at no-load and lightload conditions. Digital LDOs (DLDOs) offer advantages in terms of scalability, programmability, stability over a wide range of load currents. The importance of Digital low-dropout regulators (DLDOs) is because of their low voltage operation and process scalability.

2.3 IVR Modelling and tuning

The integration of inductive voltage regulators with onchip/on-package inductors on the same chip as the digital logic cores helps fast recovery from voltage droops (load transient) and a fast transition of the output voltage (reference transient) to support dynamic voltage and frequency scaling (DVFS) [11]. Aging, temperature and process variations affects performance of the IVRs, as any digital circuit, in deep nanometer process. Especially, variations in on-chip/on-package passives (inductance and capacitance) causes shift in the IVR's characteristics including transient response to load step and reference step resulting in an increase of the error rates. The solution lies in the development of auto-tuning mechanisms for IVR to minimize the effect of IVR's variations on the voltage/timing margin or timing error rates of digital cores. This paper presents an auto-tuning method for fully inte-

grated voltage regulators (IVRs) driving digital cores against variations in passive as well as process/temperature of the core. This paper shows the simulations using a high-frequency IVR Simulink model and digital logic in 45nm CMOS process shows that the proposed per6 formance driven auto-tuning demonstrates potential increase in system performance under inductance and threshold variation.

[20] shows a modeling approach called Ivory, to use for early design space exploration of IVR design. It uses the static and dynamic models of IVRs to study the tradeoffs of using different IVR configurations. Point-of-load regulation using digital low dropout (DLDO) regulators to provide post regulation in conjunctions with inductive voltage regulators, present a suitable solution due to their fast transient response and the ability to create a new voltage domains.

2.4 Digital LDO Transient behaviour enhancement importance and techniques

The usage of Simulink/MATLAB to model the transient response of a DLDO with a shifter is shown in [21]. It was brought out that because of the combination of discrete and continuous time operation as well the non-linearity involved the prediction of digital LDO performance in the early design stage is difficult. A time-domain behavior model in MATLAB/Simulink was built to estimate transient response performance of DLDO and voltage ripple in steady state. Digital LDO designs can be classified into i) Designs that utilize a comparator to detect the difference between the output and the reference level. They use discrete time circuits and use arrays of PMOS transistors as the power device ii) Those that translate such voltage difference into other information in order to adjust the voltage at the gate of the power device to control the output voltage. It is desirable to have fast and accurate response to large transient changes at load current or input voltage. This motivated significant research efforts on methods to predict the transient response to such changes as well as techniques to improve the LDO transient response [22]. [23] discusses a fully digital LDO with wide load range and fast transient response. High regulate accuracy is

maintained in full load range by dividing the power PMOSs into 10 different blocks with different unit-cell sizes. Light load is associated with small size power PMOSs selection while heavier loads use bigger ones, turned on/off by DLDO, in order to ensure accuracy. Also, application of a binary-search like algorithm is proposed to improve the transient speed. [21] highlights on how the transient behavior of an LDO plays an important role in the performance of an LDO. It is challenging to derive the closed-loop transfer function of the digital LDO control loop because of the variable feedback factor in the digital LDO control loop. Estimation of the digital LDO transient behaviour from its open-loop transfer function is not accurate because of the assumption that the feedback factor does not change during the system settling process. This motivated the development of simulation models as well as closed-form expressions for estimating the LDO output settling behaviour with changes in load current or reference voltage. Usage of the estimation equations for the magnitude and frequency of LDO output steady-state ripples, in the design space exploration have also been discussed.

2.5 MATLAB/Simulink versus PSPICE as modelling tools for power systems and power electronics

Modern power systems and power electronic are highly complex because of their multi parametric interactive behavior. The various parameters encompass the voltage sources (input and reference voltages), loads, power semiconductors, and control circuits. Further complexity in the interactions is because of the nonlinear behavior of the power semiconductors and the different magnitudes of the circuit's time constants. Behavioural analysis prior to prototyping of such complex interactions is possible only by suitable simulations. Capabilities of various simulators designed to simulate sample power electronic systems have been evaluated in literature.

The comparison of PSB with PSPice can be found in [24], which is relevant for this thesis as PSB uses the MATLAB environment to represent common components and devices

found in electrical power networks. Simulink's graphical interface provides a user-friendly environment where the power circuit and control system are represented in the same diagram with runtime display of the results. PSpice power system simulation has the following advantages i) An User-friendly interface for data entry (schematic capture) and output data processing. ii) Detailed models of electronic components Abundant libraries of electronic components (including several power electronic devices) and control ICs. iii) Capability of simulating mixed-signal (analog and digital) systems. Disadvantages of PSpice in power systems simulation are i) The simulation is not interactive. ii) The user has little control on the integration process iii) Electric machine and power component models (in particular three-phase components) are not available. The PSB is well suited to the simulation of medium size power systems and power electronics using variable or fixed step algorithms from Simulink. The PSB libraries contain basic elements as well as many ready-built subsystems. Control systems using Simulink blocks can be naturally integrated into the power system model. The computation capabilities of MATLAB/Simulink can be advantageously exploited in post-processing of the simulation results. In the study of power systems, it was found that PSpice suits well for device-level modeling of small size systems. The simulation of larger size power systems resulted in excessive execution time.

[20] shows the advantages of using a a fast, non SPICE based modeling approach to use for early design space exploration of IVR design. A high-level design space exploration tool capable of providing accurate conversion efficiency, static performance characteristics, and dynamic transient responses of an IVR-enabled power delivery subsystem (PDS), enabling rapid trade-off exploration at early design stage, approximately 1000 x faster than SPICE simulation, called Ivory is presented.

CHAPTER 3

ANALYTICAL MODELING

3.1 IVR Modelling

The IVR is implemented as a switched inductor voltage regulator. The overall stucture of the IVR is shown in Figure 3.1. It consists of a power stage, that has a PMOS and an NMOS that act as a switch along with an inductor (L) and a decoupling capacitor C, with ESR_L and ESR_C being their corresponding equivalent series resistances (ESRs). This power stage operates in a closed loop using a digital proportional–integral–derivative (PID) compensator to improve bandwidth and provide improved line and load regulation regulation. The error at the output is sampled by a analog-to-digital converter (ADC) at the rate $F_{samp} = NF_{SW}$, where F_{SW} is the switching frequency of the system, $N = 1$ in the case of single sampled systems and $N > 1$ for multisampled systems. The output of the compensator is the duty cycle commend d[n], that is the input to a Digital Pulse Width Modulator (DPWM), which provides the switching signal at the correct duty cycle required for output regulation. IVRs are generally operated at a high switching frequency (F_{SW}) to provide quick transient response to the system and low output ripple for smaller values of L and C. V_{in} is the input voltage provided to the system, and V_{OUT} is connected to the load which requires the regulated power supply.

The continuous time transfer function for the IVR's power stage is as follows,

$$G_{vd}(s) = V_{in}\frac{1 + sESR_C}{1 + s(ESR_L + ESR_c) + s^2LC}e^{-st_d} \tag{3.1}$$

$$t_d = t_{ADC} + t_{compensator} + t_{DPWM} \tag{3.2}$$

Here, t_d is the internal delay of the system, which consists of ADC delay (t_{ADC}), DPWM

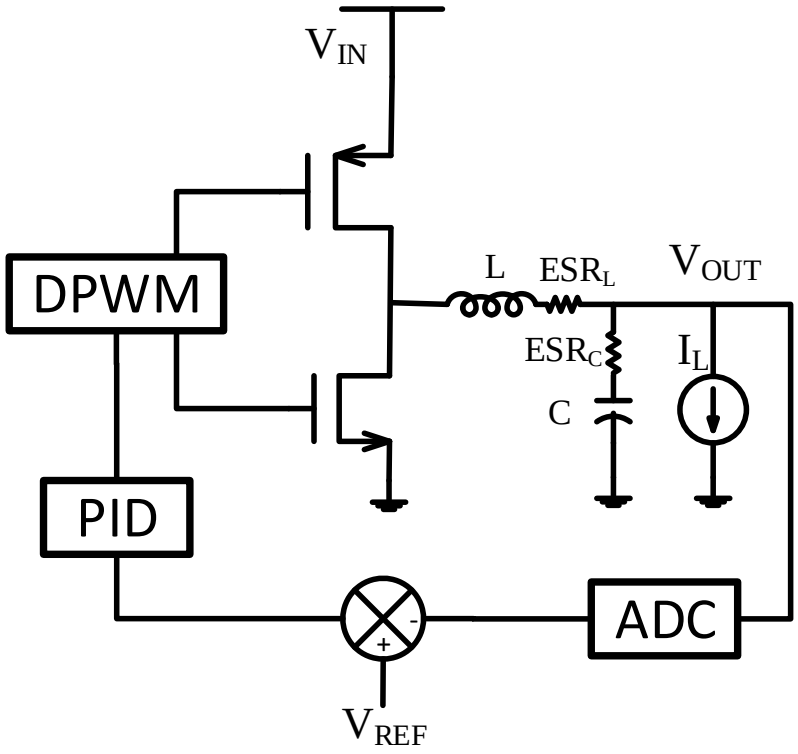

Figure 3.1: Inductive switched dc-dc regulator

delay (t_{DPWM}) and PID compensator delay ($t_{compensator}$) while In order to study the system loop behaviour in the discrete domain, we convert the continuous transfer function ($G_{vd}(s)$) to the discrete time ($G_{vd}(z)$) using the bilinear transform,

$$z = e^{sT_{samp}} \tag{3.3}$$

The transfer function of the ADC is,

$$G_{ADC}(z) = qz^{-1} \tag{3.4}$$

with $q = \frac{V_{range}}{2^n}$ being the ADC resolution for an n bit ADC and T_{samp} is the sampling frequency of the ADC. The digitised error is passed on to a digital type III compensator

(two poles and two zeroes) implemented in direct form,

$$G_{comp}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 - z^{-1}} \tag{3.5}$$

Multisampling, which is running the system's clock frequency at a higher frequency than switching frequency, can help reduce the effective delay of the DPWM and improve bandwidth of the compensated system. The DPWM compares the duty cycle command to a trailing edge sawtooth waveform to generate a Pulse width modulated signal with duty cycle $D = \frac{V_{in}}{V_{out}}$ that drives the power stage, completing the loop. The DPWM delay is given by [25],

$$t_{DPWM} = DTs - \frac{\text{floor}(ND)}{NT_s} \tag{3.6}$$

In order for the voltage regulator to be stable, careful design of the compensator is imperative. The design of the compensator requires consideration of the power stage parasitics, i.e. the inductor and capacitor equivalent series resistances (R_L and R_C), the operating frequency and limitations placed on transient performance by the external PDN.

Thus, the total loop gain is given by,

$$T(z) = G_{vd}(z) G_{comp}(z) G_{ADC}(z) \tag{3.7}$$

3.2 Digital LDO modeling

Digital Low dropout regulators are used to provide stable output voltage, with lower passive footprint than compared to IVRs due to the lack of inductance required. It consists of a PMOS array with an output capacitor (C), with compensation provided by a type III compensator, similar to the one described in the previous section. Digital LDOs do not have a large efficiency overhead as compared to switched inductor based DC-DC converter at low voltage dropouts but suffer significantly when they have to provide a larger range of

frequencies, possibly limiting their efficacy for DVFS applications. The overall architecture of the LDO is shown in Figure 3.2. The DLDO provides regulation by turning of the required number of PMOS devices in the array to supply the load current (I_L) for a fixed dropout. The control loop is similar to that of the IVR described previously.

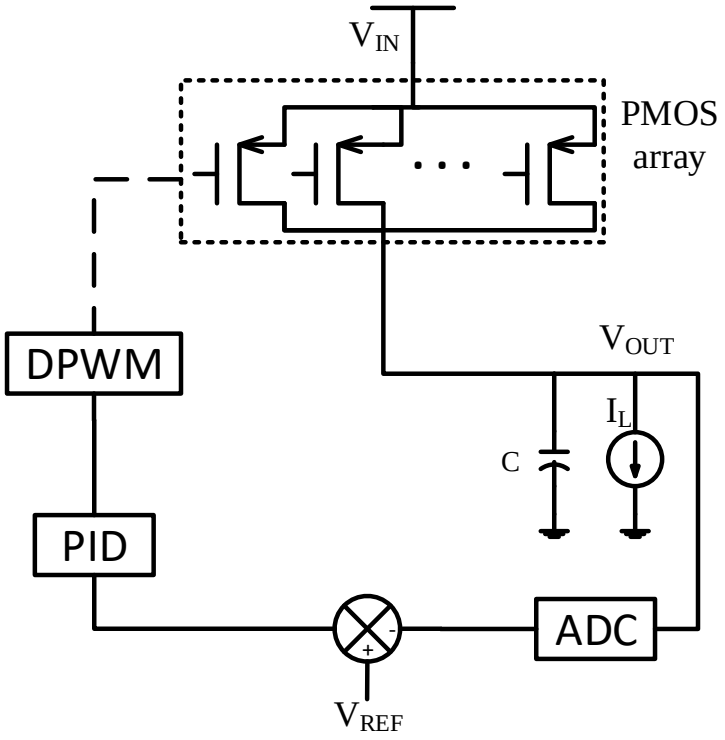

Figure 3.2: Digital Low Dropout regulator

The ADC samples and digitises the error at the point of regulation which is passed on to the PID compensator, whose output is decoded to turn on the PMOS devices. Here we describe the transfer function of the DLDO:

$$G(z) = G_o \frac{(1 - e^{\frac{\omega_L}{F_s}})}{(z - e^{\frac{\omega_L}{F_s}})} \tag{3.8}$$

$$G_o = I_{PMOS} \times (R_{PMOS} || R_L) \tag{3.9}$$

$$\omega_L = ((R_P || R_L)C)^{-1} \tag{3.10}$$

$$R_P = \frac{V_{in} - V_{out}}{I_L} \tag{3.11}$$

Where I_{PMOS} is the current carried by one PMOS device, and R_P is the equivalent resistance of the on PMOS devices at steady state, R_L is the load resistance, F_s is the sampling frequency. Similar to the IVR, V_{in} and V_{out}

The compensator is a type III compensator, similar to the IVR, but is implemented in parallel form:

$$G_{comp}(z) = K_p + \frac{K_i}{1 - z^{-1}} + K_d(1 - z^{-1}) \tag{3.12}$$

$$T(z) = G(z)G_{comp}(z)G_{ADC}(z) \tag{3.13}$$

3.3 Combined IVR-LDO Modeling

This section describes the modelling of the combined IVR-LDO system. Firstly we start with the most basic case where there exists one IVR and on DLDO with the output of the IVR serving as the voltage input of the LDO whose output is the load being driven, as shown in Figure 3.4

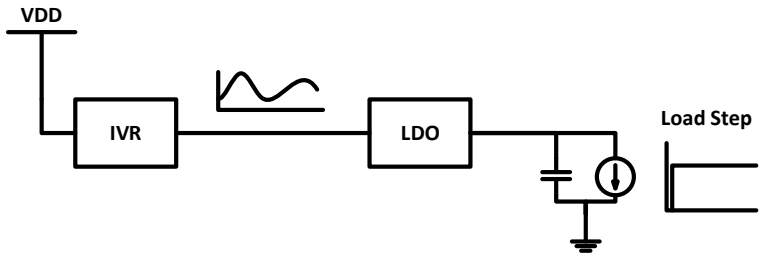

Figure 3.3: IVR-LDO system

In order to study the combined system, we need to look at the the effect of the LDO on the IVR. The input impedance of the LDO can be obtained from the equations [26],

$$\frac{\partial V_{LDO}}{\partial V_{in}} = \frac{g_m R_{PMOS} + 1}{sC_{LDO}R_{PMOS} + 1} \frac{1}{1 + A_{LG}} \tag{3.14}$$

$$Z_{LDO} = \frac{1}{sC_{LDO}} \frac{sC_{LDO}R_{PMOS} + 1}{g_m R_{PMOS} + 1}(1 + A_{LG}) \tag{3.15}$$

Equation 3.14 is the expression for the Power Supply Rejection Ratio (PSRR) of the LDO, using which we can derive the input impedance of the LDO (Z_{LDO}), which acts as the load for the IVR output.

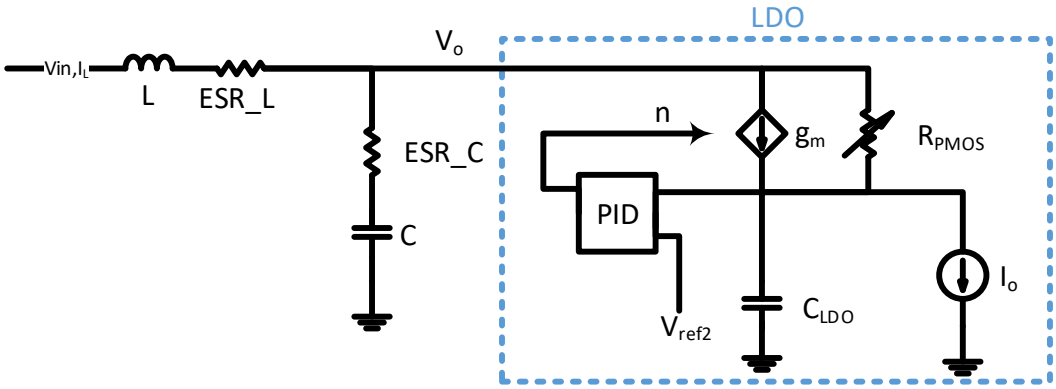

Figure 3.4: Combined system schematic

Looking at Figure 3.4, we can see that the LDO's input impedance, Z_{LDO} is loading the IVR in parallel to the capacitor, which we can use to obtain the new open loop transfer function of the IVR using $Z_{eq} = Z_C || Z_{LDO}$. This model can be easily extended to multiple LDOs by assuming the impedance provided by the LDO all act in parallel.

Figure 3.5 shows the bode plots of an IVR in isolation (Figure 5.2) and an IVR with an LDO on its load. Due to the high magnitude of the Z_{LDO} due to the closed loop gain of the LDO, we see the open loop bandwidth of the IVR is not affected, but the phase is, and therefore shows why it is imperative to consider the loading effect of the LDO while designing the compensator for the IVR.

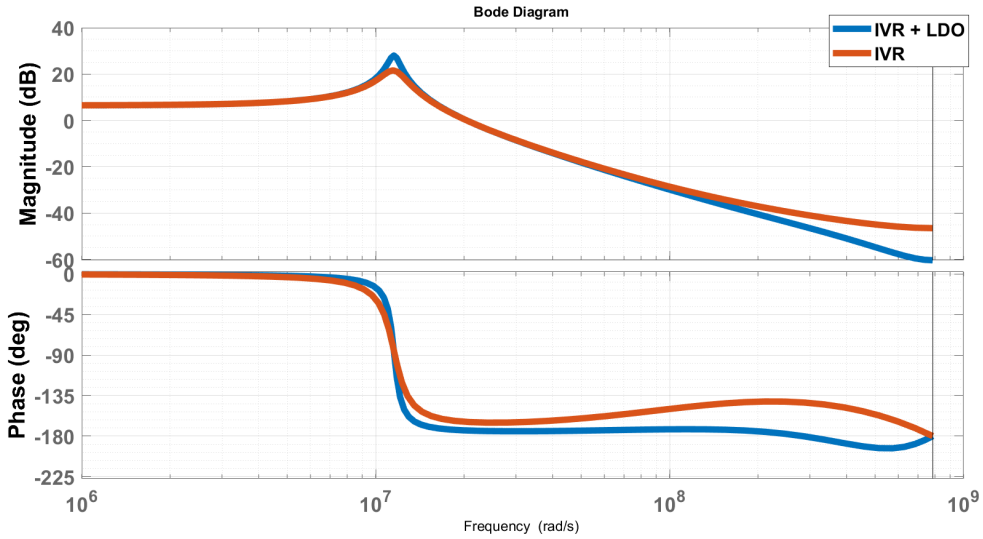

Figure 3.5: Combined system bode plots

CHAPTER 4
SIMULATION FRAMEWORK

4.1 Overview

The IVR and LDO are simulated using MATLAB and Simulink based models. The converters are modeled based on their characteristic equations in a Simulink environment and the compensator design and wrapper functions are written in MATLAB. Figure 4.1 shows the framework that has been developed. The .csv file serves as the input to the system and contains the design parameters such as V_{in}, V_{out}, the values of the passive components and their parasitic resistances (L, C, ESR_L, ESR_C), the target load current (I_L), the switching frequency (F_{SW}), and the bit precision details of the PID compensator, ADC and DPWM. All these are required to generate the PID coefficients for the required voltage regulator. A set of sample values are shown in Table 4.1. The target settling time T_{s_target} can be passed as a design constraint. The Simulink model contains the equations for the power stage, a source that is used as the current load, the ADC block which samples the output voltage and converts it into a digital word. The ADC samples the output at $F_{samp} = NF_{SW}$ which is subtracted from the digital voltage word corresponding the V_{ref}. The ADC used for the simulations is assumed to be a SAR ADC which has a delay of 1 clock cycle. This error signal is send to the PID compensator. The PID compensator is the block that the designed coefficients are entered into, and the DPWM converts the PID compensator output to a signal that is used as the input to the power stage. The DPWM contains a falling edge sawtooth waveform that switches at the switching frequency F_{SW} this is compared to the duty cycle command from the compensator to turn on and off the PMOS switches to generate the required duty cycle (D) for voltage regulation. Appendices contain the schematic details of the Simulink blocks. The output waveforms of the simulation is stored in .mat

files. These files are used to check if the transient behaviour is within the the set constraint. The successful completion of simulation exits the loop, else the simulation cycle is re-run for different set of PID coefficients.The PID/compensator design aims to generate an IVR with maximum possible bandwidth to get minimum settling time.This simulation cycle is as represented by algorithm 1 as a PID tuning method.

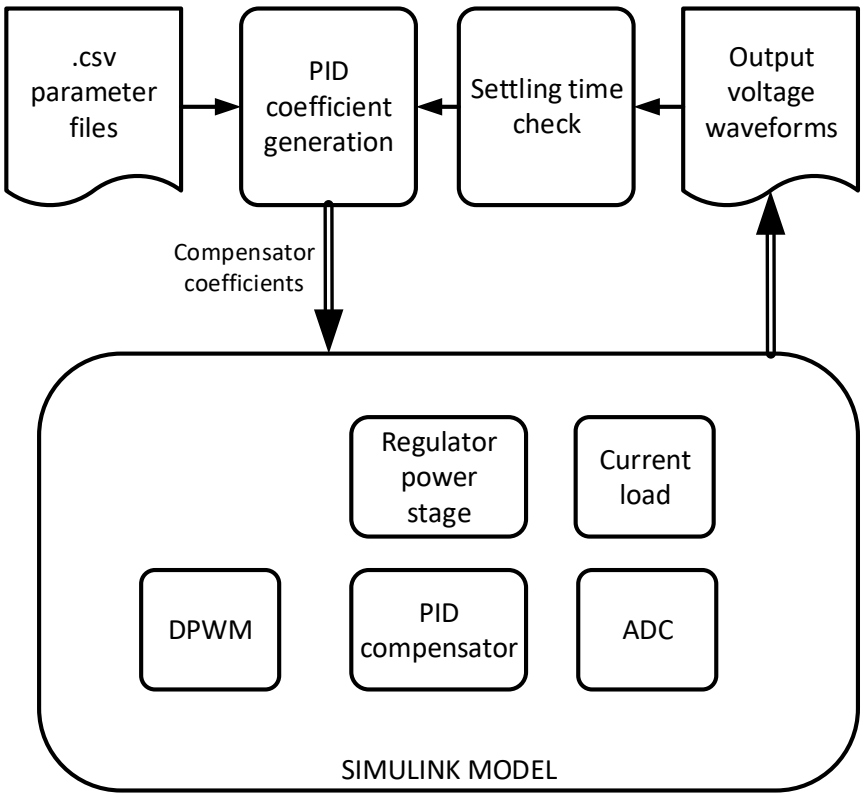

Figure 4.1: Model Development Framework

4.2 PID Tuning Method

The PID tuning method computes the open loop transfer function of the voltage regulator power stage. The initial maximum targeted bandwidth is chosen as 80% of the switching frequency. The pole-zero locations of the PID filter to achieve the target bandwidth is computed using the analytical models and the method shown in [27]. The next step is to compute the PID coefficients for the type of compensator being used (b_0, b_1, b_2). These are

Table 4.1: Input parameters for framework

Parameter	**Value**
Vin	3.6 V
V_ref	1 V
ref_step_en	0
ref_step	0.2
F_SW	125e6 Hz
N	2
phm_d	45 °
Fc	40e6 Hz
L	24e-9 H
C	22e-9 F
ESR_L	16.7e-3 Ω
ESR_C	50e-3 Ω
I_Load	1.5 A
ADC_lower_range	-0.2 V
ADC_higher_range	0.2 V
ADC_reso_bits	5
DPWM_upper_limit	1
DPWM_lower_limit	0
DPWM_reso_bits	7
load_step_en	1
I_load_init	100e-3 A
load_step_time	5e-6 s
load_step	350e-3 s
comp_gain	1
sim_time	10e-6 s
sim_step_min	1e-13 s
sim_step_max	1e-9 s
quiet	0
simu	1

then input into the the simulink model for transient simulation is that run to generate the waveforms. The transient voltage waveform is used to calculate the settling time for the current system after a load jump and is verified against the target settling time. This loop is repeated till the condition $T_s > T_{s\_target}$ is met and this is chosen as the final design.

Algorithm 1: PID Tuning Method

```
Compute open loop transfer function
Set maximum target bandwidth
do
    Calculate pole-zero location for target bandwidth
    Generate PID coefficients
    Run transient simulation in Simulink
    Verify target setting time
while T_s > T_s_target;
```

4.3 Combined Tuning

In order to obtain the best design for the combined IVR and LDO system, the steps in algorithm 2 are follows. Firstly the LDO in isolation is tuned assuming an ideal source, and then that is used to design the compensator for the IVR for the combined system as described in the previous sections. Figure 5.4 shows the transient response the of final tuned combined system to a load step.

This chapter has described the details of the framework and the tuning algorithms used. The next chapter discusses the functional evaluation of this framework and results.

CHAPTER 5

EVALUATION AND RESULTS

5.1 IVR

Figure 5.2 shows the results of the aforementioned tuning process for and IVR with $L = 150$ nH, $C = 20$ nF, $F_{SW} = 125$ MHz and $N = 2$. The Phase margin and bandwidth are improved fronm $-6.96°$ and 10 MHz to $40°$ and 17 MHz. Figure 5.1 shows the transient response of this IVR which has a settling time of $87ns$ which is under the target settling time.

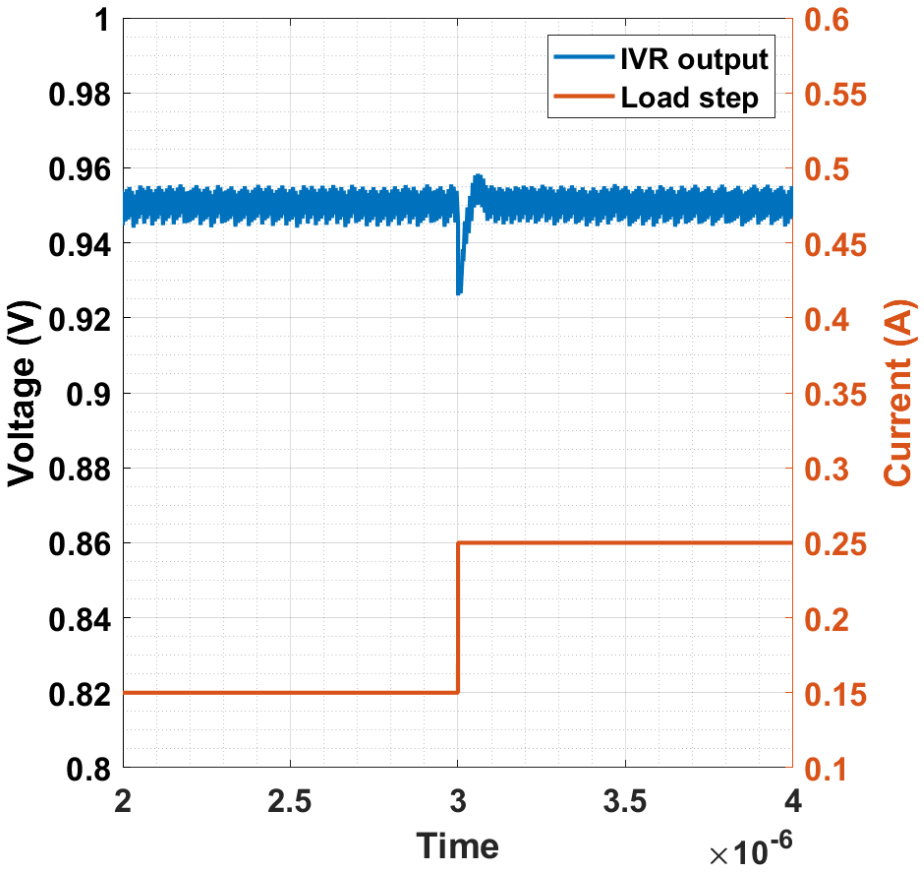

Figure 5.1: IVR Transient response

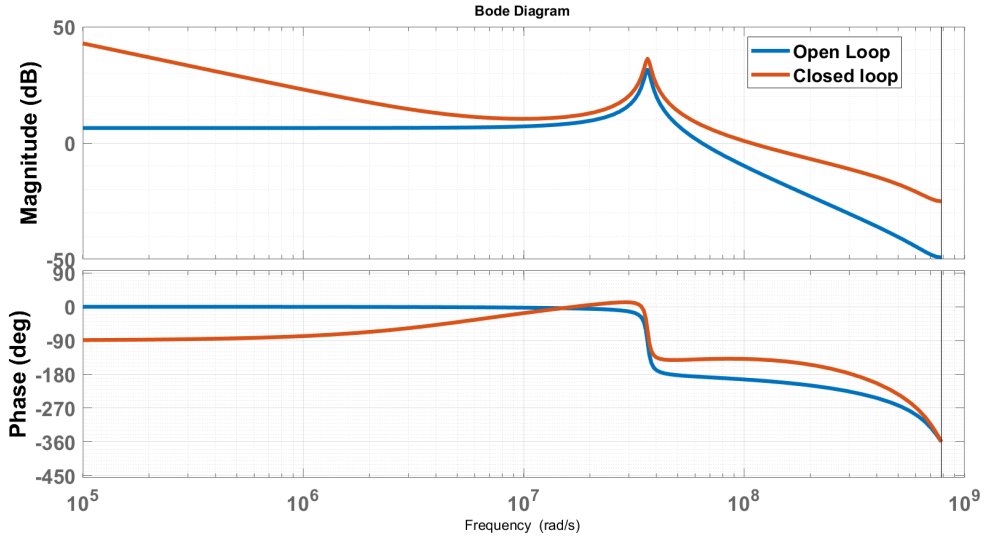

Figure 5.2: Closed loop compensation

5.2 LDO

Similarly, the transient response of the LDO is shown in Figure 5.3, with $F_{SW} = 125$ and $C = 5 = 10$ nF. Due the absence of switching as in the case of the IVR, there is no output ripple that exists.

5.3 Combined system

Figure 5.4 shows the transient time performanceof the combined IVR-LDO system. The ripple of the IVR is carried over to the LDO's output due to the relatively low PSRR of the DLDO. The final output settling time of the LDO is 200 ns which is under the target settling time. In order to show the improvement in transient response times, this process was run for different IVR-LDO capacitor configurations, and the results are shown in Figure 5.5. The first plot shows the settling time improvement of the LDO, while the second shows the same with the IVR over multiple iterations of algorithm 2. The parameters of the IVR and LDOs are shown in Table 5.1.

In order to show the improvement in transient response times, this process was run for

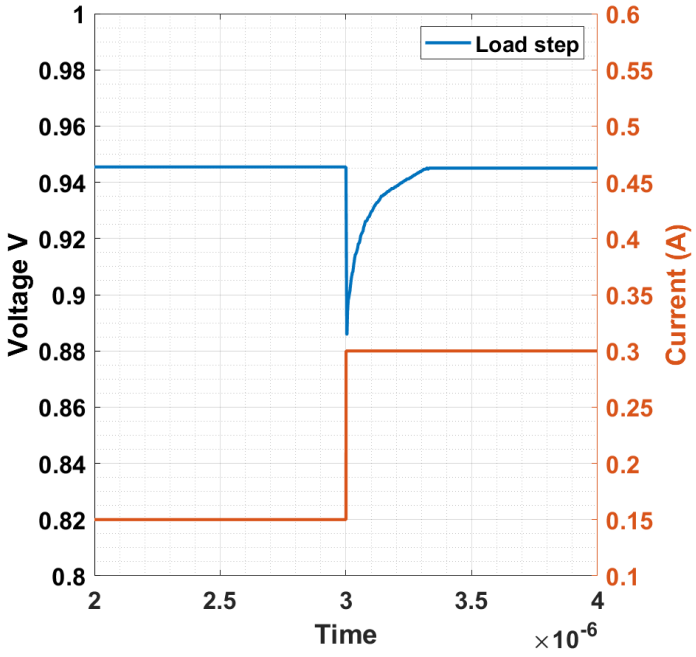

Figure 5.3: LDO transient response

Table 5.1: Regulator Simulation Parameters

	$\mathbf{V_{in}}$	$\mathbf{V_{out}}$	$\mathbf{I_L}$	**C**	**L**	$\mathbf{F_{SW}}$	**N**
IVR	2.1	0.95	$150mA$	$100nF$	$150nf$	$125MHz$	2
LDO	0.95	0.9	$150mA$	$10-100nF$	–	$250MHz$	1

different IVR-LDO capacitor configurations.

Algorithm 2: Iterative IVR-LDO Tuning

Result: Write here the result
Tune LDO in isolation;
while $T_{s-n} \neq T_{s-n}$ **do**
    Tune IVR with LDO load;
    Retune LDO with Tuned IVR;
end

Table 5.2 shows the timing details, averaged over 10 different configurations of IVR and LDO capacitances. It shows the total time taken for the entire framework, the time spent to tune the LDO, and the time spent to tune the IVR.

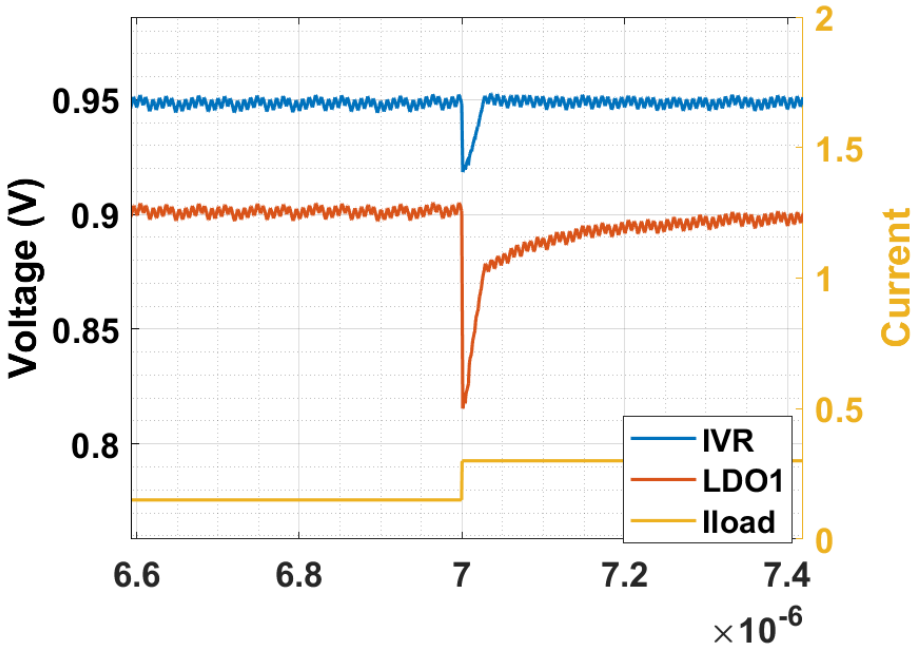

Figure 5.4: Transient response of IVR-LDO system

Table 5.2: Framework Timing Details

Total Simulation Time	206.8 s
LDO Tuning Time	102.6 s
IVR Tuning Time	104.2 s

This chapter has depicted the evaluation results of the framework along with the tuning algorithms. The observations on the results have also been outlined.

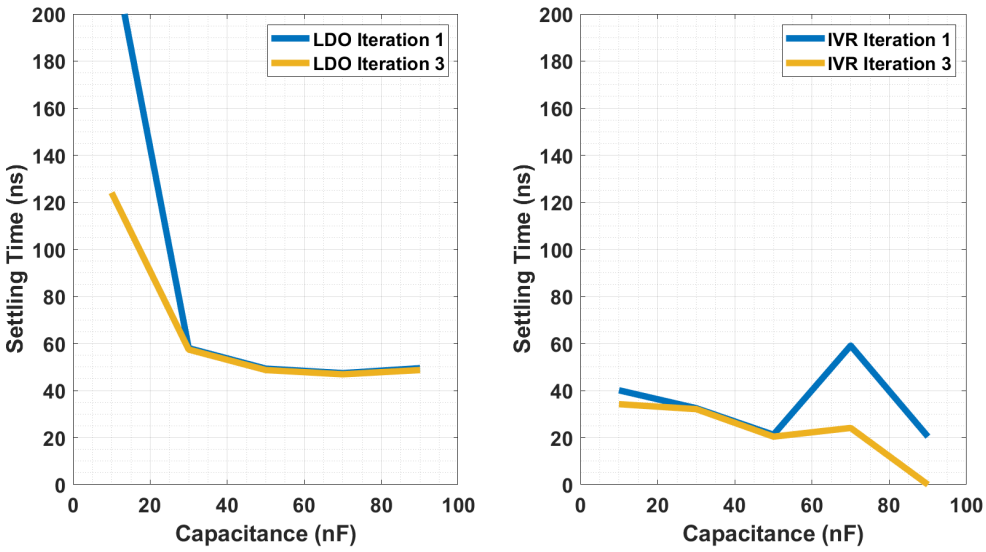

Figure 5.5: Transient response improvement over multiple iterations

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

A vital step towards the study of point-of-load power distribution demands combined modelling of IVR and LDO. In this thesis, the Simulink-MATLAB model was built. An exhaustive literature survey was carried out to understand the importance of the role of LDO in fine grained power distribution circuits, techniques for LDO modeling and its control, IVR tuning and LDO transient behaviour enhancement etc. The advantages of Simulink models over SPICE models were understood. The thesis discussed the understanding of the IVR, LDO and combined IVR-LDO analytical models and the development of the corresponding simulation model. The details of the frame work were presented. The evaluation results of this combined system model were also presented and discussed. This combined IVR-LDO model provides an avenue for design space exploration in the early phases of developing a power delivery system without the need for arduous SPICE simulations. Also the interactions between the two systems and the need for them to be developed together in order to fine tune system performance. Further evaluation and usage of this system involving increased number of LDOs can be performed.

Appendices

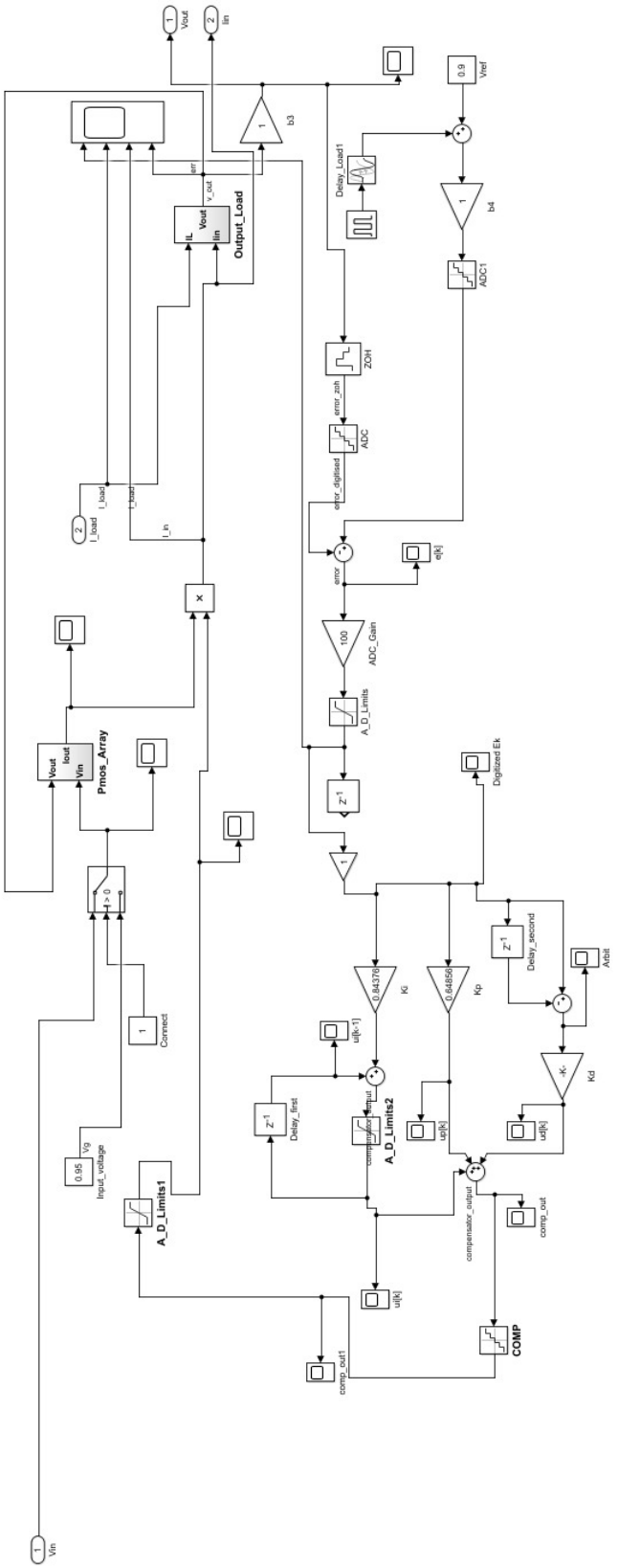

Figure 1: Simulink Model: Block1

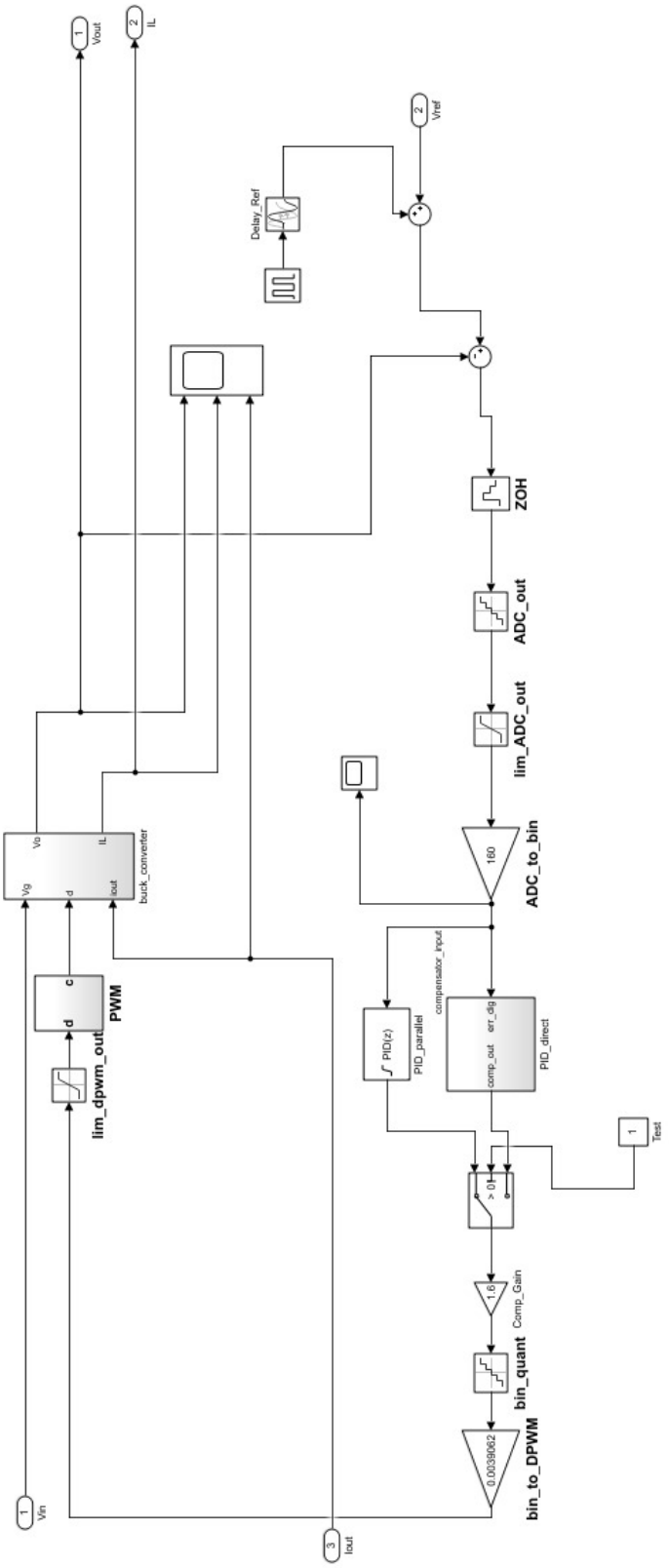

Figure 2: Simulink Model: Block2

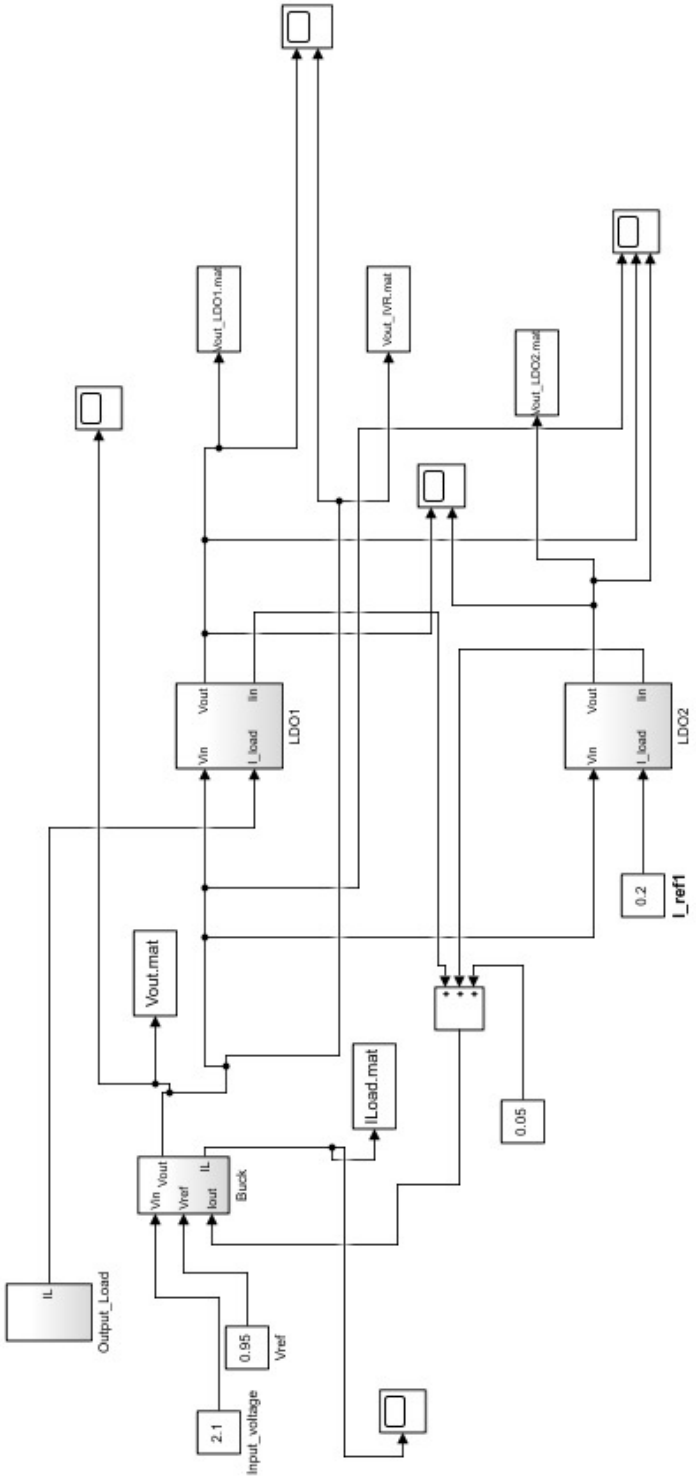

Figure 3: Simulink Model: Block3

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