DEVELOPMENT OF LOW-COST HIGH-EFFICIENCY TUNNEL OXIDE PASSIVATED CONTACT SILICON SOLAR CELLS

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DEVELOPMENT OF LOW-COST HIGH-EFFICIENCY TUNNEL OXIDE PASSIVATED CONTACT SILICON SOLAR CELLS

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This dissertation is dedicated to my wife, my parents, and my daughter for their love, encouragement, support, and patience.

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LIST OF SYMBOLS AND ABBREVIATIONS

a-Si	Amorphous silicon
BSF	Back surface field
BSRV	Back surface recombination velocity
CapEx	Capital expenditure
c-Si	Crystalline silicon
Cz	Czochralski
D_{it}	Interface defect density
EQE	External quantum efficiency
FBC	Front and back contact
FF	Fill factor
FT	Fire through
FZ	Float-zone
HIT	Heterojunction with intrinsic thin layer
HREM	High-resolution transmission electron microscopy
IBC	Interdigitated back contact
iOx	Interface oxide
IQE	Internal quantum efficiency
ITO	Indium-tin oxide
iV_{OC}	Implied open-circuit voltage
J_{0bulk}	Bulk recombination current density
$J_{0b'}$	Back surface field recombination current density
$J_{0b',metal}$	$J_{0b'}$ in the metallized rear surface areas

$J_{0b',pass}$	$J_{0b'}$ in the passivated rear surface areas
J_{0e}	Emitter recombination current density
$J_{0e,metal}$	J_{0e} in the metallized emitter areas
$J_{0e,pass}$	J_{0e} in the passivated emitter areas
J_{SC}	Short-circuit current density
LCOE	Levelized cost of energy
LPCVD	Low pressure chemical vapor deposition
NAOS	Nitric acid oxidation of silicon
PDO	Plasma deposited oxide
PECVD	Plasma-enhanced chemical vapor deposition
PERC	Passivated emitter rear cell
PERL	Passivated emitter, rear locally-doped
Poly-Si	Polycrystalline silicon
PV	Photovoltaics
QSSPC	Quasi-steady state photoconductance
RIE	Reactive ion etching
R_s	Series resistance
R_{sh}	Shunt resistance
SEM	Scanning electron microscope
SHJ	Silicon heterojunction
SIMS	Secondary ion mass spectroscopy
SiN_x	Silicon nitride
SiO_2	Silicon oxide
TCO	Transparent conductive oxide
TEM	Transmission electron microscopy

TLM	Transfer length method
TOPCon	Tunnel oxide passivated contact
V_{oc}	Open-circuit voltage
Δn	Injection level
τ	Minority carrier lifetime
τ_{eff}	Effective minority carrier lifetime

SUMMARY

Since the industrial revolution, global energy consumption has been increasing rapidly, fueled by population growth, rising energy demands due to lifestyle modernization and advancements in technology. However, more than 85% of the world energy consumption is currently satisfied by fossil fuels, which has already resulted in a significant increase in carbon dioxide in the atmosphere (from < 300 ppm to > 400 ppm) and ~1 ℃ rise in global temperature since year 1900. The concerns about the catastrophic effects of global warming have created an urgent need for affordable clean energy technologies like photovoltaics.

Photovoltaics (PV) is one of the most promising options for sustainable and clean energy supply because it can convert virtually unlimited sunlight directly into electricity without any undesirable impact on the environment. However, PV currently accounts for only ~3.3% of the total electricity generation worldwide. Even though the cost of PV modules has decreased by more than a factor of a hundred since 1976, and PV electricity has become quite competitive with fossil fuels in many parts of the world, to make photovoltaic more competitive and widespread, the levelized cost of energy (LCOE, lifetime costs divided by energy production, ¢/kWh) must be reduced further. This can be best achieved by increasing the solar cell efficiency while maintaining or reducing the module production cost. Even though some high-cost silicon cell technologies are approaching > 24% efficiency in mass production, more widely used (> 85%) lower-cost solar cells in production are still in the efficiency range of 19-22%. Therefore, the goal of this thesis is to explore a more advanced high-efficiency solar cell structure that can be

mass-produced at low cost. The specific objective is to achieve low-cost high-efficiency (> 23%) commercial ready bifacial screen-printed n-type silicon solar cells through a combination of fundamental understanding, modeling and design, technology innovations, and complete cell fabrication. This research involves developing a technology roadmap by device modeling and simulations to achieve > 23% efficiency target followed by development and implementation of required design features such as optimized boron emitter on front and tunnel oxide passivated contact (TOPCon) on the rear side of an n-type silicon wafer, in combination with advanced fine-line screen-printing metallization with floating busbars to attain the efficiency target. Chapter 1 outlines the specific tasks to accomplish this goal along with current status, opportunities and potential growth in photovoltaics.

In Chapter 2 of this thesis, the physics and operating principle of silicon solar cells are reviewed along with some key material and device properties that limit its efficiency, including the recombination loss mechanisms, bulk lifetime, recombination current density (J_0) in each layer of the solar cell, and quantum-mechanical tunneling in TOPCon structure, which provides excellent carrier selectivity by facilitating the transport of majority carriers while blocking the minority carriers to minimize recombination in diffused and metallized regions. Chapter 3 reviews the current status and the future trends in design and fabrication of silicon solar cells, including the literature survey related to carrier-selective passivating contacts.

Chapter 4 deals with the development of a technology roadmap to drive the starting efficiency of a traditional 21% n-PERT (P^+-N-N^+) cell to 23% by transforming the cell design to n-TOPCon and establishing quantitative requirements for optoelectronic

properties of each layer or region, including B emitter, rear n-TOPCon, n-base Si, screen-printed contacts and anti-reflection coating. Extensive 2D device simulations are performed using Sentaurus and Quokka 2 models to establish a technology roadmap for the ≥ 23% efficiency target using practically achievable parameters. Modelling is also used to understand and mitigate the loss mechanisms in the cells fabricated throughout this research by a combination of detailed characterization and simulations. The technology roadmap in this chapter shows how single-side front junction TOPCon cells with 23% efficiency can be achieved through optimization of B emitter, appropriate bulk lifetime and resistivity, screen-printed metallization, and passivating n-TOPCon contacts on the back. The roadmap starts with characterization and modeling of an in-house fabricated 21% n-PERT cell (P^+-N-N^+) with a very high total J_0 value of ~315 fA/cm^2 and 55 μm wide screen-printed grid lines. Note that total J_0 is the sum of J_0 contributions from each layer of the cell, including passivated and metallized B and P doped regions on front and back, as well as the J_0 of the bulk wafer. Since high J_0 is the major culprit for efficiency degradation, first an ion-implanted B emitter was designed by modeling, profile engineering and advanced screen-printed metallization that can reduce metallized emitter recombination current density J_{0e} from ~ 150 fA/cm^2 to ~ 30 fA/cm^2. Next, it was shown that by replacing full area N^+ back surface field (BSF) in the n-PERT cell with n-TOPCon can lower the metallized rear side recombination current density J_{0b}, from ~120 fA/cm^2 to < 10 fA/cm^2. Finally, bulk lifetime and resistivity combinations were established by modelling to minimize bulk recombination and resistive losses, followed by modeling and design of antireflection coating and front and back metal contact grid to minimize reflection and metal-induced recombination. The technology roadmap revealed that the total allowed J_0

for the 23 % cell efficiency target is only ~50 fA/cm^2, as opposed to 315 fA/cm^2 in the starting n-PERT cell, which can be achieved with optimized 170 Ω/□ homogeneous B emitter with metallized J_{0e} of 30 fA/cm^2 in combination with rear n-TOPCon with metallized J_{0b}, of 5 fA/cm^2 and bulk lifetime of ~2 ms (which corresponds to bulk J_{0b} of 17 fA/cm^2). In addition, grid modelling optimization revealed that we need to reduce metal-Si contact area from 6.6% to ~2.7% and contact shading to ~4.6% on the front side (B emitter) by developing fine-line screen printing (40 μm as opposed to 55 μm wide gridlines) and implementation of five floating busbars as opposed to fire-through busbars with contact resistivity of ~3 mΩ-cm^2. Modelling showed that all the above design parameters can produce 23% efficient n-TOPCon cell with V_{OC} = 707 mV, Jsc = 40.4 mA/cm^2 and FF = 80.4%.

Besides 2D device modeling in Chapter 4, a grid model calculator is developed in this chapter to rapidly optimize front and back metal grid designs (number, spacing, and width of fingers and busbars) to attain required series and contact resistances based on the doping and sheet resistance of B emitter and n-TOPCon. Our grid model calculator rapidly computes the optical shading, series resistance, and metal-induced recombination losses for different grid designs and also estimates cell V_{OC}, J_{SC}, FF, and efficiency from these loss mechanisms to establish optimum grid design for the highest cell efficiency. The calculation methodology and the accuracy of our grid model were validated with Quokka 2 model.

Chapter 5 deals with the experimental development of ion-implanted B emitter by optimization of doping profile, surface concentration, recombination current density, and sheet resistance. Based on the roadmap, target metallized J_{0e} was 30 fA/cm^2 with contact

resistivity of ~3 mΩ-cm^2. Ion-implanted emitters on textured Si surfaces were fabricated and characterized in the sheet resistance range of 48-200 Ω/□ by tailoring the implantation dose, energy, and annealing conditions. These emitters were passivated with Al_2O_3 and SiN dielectrics prior to contact formation. Nearly record low unmetallized or passivated J_0 values ($J_{0e,pass}$ < 15 fA/cm^2) were achieved in this study for R_{sheet} > 140 Ω/□. These emitters were metallized by screen-printing metal grid lines followed by rapid firing through the dielectric stack at ~770 °C. Scanning electron microscope (SEM) study and analysis of the metal/Si contact interfaces revealed that, unlike the evaporated contacts, in screen-printed contacts metal paste chemistry and firing through the dielectric can affect the emitter surface etching as well as the percentage of unetched dielectric islands under the metal contacts. It was found that this can also significantly affect the metallized J_0 value of the emitter, which led to the investigation of metal pastes. Among the various Ag pastes investigated in this study, it was found that, compared to an evaporated contact, a more aggressive Paste A increased the $J_{0e,metal}$ by 16% due to 0.13 μm deep etching of the emitter surface. On the other hand, a gentler paste B resulted in 40 % reduction in $J_{0e,metal}$ due to the presence of a significant fraction of unetched or undissolved dielectric islands under the metal grid, with no appreciable emitter surface etching. This is beneficial because it is similar to the formation of local contacts through a dielectric instead of traditional full area metal contact under the grid. We were able to achieve unmetallized J_{0e} of 12 fA/cm^2 and metallized J_{0e} of 30 fA/cm^2 on 170 Ω/□ ion-implanted B emitter with 2.7% metal-Si contact area, 4.5% metal coverage and five floating busbars using paste B. In addition, TLM measurements showed that contact resistivity was 3-5 mΩ-cm^2. These parameters are entirely consistent with the requirements of our technology roadmap for 23% cells.

Chapter 6 deals with the development of tunnel oxide passivated contacts (TOPCon) on the back side of solar cells to reduce diffusion and metal-induced recombination in the absorber, which are the two major loss mechanisms in most production cells today. It is important to recognize that in a TOPCon structure, both diffused and metallized regions are physically displaced outside the absorber via a tunnel oxide, and the band bending and barrier heights are such that majority carriers can easily tunnel through the oxide but the minority carriers are blocked. This gives rise to excellent passivation of the Si surface with very low J_0 due to carrier selectivity without compromising contact resistivity. Therefore, in this chapter, an n-TOPCon structure was developed by depositing phosphorus-doped poly-Si layers in a low-pressure chemical vapor deposition (LPCVD) reactor on top of a chemically grown tunnel oxide, followed by a high temperature anneal to crystallize and activate dopants in poly-Si. Due to high temperature (~775 °C) screen-printed fire-thorough contacts used in this research, thick (100-200 nm) poly-Si layers were grown to avoid metal penetration. Since LPCVD grows poly-Si on both sides, a masking process using dielectrics was developed to remove the poly-Si layer from the front side. The effects of screen-printing and firing, different metal pastes, and poly-Si thickness on the surface passivation quality were investigated to minimize the J_0 of the metallized and unmetallized n-TOPCon regions on the rear side. In this study, optimized n-TOPCon was formed by growing a 15 Å thick tunnel oxide in nitric acid at 100 °C on top of the n-Si absorber followed by deposition of 100-200 nm LPCVD n^+ poly-Si at 588 °C, which has a mixture of amorphous and poly-Si phases. Therefore, an anneal was required to crystallize and activate dopants in the poly-Si layer to minimize J_0. Optimum anneal temperature of 875 °C resulted in excellent $J_{0,pass}$ of ~2-5 fA/cm^2 which

decreased further to 1-2 fA/cm^2 after 750 Å SiN deposition and simulated contact firing cycle without metal contacts. Next, the impact of Ag metal contacts was investigated after firing the Ag contacts through the SiN coating. This also resulted in a very low metallized J_0 value of ~5 fA/cm^2 with 9% metal coverage on the rear side, supporting very little degradation in J_0 after contact formation. Such low unmetallized and metallized J_0 values are among the best reported for screen-printed contacts and are consistent with the requirements of our technology roadmap for 23% efficiency.

Chapter 7 involves the integration of all the promising advanced technologies developed in the above chapters to demonstrate screen-printed 23% commercial size bifacial silicon solar cells. A complete process sequence developed in this task achieved screen-printed 239 cm^2 n-TOPCon bifacial cells with efficiency of 22.6%. Detailed analysis showed slightly higher ideality or n-factor (~1.1) due to edge leakage effects which lowered the FF and efficiency. To eliminate the edge effects, we fabricated a 10 cm × 10 cm cell size within the 6-inch pseudo square wafer by laser isolation and modified the grid design with three busbars for the 100 cm^2 cells. This resulted in 22.9% efficiency, entirely consistent with our objective and technology roadmap. Note that the above cells were fabricated with homogeneous B emitters, n-Si wafers with a bulk lifetime of 1-2 ms, and fire-through grid contacts with five busbars because these were the capabilities available in the lab at the time. However, there are recent reports on the availability of better materials and contact schemes like floating multi-busbars or busbarless contacts. Therefore, based on the experimental and theoretical understanding developed in this research, a new technology roadmap was developed that shows that implementation of

selective B emitter with busbarless contacts on the front and use of 5-20 ms bulk lifetime Si can push the ~23% efficiency achieved in this research closer to 25%.

In Chapter 8, a next-generation industry-compatible double-side passivated contacts solar cell structure is proposed with TOPCon on both sides. This cell structure is composed of full area p-TOPCon on the rear and selective area n-TOPCon on the front side of an n-type Si wafer. Detailed modeling using practically achievable material and device parameters shows that ~25.4% efficiency is achievable with this design using traditional screen-printing. This is because selective n-TOPCon on the front minimizes parasitic absorption and rear junction design allows the use of thicker poly under the front grid without the need for any diffusion in the field region. The undiffused field region is passivated with Al_2O_3/SiN coating to provide a J_0 comparable to TOPCon passivated Si surface without any absorption loss. Modeling reveals that this structure does not require any front diffusion because lateral conduction to the front grid takes place through Si bulk without appreciable resistive or FF loss. Because bulk material properties are very important for such a rear junction device, an efficiency contour map is generated through numerical modeling to show that a given target efficiency can be achieved by several combinations of bulk lifetime and resistivity. However, to achieve the highest efficiency for a fixed bulk lifetime, there is an optimum resistivity. For the proposed design and structure, bulk lifetime needs to be $\geq$ 3ms to achieve > 25% cell efficiency.

In summary, we have developed a cost-effective and manufacturable process sequence to fabricate high-efficiency (~23%) screen-printed n-TOPCon cells on industrial-grade n-type Cz Si wafers using commercial-ready technologies and equipment. This innovative low-cost process sequence features optimized ion-implanted emitter with

advanced fine-line screen-printing metallization with five floating busbars, and n-type tunnel oxide passivated contacts fabricated by depositing phosphorus-doped LPCVD poly-Si on top of ~15 Å tunnel oxide grown by nitric acid oxidation. The n-TOPCon cells fabricated with this process achieved 22.6% efficiency on commercial-grade 239 cm^2 Cz silicon wafers and 22.9% efficiency on 100 cm^2 area, compared to 21% industrial n-PERT cell at the start of this research. Based on the fundamental understanding developed in this research, roadmaps for achieving ~25% front-junction single-side n-TOPCon cells and 25.5 % rear-junction double-side selective TOPCon cells are developed in this thesis to provide quantitative guidelines for future research on this topic.

The research in this thesis has resulted in 14 publications in peer-reviewed journals and international refereed conferences. This research was supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under Solar Energy Technologies Office (SETO) Agreement Number DEEE0007554, DE-EE0009350, and DE-EE0008562.

CHAPTER 1. INTRODUCTION

1.1 Statement of the Problem

The demand for energy has been increasing rapidly since the industrial revolution in 1900, however, more than 85% of the current world energy consumption is satisfied by fossil fuels, as shown in Figure 1. This is primarily due to low cost, ease of production, and availability of fossil fuels in the past. However, fossil fuels are depleting rapidly and are known to release a significant amount of carbon dioxide (CO_2) that traps heat in the atmosphere and causes global warming. This has resulted in a sharp increase in atmospheric concentration of CO_2 (> 400ppm) and ~1°C rise in global temperature, as shown in Figures 2 and 3. If the temperature continues to increase at this rate, it could result in catastrophic effects by 2050, including the rise in sea level, drought, floods, storm surges, and species extinction [1, 2], emphasizing the urgent need for developing and using renewable and clean source of energy to slow down the climate change.

Nuclear energy is a potential option to reduce CO_2 emissions. However, it produces radioactive wastes and heat that need to be disposed and managed safely. Accidents in Fukushima, Japan (March 11, 2011) and Chernobyl (April 26, 1986) have also raised numerous concerns about the safety and expansion of this clean source of energy.

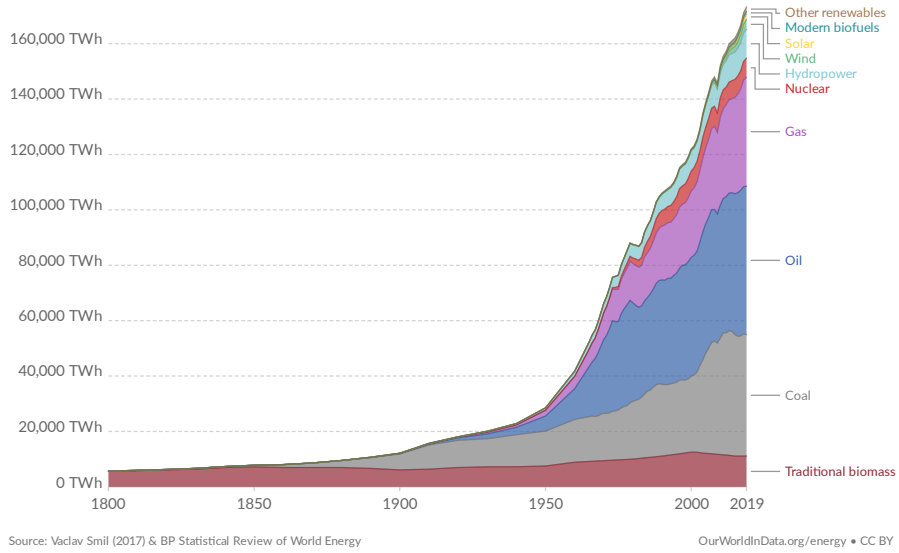


Figure 1: Global primary energy consumption by source from the year 1800 to 2019 (adapted from [3]).

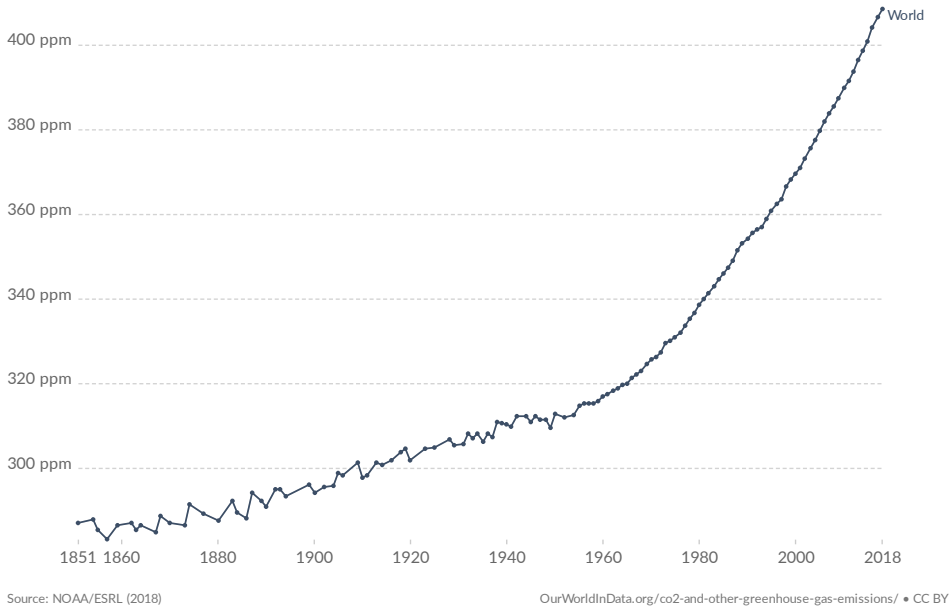


Figure 2: Global CO_2 atmospheric concentration measured in parts per million (ppm) from the year 1851 to 2018 (adapted from [3]).

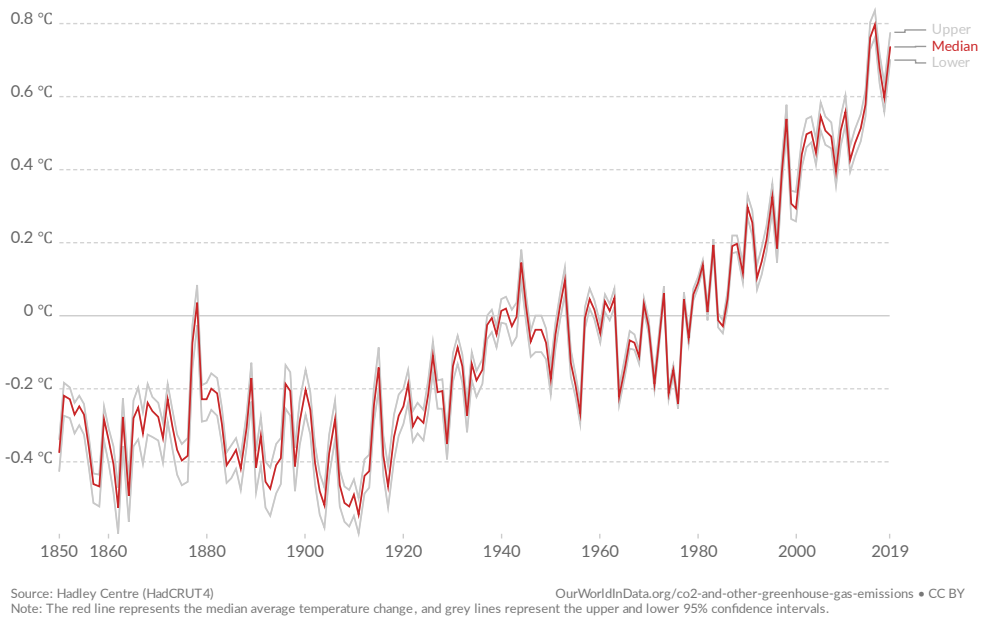


Figure 3: Global average temperature anomaly relative to the 1961-1990 average temperature from the year 1850 to 2019 (adapted from [3]).

Photovoltaic (PV) energy is one of the most promising options for renewable energy because it is safe and can convert virtually unlimited sunlight directly into electricity with minimal impact on the environment. In addition, price of solar modules has dropped by more than a factor of a hundred in the last four decades due to technology innovations and massive scale of production. In 1976, the PV module price was about one hundred dollars per watt with total amount of installed PV of less than one megawatt as shown by the PV learning curve in Figure 4. Today, the total installed PV in the world has reached ~789 gigawatts [4], and the PV module price has tumbled down by a factor of 500 to about 20 cents per watt. This is good enough to produce electricity at the rate of ~5 cents per kilowatt-hour for utility-scale applications (Figure 5), which is already at grid parity with fossil fuels in many parts of the world. Currently about 60% of world electricity is

produced from fossil fuels [5] and PV contributes to only ~3% (Figure 6). However, recent 2020 Bloomberg New Energy Outlook ([6], Figure 6) projects that by 2050, 56% of electricity will be provided by solar and wind energy. Many organizations, including US Department of Energy, project that PV will become the cheapest and dominant source of electricity by 2030 (~2¢/kWh) (Figure 5, [7]) through further technology advancements, scale up and cheaper storage options.

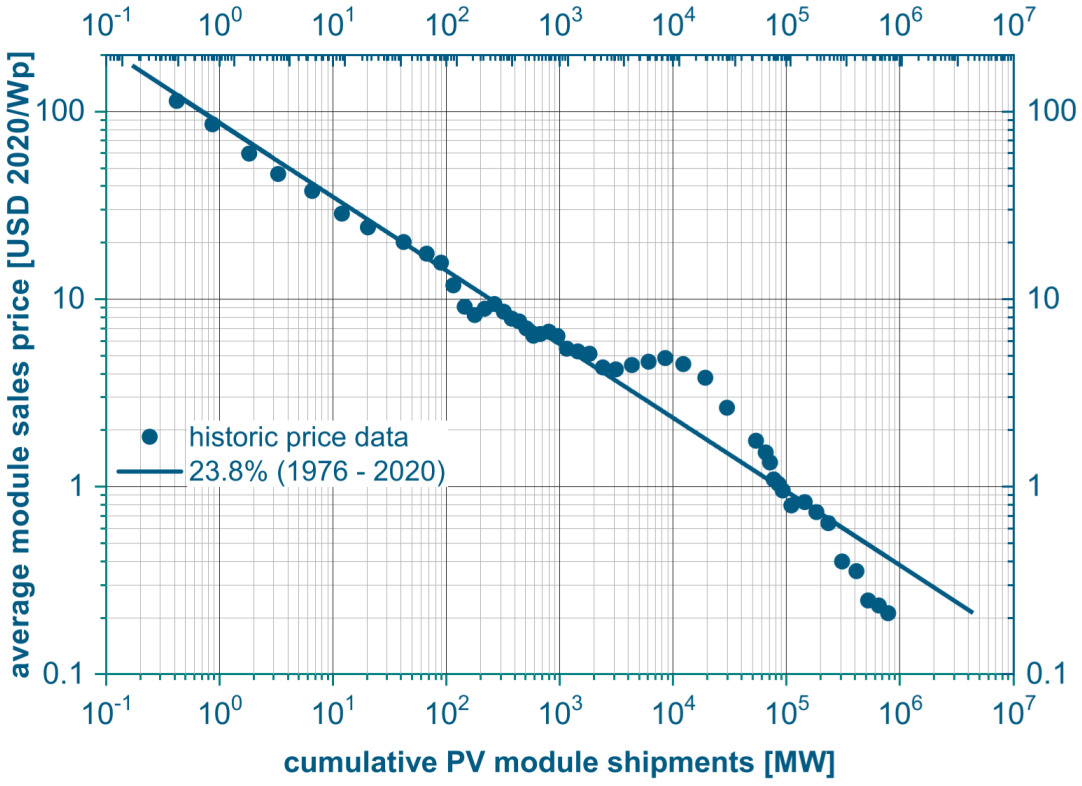


Figure 4: Learning curve for module price as a function of cumulative shipments (adapted from [4]).

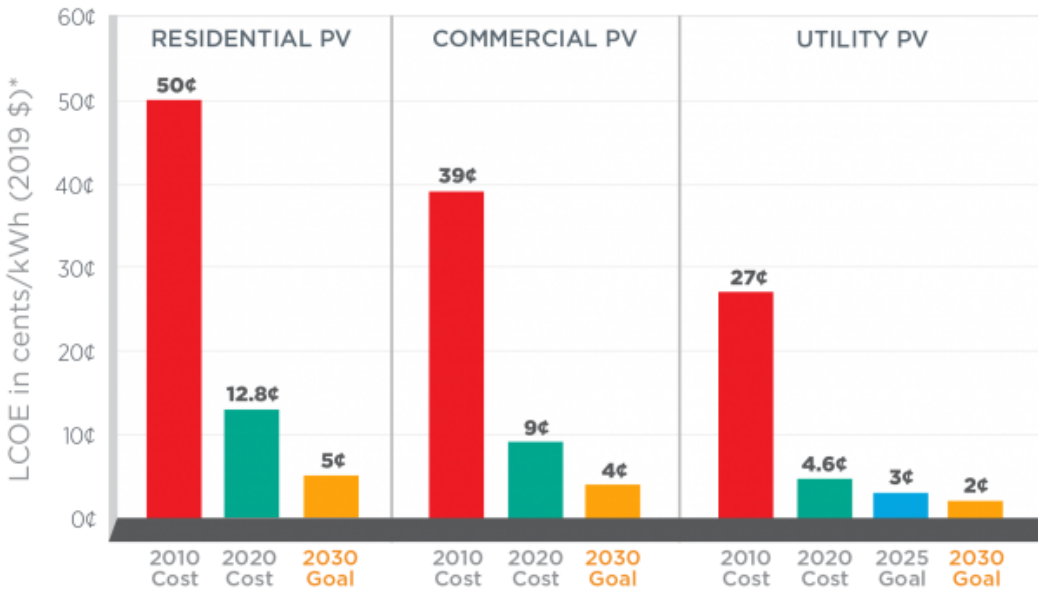


Figure 5: Photovoltaics LCOE price goals of the US Department of Energy Solar Energy Technologies Office [7]. The LCOE progress and targets are calculated based on average U.S. climate and without the investment tax credit or state/local incentives.

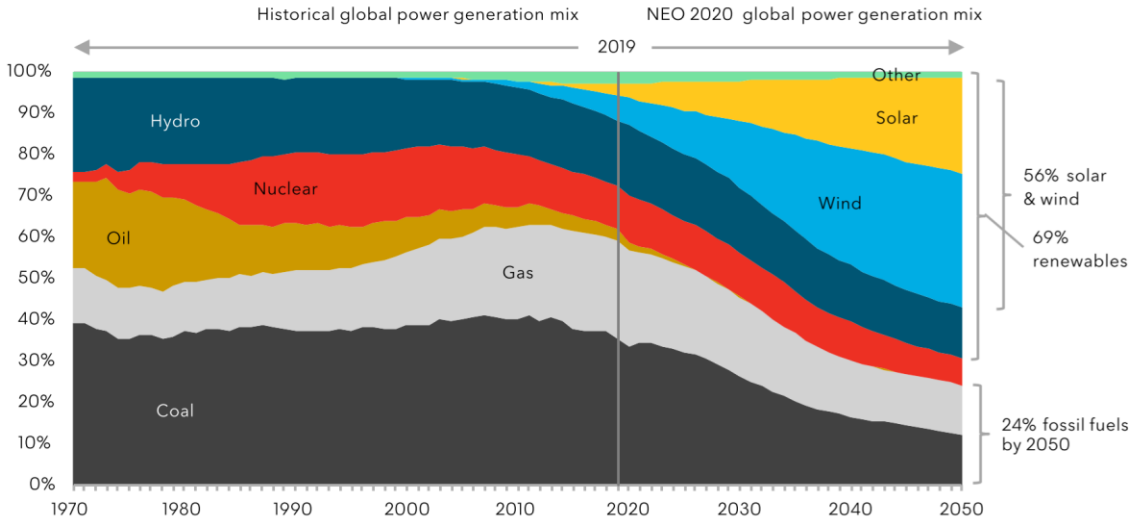


Figure 6: Global electricity generation mix shift from 1970 to 2050 (Source: BloombergNEF [6]).

To make photovoltaic energy more competitive and pervasive, it is essential to further reduce the levelized cost of PV electricity (LCOE) from ~5¢/kWh to 2¢/kWh. This can be achieved by increasing the solar cell efficiency while maintaining or decreasing the module production and installation costs [8]. Highly efficient solar cells not only produce more power but also reduce the footprint and balance of system costs. Currently more than 90% of solar cells are produced from silicon material and their efficiency is largely limited by recombination in the diffused and metallized regions in the silicon absorber or base of the solar cells. Therefore, the overall goal of this dissertation is to achieve commercially viable low-cost high-efficiency screen-printed silicon solar cells with carrier selective tunnel oxide passivated contacts (TOPCon), which decouple the diffused and metallized region from the absorber via tunnel oxide while maintaining process simplicity and lower manufacturing cost. In addition, these cells will be bifacial (gridlines on both sides) which will allow harvesting of albedo light from the rear side, further increasing effective module efficiency or power output.

1.2 Specific Research Objectives

One of the key remaining obstacles to approaching the theoretical limit of silicon solar cell efficiency (29.43% [9]) is minority carrier recombination in the diffused and metallized regions in the Si absorber. This is also the major loss mechanism in most current production Si cells because of which their efficiency is in the range of 19-22%. Challenge is to suppress or eliminate this minority carrier recombination while maintaining efficient majority carrier transport.

Tunnel oxide passivated contact (TOPCon) is a very promising and emerging technology because it eliminates the need for direct metal contact and diffusion into the absorber material without appreciably affecting the majority carrier transport. In a TOPCon structure, the diffused and metallized regions are displaced out of the Si absorber with the help of an ultra-thin tunnel oxide in between, which blocks the flow of minority carriers to diffused and metallized regions to prevent recombination but allows the majority carriers to tunnel through for conduction. Very high efficiency (25.8%) small area TOPCon R&D cells have been reported recently in the literature [10] by using non-manufacturable and expensive technologies involving vacuum evaporated full area silver on TOPCon in combination with multiple photolithography steps. In addition, very expensive float-zone (FZ) silicon wafers were used instead of low-cost Czochralski (Cz) wafers. Nevertheless, such high-efficiency cells demonstrate the existence proof of the concept and the potential of poly-SiO_2 passivated contacts for next-generation commercial Si cells.

To improve cell efficiency and reduce production cost simultaneously will require technology innovations, clever cell design, optimized and simple process sequence, and the use of proven low-cost high-throughput commercial equipment. This provided the motivation in this research to develop technologies and a low-cost manufacturable process sequence for a single-side TOPCon cell design that can boost silicon cell efficiencies to $\geq$23% on large-area 239 cm^2 commercial-grade n-type Czochralski Si wafers. In this research, ion implantation is used for forming B emitter on the front, LPCVD is used for n-TOPCon on the back, and low-cost high-throughput screen-printed contacts are applied on front and back with no photolithography steps. This research is divided into the following five tasks.

1.2.1 Task 1: Development of a Technology Roadmap To 23% Efficiency TOPCon Solar Cells

In this task, extensive 2D device modeling is performed using Sentaurus and Quokka advanced simulation tools to establish cell designs and material parameters that can attain > 23% TOPCon cells. This involves quantitative understanding and optimization of B emitter profiles, bulk lifetime, establishing required surface passivation quality of B emitter and rear n-TOPCon, allowed metal-induced recombination on front and back, and screen-printed contact parameters and grid designs to minimize, resistive, shadow and recombination losses. Passivation quality of B emitter and n-TOPCon region is quantified in terms of recombination current density, J_{0e} and $J_{0b'}$, respectively, and the effective bulk lifetime in the wafer is characterized in terms of $J_{0,bulk}$. In addition, J_{0e} and $J_{0b'}$ are subdivided into metallized and unmetallized (passivated) components. Total J_0, which dictates the cell efficiency, will be referred to as the sum of all the above J_0 values. A technology roadmap is developed with required unmetallized and metallized J_0 values and material parameters in each layer of the solar cell to achieve the target efficiency. This involved theoretical calculations of doping profiles, sheet resistance, and contact parameters for doped regions of the device. Sentaurus Device model is used to generate J_0 vs surface recombination velocity (SRV) curves from the simulated and/or measured doping profiles. Then, from the knowledge of SRV on top of the doped profiles (surface) and at the metal-Si interface (~10^7 cm/s), J_0 contributions from passivated and metallized regions are extracted for different profiles to select the best candidate.

To start the modeling, a traditional state-of-the-art 21% n-PERT cell (p^+-n-n^+) with diffused boron emitter and phosphorus back surface field on n-base Cz Si wafers was

fabricated and modeled to establish a benchmark and validate the models. This cell had total J_0 value of ~315 fA/cm^2 and 55 μm wide screen-printed metal gridlines and bulk lifetime of ~1 ms. Next, various TOPCon cell designs are explored by device modeling by varying practically achievable material and device parameters (passivated and metallized J_0, bulk lifetime, screen printed contact parameters and grid design, etc.) to establish the best pathway to raise the cell efficiency from 21% to ~23%. Our technology roadmap revealed that the total J_0 allowed for 23 % cell is only 50 fA/cm^2 which can be achieved with 30 fA/cm^2 J_{0e} for metallized B emitter, 5 fA/cm^2 $J_{0b,}$ for metallized rear n-TOPCon and bulk lifetime of 1-2 ms, corresponding to $J_{0,bulk}$ of < 20 fA/cm^2. A grid model is also developed in this task to optimize front and back grid designs (number, spacing and width of fingers and busbars) for bifacial Si solar cells to attain required series and contact resistances based on the sheet resistance of B emitter and n-TOPCon. This grid model calculator computes the optical shading, series resistance, and metal-induced recombination losses for different grid designs and calculated cell V_{OC}, J_{SC}, FF and efficiency from these loss mechanisms to establish optimum grid design for the highest cell efficiency. Figure 7 shows the structures of the starting 21% n-PERT cell and the proposed ~23% n-TOPCon cell modeled in this task.

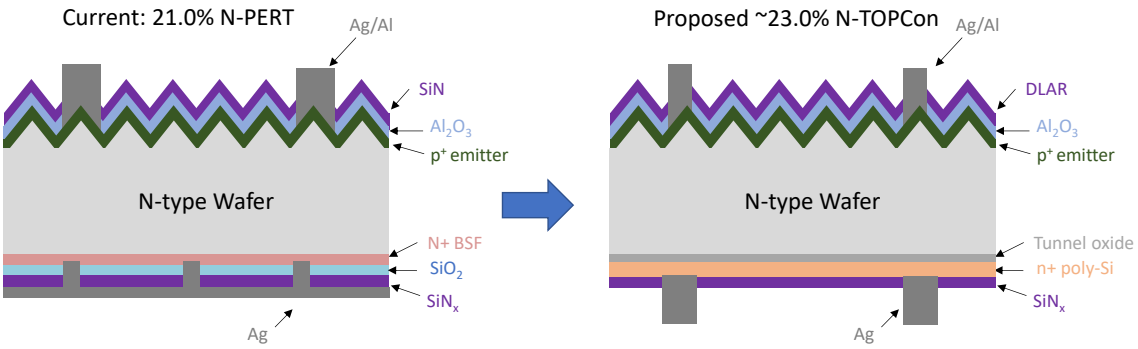


Figure 7: Current 21% n-PERT cell structure and proposed ~23% n-TOPCon cell structure.

1.2.2 Task 2: Technology Development and Formation of Optimized Ion-Implanted Boron Emitter with Metallized J_{0e} of 30 fA/cm^2

Technology roadmap in Task 1 established the metallized J_{0e} target of ~30 fA/cm^2 for B emitter to achieve 23% efficiency. Task 2 deals with the experimental development of ion-implanted homogeneous B emitter with unmetallized J_0 target of < 15 fA/cm^2 and metallized J_{0e} of ~30 fA/cm^2 with ~2.7% metal-Si contact area. This task involves profile engineering, surface passivation of the B emitter, and proper contact formation using optimized grid design and screen-printed contacts.

Emitter profiles and dielectric passivation are investigated in this task to lower the unmetallized $J_{0e,pass}$ while screen-printing paste chemistry, grid design and firing conditions are optimized to minimize $J_{0e,metal}$. Ion-implanted profiles are modeled and fabricated in the sheet resistance range of 48-200 Ω/□ with varying surface concentration, junction depth, and surface passivation to achieve the target unmetallized and metallized J_{0e} values. Implantation and annealing conditions were tailored to achieve the desired emitter profiles

and sheet resistance. Symmetric test structures with passivated B emitters on both sides, with and without metal contacts, are fabricated and characterized using measurement techniques like quasi-steady-state photoconductance (QSSPC) analysis to extract metallized and unmetallized J_{0e} values of implanted emitters. In addition, transfer length measurements (TLM) are performed to determine the contact resistivity to select the right emitter and doping profile that satisfies the J_0 as well as contact resistivity requirements of the roadmap.

1.2.3 Task 3: Development, Optimization and Fabrication of Rear Side N-TOPCon with Metallized $J_{0b'}$ of 5 fA/cm^2

Tunnel oxide passivated contacts consist of an ultra-thin (~15Å) SiO_2 layer between the Si wafer and doped poly silicon. Since metal contacts are formed to the poly silicon layer, there is neither any intentional diffusion or direct metal contact to Si absorber. This reduces both diffusion and metal-induced recombination in Si to significantly reduce the $J_{0b'}$ on the rear side of the cell. Due to appropriate band bending, tunnel oxide allows the flow of majority carriers but blocks or retains the minority carriers in the bulk, giving rise to carrier selectivity and excellent passivation at the Si/SiO_2 interface. Based on our technology roadmap, the objective of this task is to develop an n-TOPCon on the rear side with metallized J_0 of ~5 fA/cm^2 with ~10% metal-poly-Si contact area.

In this task, tunnel oxide is grown by nitric acid oxidation of Si at ~100 ℃ followed by deposition of optimized phosphorus-doped polysilicon to form n-TOPCon on the back of an n-type Si wafer. This TOPCon is then capped with PECVD grown SiN to facilitate the formation of screen-printed contacts which are fired through SiN. In this research, low-

pressure chemical vapor deposition (LPCVD) is used to deposit doped Si at < 600 ℃ on top of the tunnel oxide, followed by a high temperature anneal to crystallize and activate dopants in poly-Si. Since LPCVD film grows on both sides of the wafer, a dielectric masking process is developed to obtain TOPCon only on the rear side. In this task, poly-Si deposition conditions, thickness, doping, and anneal temperature are optimized, in combination with screen printing metal paste and firing conditions, to minimize J_{0b}, and achieve the roadmap target value of 5 fA/cm^2

1.2.4 Task 4: Fabrication of High-Efficiency (~23%) N-TOPCon Solar Cells by Process Development and Integration of Advanced Technologies

In this task, all the technology enhancements from above tasks are integrated into a process sequence to achieve ~23% efficient low-cost commercial ready n-TOPCon cells. Throughout this research, fabricated cells are characterized and analyzed by light and dark I-V measurements, J_{SC}, V_{OC}, efficiency, and J_0 measurements, as well as series, shunt, and all the contact parameters that can affect fill factor. These parameters along with the measured doping profiles and other relevant parameters from tasks 1-3 are used to match the measured and modeled performance of the fabricated cells (V_{OC}, J_{SC}, FF and efficiency) to understand and quantify the loss mechanisms and provide guidelines and directions for further improvements. For example, modelling and measurements are used to determine the metal-induced recombination ($J_{0,metal}$) as well as J_0 of the unmetallized or passivated regions ($J_{0,pass}$) on the front emitter as well as on rear side TOPCon and bulk lifetime or $J_{0,bulk}$ is determined by subtracting the above four J_0 values from the total J_0 of the cell, which is determined from V_{OC} and J_{SC} of the cell. Comparison of the extracted all five J_0 components in the fabricated cells with the target values in the roadmap (Task1) is used

throughout the research to guide the experimental development toward ~23% n-TOPCon cell. Based on the fundamental and experimental understanding developed in this research, guidelines are provided to achieve ~25% single-side front-junction TOPCon cells.

1.2.5 Task 5: Modelling and Understanding of > 25% Rear Junction Double-Side Passivated Contact Solar Cells with Selective Area TOPCon on Front

The objective of this task is to apply the fundamental understanding developed in this research to establish a cell design and roadmap to ~25.5% efficiency screen-printed bifacial rear junction selective TOPCon cells. Device modeling is performed to propose > 25% efficient next-generation industry-compatible rear junction double-side passivated contacts solar cell structure with full area p-TOPCon on the rear and selective area n-TOPCon under the front grid pattern (selective TOPCon). This design enables the use of thicker TOPCon (> 100nm) on the front for traditional screen-printed contacts without incurring metal-induced damage, high parasitic absorption loss, and compromise in lateral transport or carrier collection on the front side. Rear junction design with appropriate bulk lifetime and resistivity combination eliminates the need for heavy doping in the front field region because carriers can flow through the bulk Si without appreciable FF loss. High V_{OC} is maintained because high-quality Si surface passivation in the field region by Al_2O_3/SiN can give J_0 comparable to the TOPCon.

CHAPTER 2. BASIC OPERATION OF SILICON SOLAR CELLS AND RECOMBINATION MECHANISMS

2.1 Basic Operation of a Solar Cell and Structure of an N-TOPCon Cell

The photovoltaic effect is the generation of voltage and electric current from photons present in the light source. A solar cell is a semiconductor device that converts the energy of sunlight directly into electricity without any undesirable impact on the environment during the energy conversion. Basic operation of solar cell can be described by following three simple steps shown in Figure 8:

1. Photons in solar spectrum with energy higher than the bandgap of the semiconductor are absorbed in it by exciting electrons from the valence band to the conduction band, resulting in generation of very large number of electron-hole pairs.
2. Light generated electron-hole pairs are separated by the high electric field of an asymmetric p-n junction inside the solar cell, resulting in charge separation which gives rise to photovoltage.
3. Carriers are extracted into an external circuit when a load is connected.

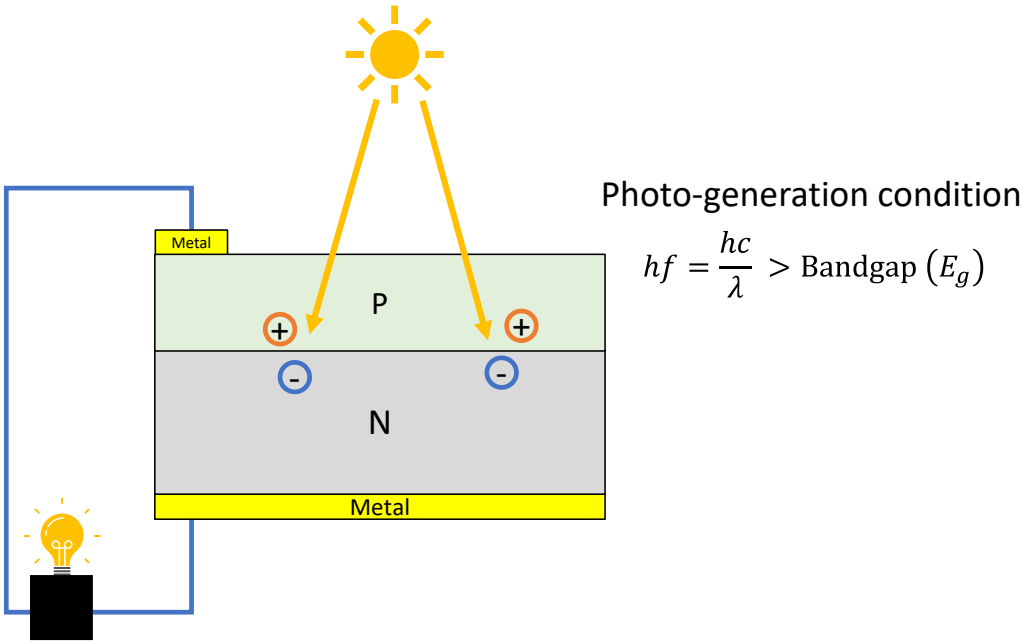


Figure 8: A schematic of a simple solar cell structure.

Figure 9 shows the typical current-voltage (IV) and power-voltage curve of a solar cell. The solar cell efficiency is defined by the equation below:

$$Efficeincy = \frac{P_{out}}{P_{in}} = \frac{V_{MP} \times I_{MP}}{P_{in}} = \frac{V_{OC} \times I_{SC} \times FF}{P_{in}} \quad \textbf{(1)}$$

Where P_{in} is power input from incident sunlight (1000 W/m^2 for standard test condition), P_{out} is power output of a solar cell, V_{MP} is voltage at maximum power (MP) point, and I_{MP} is electric current at maximum power point, V_{OC} is open-circuit voltage, I_{SC} is short-circuit current and fill factor (FF) is a measure of "squareness" of the IV curve, defined as:

$$FF = \frac{P_{MP}}{V_{OC} \times I_{SC}} = \frac{V_{MP} \times I_{MP}}{V_{OC} \times I_{SC}} \quad \textbf{(2)}$$

The cell efficiency is also defined as the product of V_{OC}, J_{SC} and FF divided by the input power P_{in} (Eq. (1)). Therefore, larger the V_{OC}, J_{SC}, and FF, higher the cell efficiency.

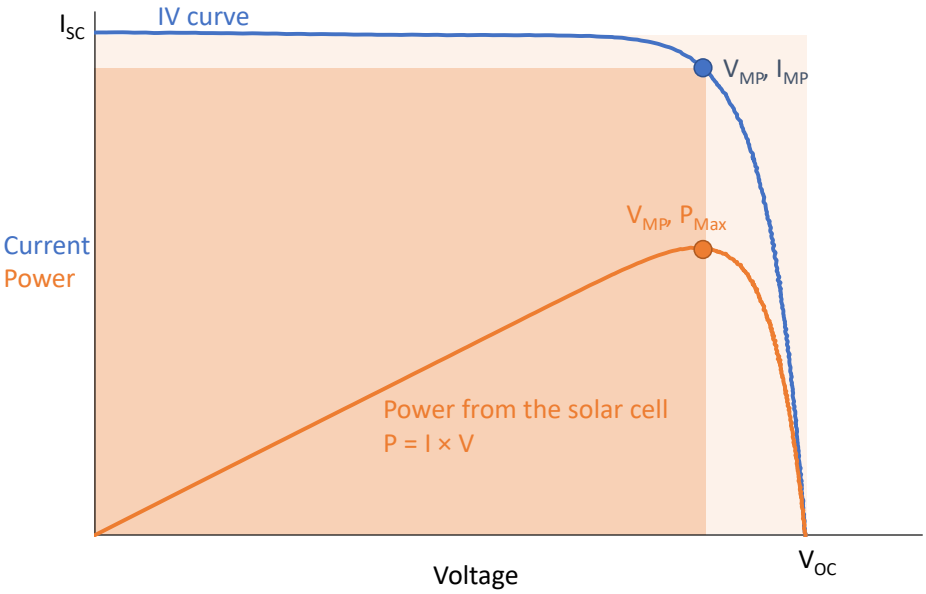


Figure 9: The current-voltage (IV) and power-voltage curve of a solar cell.

Figure 10 illustrates a schematic structure of an n-type tunnel oxide passivated contacts (n-TOPCon) silicon solar cell, which is the major focus of this thesis. An n-TOPCon solar cell is composed of a very thin tunnel oxide capped with phosphorus-doped n^+ poly-Si on the rear side, and a boron-doped p^+ emitter on the front side of an n-type Si wafer. The boron emitter forms the p-n junction, which creates an internal electric field in the depletion region. The light-generated electrons and holes are separated by the internal electric field. The front Al_2O_3/SiN layers serve as surface passivation and anti-reflection

coating at the same time, which reduce the surface recombination and optical losses. The n-TOPCon structure on the rear side is composed of a very thin tunnel oxide capped with heavily phosphorus-doped poly-Si layer, which offers an ingenious solution to reducing or eliminating diffusion- and metal-Si contact-induced recombination losses in bulk Si. The front and rear contacts are commonly formed with screen-printing technology in the industry, because of its simplicity, high throughput, and low manufacturing cost. Carrier recombination is the major loss mechanism responsible for the gap between current production cell efficiencies (19-22%) and theoretical efficiency (29.43%) [9] of silicon cells. Therefore, the recombination losses in the B emitter, rear side n-TOPCon, contacts and bulk Si will be quantified by device fabrication and modeling in this research to provide guidelines for technology development and design optimization of TOPCon cells.

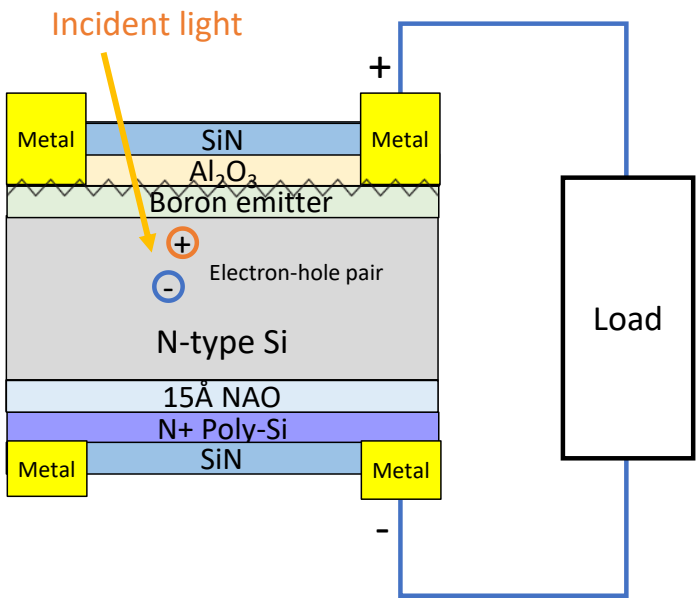


Figure 10: Structure of the n-type TOPCon Si solar cell with boron-diffused emitter on front and tunnel oxide passivated contacts on the rear.

2.2 Recombination Mechanisms in Si Solar Cells

When solar cells are under illumination, photogenerated carriers either flow into an external circuit to provide electric current, or recombine inside the device and release the energy as heat or light in the semiconductor. Recombination loss limits the maximum voltage and current of the solar cell, and is the source of major efficiency loss mechanism in current commercial Si solar cells [11]. Since there are several recombination mechanisms in Si solar cells, a fundamental understanding and description of various recombination mechanisms are reviewed next in order to quantify them and improve solar cell performance.

There are four types of recombination process in a silicon solar cell:

1. Radiative recombination
2. Auger recombination
3. Shockley-Read-Hall recombination
4. Surface recombination

These recombination mechanisms occur simultaneously in solar cells. The recombination rate (R) is characterized by a lifetime (τ) defined as:

$$\tau \equiv \frac{\Delta n}{R} \qquad \textbf{(3)}$$

where Δn is the excess carrier concentration (cm^{-3}). Longer lifetime is desirable to avoid recombination and enhance carrier collection in the external circuit. Net effective lifetime is the parallel combination of all the recombination mechanisms:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{surface}} \quad \textbf{(4)}$$

2.2.1 Radiative Recombination

Radiative recombination is also called band-to-band recombination. As shown in Figure 11, an electron in the conduction band recombines with a hole in the valence band. The energy is released as a photon. The radiative recombination rate R_{rad} is given by:

$$R_{rad} = B\,(n\,p - n_i^2) \quad \textbf{(5)}$$

where B is the radiative recombination coefficient, n and p are the electron and hole concentrations, and n_i is the intrinsic carrier concentration.

Radiative recombination is more significant in direct bandgap semiconductors like GaAs and GaN. In indirect bandgap materials like Si, where the conduction band minimum is not aligned with the valence band maximum, the radiative recombination is extremely low because it requires the participation of a phonon of the right momentum to complete the recombination process. This reduces the probability of radiative recombination in Si and is reflected in the low value of $B = 4.73 \times 10^{-15}$ cm/s for Si at room temperature [12]. Therefore, the radiative recombination in Si usually can be neglected. The radiative recombination lifetime can be expressed as [13]:

$$\tau_{rad} = \frac{1}{B(n_0 + p_0 + \Delta n)} \quad \textbf{(6)}$$

where n_0 and p_0 are electron and hole concentrations in thermal equilibrium, respectively.

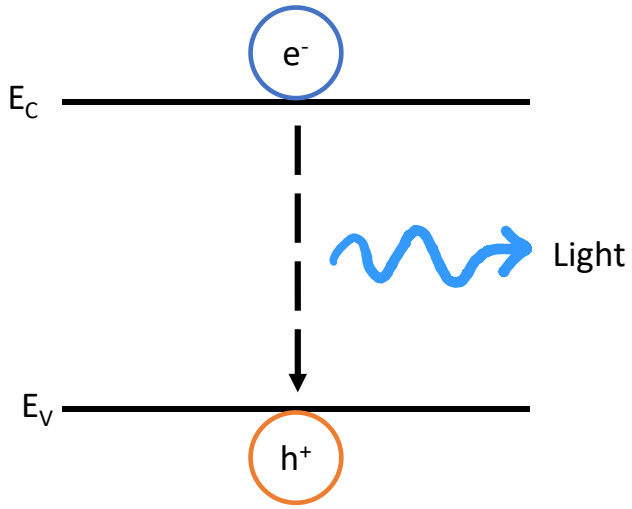


Figure 11: Schematic representation of radiative recombination.

2.2.2 Auger Recombination

Auger recombination happens when an electron in the conduction band recombines with a hole in the valence band, and the excess energy is transferred to another electron ("eeh" process) or hole ("ehh" process). A schematic representation of an Auger recombination process is shown in Figure 12. The recombination rates of both processes (R_{eeh} and R_{ehh}) are proportional to the involved carrier densities:

$$R_{eeh} = C_n(n^2\,p - n_0^2 p_0) \quad \textbf{(7)}$$

$$R_{ehh} = C_p(n\,p^2 - n_0 p_0^2) \quad \textbf{(8)}$$

$$R_{Auger} = R_{eeh} + R_{ehh} = C_n(n^2\,p - n_0^2 p_0) + C_p(n\,p^2 - n_0 p_0^2) \quad \textbf{(9)}$$

$C_n$and $C_p$are the respective Auger coefficients. In high-level injection ($\Delta n \gg N_{dop}$) , the Auger lifetimes can be approximated by:

$$\tau_{\text{Auger ,hi}} = \frac{1}{\left(C_{\text{n}} + C_{\text{p}}\right)\Delta n^2} = \frac{1}{C_{\text{A}}\Delta n^2} \quad \textbf{(10)}$$

and for low-level injection conditions ($\Delta n \ll N_{dop}$):

$$\tau_{\text{Auger ,li}} = \frac{1}{C_{\text{n}} N_{\text{dop}}^2} \text{ for n-type silicon} \quad \textbf{(11)}$$

$$\tau_{\text{Auger ,li}} = \frac{1}{C_{\text{p}} N_{\text{dop}}^2} \text{ for p-type silicon} \quad \textbf{(12)}$$

where $\Delta n = n - n_0 = p - p_0$ is the excess carrier density, n_0 and p_0 are the thermal equilibrium concentration of electrons and holes, N_{dop} is the net dopant concentration, and $C_A \equiv C_n + C_p$ is the ambipolar Auger coefficient. A more recent empirical expression on Auger recombination by Richter et al. can be found in [14]. Auger recombination is generally dominant in the heavily doped regions of the Si solar cells but may also become important in the bulk if it goes into high level injection. Reducing the heavy doping reduces the Auger recombination.

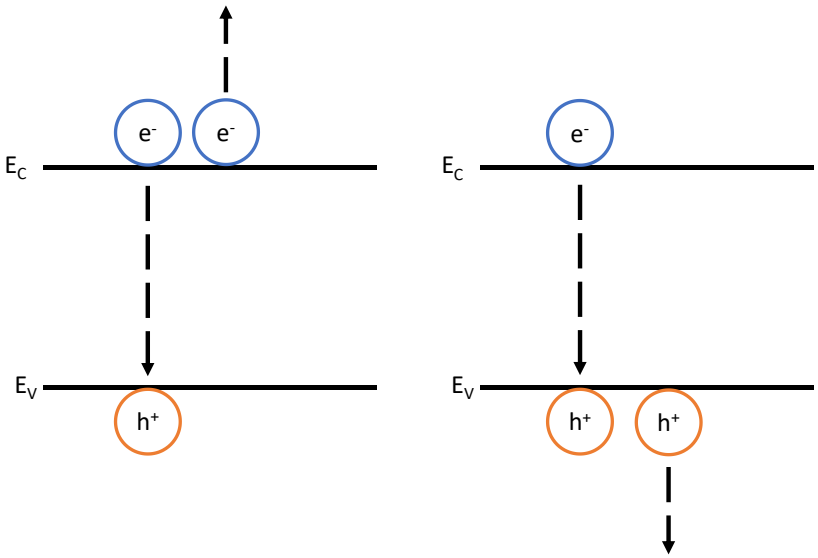


Figure 12: Schematic representation of Auger recombination, where energy is transferred to an electron (left) or a hole (right).

2.2.3 Shockley-Read-Hall (SRH) Recombination

SRH recombination occurs through extrinsic defects and is only absent in perfectly pure materials. SRH recombination involves (1) trapping of electron or hole by a defect state within the bandgap followed by (2) recombination at the same defect with another type of carrier (hole or electron) before the first trapped carrier can be released into a lower energy state. The schematic of the SRH process is illustrated in Figure 13.

The SRH recombination rate is calculated by the equation [15, 16]:

$$R_{SRH} = \frac{pn - n_{ieff}^2}{\tau_{n0}(p + p_1) + \tau_{p0}(n + n_1)} \quad \textbf{(13)}$$

where

$$\tau_{n0} = \frac{1}{v_{the} \cdot \sigma_n \cdot N_t}, \tag{14}$$

$$\tau_{p0} = \frac{1}{v_{thh} \cdot \sigma_p \cdot N_t} \tag{15}$$

and

$$n_1 = n_{ieff} \cdot \exp\left(\frac{E_t - E_i}{kT}\right) \tag{16}$$

$$p_1 = n_{ieff} \cdot \exp\left(\frac{E_i - E_t}{kT}\right) \tag{17}$$

where σ_n and σ_p are the capture cross-sections of electrons and holes, v_{the} and v_{thh} are the thermal velocities of electrons and holes, N_t is the concentration of defect states, and E_t is the energy of the defect state.

The SRH recombination lifetime can be expressed as [15, 16]:

$$\tau_{SRH} = \frac{\tau_{p0}(n_o + n_1 + \Delta n) + \tau_{n0}(p_o + p_1 + \Delta p)}{p_o + n_o + \Delta n} \tag{18}$$

SRH recombination is often the dominant recombination mechanism inside the bulk Si wafer and plays a very important role in achieving high efficiency. Deep or mid-gap traps are generally more harmful than shallow traps near band edges.

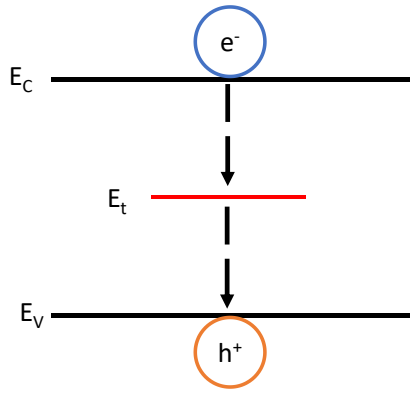


Figure 13: Schematic representation of SRH recombination. The red line in the middle represents a defect level.

2.2.4 Surface Recombination

In real materials, defects are more likely to occur at surfaces and at the interfaces between different materials, called surface states. Surface states are the result of the abrupt termination of a crystalline phase, which forms dangling bonds. The surface recombination via surface states can be explained through some modification of the SRH recombination theory.

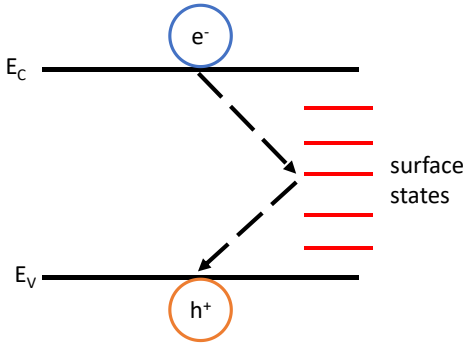


Figure 14: Schematic representation of surface recombination.

For a single level surface state, the surface recombination rate $R_{surface}$ is given by:

$$R_{surface} = \frac{p_s n_s - n_{ieff}^2}{\frac{p_s + p_1}{S_n} + \frac{n_s + n_1}{S_p}} \quad \textbf{(19)}$$

where p_s and n_S are the hole and electron concentrations at the surface. S_n and S_p are surface recombination velocities for electrons and holes, which are related to surface state density (N_{st}) and the capture cross-sections of electron and hole (δ_n and δ_p):

$$S_n \equiv \delta_n v_{th} N_{st} \quad \textbf{(20)}$$

$$S_p \equiv \delta_p V_{th} N_{st} \quad \textbf{(21)}$$

The surface recombination velocity can be obtained as:

$$S \equiv \frac{R_{surface}}{\Delta n} = \frac{n_s + p_s + \Delta n}{\frac{n_s + n_1}{S_p} + \frac{p_s + p_1}{S_n}} \quad \textbf{(22)}$$

In real situations, surface states are not localized at a single-energy level but are continuously distributed throughout the bandgap of a semiconductor. The total surface recombination rate can be obtained by integrating Eq. (19) over the entire energy bandgap:

$$R_{surface} = \int_{E_v}^{E_c} \frac{n_s p_s - n_i^2}{\frac{n_s + n_1(E)}{\delta_p(E)} + \frac{p_s + p_1(E)}{\delta_n(E)}} v_{th} \cdot D_{it}(E) dE \quad \textbf{(23)}$$

where E_V is the conduction band energy, E_C is the valence band energy, and D_{it} is the density of surface states per unit energy.

Surface recombination can be reduced by (1) reduction of the surface defect density D_{it} , and (2) reduction of the concentration of electrons or holes at the surface. The former can be achieved by chemical passivation of surface defects, which are predominantly broken silicon-silicon bonds, called dangling bonds. The latter can be done by field-effect passivation. As both an electron and a hole are needed for each recombination process, the surface recombination can be significantly reduced if either electron or hole concentration is much lower than the other. This can be achieved by the formation of a doped profile near the surface, or by fixed external charges on top of the Si surface. Surface recombination is another dominant loss mechanism in Si solar cell. Recombination velocity of a free Si surface can be ~10^5 cm/s but can be reduced to < 5cm/s by growing an appropriate dielectric SiO_2 or by depositing negatively charged Al_2O_3 [17]. On the other hand, Si surface recombination velocity increases to silicon thermal velocity (~10^7 cm/s) with metal contacts [18]. Both bulk and surface recombination effects are expressed in terms of recombination current density J_0 of that region:

$$J_0 = q\frac{D\ n_i^2}{L\ N} \times F \tag{24}$$

where F is:

$$F = \frac{\frac{S\ L}{D} + \tanh\left(\frac{W}{L}\right)}{1 + \frac{S\ L}{D}\tanh\left(\frac{W}{L}\right)} \tag{25}$$

N is doping concentration, L is diffusion length of minority carrier, D is diffusivity of minority carrier, and W is the width of the doped region. That is why special emphasis is placed on the determination of J_0 values of each region in this thesis. Total J_0 of a solar cell is the sum of J_0 contribution from each region.

The four recombination mechanisms occur simultaneously in a semiconductor material. The effective recombination rate R_{eff} can be expressed as the sum of all recombination rates:

$$R_{eff} = R_{rad} + R_{Auger} + R_{SRH} + R_{surface} \quad \textbf{(26)}$$

And the effective lifetime is given as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{surface}} \quad \textbf{(27)}$$

2.3 The Recombination Current Density J_0

The carrier recombination in the highly-doped region of Si solar cells is usually characterized by recombination current density J_0, which represents the combined effects of Auger, SRH, and surface recombination in the highly-doped region. Eq. (28) describes the operation of a solar cell where external circuit current is expressed by the superposition of a light generated short-circuit current J_{SC} and a recombination current loss due to the light-induced forward-biased voltage that develops across the load connected to the solar cell [19].

$$J = J_{SC} - J_0\left(\mathrm{e}^{\frac{qV}{kT}} - 1\right) \quad \textbf{(28)}$$

When the cell is in open-circuit condition, there is no net current between the terminals ($J = 0$) and Eq. (28) can be simplified as:

$$J_{SC} = J_0\left(\mathrm{e}^{\frac{qV_{OC}}{kT}} - 1\right) \quad \textbf{(29)}$$

From which the open-circuit voltage can be expressed as

$$V_{OC} = \frac{kT}{q}\ln\left(\frac{J_{SC}}{J_0} + 1\right) \quad \textbf{(30)}$$

which clearly shows that total recombination current density J_0 must be minimized to achieve high open circuit voltage. Recombination in any region (emitter, base, back surface field and contacts) of the solar can be quantified in terms of J_0 and the sum of all the J_0 values is referred to as total J_0 that dictates the V_{OC} in Eq. (30). This concept will be used extensively in this research for achieving high V_{OC} and cell efficiency.

The J_0 contribution from the emitter or back-surface field regions in this research was determined by measuring carrier lifetime as a function of injection level using photoconductance decay tool (Figure 15) on a symmetric test structure, coupled with J_0 extraction method proposed by Kane-Swanson [20]. The sample to be measured is placed on a coil with an oscillating magnetic field. The coil couples inductively to the sample, and the measured signal output of the circuit is proportional to the conductance of the sample. A pulse of light from a flash lamp generates electron-hole pairs in the sample. The excess

carrier concentration Δn becomes a nearly uniform distribution throughout the wafer after several transit times. The decay of Δn is recorded as a function of time from which effective lifetime τ_{eff} at different injection levels is obtained using the following equation:

$$\frac{1}{\tau_{\text{eff}}} \equiv -\frac{1}{\Delta n}\frac{d\Delta n}{dt} \tag{31}$$

τ_{eff} includes both bulk and surface recombination in that region. Since the sample substrate is in high-level injection in this experimental technique during the photoconductance measurement, Δn is almost equal to total electron concentration n. Therefore, τ_{eff} can be expressed as [21]:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{SRH}}} + 2J_0\frac{n}{qn_i^2 w} + C_A n^2 \tag{32}$$

where τ_{SRH} is the bulk Shockley-Read-Hall (SRH) lifetime, J_0 is the emitter recombination current density, w is the wafer thickness, and C_A is the ambipolar bulk Auger coefficient. As shown in Figure 16, when $\frac{1}{\tau_{eff}} - C_A n^2$is plotted as a function of injection level, the recombination current density J_0 can be extracted from the slope of the line, and $\frac{1}{\tau_{SRH}}$ can be extracted from the intercept of the line. This technique has been used in this research to extract the J_0 of unmetallized and metallized B emitter and TOPCon regions by preparing symmetric samples with the region of interest on both sides of a high lifetime wafer that goes into high level injection under illumination. Slope of effective lifetime vs injected level curve was used to quantify the recombination in the doped regions.

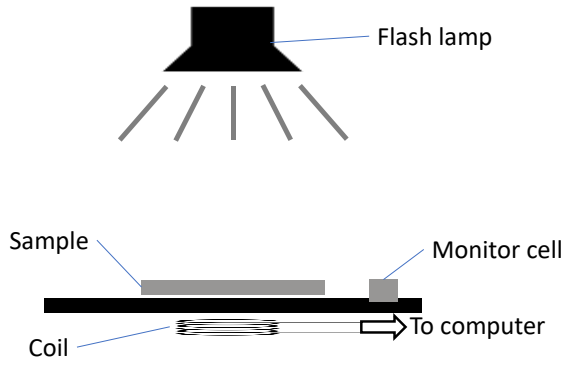


Figure 15: Schematic diagram of photoconductance decay lifetime tester used for evaluation of J_0.

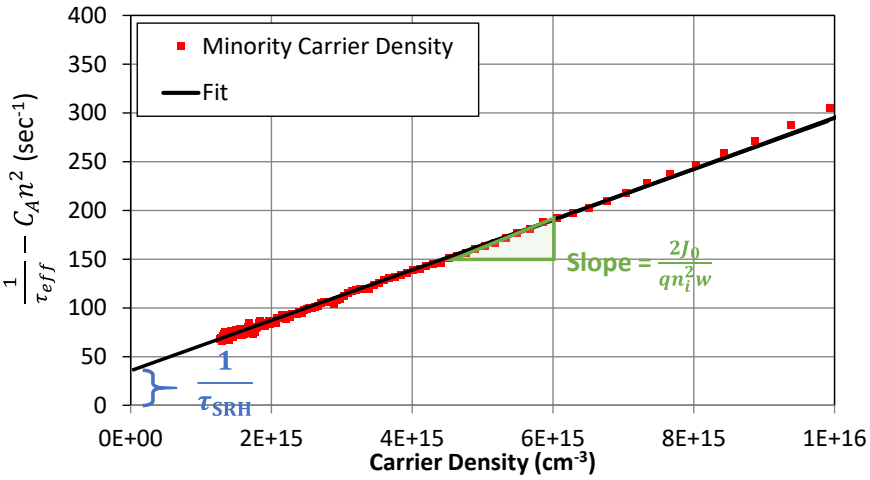


Figure 16: Extraction of recombination current density J_0 and bulk SRH lifetime from the ($1/\tau_{eff} - C_A n^2$) vs n curve.

2.4 Quantum-Mechanical Tunneling

In order to understand the carrier transport mechanism in the tunnel oxide passivating contacts, we need to understand quantum-mechanical tunneling. In classical

mechanics, particles that do not have enough energy to surmount a barrier cannot reach the other side. However, in quantum mechanics, if the barrier is thin enough, these particles can tunnel through the other side. Here we assume a negligible potential drop takes place across the thin tunnel barrier, such that a rectangular barrier can be assumed, as shown in Figure 17. The direct tunneling mechanism dominates in this case, and the Fowler-Nordheim tunneling [22, 23] can be neglected.

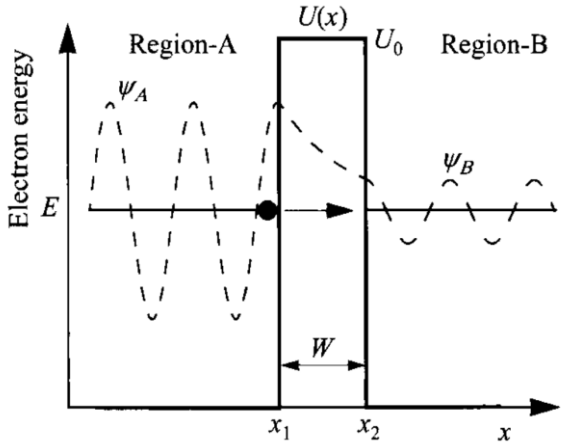


Figure 17: Wafer functions showing electron tunneling through a rectangular barrier. (Adapted from [24]).

To calculate the tunneling probability, the wavefunction ψ can be determined by the Schrödinger equation:

$$\frac{d^2\psi}{dx^2} + \frac{2m^*}{\hbar^2}[E - U(x)]\psi = 0 \tag{33}$$

With a rectangular barrier of height U_0 and width W, ψ has a general form of exp $(\pm ikx)$ where $k = \sqrt{2m^*(E - U_0)}/\hbar$. Note that $E < U$ for tunneling, so the term within the

square root is negative, and k is imaginary. The solution of the wavefunctions and the tunneling probability are calculated to be [24]:

$$T_t = \frac{|\psi_B|^2}{|\psi_A|^2} = \left[1 + \frac{U_0^2 sinh^2\,(|k|W)}{4E(U_0 - E)}\right]^{-1} \approx \frac{16E(U_0 - E)}{U_0^2} exp\left(-2\sqrt{\frac{2m^*(U_0 - E)}{\hbar^2}}W\right) \tag{34}$$

With known tunneling probability, the tunneling current J_t can be calculated from the product of the number of available states in the originating Region-A (Figure 17) and the number of empty states in the destination Region-B, and the result is the well-known Tsu-Esaki equation [25]:

$$J_t = \frac{qm^*}{2\pi^2\hbar^3}\int F_A N_A T_t (1 - F_B) N_B dE \tag{35}$$

where $F_A, F_B, N_A,$ and N_B represent the Fermi-Dirac distributions and densities of states in the corresponding regions. From the Tsu-Esaki expression (Eq. (35)) we can understand that a large tunnel current requires not only a high transmission coefficient (T_t) but also the number of occupied states before the barrier (N_A) and the number of the available states behind the barrier (N_B) which needs to be large as well. They are dictated by the position of the Fermi levels and change in the applied bias. Highly doped poly-Si is used on top of the bulk Si in the TOPCon structure creates a majority carrier accumulation layer in bulk Si via band bending in combination with large number of empty states in the poly-Si to accept the majority carriers from the bulk to facilitate their transport. In contrast, minority carries are blocked or repelled at the interface. This mechanism results in high carrier

selectivity, reduced surface recombination, and low contact resistivity in the tunnel oxide passivating contacts. Numerical simulations using Tsu-Esaki formula for the TOPCon tunneling current are reported in [26, 27], along with the explanation of excellent cell performance with TOPCon.

CHAPTER 3. LITERATURE REVIEW

3.1 Crystalline Silicon Solar Cells - Current Status and Future Trends

Crystalline silicon (c-Si) wafer-based photovoltaic technology accounts for over 90% of the total commercial PV production in the world [28] due to high energy conversion efficiency, long term reliability, low cost and well-established Si manufacturing base and infrastructure. With the advent of novel cell structures and advanced fabrication technologies, cell efficiencies have also improved steadily. Figure 18 shows a schematic diagram of the main production Si cell technologies today, including full Al-BSF, PERC, HIT, TOPCon and IBC cells. Figure 19 shows the efficiency progress and current production cell efficiency for each cell design. According to the International Technology Roadmap for Photovoltaic (ITRPV) report in 2021 [4], traditional n^+-p-p^+ full aluminum back surface field (Al-BSF) cell technology had been the work horse of PV industry for several decades but is expected to phase out in the next five years (Figure 20) because of the efficiency potential of only 20%. Passivated emitter and rear cell (PERC), which already has >50% market share today, has become the mainstream Si solar cell technology (Figure 20) and is expected to grow in market share. The major improvement in PERC cell structure [29] (Figure 18 (b)) over the traditional Al-BSF cell structure (Figure 18 (a)) is the presence of an insulating dielectric layer between the bulk Si at the back with the locally diffused p^+ region and metal contact to minimize high recombination at the full-area diffused and metal-Si contacts in Al-BSF cell. However, to allow the current flow from the rear sides, localized rear contacts are formed by laser ablation, where the high recombination may still exist in addition to resistance loss due to the lateral carrier transport

in the bulk region between the contacts. [30]. Figure 21 shows current production efficiency of PERC cells is about 21-22% with a potential of 23.5%, as predicted by Hermle [31]. Figure 21 also shows that next generation passivated carrier selective contact solar cells like TOPCon and HIT can achieve >25% efficiency due to further reduction in diffusion and metal contact induced recombination in Si. This provided the motivation to develop high efficiency commercial TOPCon solar cells in this thesis which can also be produced at a cost comparable to or lower than PERC cells. Understanding and operation of these two carrier-selective passivated contact solar cells are reviewed below.

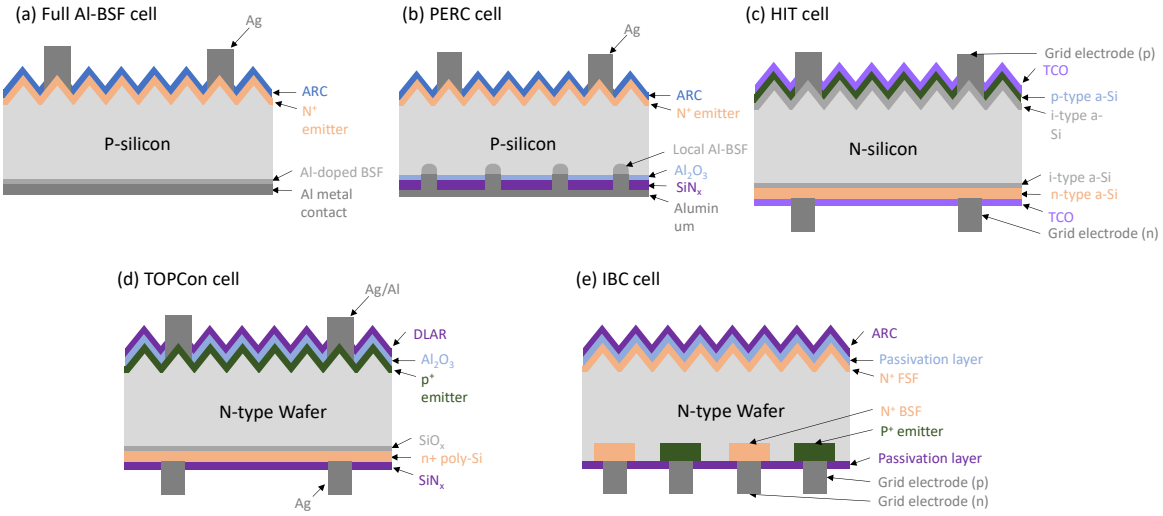


Figure 18: Schematic diagrams of the main production Si cell technologies: (a) Full aluminum-doped back surface field (Al-BSF) cell, (b) passivated emitter rear cell (PERC), (c) Heterojunction with intrinsic thin layer (HIT) cell, (d) tunnel oxide passivated contact (TOPCon) cell, (e) interdigitated back contact (IBC) cell.

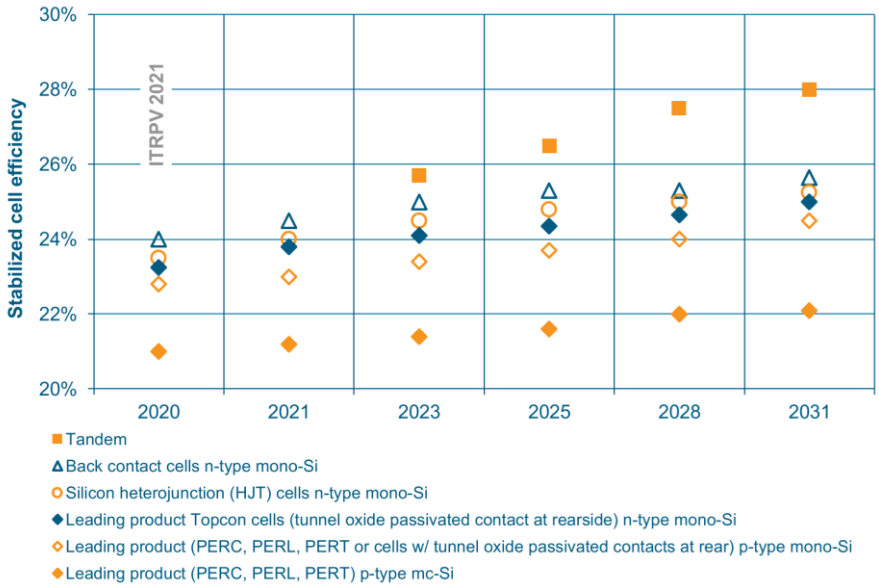


Figure 19: The expected average stabilized efficiency values of c-Si solar cells in mass production. Adapted from [4].

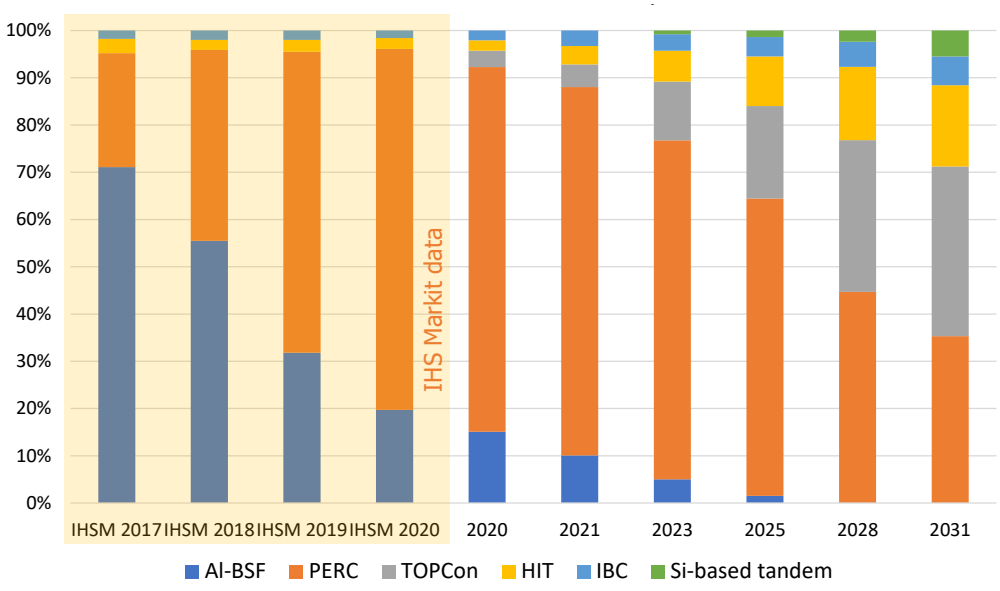


Figure 20: Trend of market shares for different cell technologies from 2017 to 2031. Replotted from [4, 32-34].

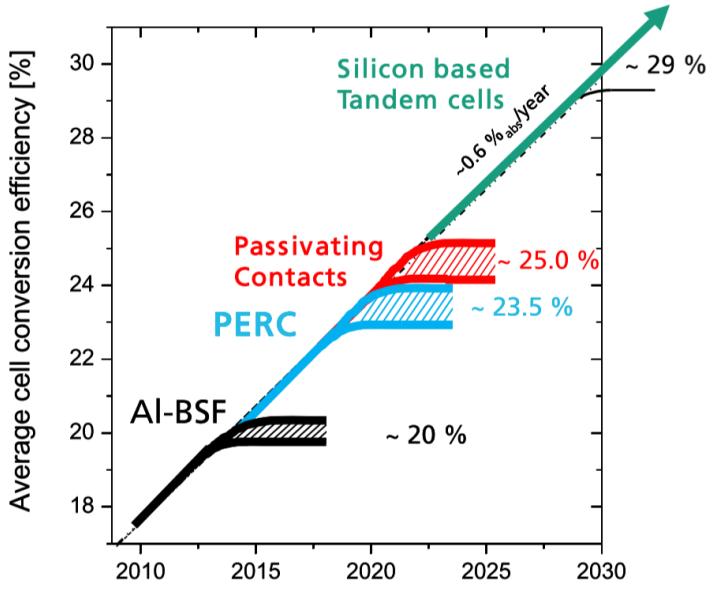


Figure 21: Potential further technological development in silicon photovoltaics. Adapted from [31].

3.2 Heterojunction with Intrinsic Thin layer (HIT) Solar Cell

HIT cells hold the current record for highest efficiency (> 25%) commercial size solar cells. The fundamental limit of high recombination on the Si/metal contacts is addressed by carrier-selective passivating contacts. These consist of a buffer layer in-between of a c-Si wafer and a highly doped layer that decouples the bulk silicon from the doped region and metal contacts. This effectively reduces electron-hole recombination at the c-Si surface while working as contacts to extract either electrons or holes from the c-Si absorber. The most well-known example of passivated contacts is HIT (Heterojunction with Intrinsic Thin layer) solar cell. In this cell structure, an intrinsic a-Si layer is deposited on both surfaces of the c-Si absorber to physically displace the doped and metallized regions outside the absorber without compromising the flow of majority carrier transport

and current collection. Table 1 shows the IV parameters from recent HIT cells which have achieved excellent V_{OC} of 750 mV with front and back contacted (FBC) cell [35] (Figure 22) and efficiency >26% with interdigitated back contacts (IBC) [36] (Figure 23). However, HIT cells suffer from J_{SC} loss due to high parasitic absorption in the a-Si layers, and the structure cannot withstand the industrial high-temperature process or firing for metallization, which is limited to low-temperature (< 200 °C), and significantly increases the manufacturing costs. Metallization in HIT cell generally requires low-temperature indium-tin-oxide (ITO) deposition in combination with thick and expensive screen-printed silver pastes for metallization which are fired at low temperature. In addition, the CapEx for a-Si deposition is expensive. That is why HIT cells or modules are much more expensive than PERC and their market share is less than 5% in spite of much higher efficiency than PERC.

Table 1: IV parameters of recent HIT cells from the literature.

Institute	Cell type	Area [cm^2]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Eff [%]	Thickness [µm]	Reference
Kaneka	IBC	79	738	42.65	84.9	26.7	165	[36, 37]
Panasonic	IBC	143.7	740	41.8	82.7	25.6	150	[38]
Kaneka	FBC	151.9	738	40.8	83.5	25.1	160	[39]
Panasonic	FBC	101.8	750	39.5	83.2	24.7	98	[35]

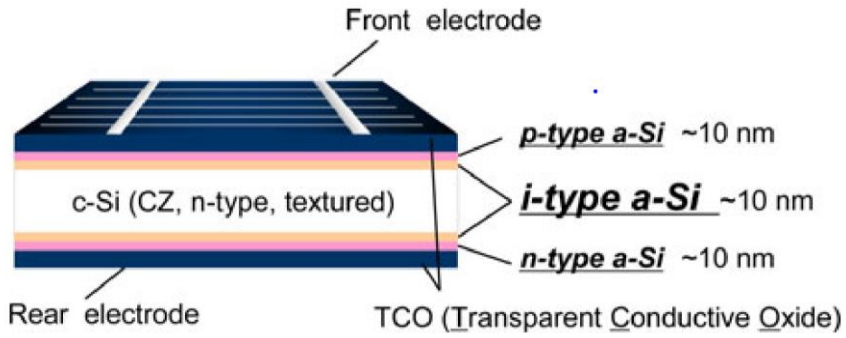


Figure 22: Structure of a FBC HIT solar cell [35].

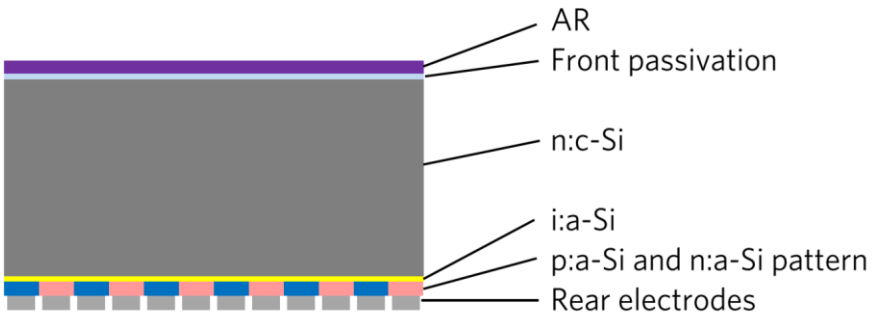


Figure 23: Structure of an IBC HIT solar cell [36].

Figure 24 shows the energy band diagram for the HIT solar cell. Carrier selectivity is achieved by the difference in bandgap between crystalline and a-Si, and the corresponding valence and conductance band offsets. On the rear side of the FBC HIT cell, the band offset is very small for the conduction band, so electrons can easily tunnel or hop into the n^+ a-Si layer, which then transports them to the metal contact on the back for current collection or energy extraction. Note that holes run into a very large band offset preventing their flow from the absorber into the contact. This reduces contact recombination dramatically. In addition, hydrogenated a-Si passivates the silicon surface

or this interface, which also reduces the surface recombination. This results in very low J_0 (< 1 fA/cm^2) and high V_{OC} (> 735 mV) [36]. By depositing p-doped a-Si on the other side gives an excellent hole selective contact. Thus HIT cells have optimal carrier selective contacts, which passivate the defects on the Si surface while simultaneously being selective and conductive for only one type of carrier.

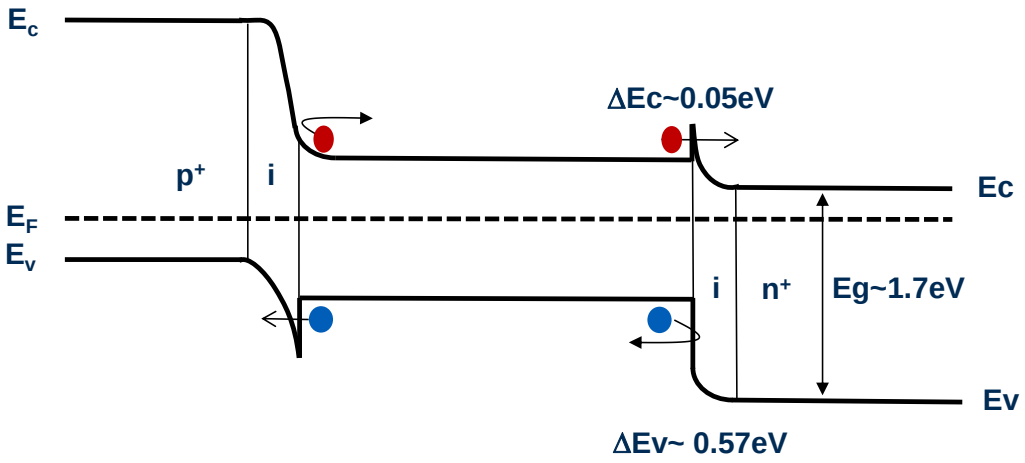


Figure 24: Schematic band diagram of HIT cell.

3.3 Tunnel Oxide Passivated Contact (TOPCon) Solar Cell

An alternative approach to HIT cell is to use tunnel oxide passivated contact (TOPCon), which is based on a stack of ultra-thin SiOx layer capped with a doped poly-Si layer (Figure 25) instead of intrinsic and doped a-Si layers. Excellent surface passivation, elimination of direct metal contact with absorber material, and great thermal stability at high temperatures [40-42] have been demonstrated for TOPCon structure. Figure 26 from the 2019 IEEE Photovoltaic Specialist Conference (PVSC) experts panel discussion suggest that TOPCon can beat both PERC and heterojunctions (HJ) for the lowest levelized cost of energy (LCOE). TOPCon cells can achieve HIT cell-like efficiencies at a cost

comparable or lower than PERC cells to achieve US Department of Energy 2030 LCOE target of 2¢/kWh [7], which will require ~25% modules at ~25¢/W.

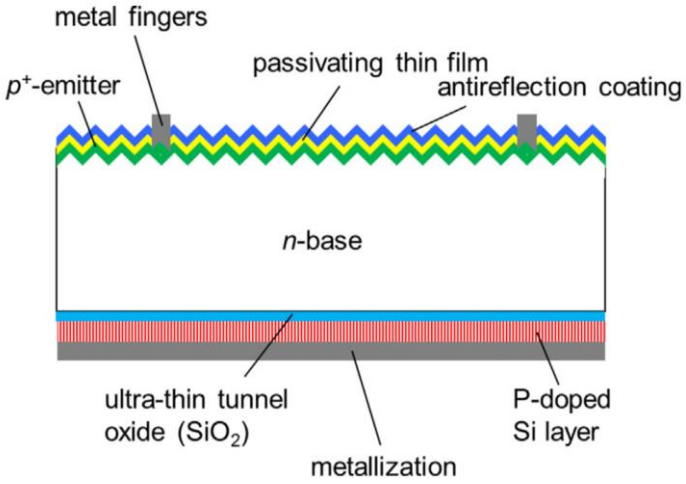


Figure 25: Structure of a solar cell with the tunnel oxide passivated contact (TOPCon).

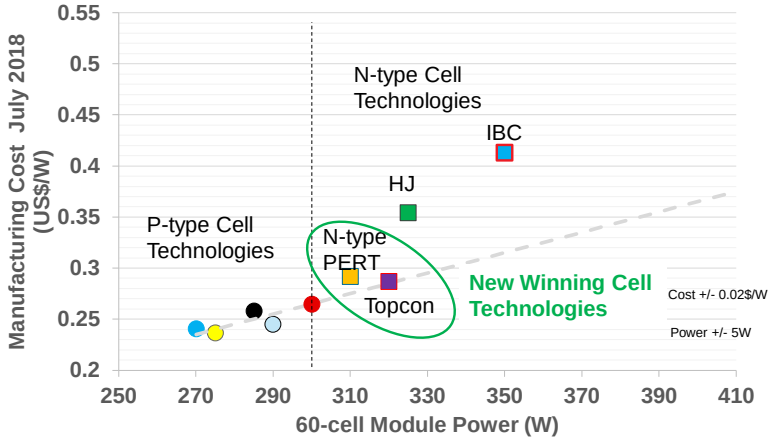


Figure 26: Manufacturing cost and power output of existing and future commercial p- and n-type PV products. The dashed line is the line of equal LCOE (US$0.01/10W) (Presented by Pierre Verlinden at 2019 IEEE PVSC).

Small area (4 cm^2) TOPCon R&D cells have already achieved efficiency approaching 26.0% with V_{OC} of 732mV on float-zone (FZ) Si wafers and thermally evaporated metal contacts [43]. Table 2 shows IV parameters of small area (~4 cm^2) R&D TOPCon cells in literature. Some investigators have also reported low recombination current density (J_0) (< 10 fA/cm^2) [42, 44-47] for n-TOPCon with ~1.5 nm SiO_x capped with phosphorus-doped poly-Si. However, to displace PERC by TOPCon cells for mass production, use of low-cost Czochralski (Cz) Si wafers in combination with traditional low-cost high-throughput industrial screen-printing process needs to be incorporated in TOPCon technology without sacrificing efficiency. This provided the motivation in this research to implement an industrial friendly process and approach, using traditional screen-printing metallization, to demonstrate high efficiency (~23%) single side TOPCon cells on Cz wafers without increasing cost and complexity.

Table 2: IV parameters of small area (~4 cm^2) R&D TOPCon cells in literature.

Institute	Cell type	Wafer type	Area [cm^2]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Eff [%]	Reference
ISFH	IBC	P-FZ	-	727	42.6	84.3	26.1	[48]
FISE	FBC, RJ	N-FZ	4	732	42.1	84.3	26.0	[43]
FISE	FBC, FJ	N-FZ	4	724	42.9	83.1	25.8	[10]
Georgia Tech	FBC, FJ	N-FZ	4	711	41.2	81.4	23.8	[46]

-: Data not reported in the referenced literature

Figure 27 shows the R&D efficiency evolution of notable front and back contact (FBC) silicon solar cells with PERL (Figure 21), HIT (Figure 22) and TOPCon (Figure 25)

cell architectures. The performance of PERL cells is limited by recombination at the local metal contacts to Si wafer with heavy doping underneath [49], which results in lower V_{OC} compared to HIT and TOPCon (Figure 27(b)), where there is no diffusion and metal contacts to Si absorber. HIT cells exhibit excellent V_{OC} (Figure 27(b)) due to the full-area passivating contacts on both front and back surfaces, however, J_{SC} of HIT cells (Figure 27(c)) is limited by the parasitic absorption losses due to the full-area a-Si:H layer at the front surface and the transparent conductive oxide (TCO) on top required for lateral current transport [43]. Figure 27 (a) shows that efficiency of single-side TOPCon R&D cells is now ahead of both HIT and PERL structure, because it benefits from both full-area passivating contact on the rear side, and transparent high-quality dielectric surface passivation on the front side. The challenge is to demonstrate manufacturable large area cells with such efficiencies. At the start of this thesis there was no TOPCon cell production but very recently some companies have announced pilot production of TOPCon cells.

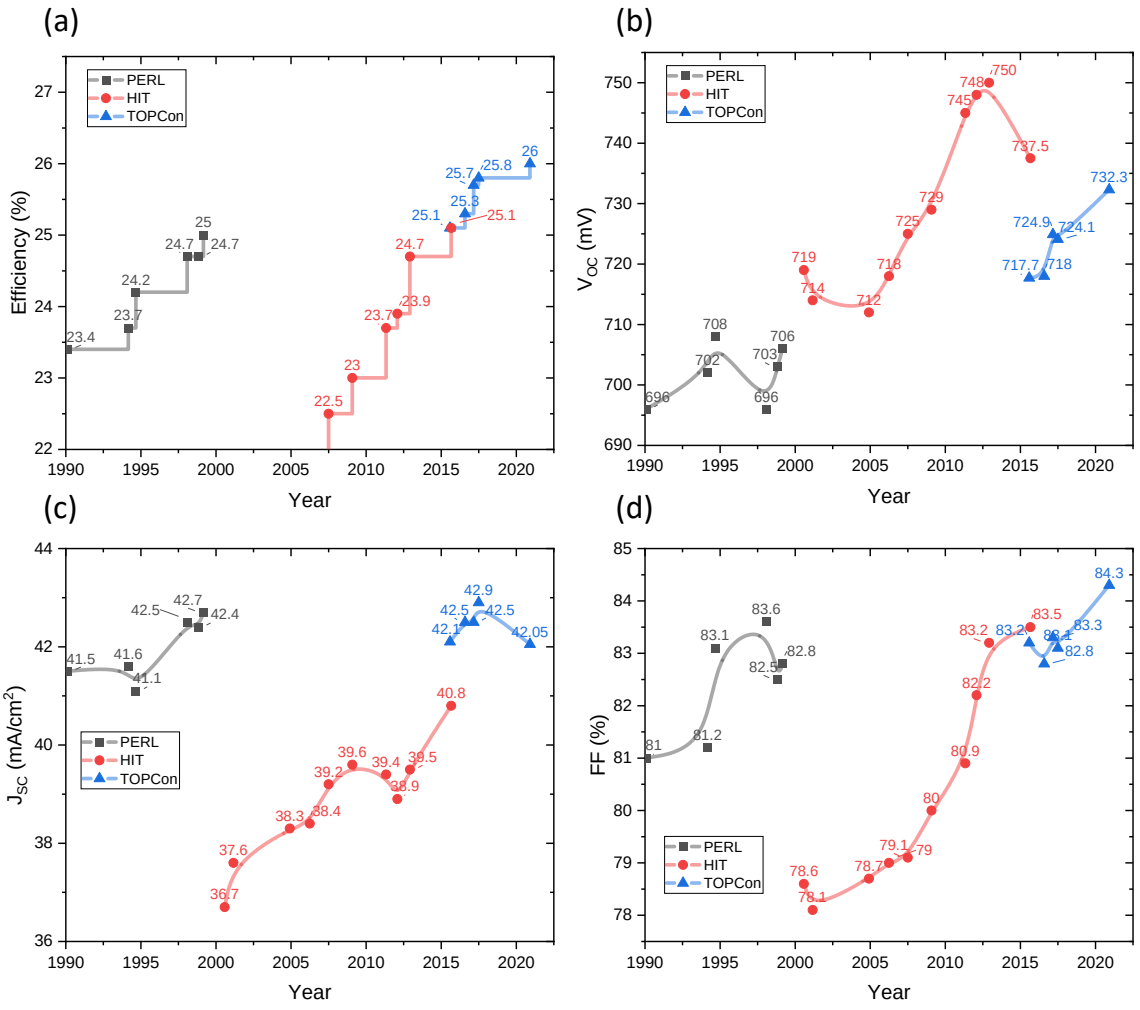


Figure 27: Efficiency evolution over the past 30 years for different high efficiency cell architectures: PERL, TOPCon and HIT with front and back contacts in small area R&D cells (Replotted from [43]).

3.4 Operating Principle and Fundamental Understanding of Carrier Selective TOPCon Structure for Achieving Excellent Passivation

This section reviews the basic operation of n-TOPCon passivated contact and the mechanisms that contribute to excellent passivation. Figure 28 shows the schematic band diagram of the electron selective n-TOPCon, and how and why it provides such good

surface passivation. A combination of high carrier selectivity and significantly reduced interface recombination is the key to excellent passivation from TOPCon. There are four parallel mechanisms that contribute to carrier selectivity:

(1) Heavily doped n^+ poly-Si creates an accumulation layer at the absorber/tunnel oxide interface due to the work function difference between the n^+ poly-Si and the n-type c-Si absorber. This band bending induces an electron-rich accumulation layer at SiO_2/Si interface, which presents a barrier for minority carrier holes to get to the tunnel oxide while assisting majority carrier electrons to migrate toward the oxide/Si interface to increase the supply of electrons [26, 50]

(2) Tunnel oxide provides the second level of carrier selectivity, because it has a larger tunneling barrier for holes (4.5 eV) than for electrons (3.1 eV) [51, 52]

(3) A large number of available states in the conduction band of the poly-Si layer in combination with a large number of electrons at the absorber/oxide interface allows electrons in the n-Si to easily tunnel through the ultrathin oxide into n^+ poly-Si. However, there are fewer holes near the valence band edge of the absorber because of band bending and may also not be able to tunnel through if the valance band edge of Si falls within the forbidden gap of n^+ poly-Si [26, 53]. Since minority carriers are unable to tunnel through, their recombination in the n^+-doped poly or metal contacts is reduced or eliminated.

(4) Besides carrier selectivity, minority carrier recombination is also reduced at the interface defects due to field-effect which increases electron concentration (accumulation layer) and reduces hole concentration at the Si-oxide interface. This asymmetric concentration of electrons and holes reduces defect-induced Shockley-

Read-Hall (SRH) recombination at the interface [54, 55], further lowering the J_0 value associated with this TOPCon structure.

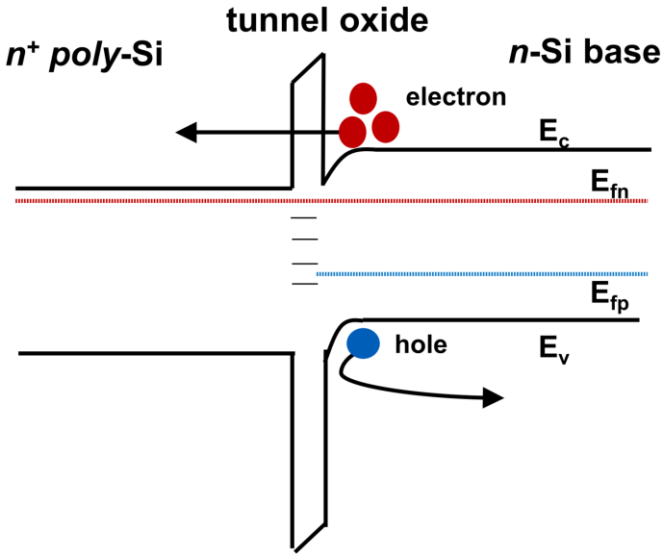


Figure 28: Schematic band diagram of tunnel oxide passivated contact.

Same mechanism works on p^+ poly-Si for hole-selective passivating contacts, however, slightly higher recombination in p-TOPCon relative to n-TOPCon has been reported [11, 56]. The fundamental differences between n- and p-TOPCon can be attributed to: (1) higher oxide barrier height for holes than electrons [57], (2) boron-doped silicon films have a higher defect density [58] and (3) the boron penetration through the tunnel oxide causes more defects [59]. Therefore, this research will focus on single side n-TOPCon cells with B diffused emitter on front and n-TOPCon on the rear of a n-type Si wafer.

3.5 Progress in Industrial Screen-Printed N-TOPCon Cells.

Previous section discussed why TOPCon structure gives such good surface passivation, and this section will review how good it is with respect to metal-induced recombination, especially for high-temperature screen-printed metallization. High efficiency (> 25.7%) small area R&D cells have been achieved with n-TOPCon structure in literature (Table 2). However, these cells were produced by photolithography processes and full-area evaporated Ag contact on rear n-TOPCon [10]. Since evaporated metal contacts are not viable for PV because of cost and throughput, implementation of traditional screen-printed metal contacts will be investigated in this research without compromising the passivation quality The poly-Si thickness, firing conditions, and paste chemistry need to be optimized to prevent the penetration of the metal paste through the poly-Si and tunnel oxide. While thicker poly-Si should help screen-printed contacts, it also increases parasitic absorption, which in turn decreases short circuit current [60, 61]. Proper poly-Si thickness is essential to achieving the lowest J_0 and highest V_{OC} without sacrificing J_{SC}.

Recently, few investigators have reported very low J_0 (< 10 fA/cm^2) for screen printed n-TOPCon structure using thicker poly-Si layers (200-300 nm), which has resulted in commercial size cell efficiencies of 21-23.5% [62-67]. In spite of these encouraging results, there is limited understanding of loss mechanisms in such commercial ready screen-printed cells. This provided the motivation in this thesis to fabricate, characterize and model such high efficiency commercially viable bifacial single-side TOPCon cells with screen-printed metallization on both sides. Figure 29 and Table 3 summarize the status of manufacturable screen-printed TOPCon solar cells in the literature. At the onset of this research in 2017, the efficiency of manufacturable TOPCon cells was only ~20.7%, that is

why we set an efficiency target of ~23% for manufacturable TOPCon cells in this research. Since then, couple of organizations, including Georgia Tech, Trina and SERIS have reported manufacturable TOPCon cell efficiencies in the range of 22.5-24.5% with very recent press releases from Jinko Solar claiming efficiency approaching ~25%. In addition, Trina, Jolywood and Jinko corporations have announced pilot production of this promising PV technology.

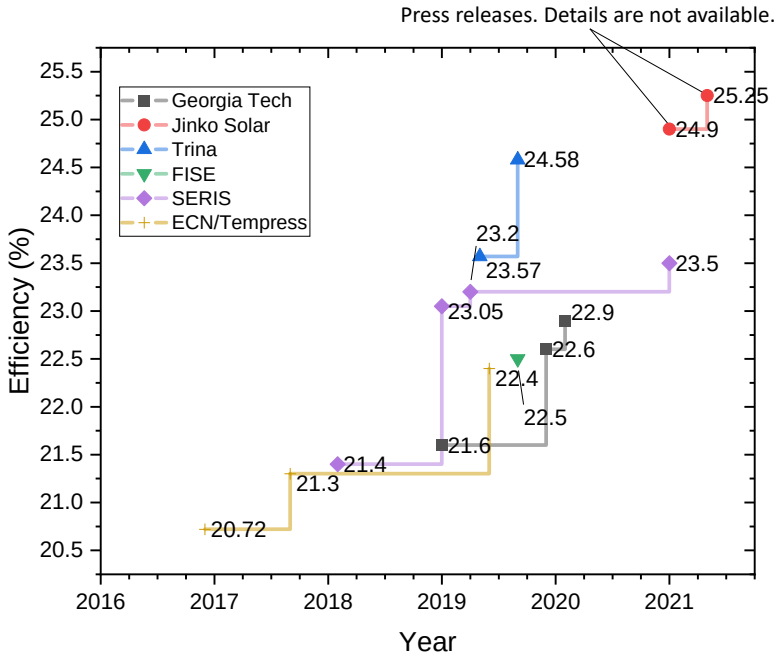


Figure 29: Evolution of industrial manufacturable n-TOPCon cells from publications, conference, and recent press releases. Detailed information and references are listed in Table 3.

Table 3: Literature survey of screen-printed n-TOPCon solar cells on large area n-type Cz wafers.

Year/ Month	Institute	Area [cm^2]	Front emitter	Front Busbar	iOx	Poly-Si layer	Metallization on poly-Si	Voc [mV]	Jsc [mA/cm^2]	FF [%]	Efficiency [%]	$J_{0b',pass}$ [fA/cm^2]	$J_{0b',metal}$ [fA/cm^2]	Ref.
2019/12	Georgia Tech	239	180 Ω/□ boron implanted.	5 floating busbars	Wet-chemical	LPCVD poly, 200nm	Screen-printed FT Ag, 5BB, 300 fingers,	702	40.3	79.7	22.6	~2	~31	This work, [68]
2020/2	Georgia Tech	100	170 Ω/□ boron implanted	Fire-through busbars	Wet-chemical	LPCVD poly, 200nm	Screen-printed FT Ag, 3BB, 200 fingers	693	40.9	80.6	22.9	~1	~31	This work, [69]
2021/5	Jinko Solar	267.4	- (Press release, details are not available)					-	-	-	25.25	-	-	[70]
2021/1	Jinko Solar	267.8	- (Press release, details are not available)					-	-	-	24.9	-	-	[71]
2019/9	Trina	244.62	Boron diffusion	Floating 9 busbars	Thermal oxide	LPCVD intrinsic poly, 200nm + $POCl_3$ diffusion	Scree-printed FT Ag	716.8	40.57	84.52	24.58	1.3	50.7	[72, 73]
2019/5	Trina	258.3	Boron diffusion	Floating busbars	Thermal oxide	LPCVD intrinsic poly, 200-300nm + $POCl_3$ diffusion	Scree-printed FT Ag	716.7	40.14	82.0	23.57	2.6	-	[66]
2019/9	FISE	244.3	BBr3 diffusion, 122 Ω/□.	Busbarless metal grid	Thermal oxide 1.2nm	PECVD, 170nm	Busbarless metal grid	691.2	40.4	80.7	22.5	-	-	[67]
2021/1	SERIS	244.3	Boron diffusion	-	PECVD in-situ oxide	-	Screen-printed FT metal contact	697	41.4	81.3	23.5			[74]
2019/4	SERIS	244.3	Boron diffusion	-	PECVD in-situ oxide	PECVD with high atomic O-content	Screen-printed FT metal contact	695	41.3	80.8	23.2	-	-	[75]

Table 3 (continued)

2019/1	SERIS	244.3	Boron diffusion	-	PECVD in-situ oxide	PECVD, 250nm with high atomic O-content	Screen-printed FT metal contact	694	41.0	81.0	23.05	-	-	[76]
2018/2	SERIS	244.3	Boron diffusion	Non-floating busbars	In-situ by LPCVD	LPCVD poly	Screen-printed FT Ag, 5BB (H-pattern, finger number is not mentioned)	673	39.2	81.2	21.4	4	-	[64]
2019/6	ECN, Tempress	244 cm^2	-	-	-	-	Screen-printed FT metal contact	696	-	-	22.4	-	-	[77] (indirect ref)
2017/9	ECN, Tempress	6" Cz	Boron diffusion	-	Thermal oxide	LPCVD intrinsic poly + POCl3 diffusion. 200nm	Screen-printed FT pastes	679	39.2	79.9	21.3	-	100-200	[62]
2016/12	ECN, Tempress	6" Cz	Boron diffusion	-	NAOS	-	-	675	38.8	79.1	20.72	7.7	-	[63]

-: Data not reported in the referenced literature; FT: Fire-through; BB: Busbars

CHAPTER 4. TASK 1: DEVELOPMENT OF A TECHNOLOGY ROADMAP TO 23% EFFICIENCY TOPCON SOLAR CELLS

In Task 1, we implemented several models including Sentaurus and Quokka 2 for 2D device simulation, Sentaurus Process model for simulating implanted emitter profiles, PV Lighthouse OPAL 2 optical model for designing antireflection coating, an in-house grid model for optimizing contact grid designs with and without floating busbars. In addition to developing a technology roadmap, these models are used throughout this research to analyze the fabricated cells and understand the loss mechanisms. To begin with, we fabricated and modeled a 21% traditional n-PERT cell with diffused p^+ boron emitter on the front and P-doped n^+ back surface field on the rear side of a n-type Si wafer. Then, we characterized and model this cell with the help of Sentaurus and Quokka 2 models to establish a benchmark or starting point for the technology roadmap. Device modeling was extended to develop a realistic roadmap for driving this efficiency to $\geq$ 23% through practically achievable advanced cell design features and technology enhancements. This involved transforming the cell design from PERT to TOPCon and identifying and quantifying required enhancements in B emitter, rear n-TOPCon region, bulk lifetime and resistivity, optical properties including reflectance and light trapping, and contact parameters including shading, resistance and fill factor that can lead to 23% n-TOPCon cell efficiency. In addition, detailed modeling was performed to quantify the efficiency enhancement from each cell design feature and technology improvement. Modeling was also used in combination with detailed cell characterization to quantify and understand the loss mechanisms in the fabricated cells throughout this research. The cell efficiency

roadmap was used to guide the experimental work and validate the technology development. Each layer of the device was investigated and optimized individually, and then integrated into a process sequence to achieve the target efficiency. Finally, based on the fundamental and applied know-how developed in this research, a new roadmap was developed for ~25% efficient manufacturable TOPCon cells.

4.1 Device Modeling of Si Solar Cells

Device simulations of Si solar cells can optimize device design and performance much faster than experimentation by minimizing the time, expense, and trial runs associated with device fabrication. In addition, simulations can also be used to understand, analyze, and predict electrical and optical losses. Thus, information that is often difficult to obtain experimentally can be revealed more easily through modeling. That is why the first step in this research was to establish a roadmap to 23% efficiency by modeling and fundamental understanding.

Sentaurus [78] is the most widely used device simulator in the semiconductor industry. In Sentaurus model, all points in the finite element mesh are solved with the Poisson equation and the continuity equations. This also makes Sentaurus an ideal simulator for optimizing the doping profiles in the diffused regions, as well as the contact mechanisms between the metal and silicon surfaces. Therefore, Sentaurus is used in this research to optimize and simulate the effects of different boron implanted emitter profiles and screen-printed metal pastes on J_{0e} and contact resistivity of our solar cells. For example, Sentaurus model can generate B profiles based on process conditions along with the corresponding J_0 vs surface recombination velocity (SRV) curve for that profile, since J_0

is a function of doping as well as SRV. Since SRV at metal-Si interface is ~1×10^7 cm/s one can obtain the J_0 for the metallized region for a known doping profile without experimentation. J_0 of the unmetallized regions on front and back was determined experimentally by making symmetric unmetallized structures on high lifetime Si wafer followed by photoconductance decay measurements described in Section 2.3. Once we know the J_{0e} of the un-metallized region by experimentation, corresponding SRV can be extracted from the same J_{0e} vs SRV curve. Such techniques were utilized and validated in this research to achieve optimum B emitter profile that will result in lowest total J_{0e} without compromising contact resistivity.

Sentaurus is a very powerful semiconductor simulator, but it comes with the drawbacks of availability and complexity in simulation setup and computation time, due to the doping concentration and carrier densities varying over orders of magnitude within a few microns. Quokka 2 [79] is a freely available solar cell simulator. It simplifies the full set of charge carrier transport equations to the conductive boundary model [80], and the quasi-neutrality assumption [79]. In the conductive boundary model, recombination current density (J_0) and sheet resistance (R_{sheet}) are used as simulation inputs [81], which are also the properties commonly known and used to characterize doped regions in solar cells. There is no need for the detailed doping profile. In contrast, Sentaurus requires complicated doping profiles and surface recombination velocity as inputs, which are harder to characterize and needs additional calculation or conversion from measured data. Therefore, in this work, Quokka 2 is used more extensively for device simulations to estimate solar cell parameters and efficiency especially when the detailed resolution in doping profiles is not available.

4.2 Development of a Technology Roadmap for > 23% Efficient n-TOPCon Cells

This study started with the fabrication of traditional p^+-n-n^+ PERT cells with full area boron and phosphorus diffusions on front and back of a n-base Si. These cells are characterized and modeled with Quakka simulations to validate the device modeling capabilities. The simulations are then extended to establish a technology roadmap to achieve target cell efficiency of 23%. Analysis of our ~21% PERT cells showed that based on our starting material quality and processing, we can maintain bulk lifetimes in the range of 1-2 ms in the finished cells. Therefore, we have created a technology roadmap with a bulk lifetime of 1.5 ms.

Figure 30 shows the starting n-PERT and final n-TOPCon cell structures. Figure 31 shows the technology roadmap to > 23% efficiency developed in this research including proposed step-by-step cell design features and technology enhancements, starting with the traditional 21% N-PERT cell fabricated at the start of this project. Our characterization and modeling revealed that this PERT cell has a total J_0 = 304 fA/cm^2, V_{OC} = 661 mV and J_{SC} = 39.2 mA/cm^2. This modeling was performed using the 2D Quokka 2 simulator. Since low J_0 or reduced total recombination is the key to high V_{OC}, J_{SC} and efficiency, in Figure 31 we have also determined and specified the individual contributions to total J_0 from the 1) front and back metallized regions 2) unmetallized B emitter and back surface field regions, and 3) the bulk wafer. This information is valuable in identifying the regions that limit cell performance. It is important to recognize that total J_0 of the solar cell is the sum of all five J_0 contributions:

$$J_{0,total} = \left(J_{0,metal} + J_{0,pass}\right)_{front} + \left(J_{0,metal} + J_{0,pass}\right)_{back} + J_{0,bulk} \quad \textbf{(36)}$$

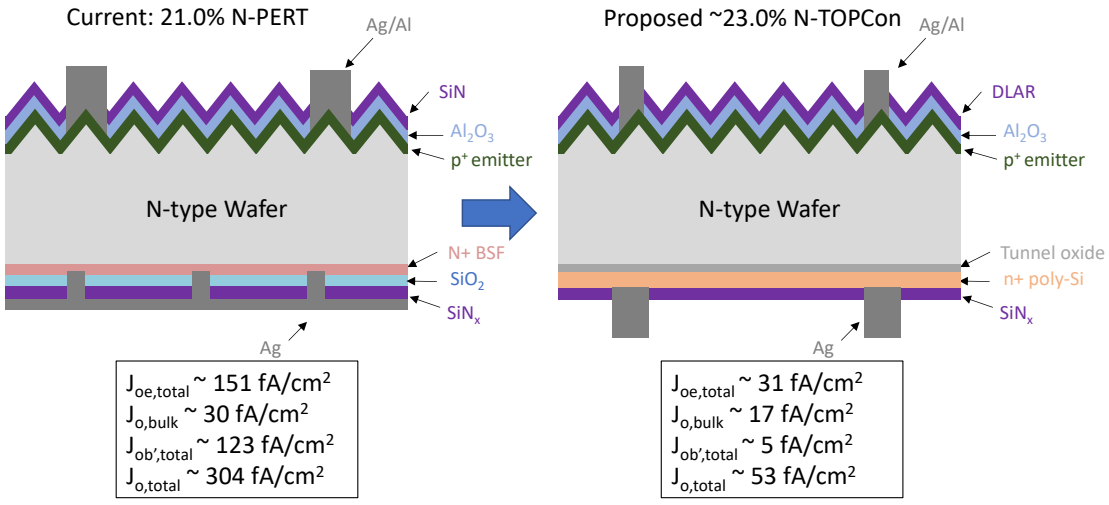


Figure 30: Schematic diagram of the starting 21% n-PERT structure and proposed ~23% n-TOPCon structure with recombination current density (J_0) targets for different regions.

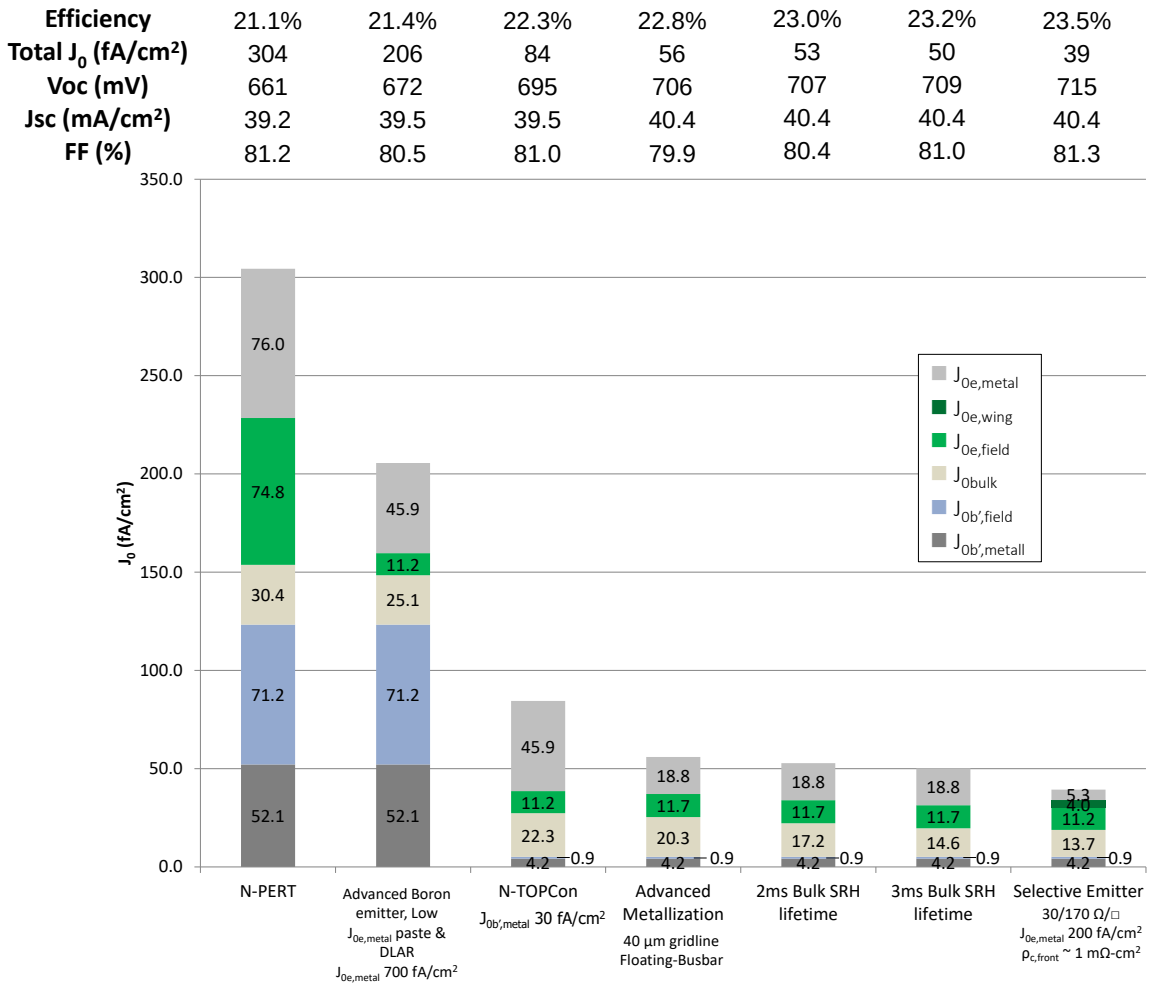


Figure 31: Technology roadmap for >23% n-TOPCon cells, starting with our 21% n-PERT cell. Each bar shows J_0 contribution from metallized and unmetallized regions on front and back as well as from the base material along with all the key cell parameters and efficiency.

Table 4 shows the physical models used for device simulations. Table 5 shows the detailed input and output parameters for each cell design or bar on the roadmap. Notice that in our 21% PERT cell, B emitter is 95 Ω/□ with single-layer AR coating, metal grid coverage of 6.5% and fire-through busbars. This resulted in metallized J_{0e} of ~150 fA/cm^2 just from the B emitter only. Similarly, full area P diffused BSF on the rear with screen-

printed contact resulted in very high metallized $J_{0b'}$ of 123 fA/cm^2. In addition, J_{0e} and $J_{0b'}$ are subdivided into recombination contribution from the metallized and unmetallized regions on front and back. Finally, the bulk contribution of 30.4 fA/cm^2 to total J_0 was determined from the difference between total J_0 of 304 fA/cm^2, obtained from the V_{OC} and J_{SC} of the cell, and the known metallized J_{0e} and $J_{0b'}$ numbers:

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_0} + 1\right) \quad \textbf{(37)}$$

$$J_{0,bulk} = J_0 - J_{0e} - J_{0b'} \quad \textbf{(38)}$$

Table 4: Physical models for the device simulations.

Physical model	**Reference**
Auger recombination	Richter et al. [14]
Radiative recombination	Trupke et al. [12]
Mobility	Arora et al. [82]
Intrinsic carrier density	Green et al. [83]
Bandgap narrowing	Schenk et al.[84]

Table 5: Quokka 2 modeling results and input parameters for the n-PERT and n-TOPCon cells.

	N-PERT	Advanced Boron emitter, Low $J_{0e,metal}$ paste, & DLAR	N-TOPCon	Advanced Metallization	2ms Bulk SRH lifetime	3ms Bulk SRH lifetime	Selective Emitter
Efficiency	**21.1%**	**21.4%**	**22.3%**	**22.8%**	**23.0%**	**23.2%**	**23.5%**
Total J_0 (fA/cm^2)	**304**	**206**	**84**	**56**	**53**	**50**	**39**
Voc (mV)	**661**	**672**	**695**	**706**	**707**	**709**	**715**
Jsc (mA/cm^2)	**39.2**	**39.5**	**39.5**	**40.4**	**40.4**	**40.4**	**40.4**
FF (%)	**81.2**	**80.5**	**81.0**	**79.9**	**80.4**	**81.0**	**81.3**
Cell size (cm^2)	239	239	239	239	239	239	239
Anti-Reflection Layer	Single Layer	Double Layers	Double Layers	Double Layers	Double Layers	Double Layers	Double Layers
Front finger width W_f (μm)	55	55	55	40	40	40	40
Front shading coverage	6.55%	6.55%	6.55%	4.59%	4.59%	4.59%	4.59%
Front metal contact coverage	6.55%	6.55%	6.55%	2.67%	2.67%	2.67%	2.67%
Busbar number / width (μm)	5 / 900	5 / 900	5 / 900	5/600	5/600	5/600	5/600
Floating or Fire-through BB	Fire-through BB	Fire-through BB	Fire-through BB	Floating BB	Floating BB	Floating BB	Floating BB
Wafer Thickness (μm)	180	180	180	180	180	180	180
Front Contact Resistivity (mΩ-cm^2)	1	3	3	3	3	3	1
Selective emitter sheet resistance (Ω/□)	NA	NA	NA	NA	NA	NA	30
Selective emitter junction width (μm)	NA	NA	NA	NA	NA	NA	100
Wing J_0 (fA/cm^2)	NA	NA	NA	NA	NA	NA	100

Table 5 (continued)

Front passivated J_0 (fA/cm^2)	80	12	12	12	12	12	12
Front contact $J_{0,metal}$ (fA/cm^2)	1160	700	700	700	700	700	200
Front emitter sheet resistance (Ω/□)	95	170	170	170	170	170	170
Substrate resistivity (Ω-cm)	2	2	2	2	2	2	2
mid-gap SRH Lifetimes ($\tau_n=\tau_p$) (ms)	1.5	1.5	1.5	1.5	2	3	3
Back Contact Resistivity ($m\Omega\text{-}cm^2$)	1	1	2	2	2	2	2
Rear passivated J_0 (fA/cm^2)	72	72	1	1	1	1	1
Rear contact $J_{0,metal}$ (fA/cm^2)	4600	4600	30	30	30	30	30
Rear contact percentage	1.13%	1.13%	13%	13%	13%	13%	13%

Table 5 summarizes all the details and input parameters used in modeling to generate the step-by-step roadmap. These inputs establish the material and device parameters that need to be achieved simultaneously in a cell through technology developments to attain all five J_0 components (Figure 31) and target cell efficiency. Roadmap clearly shows what improvements are needed in B emitter, n-TOPCon, screen printed metallization and bulk lifetime to gradually get to 23% cell efficiency. Notice that total allowed J_0 for achieving 23% efficient cell is only about 50 fA/cm^2 (bar 5 in Figure 31) as opposed to 304 fA/cm^2 in 21% PERT cell. It was found that a metallized J_{0e} of 30 fA/cm^2 for B emitter and J_{0b}, of 5 fA/cm^2 for the rear TOPCon region, in combination with

1-2 ms bulk lifetime, two-layer antireflection coating, and 40 μm wide 106 grid lines with five floating busbars on the front can attain our efficiency target. Therefore, we had to improve and design each layer of the n-PERT cell to minimize J_0 using practically achievable parameters. The roadmap not only tells us how much J_0 reduction is needed in each region, but it also provides guideline about how to achieve that. For example, the second bar in roadmap shows that we can obtain 21.4% efficient cells by lowering the total J_0 from 304 to 206 fA/cm^2 which can be achieved by reducing the metallized J_{0e} of the B emitter from 150 to 57 fA/cm^2. Roadmap also outlines that this can be achieved by a combination of raising emitter sheet resistance from 95 to 170 Ω/□ to lower the unmetallized J_{0e} and then finding or using an advanced screen-printed metal paste and firing scheme that can reduce metal-Si recombination to lower the full area $J_{0e,metal}$ from 1160 fA/cm^2 to 700 fA/cm^2 (Table 5). These guidelines are followed in technology development section.

The second bar in the roadmap shows that once we fix the emitter, the cell performance becomes limited by the two high J_0 regions below the base. The third bar in the roadmap shows that if we can develop a carrier selective n-TOPCon to replace the n^+ BSF on the rear side and succeed in lowering the metallized J_0 of the PERT cell from 123 fA/cm^2 to 5 fA/cm^2 (Table 5), we can raise the cell efficiency to 22.3%. This is a challenging but achievable task because in a TOPCon structure (Chapter 3) both diffused and metallized regions are displaced outside the absorber to reduce or eliminate minority carrier recombination in these regions. In addition to lowering rear side J_0, modeling shows that we also need to tailor the thickness and doping of the rear poly to achieve contact resistivity of ~ 2 mΩ-cm^2 and good FF.

The fourth bar in the technology roadmap in Figure 31 shows that we need to improve our screen-printing technology to reduce the front grid line width from 55 to ~40 μm, busbar width from 900 to 600 μm and incorporate floating busbars to reduce shading and metal-Si contact on the front side. These screen-printing enhancements will raise the efficiency to 22.8% (Table 5). Since anytime we change sheet resistance or screen-printing parameters on front and back, we have to re-optimize the grid design (number of grid lines, grid spacing and busbars) to maintain low contact and series resistance. This is done with the help of our in-house grid model, which was developed in this research and will be discussed in the next section.

The fifth bar shows the importance of bulk lifetime because once the metallized J_{0e} and $J_{0b'}$ become very small, bulk J_{0b} starts to play a major role in limiting the cell efficiency. Modeling shows that at this point if we can increase bulk lifetime from 1.5 ms to 3 ms, the cell efficiency can climb to 23.2%.

Even though the objective of this research was to get to ~23% efficiency using a homogeneous B emitter, the last bar in the roadmap shows that implementation of a p^+/p^{++} selective emitter (170/30 Ω/□) with metallized J_{0e} of < 25 fA/cm^2 and contact resistivity of ~1 mΩ-cm^2, instead of 30 fA/cm^2 and ~3 mΩ-cm^2 for the homogeneous emitter, can raise the cell efficiency further to 23.5%. Experimental development of selective emitter was not part of this thesis.

4.3 Modelling and Understanding the Impact of Bulk Lifetime and Resistivity on the Efficiency of Proposed TOPCon Cell Design

Selection of bulk material is crucial for achieving high efficiency cells. To understand and highlight the importance of bulk resistivity and lifetime, model calculations were performed to first quantify the impact of bulk lifetime alone and then investigate the combined effect of lifetime and resistivity on the efficiency of proposed TOPCon cell design (Figure 32 and Figure 33). Figure 32 shows that, with a higher than 2 ms SRH lifetime, our n-TOPCon cell design can achieve > 23% efficiency with a homogeneous B emitter on the front. In our roadmap, we used 1.5 ms lifetime because that is what we got in our PERT cell using the starting Cz material we had. However, SRH lifetimes greater than 20 ms in n-type Cz wafers have been achieved and reported [85, 86] in the literature. In particular, SunPower has demonstrated ~17 ms lifetime on their champion 25% IBC cell [87]. Modeling in Figure 32 shows that availability of 20 ms lifetime can raise the cell efficiency of our TOPCon cell design to greater than 23.5%.

Besides lifetime, bulk resistivity also plays an important role in determining the efficiency and there is a synergistic effect of the two on efficiency. Therefore, we extended model calculations to generate an efficiency contour map as a function of bulk resistivity and SRH lifetime in Figure 33. The white dashed line shows the optimum bulk resistivity that results in maximum efficiency for a given each SRH lifetime. Note that optimum resistivity increases with increasing SRH lifetime initially due to reduced Auger contribution to lifetime in the resistivity range of 0.1 to 1 Ω-cm without appreciable compromise in conductivity or R_S. However, when $\tau_{n0} = \tau_{p0} > \sim 4\, ms$, the optimum resistivity switches to > 20 Ω-cm bulk resistivity because material goes into high level injection so initial resistivity does not limit the bulk conductivity. Also notice that relative benefit of lifetime on efficiency after 5 ms diminishes because diffusion length becomes

long enough to influence further carrier collection. On the other hand, Figure 33 shows that 23% TOPCon cell efficiency cannot be achieved if the bulk lifetime is below 1 ms, regardless of bulk resistivity.

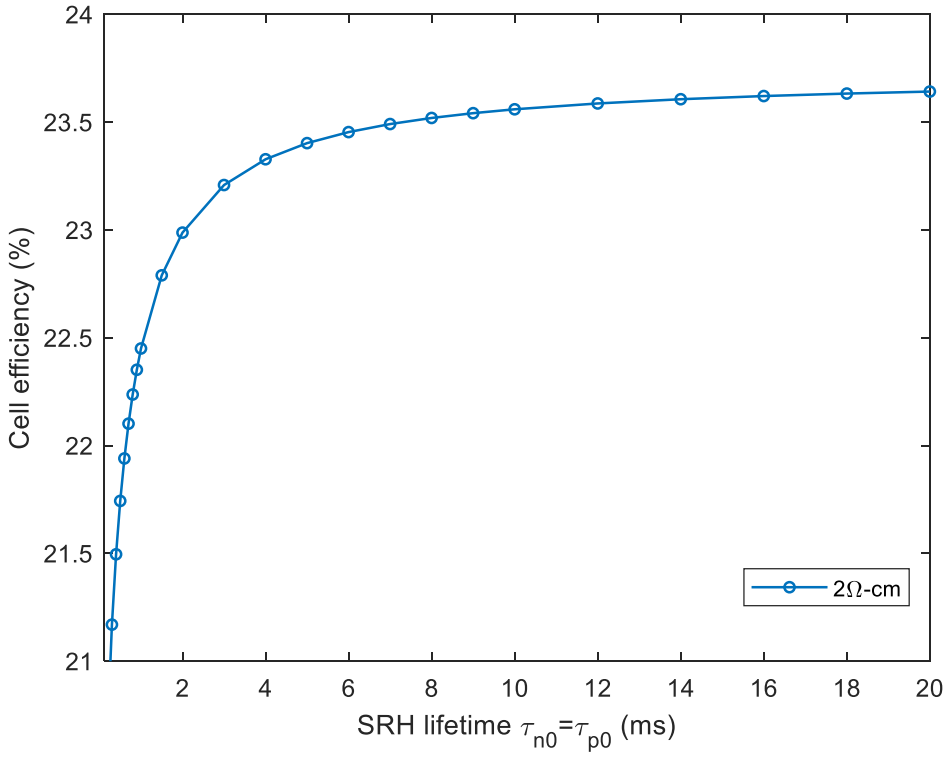


Figure 32: Efficiency vs mid-gap SRH lifetime of n-TOPCon cells with advanced metallization (bar 4 in Figure 31). It shows that 23% efficiency can be achieved with 2 ms lifetime without a selective emitter, and 23.2% efficiency can be achieved with 3 ms lifetime.

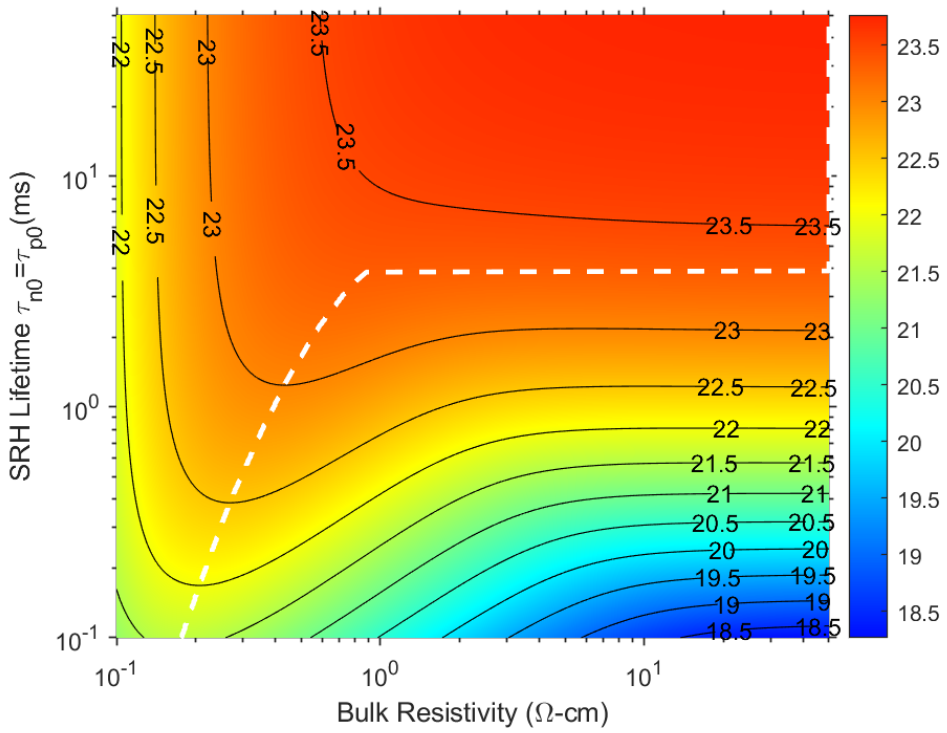


Figure 33: Efficiency contour map of n-TOPCon cells with advanced metallization (bar 4 in Figure 31) as a function of bulk resistivity and mid-gap SRH lifetimes. The white dashed line corresponds to the optimum bulk resistivity that results in maximum efficiency at each SRH lifetime.

4.4 Modeling The Impact of Metallized J_{0e} and $J_{0b'}$ and Front and Back Contact Resistivity on TOPCon Cell Efficiency

Both low metallized J_0 and contact resistivity are important for high efficiency because J_0 affects V_{OC} and contact resistivity influences FF. To understand the effect of metallized front emitter ($J_{0e,total}$) and the rear n-TOPCon ($J_{0b',total}$) on the n-TOPCon cell, efficiency sensitivity curves were plotted in Figure 34 and Figure 35, respectively. Modeling revealed that an increase of 5 fA/cm^2 on J_{0e} or $J_{0b'}$ for our proposed cell design would cause ~0.1%$_{abs}$ decrease in cell efficiency.

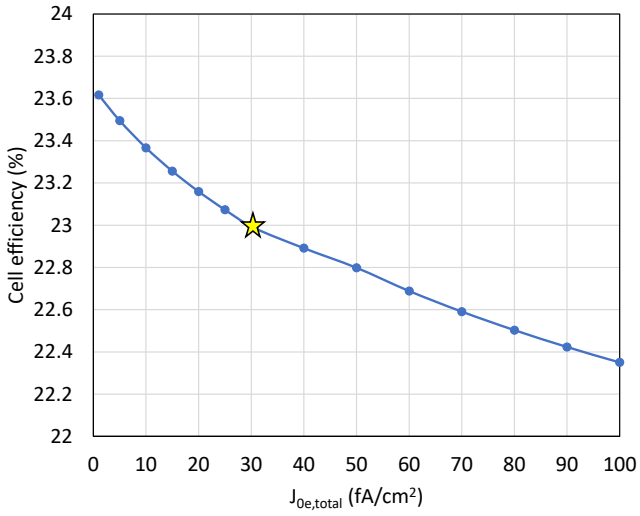


Figure 34: Quokka 2 simulated cell efficiency as a function of $J_{0e,total}$, assuming 2 ms bulk lifetime (column 5 in Table 5). The star shows the metallized J_{0e} of our 23% cell design.

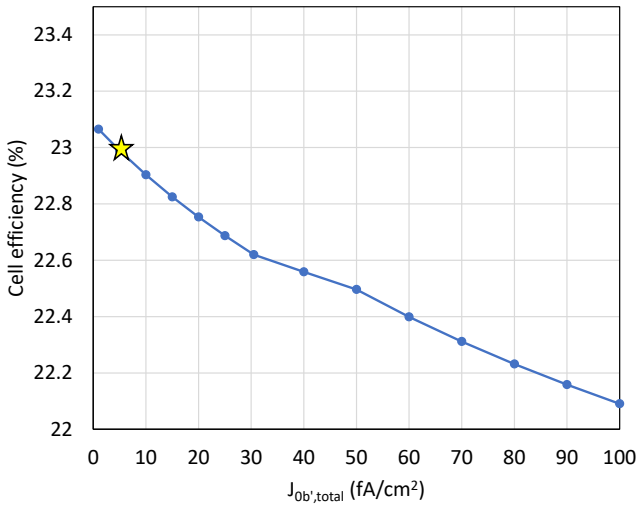


Figure 35: Quokka 2 simulated cell efficiency as a function of $J_{0b',total}$ of the proposed 23% n-TOPCon cell (column 5 in Table 5). The star shows the metallized $J_{0b'}$ of our 23% cell design.

The effect of front and rear contact resistivities on cell efficiency are also examined in Quokka 2 device simulations by varying the contact resistivity only. The cell efficiency as a function of front and rear contact resistivities are plotted in Figure 36. Modeling shows that every 2 mΩ-cm^2 increase in contact resistivity on the front side decreases cell efficiency by 0.1%$_{abs}$. However, on the rear side it causes only 0.02%$_{abs}$ less in efficiency. This is because there is no trade-off due to light shading on the rear side which allows 5 times more metal coverage on the rear side to reduce the sensitivity to contact resistance. The optimization of grid design and gridline metal coverage is discussed in the next section.

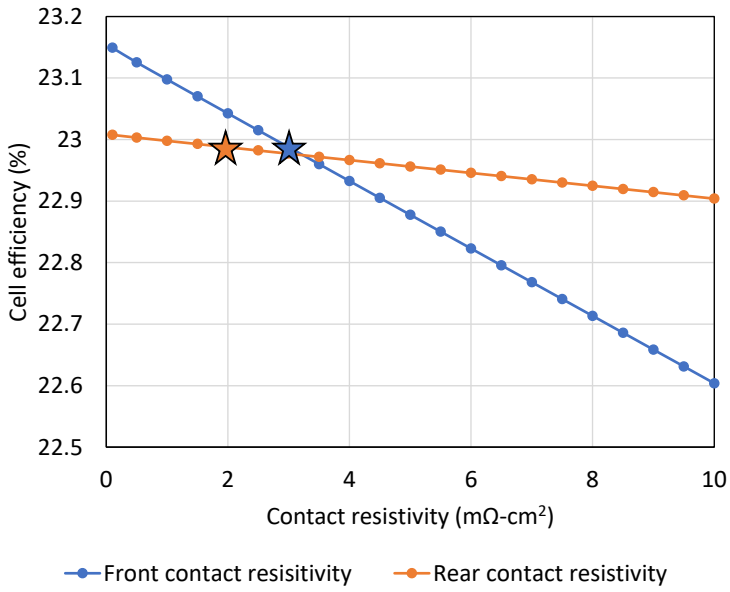


Figure 36: Quokka 2 simulated cell efficiency as a function of front and rear contact resistivities of the proposed 23% n-TOPCon cell (column 5 in Table 5). The stars show the contact resistivity of our 23% cell design.

4.5 Development of a Grid Design Model and Calculator for Optimizing Front and Rear Contact Grid Designs for Bifacial TOPCon Solar Cells

Grid pattern consists of large number of grid lines (100-130) and few (5-10) busbars. Grid lines collect the carriers generated in base after their separation and lateral transport through the doped regions between the grid lines. Carriers collected by the grid lines are then feed into the busbars which transport them into the external circuit for power generation (Figure 37). Thus, grid design must account for bulk resistance, sheet resistance in between grid lines, contact resistance, grid resistance and busbar resistance to calculate the total series resistance. Since higher resistance degrades FF and more grid lines increase shading and metal induced recombination or J_0, the grid design optimization involves not only minimization of series resistance but account for shading and metal-induced recombination losses to minimize the total loss. Figure 38 shows that more gridlines generally reduce the series resistance but increase shading or J_{SC} and $J_{0,metal}$ Therefore, designing an optimum grid pattern is critical to optimize the cell efficiency.

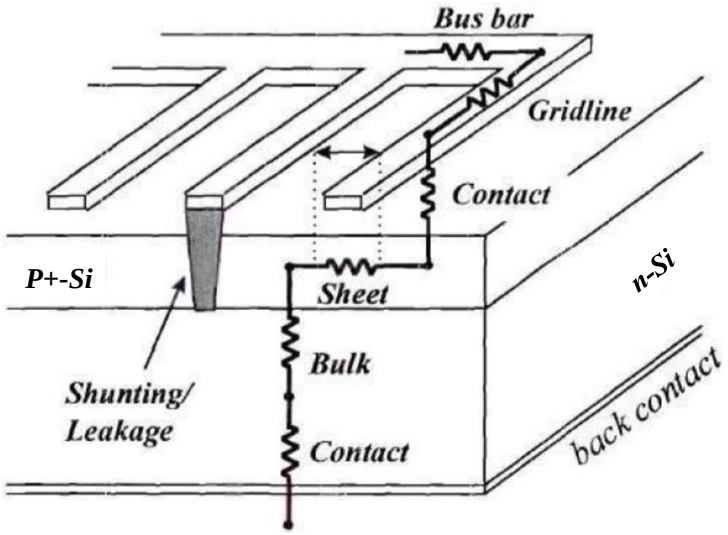


Figure 37: Resistive components in a solar cell.

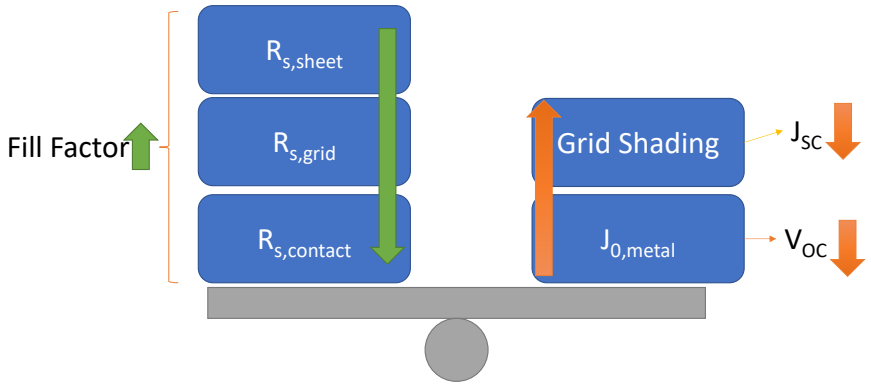


Figure 38: The trade-off of the grid line design. The arrows in the figure show the trend when the grid metal coverage increases on the front side.

Several commercial and noncommercial grid design models, like PV Lighthouse [88], only consider series resistance and optical shading without considering the metal-induced recombination, which becomes very important as you go toward very high efficiency cells. Device simulators like Sentaurus and Quokka 2 are possible candidates for optimizing the grid design. However, these simulators are very limited and complicated for grid optimization, since the size of the unit cell is defined by the least common multiplier (LCM) of the front and rear grid spacing, and the size of the unit cell need to be small to have a reasonably low computation time in Sentaurus and Quokka. Therefore, an optimum grid design calculator was developed in this task for front and rear contact bifacial solar cells accounting for metal induced recombination in fabricated cells in this research.

4.5.1 Series Resistance Calculation

For the calculation of individual components of series resistance in silicon solar cells, Meier's methodology [89] is adapted in our model based on experimentally measured parameters from fabricated cells. Figure 39 shows a schematic diagram of a cell with a five-busbar pattern used in this study. In this example, an n-TOPCon cell is modeled and analyzed with 40 μm wide gird fingers on top of 180 Ω/□ B emitter on the front side, and 60 μm wide grid finger on top of 64 Ω/□ n-TOPCon on the rear side. Four-point measurements are used to prevent measurement errors coming from the resistance of probes. The measurement methods are shown in Figure 40 and described in details in Meier's paper [89].

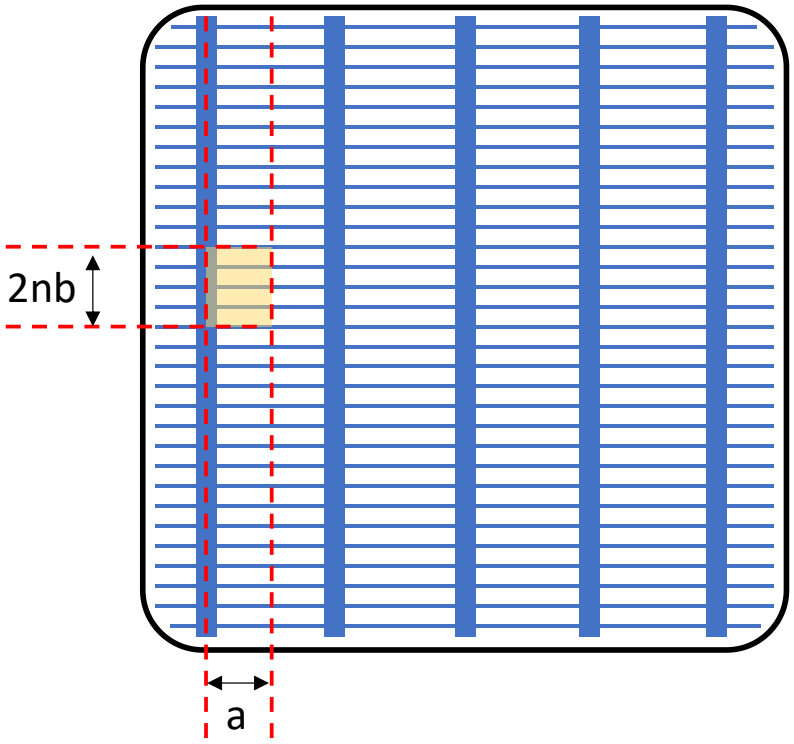


Figure 39: Schematic diagram of a solar cell with five busbars grid pattern. The yellow-colored region represents the unit cell of the series resistance analysis.

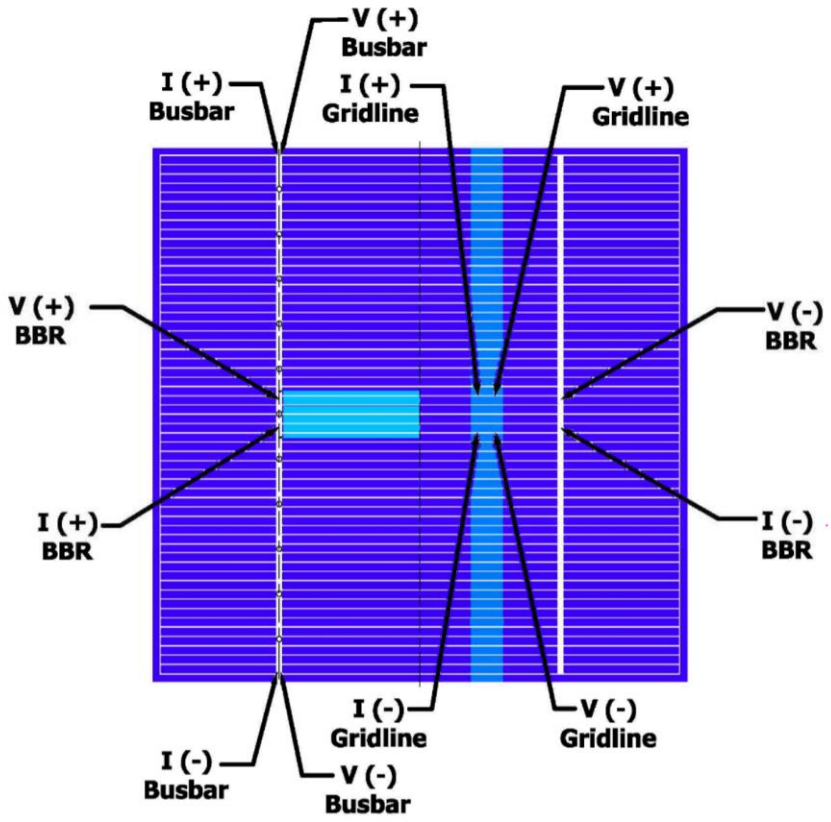


Figure 40: Schematic diagram showing placement of probes in a four-point measurement for determining series resistance components associated with gridline (busbar-to-busbar resistance, BBR), busbar (Busbar), and emitter sheet resistance (Gridline) (adapted from [89]).

The metal-Si contact resistivity (ρ_C) is determined by transfer length method (TLM) [90, 91], using more than three contacts with varying spacing, as shown in Figure 41. The measured total resistance between two contacts (R_T) is:

$$R_T = 2R_{metal} + 2R_C + R_{Si} \quad \textbf{(39)}$$

Where R_m is the resistance due to contact metal, R_C is the contact resistance at metal/Si interface, and R_{Si} is the silicon resistance between the two contacts. In most cases, the

resistivity of metal is extremely low that $R_{metal} \ll R_C$, so R_{metal} can be ignored. The Si resistance between two contact is:

$$R_{Si} = R_{sheet}\frac{d}{Z} \tag{40}$$

where R_{sheet} is the sheet resistance of the silicon, d is the distance between contacts, and Z is the width of the metal contact, as shown in Figure 41. From Eq. (39) and (40), the total resistance between two contacts can be calculated as:

$$R_T = R_{sheet}\frac{d}{Z} + 2R_C \tag{41}$$

By measuring R_T of different distances (d), the total resistance (R_T) as a function of distances (d) can be plotted, as shown in Figure 41. According to Eq. (41), the intercept of the plot at d=0 is just twice the contact resistance. The sheet resistance R_{sheet} can also be found from the slope of the line. The intercept at R_T=0 gives $-d = 2L_T$, where L_T is the transfer length. The transfer length L_T is defined as:

$$L_T = \sqrt{\frac{\rho_c}{R_{sheet}}} \tag{42}$$

which can be thought as the distance over which most of the current transfers from the semiconductor in to the metal or from the metal into the semiconductor.

For a grid width of L, the contact resistance can be expressed as [91]:

$$R_C = \frac{\rho_c}{L_T Z} \coth\left(L/L_T\right) \tag{43}$$

For $L \leq 0.5\, L_T$, which means the effective contact area is the actual contact area ($L \times Z$), and is the most cases of solar cells with good contacts, the Eq. (43) can be simplified to:

$$R_C \approx \frac{\rho_c}{L\, Z} \tag{44}$$

the contact resistivity (ρ_C) can be obtained as:

$$\rho_C \approx R_C\, L\, Z \tag{45}$$

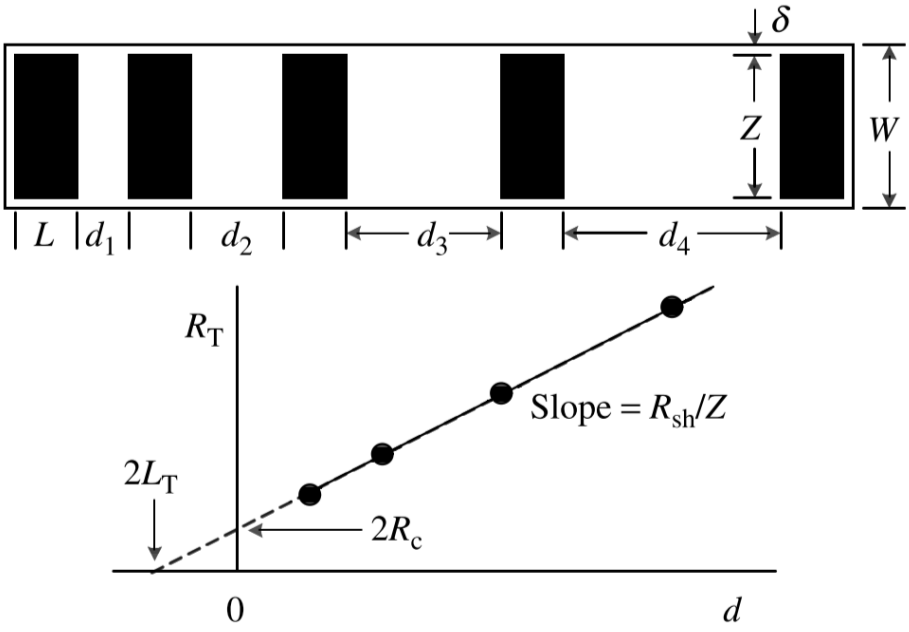


Figure 41: A transfer length method test structure and a plot of total resistance as a function of contact spacing, d. Z is the length of the metal contact, and W is the width of the test sample. The δ = W-Z should be as small as possible.

Table 6 shows the experimentally measured and calculated parameters for the n-TOPCon cell, and Table 7 shows the equations used to calculate various resistive components that contribute to series resistance.

Table 6: Experimentally measured parameters (yellow-shaded) and calculated parameters (green-shaded) for the analyzed n-TOPCon cell.

	Item	Symbol	Value	Unit
Geom - Cell	Cell side length	l	15.6	cm
	Cell thickness	t_w	180	μm
	Cell resistivity	ρ	2	Ω-cm
Geom - Front grid	Front Lines	$n_{gl,front}$	100	
	Front Line width		40	μm
	Front grid - Half spacing	b_{front}	0.074	cm
	Front grid metal shading / contact %		2.72%	
	Front Busbar Numbers		5	#
	Front Busbar Width		600	μm
	Front Floating busbar	1 yes/ 0 no	1	
	Front busbar shading %		1.92%	
	Front busbar contact %		0.00%	
	Unit cell width (pick-up probe spacing)	2nb	1	cm
	Front finger length	a	1.56	cm
	How many fingers per unit cell width	n_{front}		
Geom - Back grid	Back Lines	$n_{gl,back}$	300	
	Back Line width		60	μm
	Back grid -Half spacing	b_{back}	0.026	cm
	Back grid metal shading / contact %		11.54%	
	Back Busbar Numbers		5	#
	Back Busbar Width		600	μm
	Back Floating busbar	1 yes/ 0 no	0	
	Back busbar contact %		1.92%	
	Back finger length	a	1.56	cm
Front sheet	Front sheet resistance		180	Ω/□
Front Busbar	Length when measure busbar resistance	$R_{bus,length}$	9	cm
	Front Busbar resistance	R_{bus}	0.272	Ω
	$\rho_f/(tw') = 2*Rbus/l$	$2*R_{bus}/l$	0.060	Ω/cm

Table 6 (continued)

Front gridline	Front Busbar to busbar resistance	$BBR_{front,measure}$	0.05	Ω
	Front Lines when measure BBR front	$n_{gl(BBRfront,measure)}$	106	
	Front finger length when measure BBR front	$a_{(BBRfront,measure)}$	1.56	cm
	$\rho_f/(tw) = (ngl/2a)*BBR$		1.699	Ω/cm
Front contact	Front contact %	f_{fm}	2.72%	
	Front contact resistivity	$\rho_{C,front}$	3	mΩ-cm^2
Back sheet	Back sheet resistance		64	Ω/□
Back gridline	Back busbar to busbar resistance	$BBR_{back,measure}$	0.05	Ω
	Back Lines when measure BBR front	$n_{gl(BBRfront,measure)}$	100	
	Back finger length when measure BBR front	$a_{(BBRback,measure)}$	1.56	cm
	Full metal on back (neglect $R_{s, back}$)	1 yes/ 0 no	0	
Back Contact	Back contact %	f_{bm}	13.46%	
	Back contact resistivity	$\rho_{C,front}$	2	mΩ-cm^2
J_0	$J_{0e,pass, 100\%}$		12	fA/cm^2
	$J_{0e,metal, 100\%}$		706	fA/cm^2
	J_{0bulk}		22	fA/cm^2
	$J_{0b', pass, 100\%}$		1	fA/cm^2
	$J_{0b', metal, 100\%}$		30	fA/cm^2

4.5.2 Determination of J_{SC}, $V_{OC,}$ and Efficiency as a Function of Front and Rear Grid Design Using the Grid Model

As the front metal coverage decreases, the short-circuit current J_{SC} increases due to reduced shading of light, V_{OC} increases due to reduced metal-induced recombination or metal-Si contact area, and fill factor FF decreases due to increased series resistance (Figure 38). Therefore, an optimum grid design is needed to maximize cell efficiency.

Table 7: Analytical expression and calculated values of series resistance components for the n-TOPCon cells.

R_S component	Expression	Value [Ω-cm^2]
R_S (front busbar)	$\frac{1}{3} a\, n^2\, b^2 (\frac{2R_{bus}}{l})$	0.008
R_S (front gridline)	$\frac{1}{3} a\, b\, n_{gl}\, (BBR_{front})$	0.215
R_S (front contact)	$\frac{\rho_{C,front}}{f_{fm}}$	0.117
R_S (front sheet)	$\frac{1}{3} b^2 R_{sheet,front}$	0.365
R_S (substrate)	$\rho\, t_w$	0.036
R_S (back sheet)	$\frac{1}{3} b^2 R_{sheet,front}$	0.009
R_S (back contact)	$\frac{\rho_{C,back}}{f_{bm}}$	0.015
R_S (back gridline)	$\frac{1}{3} a\, b\, n_{gl}\, (BBR_{back})$	0.056
Total R_S		**0.821**

Our model assumes 100% of light under the front metal contact is optically shaded and then calculates the unmetallized J_{SC} ($J_{SC,no\_shading}$) of the cell from the measured metallized J_{SC0} and the metal coverage (f_{fm0}) of the refence or fabricated cell of the same structure:

$$J_{SC,n0\_shading} = \frac{J_{SC0}}{1-f_{fm0}} \quad \textbf{(46)}$$

and the J_{SC} as a function of front metal coverage (f_{fm}) is calculated as:

$$J_{SC} = J_{SC0} \times (1 - f_{fm}) \quad \textbf{(47)}$$

Figure 42 shows an example of the contour map of J_{SC} generated by our grid calculator with the parameters defined in Table 6, with varying number of front and rear grid lines. It shows ~0.11 mA/cm^2 J_{SC} decrease with the increase of every 10 grid lines on the front side, with no impact from the number of grid lines on the back since the light is shaded only by the front metal grid.

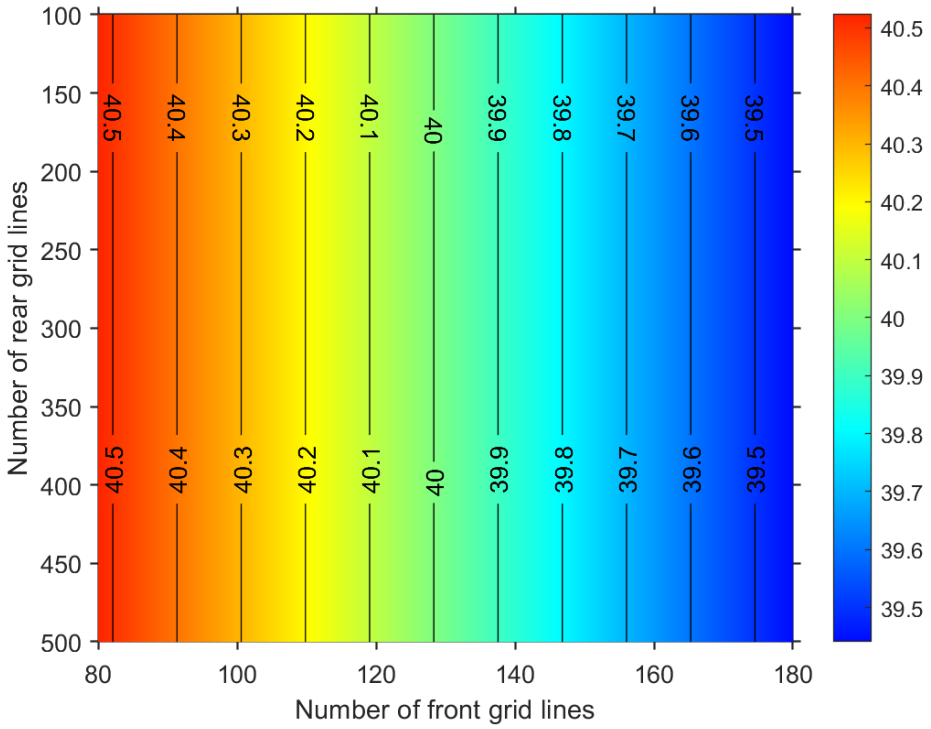


Figure 42: Short-circuit current (J_{SC}, in mA/cm^2) contour as a function of number of front grid lines (x-axis) and rear grid lines (y-axis).

To determine the open-circuit voltage (V_{OC}), model first calculates the total recombination current density J_0 by adding the area-weighted J_0 on the front and back side, as well as in the silicon bulk:

$$J_0 = f_{fm} \times J_{0e,metal} + (1 - f_{fm}) \times J_{0e,field} + f_{bm} \times J_{0b',metal} + (1 - f_{bm}) \times J_{0b',field} + J_{0,bulk} \quad \textbf{(48)}$$

where the J_{0e} and $J_{0b'}$ components are experimentally measured from photoconductance decay measurement on symmetric test structures [20], and the front and back metal coverage (f_{fm} and f_{bm}) are calculated by the number and width of gridlines. $J_{0,bulk}$ is obtained from the reference cell with known total J_0 and other four J_0 components [4]. Next, the open-circuit voltage is calculated as a function of metal coverage from the J_0 and J_{SC} values calculated from Equations (47) and (48):

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_0} + 1\right) \quad \textbf{(49)}$$

Figure 43 shows the contour map of V_{OC} as a function of number of front and rear grid lines using our grid calculator with the parameters defined in Table 6. These calculations show that for our n-TOPCon cell structure V_{OC} drops by ~0.9mV with the increase in every 10 grid lines on the front side, while V_{OC} drops only ~0.05 mV for every 10 grid lines on the rear side. The much lower V_{OC} loss on the rear n-TOPCon side supports the excellent passivation quality of our n-TOPCon compared to the B emitter, and allows more metal coverage on the rear side to reduce series resistance without compromising J_0 and cell efficiency.

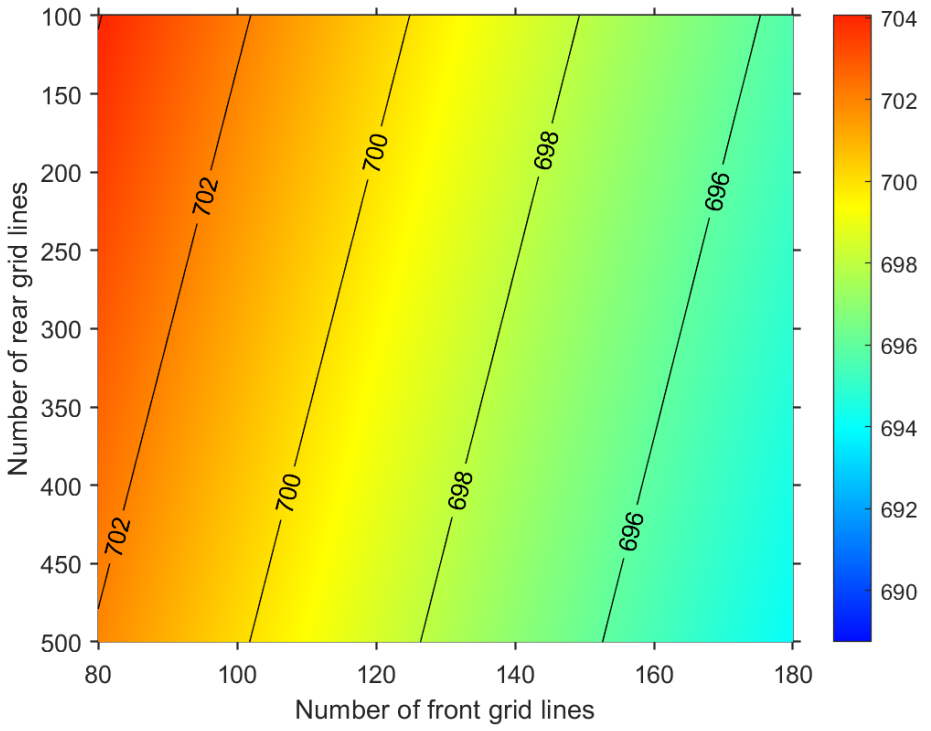


Figure 43: Open-circuit voltage (V_{OC}, in mV) contour as a function of number of front grid lines (x-axis) and rear grid lines (y-axis).

4.5.3 Determination of FF as a Function of Front and Rear Grid Design Using the Grid Model

To assess the impact of grid lines on both sides on FF, the model first calculates the total series resistance from the equations in Table 7, and then calculates FF using the following set of equations and the methodology proposed by Green [92]:

$$v_{oc} = \frac{qV_{oc}}{nkT} \quad \textbf{(50)}$$

$$FF_0 = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \quad \textbf{(51)}$$

$$R_{CH} = \frac{V_{oc}}{J_{sc}}, r_s = \frac{R_s}{R_{CH}}, \text{ and } r_{sh} = \frac{R_{sh}}{R_{CH}} \quad \textbf{(52)}$$

$$FF_s = FF_0(1 - r_s) \quad \textbf{(53)}$$

$$FF = FF_S\left(1 - \frac{(v_{oc} + 0.7)FF_s}{v_{oc}r_{sh}}\right) \quad \textbf{(54)}$$

Figure 44 shows the contour map of FF as a function of front and back grid lines using the parameters defined in Table 6. As expected, FF increases with the increase in front and back grid lines because of decrease in R_S. Since both V_{OC} and J_{SC} decrease with increase in number of grid lines, the optimum grid design is dictated by efficiency or the trade-off between FF, V_{OC} and J_{SC}.

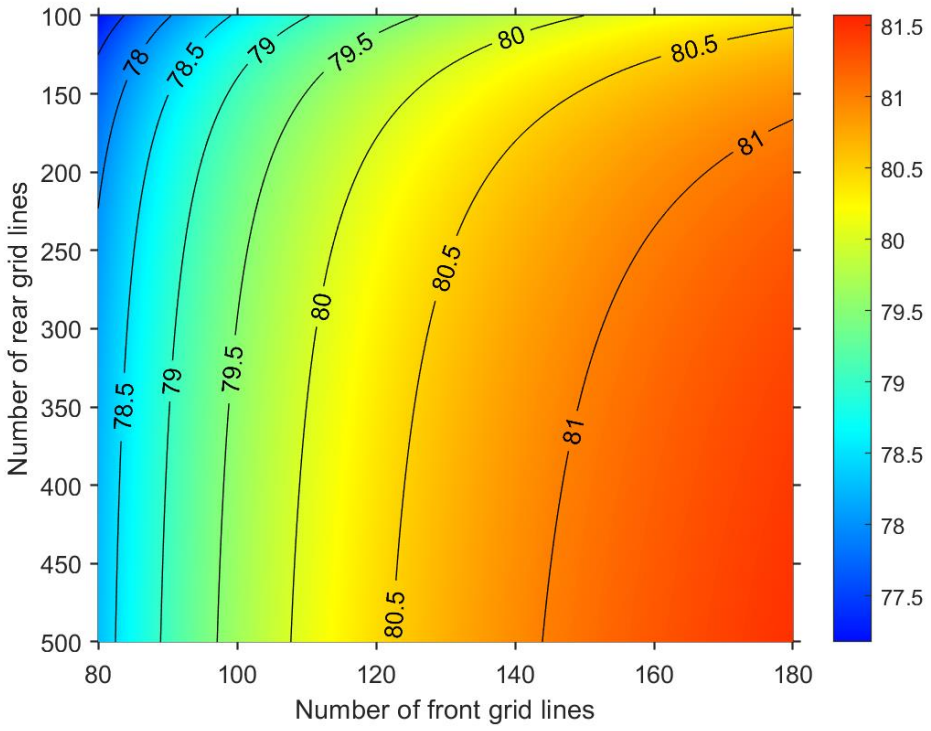


Figure 44: Fill factor (FF, in %) contour as a function of number of front grid lines (x-axis) and rear grid lines (y-axis).

From the calculated values of J_{SC}, V_{OC} and FF as a function of metal coverage, our grid model then calculates the cell efficiency η by:

$$\eta = \frac{V_{OC}\, J_{SC}\, FF}{P_{in}} \tag{55}$$

where P_{in} is the input power density, which is 1000 W/m^2 under 1 sun with the global AM1.5 spectrum [93].

Figure 45 shows a contour map of the cell efficiency generated from the grid model for our n-TOPCon cell design as a function of grid design or the number of front and rear

grid lines. It shows that the optimum number of grid lines for the highest cell efficiency is in the range of 105 - 135 for the front side, and 250 - 800 for the rear side. Since there is no optical shading on the rear side and the metal-induced recombination in the n-TOPCon is extremely low, the optimum number of rear grid lines can be much higher than the front side. Therefore, based our grid modelling and understanding, we chose to screen print 300 grid lines on the rear n-TOPCon and 105-120 lines on the 170 Ω/□ B emitter on the front side. Note that if we want to change the emitter sheet resistance or any other grid parameter in Table 6, grid model can rapidly generate the new efficiency contour plot to optimize the grid design.

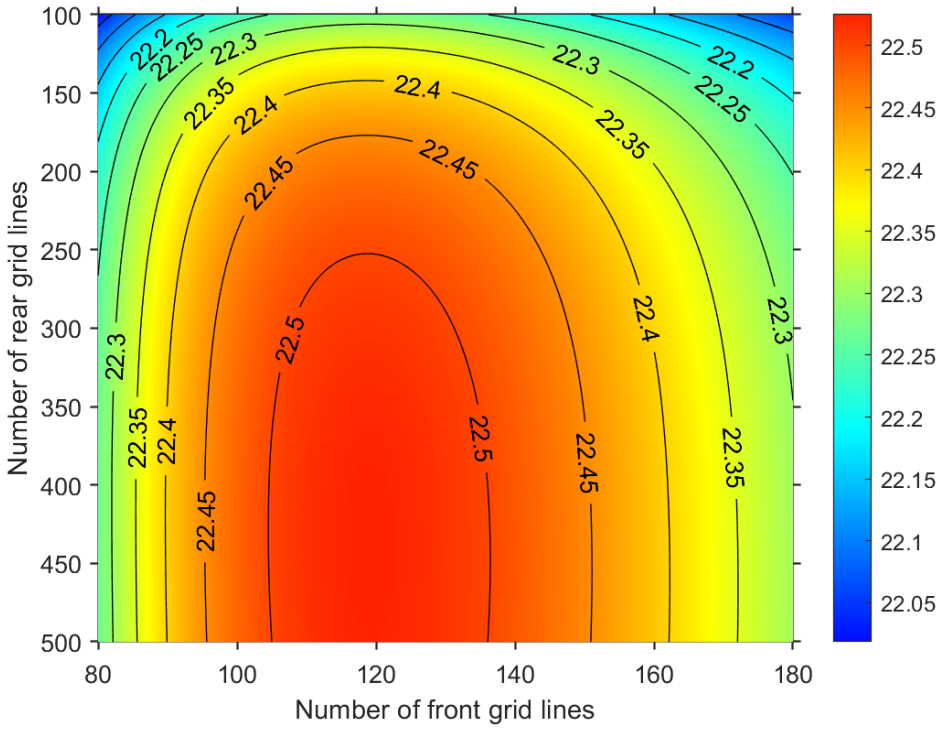


Figure 45: Cell efficiency (in %) contour as a function of number of front grid lines (x-axis) and rear grid lines (y-axis).

For example, Table 8 shows several different B emitters fabricated in this study with known values of $J_{0e,pass}$, $J_{0e,metal}$ and contact resistivity. Figure 46 shows the calculated cell efficiencies from the grid model for different B emitter parameters listed in Table 8. It shows that we can use 105-120 grid lines on the front without an appreciable loss in efficiency (< $0.03\%_{abs}$) for all B emitters with sheet resistance in the range of 60-180 Ω/□. Therefore, we selected 106 lines for the front grid design in this study (Figure 46).

Table 8: J_0 values and contact resistance estimation for different B emitters based on literature and initial measurements.

B Emitter Sheet Resistance (Ω/□)	$J_{0e,pass}$ [fA/cm^2]	$J_{0e,metal}$ [fA/cm^2]	Contact resistance [mΩ-cm^2]
30	90	164	0.5
60	70	271	1
90	50	378	1.5
120	30	485	2
150	20	593	2.5
180	12	700	3

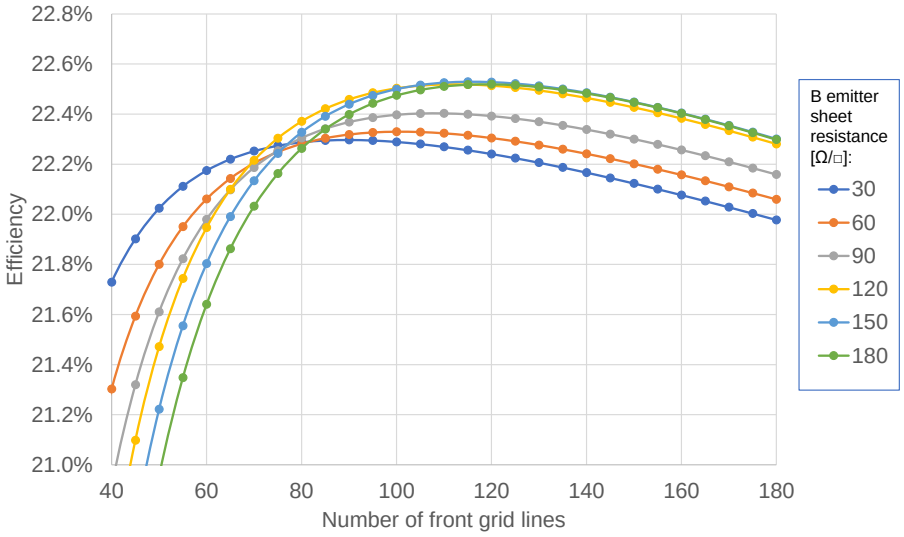


Figure 46: Simulated cell efficiency from grid calculator as a function of numbers of front fingers for various B emitters fabricated in this research.

4.5.4 Validation of the Grid Calculator Results with Advanced Quokka 2 Device Model

To validate the output of our grid calculator developed in this research, the advanced Quokka 2 device model [79, 94] was used selectively to compare the cell parameters. Note that in Quokka 2 and other device simulators like Sentaurus, the front and rear spacing needs to have a reasonably small least common multiple (LCM) number, therefore, useful contour maps like Figure 42-45 as a function of front and rear numbers of gridlines are very difficult to produce. In Quokka 2, we selected 6 different front/rear line configurations, with the same J_0 and R_S component parameters (Table 6, Table 7). $J_{generation} = 42.27\, mA/cm^2$ was used in Quokka for J_{SC} correction, and $J_{SC,without\ shading} = 42.20\, mA/cm^2$ was used in our grid model to align the J_{SC} for the first condition (front 100 lines and rear 300 lines). The small $0.07\, mA/cm^2$ difference

comes from the recombination loss in the output current, which our simple grid calculator does not account for. A bulk lifetime = 1.4 ms is used in Quokka for all cases which corresponds to $J_{0,bulk}$ = 22fA/cm^2 in grid calculator. Rest of the parameters are identical in both models.

Table 9 shows that our grid model calculator provides almost the same J_{SC} as Quokka 2 for all 6 cases. There is less than 1 mV deviation in V_{OC}, and less than 0.2%$_{abs}$ (1%$_{relative}$) deviation in cell efficiency values, demonstrating reasonably high accuracy of our simple and rapid gird calculator. Some small deviations in series resistance and FF values are probably due to slight deviations in resistivity under illumination.

Table 9: Comparison of the Grid model and Quokka simulation results.

# of Front lines	# of Rear Lines	Simulator	Eff. (%)	ΔEff	Voc (mV)	ΔVoc	Jsc (mA/cm^2)	ΔJsc	FF (%)	ΔFF	Rs (Ω-cm^2)	ΔRs
100	300	Grid model	22.47	+0.12	701.1	-0.30	40.31	0.00	79.5	+0.40	0.821	+0.025
		Quokka	22.35		701.4		40.31		79.1		0.796	
200	300	Grid model	22.17	+0.03	693.4	-0.90	39.22	-0.01	81.5	+0.20	0.381	+0.001
		Quokka	22.14		694.3		39.23		81.3		0.38	
75	300	Grid model	22.16	+0.17	703.4	+0.40	40.58	0.00	77.6	+0.50	1.216	+0.056
		Quokka	21.99		703		40.58		77.1		1.16	
120	600	Grid model	22.52	+0.08	698.1	-0.40	40.09	0.00	80.5	+0.40	0.612	+0.013
		Quokka	22.44		698.5		40.09		80.1		0.599	
100	100	Grid model	22.23	+0.15	702.2	+0.10	40.31	0.00	78.5	+0.50	1.027	+0.032
		Quokka	22.08		702.1		40.31		78.0		0.995	
175	350	Grid model	22.33	+0.05	695	-0.80	39.5	0.00	81.3	+0.20	0.421	+0.004
		Quokka	22.28		695.8		39.5		81.1		0.417	

4.6 Summary

In this task, we have set up the unit cells and methodology to implement the use of Sentaurus and Quokka 2 device models to establish a technology roadmap to 23% TOPCon

cells. The roadmap identifies and quantifies practically achievable material and device parameters and technology enhancements required to raise the efficiency of 21% n-PERT cell to 23% efficient n-TOPCon cell. Roadmap also outlines how to achieve proposed enhancements by technology developments in B emitter, n-TOPCon region, bulk lifetime, optical properties and contact parameters. In addition to specifying the required design modification for each layer, roadmap quantifies how much efficiency improvement is expected from each technology development. For example, it not only points that we need to reduce total J_0 from 304 to 50 fA/cm^2 to raise the efficiency from 21% to 23% but also shows that this can be achieved by reducing metallized J_{0e} from 150 to of 30 fA/cm^2 by developing 170 Ω/□ B emitter with 2.67% metal-Si contact area, replacing n^+-BSF with 120 fA/cm^2 J_{0b}, by a 5 fA/cm^2 rear n-TOPCon with 13% meal-Si contacts area, using ~2ms bulk lifetime n-type wafer, implementing two layer SiN/SiO_2 anti-reflection coating, and 40 μm wide 106 grid lines with five floating busbars on front. The importance of the right combination of bulk resistivity and lifetime is also investigated which shows that 23% efficiency cannot be reached with our TOPCon cell design if bulk lifetime is below 1 ms, regardless of resistivity. In addition, there is an optimum resistivity for each lifetime below 5 ms but above that lifetime material goes into high-level injection and higher resistivity (≥20 Ω-cm) becomes preferable.

Besides improving B emitter and TOPCon layers, it is also critical to minimize contact-grid-induced shading, resistance and recombination losses. To ensure the optimum front and back grid designs for bifacial n-TOPCon cells fabricated in this study, a simple grid model was developed and applied, which not only calculates the optical shading and series resistance losses but also accounts for metal-induced recombination loss to provide

the optimum front and back metal grid design for the highest possible cell efficiency. This model was validated with more advanced Quakka 2 model. It was found that for our proposed 120-170 Ω/□ homogeneous B emitters and 60 Ω/□ rear n-TOPCon, 100-120 gridlines on front and 300 gridlines on the rear side will be optimum in combination with 5 busbars.

CHAPTER 5. TASK 2: TECHNOLOGY DEVELOPMENT AND FORMATION OF OPTIMIZED ION-IMPLANTED BORON EMITTER WITH METALLIZED J_{0E} OF 30 FA/CM^2

Technology roadmap in Task 1 established the metallized J_{0e} target of ~30 fA/cm^2 for B emitter in order to achieve 23% efficiency. It is well known that metal-induced recombination can be reduced by forming selective B emitter (p^{++}/p^{+}) where highly-doped areas beneath the metal contacts reduce $J_{0e,metal}$ while passivated regions between the gridlines provide lower $J_{0e,pass}$ due to lower doping, better surface passivation, reduced Auger recombination and bandgap narrowing. However, formation of selective B emitter adds extra steps, cost and process complexity [95] that may negate the benefit of efficiency enhancement for industrial solar cells. An attractive low-cost alternative to achieving lower metallized emitter recombination current density (J_{0e}) involves optimizing homogeneous B emitter profile with excellent surface passivation in combination with the reduced metal-Si contact area and optimized screen-printing paste and firing scheme to reduce both $J_{0e,pass}$ and $J_{0e,metal}$ without appreciably compromising contact resistivity (ρ_C) and fill factor (FF). This provided the motivation in this task to develop B doped homogeneous emitters contacted by advanced screen-printing to achieve metallized J_{0e} comparable to selective B emitters.

This task investigates the effect of doping profile and sheet resistance of ion-implanted homogeneous B emitter on the J_{0e} and efficiency of bifacial n-TOPCon cells by a combination of ion-implanted doping profile simulations and device modeling, technology development, complete cell fabrication and characterization. It is well known

that the screen-printed Ag/Al contacts to B emitters can be made with much lower surface concentration ($<2\times10^{19}$ cm^{-3}) compared to the screen-printed Ag contacts to phosphorus (P) doped n-type emitters ($\sim1\times10^{20}$ cm^{-3}) due to the work function difference. This provides an opportunity to lower unmetallized $J_{0e,pass}$ by reducing B doping without sacrificing contact quality. However, reduced doping makes the metal-induced recombination much worse, because lightly doped emitters are more transparent and sensitive to surface recombination velocity.

Due to the above tradeoffs, it is challenging to tailor the doping profile of a homogeneous B emitter to achieve low J_{0e} values in the passivated as well as metallized regions simultaneously, while maintaining good ohmic contact and acceptable sheet resistance for high FF. This problem can be mitigated by driving the B emitter profile or junction deep to decouple the effect of the metallized surface regions, optimizing screen-printed contacts and firing to lower $J_{0e,metal}$, and reducing the direct metal-Si contact area. In this study, we have employed ion implantation to form B emitters because, besides time and temperature, it provides additional controls like implantation energy and dose for profile engineering and management. Ion implantation also provides opportunities for higher cell efficiency because of better areal uniformity, more precise control of doping profile, and excellent chemical purity of the beam. Efficiency improvement and lower recombination current density with B and P implanted regions have been published by several groups [96-103] with screen-printed cell efficiencies approaching 21%.

In addition to profile optimization, we investigated different screen-printing metal pastes and firing schemes to minimize $J_{0e,metal}$ and quantify contact resistivity. Next, we used this information in Sentaurus 2D device simulations to quantify the tradeoffs between

J_0 contribution from metallized and unmetallized regions to design and select the optimum B emitter profile. Unlike the uniformly evaporated contacts where SRV is fixed at ~10^7 cm/s, screen-printed metal's $J_{0,metal}$ or SRV can be very different due to highly non-uniform contact interface with very different direct metal-Si contact fraction, metal paste etching, and thin glass layer in between. Therefore, a study was conducted to see if $J_{0e,metal}$ for a given emitter profile can be altered by the choice of screen-printing paste and firing conditions. Experimental values of full area $J_{0e,metal}$ were determined for different screen-printed fire-through metal pastes to demonstrate that $J_{0e,metal}$ can increase or decrease appreciably depending on the aggressiveness of the glass frit in the paste and its interaction with the emitter surface, as well as passivating dielectric underneath the grid. According to our technology roadmap in Task 1, the goal of this task is to achieve a total metallized J_{0e} of ~30 fA/cm^2 with a homogeneous B emitter for ~23% n-type cells with n-TOPCon rear contact.

5.1 Fabrication of Passivated and Metallized Ion-Implanted B Emitters and the Procedure for Determining Corresponding J_{0pass} and J_{0metal} Values

Several ion-implanted B emitters in the sheet resistance range of 48-200 Ω/□ were fabricated and characterized in terms of sheet resistance, doping profiles, specific contact resistivity, $J_{0e,pass}$ and $J_{0e,metal}$. To quantify the emitter recombination current density (J_{0e}), symmetric $p^+/n/p^+$ test structures were prepared by B implantation and annealing on both sides of 200 μm thick 20 Ω-cm 6-inch pseudo square high bulk lifetime n-type monocrystalline Czochralski (Cz) wafers. After saw damage etching and texturing followed by a standard RCA clean process, the wafers received B implantation at 10 keV with doses ranging from 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2} on both sides. All samples were

annealed at 1050 °C for 1 hour in N_2 ambient followed by an in-situ oxidation for 30 minutes in O_2 ambient to remove implanted damage, activate dopants and drive the junction deep. After etching the thermal oxide in a dilute HF solution, the sheet resistance of implanted B emitters (R_{sheet}) was measured by a four-point probe. After a standard RCA clean, ~100 Å thick aluminum oxide (Al_2O_3) layer was deposited for surface passivation by plasma-assisted atomic layer deposition (ALD) on both sides, followed by plasma-enhanced chemical vapor deposition (PECVD) of SiN_x/SiO_2 stack on top of the Al_2O_3 for emitter surface passivation as well as antireflection coating. Next, samples were subjected to a firing cycle without any printed metal paste to simulate the effect of screen-printed contact firing on the passivation quality of the unmetallized portion of the emitter. Finally, $J_{0e,pass}$ was measured under high-level injection using the photo-conductance decay (PCD) method proposed by Kane and Swanson [20] described in Chapter 2.

In order to quantify the recombination current density contribution due to metallized portion of the B emitter ($J_{0e,metal}$), 40 μm wide metal gridlines with varying pitch and metal fraction (f_{metal}) were screen-printed only on the rear side of the symmetric structure (Figure 47). Several different pastes were investigated, but only the two most pertinent ones (A and B) are reported to highlight the importance of paste chemistry on $J_{0e,metal}$. To evaluate the effect of pastes A and B on $J_{0e,metal}$, the two commercial Ag/Al pastes were applied only on one side of symmetric $p^+/n/p^+$ test samples (Figure 47) with 170 Ω/□ p^+ emitter implanted with 1.2×10^{15} cm^{-2} B dose on both sides. After firing, the Ag/Al bulk electrode was etched away in $HCl:H_2O_2:H_2O$ =1:1:1 solution, leaving only the thin glass layer on Si surface with embedded metal crystallites into the emitter. $J_{0e,metal}$ for the two pastes was then determined by fitting the measured total J_0 of etched samples as a

function of the f_{metal}. Since J_0 for the test structure in Figure 47 with metal contacts on one side can be expressed as:

$$Measured\ total\ J_0 = J_{0e,front,metal} \times f_{metal} + J_{0e,front,pass} \times (1 - f_{metal}) + J_{0e,rear,pass} \quad \textbf{(56)}$$

This reduces to a linear relationship between J_0 and metal fraction f with:

$$Slope\ of\ J_0\ vs\ f_{metal} = J_{0e,front,metal} - J_{0e,front,pass} = J_{0e,metal} - J_{0e,pass} \quad \textbf{(57)}$$

$$and\ Intercept = J_{0e,front,pass} + J_{0e,rear,pass} = 2 \times J_{0e,pass} \quad \textbf{(58)}$$

Therefore,

$$J_{0e,pass} = \frac{Intercept}{2} \quad \textbf{(59)}$$

$$J_{0e,metal} = Slope + J_{0e,pass} \quad \textbf{(60)}$$

Thus, both $J_{0e,metal}$ and $J_{0e,pass}$ can be obtained from the slope and intercept of the linear plot of measured total J_0 and metal fraction. In addition, the specific contact resistivity between screen-printed Ag/Al contact and the implanted B emitters for the two pastes was measured by transfer length method (TLM), as described in Chapter 4, using separate test samples prepared with unequally spaced screen-printed lines. Finally, the profile of the 170 Ω/□ emitter was measured by electrochemical capacitance-voltage measurement (ECV) to

match and validate the Sentaurus Process model used in this study to generate various implanted profiles.

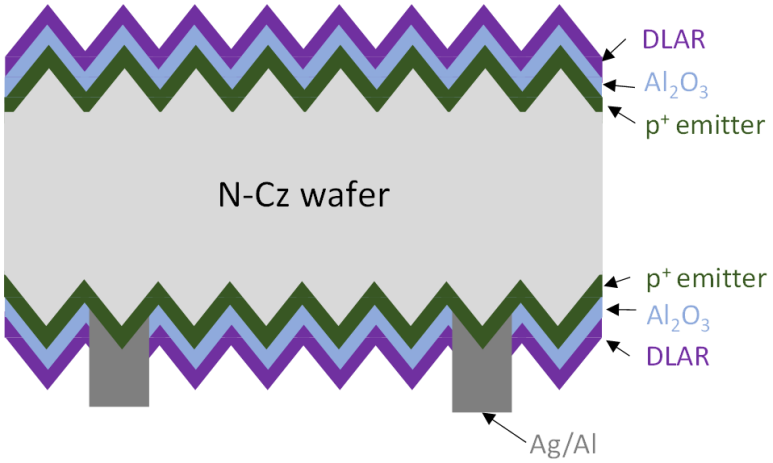


Figure 47: Schematic of symmetric $p^+/n/p^+$ test samples with implanted p^+ emitter on both sides and screen-printed Ag/Al paste on one side to investigate the impact of screen-printed metallization on J_0 and extract J_{0pass} and J_{0metal} components.

5.2 Characterization of Unmetallized Ion-implanted B Emitters as a Function of Implantation Dose

Figure 48 shows the sheet resistance (R_{sheet}) of the ion-implanted B emitters fabricated in this study as a function of B ion-implantation dose using 10 keV implantation energy and the above mentioned 1050 ℃ anneal. As expected, R_{sheet} decreases from 200 Ω/□ to 48 Ω/□, as the B implantation dose increases from 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2}. Figure 49 shows the measured $J_{0e,pass}$ for the ion-implanted textured B emitters fabricated in this study as a function of B emitter sheet resistance. The solid squares show our results, and the open symbols show literature data from [104-106] for comparison. Notice, very low $J_{0e,pass}$ < 15 fA/cm^2 were achieved for R_{sheet} > 140 Ω/□. Figure 50 shows the measured

contact resistivity as a function of B emitter sheet resistance. Contact resistivity of less than 5 mΩ-cm^2 was achieved for both pastes A and B for ≤ 170 Ω/□ implanted emitters with surface concentration of 6 × 10^{18}/cm^3, which is acceptable for high-efficiency cells from the viewpoint of contact and sheet resistance. The next step was to determine the metallized J_{0e}, which is composed of the passivated region between the gridlines and metallized emitter portion under the grid. To quantify and explain the difference between the metallized J_0 for the two pastes, we used an implanted doping profile and established a baseline or reference value of $J_{0e,metal}$ for that profile assuming evaporated or uniform full area metal-Si contact interface with SRV = 10^7 cm/s. This reference value was compared with the experimentally determined values of $J_{0e,metal}$ for the screen printed contacts to estimate the efficacy of different pastes with respect to evaporated contacts. These results are discussed in the next section.

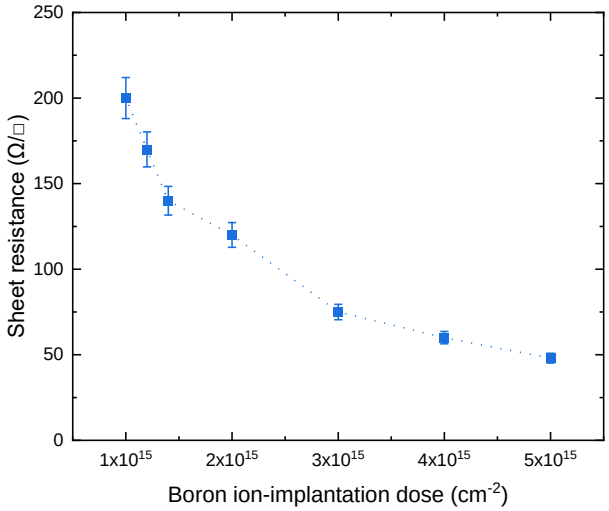


Figure 48: Boron emitter sheet resistance as a function of boron ion-implantation doses for 10 keV implantation energy and 1050 ℃ post-implantation anneal.

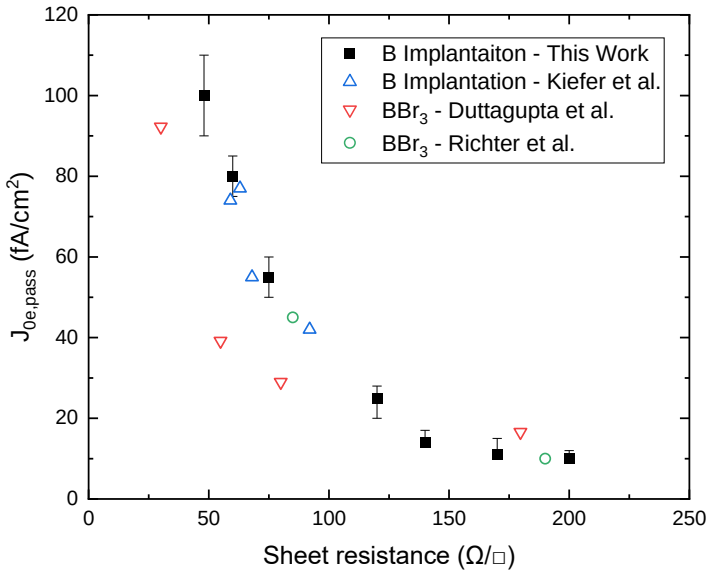


Figure 49: Experimentally measured $J_{0e,pass}$ in this study (solid symbols) and selected literature data (open symbols) [104-106] as a function of boron emitter sheet resistance on textured surface.

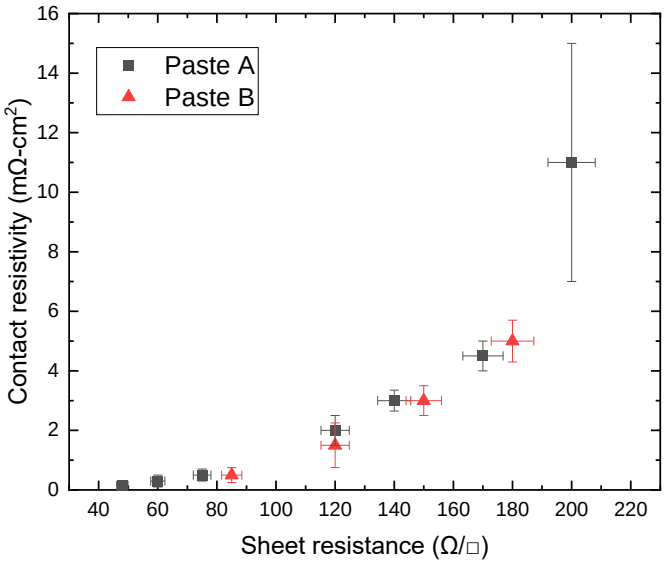


Figure 50: Measured contact resistivity as a function of boron emitter sheet resistance for paste A and B.

5.3 Modeling to Establish a Baseline Metallized $J_{0e,metal}$ Value for Implanted B Emitters Assuming Uniform Metal Contact Interface with Surface Recombination Velocity (SRV) = 10^7 cm/s

Sentaurus Process model was used to simulate various implanted B profiles in this study. In this process model, we selected 'Monte Carlo model' for simulating distribution of implanted B and 'Boron-interstitial clusters' (BIC) model for simulation of dopant activation and clustering. This was validated by direct ECV measurements of couple of profiles. Figure 51 shows a reasonably good match between the measured B profile by ECV and the simulated profile for the 170 Ω/□ emitter. The small deviations between simulation and measurement are attributed to the actual diffusion mechanism and assumed oxidation enhanced diffusion model. This validation provided a good basis for simulating B emitter profiles implanted with different doses, as shown in Figure 52. These profiles were then fed into the Sentaurus Device model to generate J_0 vs SRV curves for the simulated profiles by varying SRV, as shown in Figure 53. Full area baseline $J_{0e,metal}$ value for each emitter was extracted assuming a uniform 100% metal-Si contact area with SRV = 10^7 cm/s. This baseline $J_{0e,metal}$ value is used as a reference to compare the measured $J_{0e,metal}$ values for different screen-printed metal pastes to assess the quality of different screen-printed contacts. It is important to recognize that actual screen-printed contact interface is highly non-uniform and can have $J_{0e,metal}$ greater or less than the baseline case depending on the paste and firing conditions. Unlike the uniform metal evaporated contacts, Figure 54 shows a schematic of a typical non-uniform screen-printed interface [107]. If there are metal crystallites embedded into the emitter in conjunction with over-etching of the passivation layer by glass frit (resulting in partial truncation of the emitter profile), then

$J_{0e,metal}$ could be higher than the baseline case. On the other hand, if there are some unetched passivating dielectric or SiN islands under the metal grid (resulting in local contacts), then $J_{0e,metal}$ can be lower than the baseline $J_{0e,metal}$ value.

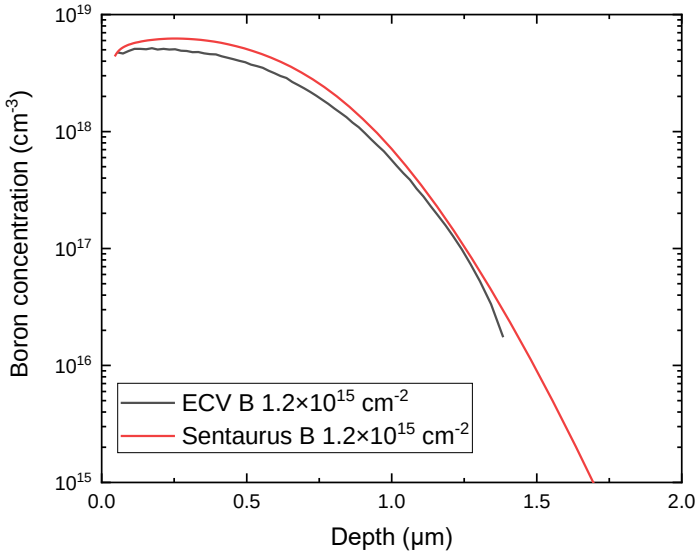


Figure 51: Comparison between the ECV measurement and the Sentaurus Process simulation for B emitter profile with implanted dose of 1.2×10^{15} cm^{-2}.

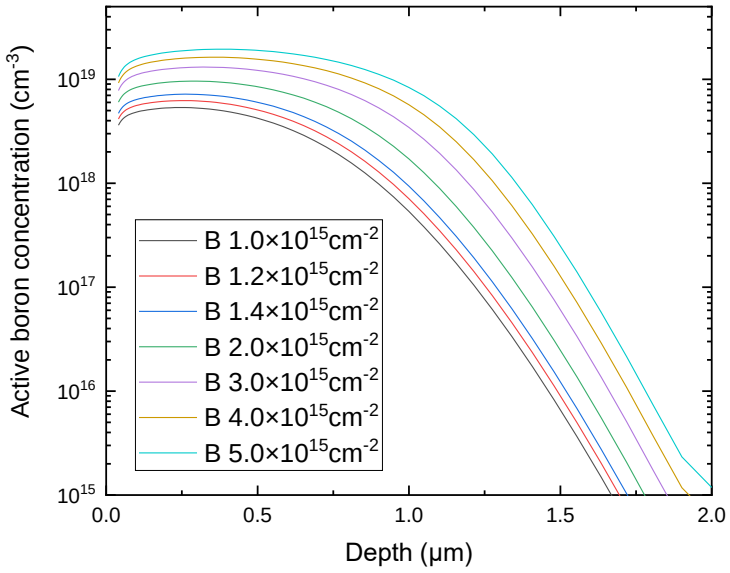


Figure 52: Simulated boron profiles with different implanted boron doses with Sentaurus Process simulation.

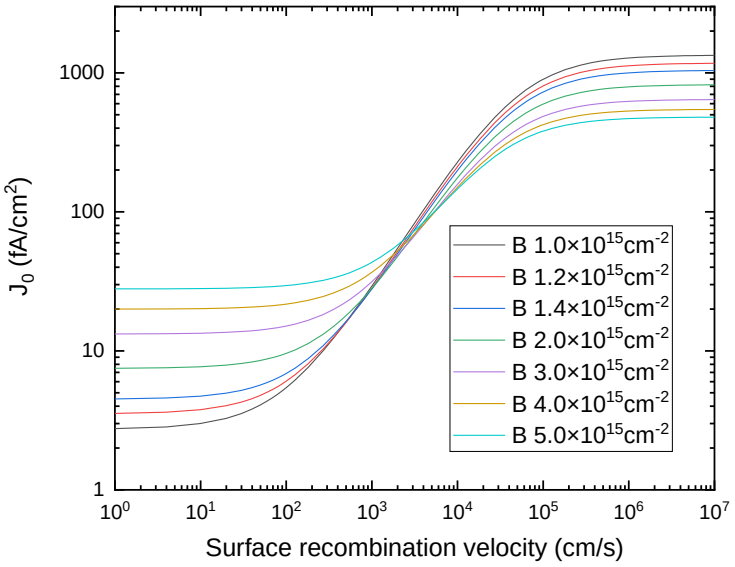


Figure 53: Sentaurus calculated J_{0e} as functions of surface recombination velocity with different boron implant doses.

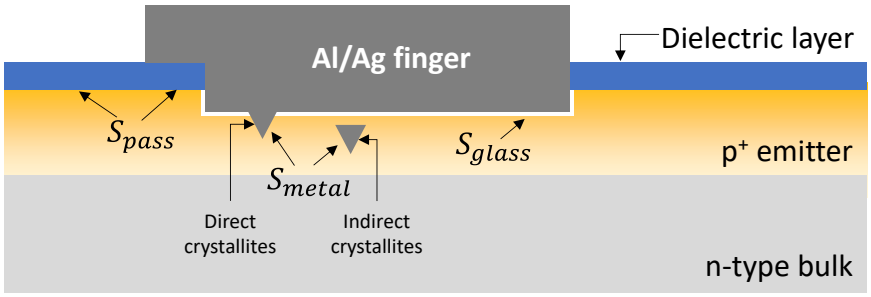


Figure 54: Schematic diagram of the features of metal-Si contact formation after firing.

5.4 Modeling and Quantitative Understanding of the Significant Difference in Measured $J_{0e,metal}$ for Pastes A and B

Formation of screen-printed contacts involves firing-induced etching or dissolution of passivation and antireflection coatings by molten glass frit, followed by solidification of a very thin glass layer between the Si emitter surface and bulk Ag/Al electrode [108-110]. Some Ag crystallites are also formed at the Si surface and become partially embedded into the Si emitter surface to form either direct contact to the top metal electrode or indirect contact through the glass layer above it (Figure 54), which can conduct by tunneling or hopping through the suspended fine Ag particles in glass layer [110, 111]. Any appreciable etching of the emitter surface layer by glass frit during this process is known to increase sheet resistance and $J_{0e,metal}$ and lower implied FF, because metal contacts are made deeper into the emitter compared to the original surface [107, 112, 113]. On the other hand, if the frit is not very aggressive, the entire dielectric layer underneath the metal electrode may not dissolve, resulting in the formation of non-uniformly distributed dielectric islands underneath the grid [107]. This will reduce the $J_{0e,metal}$ value due to local contacts through

the dielectric layer relative to the full-area evaporated baseline contact. That is why we first established the baseline $J_{0e,metal}$ value for reference. Local contacts will be preferred for higher efficiency cells provided contact area is large enough to give reasonable contact resistivity and series resistance.

In the previous section, we defined the baseline contact as a contact with uniform interface and 100% metal-Si contact with SRV = 10^7 cm/s. Baseline $J_{0e,metal}$ was found to be 1172 fA/cm^2 for our 170 Ω/□ emitter (Figure 53). However, linear plots of total J_0 as a function of f_{metal} for pastes A and paste B on 170 Ω/□ emitter in Figure 55 reveal very different $J_{0e,metal}$ values. For both pastes A and B, the intercept ($2 \times J_{0e,pass}$) gave $J_{0e,pass}$ value of ~11 fA/cm^2, but the slope ($J_{0e,metal} - J_{0e,pass}$) gave $J_{0e,metal}$ = 1358 fA/cm^2 for paste A, which is 15% higher than the simulated baseline value. On the contrary, $J_{0e,metal}$ for paste B was found to be 707 fA/cm^2 , which is 40% lower than the baseline contact. To understand the reason for this significant difference, the silicon surfaces under the metal contacts were analyzed by SEM after first removing the bulk metal gridline in HCl:H_2O_2:H_2O 1:1:1 solution, and then etching the glass layer in dilute HF solution. The SEM pictures for the two pastes are shown in Figure 56.

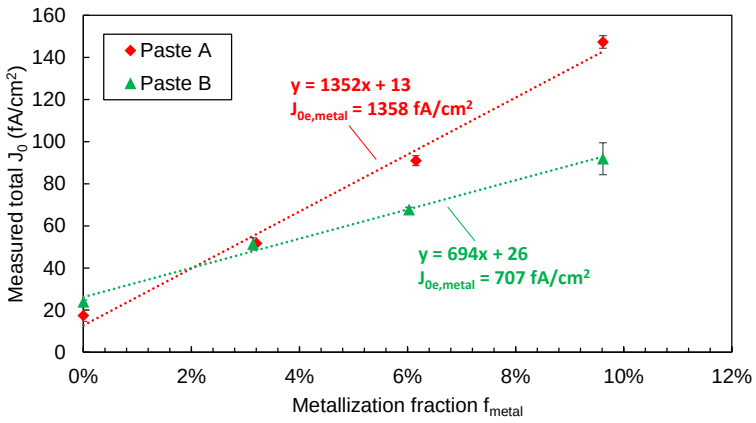
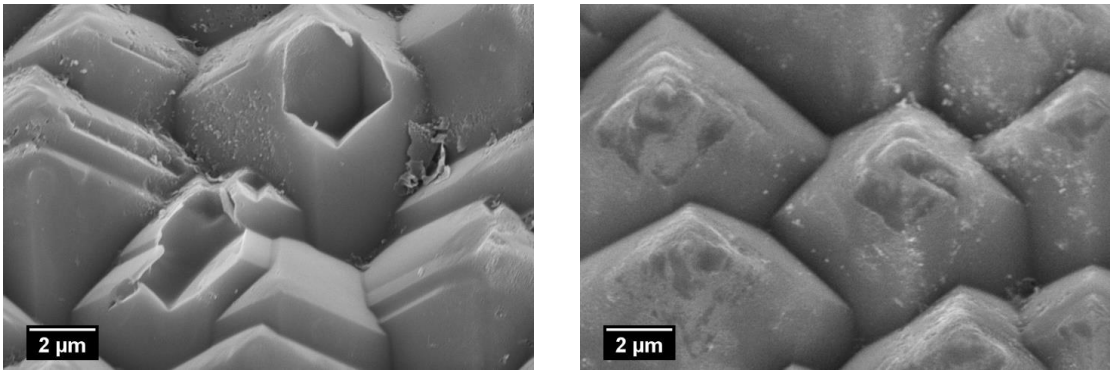


Figure 55: Plot of measured total J_0 as a function of metallization fraction f_{metal} with metal paste A and paste B. $J_{0e,metal}$ is extracted from the slope ($J_{0e,metal} - J_{0e,pass}$) of the fitted line.



(a) Paste A (b) Paste B

Figure 56: SEM images of silicon surfaces under metal contacts after removal of the fired screen-printed metal gridline and glass from fired metal gridlines with paste A and paste B.

Figure 56 (a) shows that in the case of paste A, the edges of pyramids are rounded with sporadic deep holes, and there are virtually no cloudy regions on the faces of the pyramids. Deep holes are indicative of penetrating metal crystallites, which came off

during removal of metal and glass layers. Rounding indicates the possibility of etching of the emitter surface, and the lack of cloudy regions suggests the absence of unetched dielectric islands. This suggests that frit chemistry and firing of paste A is more aggressive than desired. This is consistent with the observed increase in $J_{0e,metal}$ over the baseline contact, because both embedded metal crystallites and over-etching of dielectric layer will increase $J_{0e,metal}$, since the metal contact is made below the original emitter surface. To estimate the average emitter depth removal, we applied Daniel Inns' [112] and Koduvelikulathu's [114] methodology, which involves using a truncated profile after removing a slice of the emitter near the surface, generating a plot of J_{0e} vs SRV curve, and then determining full area $J_{0e,metal}$ at SRV=10^7 cm/s. Figure 57 shows a graph of $J_{0e,metal}$ vs emitter etch depth for paste A, which reveals an effective metal penetration depth of 130 nm at which $J_{0e,metal}$ matches the measured value of 1358 fA/cm^2.

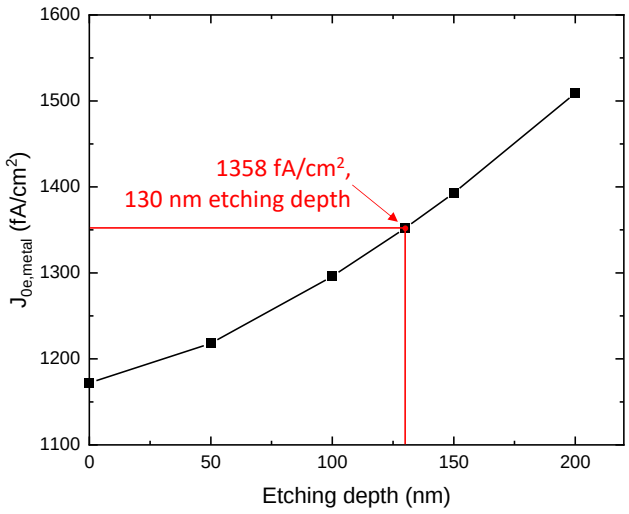


Figure 57: Simulated paste A $J_{0e,metal}$ with varied metal etching depth for 170 Ω/□ B emitter. For a uniform 130 nm surface etching, the simulated $J_{0e,metal}$ matches with the experimentally measured $J_{0e,metal}$ (1358 fA/cm^2).

Contrary to paste A, measured $J_{0e,metal}$ for paste B was found to be much lower (707 fA/cm^2) than the simulated baseline $J_{0e,metal}$ = 1172 fA/cm^2. Figure 56(b) shows that unlike paste A, the pyramids after firing with paste B do not show voids. Only minimal damage or imprints on the silicon surface are observed after the removal of metal and glass layer. This suggests no appreciable metal penetration or over etching of the emitter. However, appreciable fraction of cloudy regions on the sides of the pyramids are observed, suggesting the presence of unetched dielectric islands under the metal grid lines which were not completely removed during etching of the metal and glass layers. The presence of unetched dielectric layers has been reported by several investigators [107, 108] for the Ag/Al pastes and, as discussed earlier, may lower the $J_{0e,metal}$ by reducing the effective metal-Si contact due to local contacts.

To obtain a quantitative understanding of this effect, we calculated $J_{0e,metal}$ by assuming no emitter surface etching and variable metal-Si contact area fraction under the grid due to dielectric islands. Total $J_{0e,metal}$ was calculated as a function of unetched dielectric area fraction ($f_{dielectric}$) according to $J_{0e,metal} = 11\ f_{dielectric} + 1172 \times (1\text{-}f_{dielectric})$ where 1172 fA/cm^2 represents the calculated full area baseline metal contact for this profile and 11 fA/cm^2 corresponds to the measured full area the $Al_2O_3/SiN_x/SiO_2$ passivated emitter. Figure 58 shows the calculated $J_{0e,metal}$ as a function of dielectric area fraction under the grid, which reveals that paste B contact interface has ~40% unetched dielectric islands at which calculated $J_{0e,metal}$ in Figure 58 matches the measured value of 707 fA/cm^2.

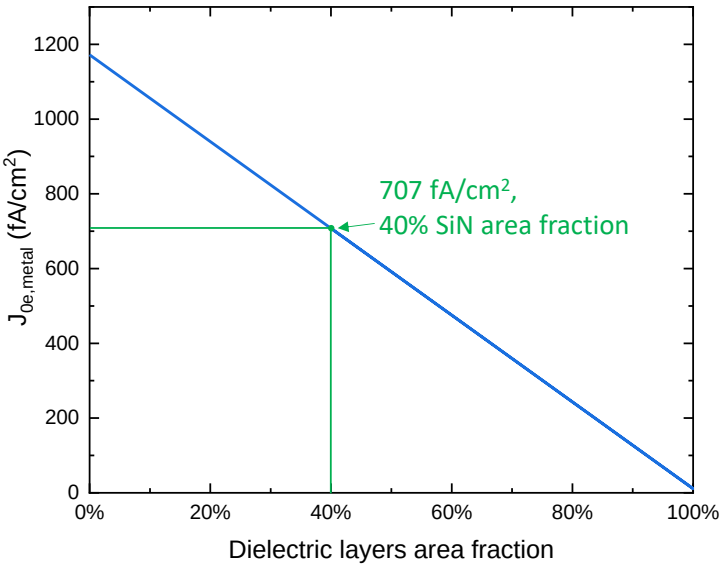


Figure 58: Simulated paste B $J_{0e,metal}$ with varied dielectric area fraction under the grid for 170 Ω/□ B emitter. With 40% unetched dielectric area fraction underneath metal contact, the simulated $J_{0e,metal}$ matches with the measured $J_{0e,metal}$ (707 fA/cm^2).

Next, we performed model calculations to estimate full area $J_{0e,metal}$ for all the B emitter profiles or sheet resistances fabricated in this study for the two pastes assuming emitter etch depth of 130 nm for paste A and unetched dielectric area fraction of 40% for paste B (Figure 59). These values were then used in device modeling to predict the cell efficiency and select the optimum emitter, since $J_{0e,pass}$ and $J_{0e,metal}$ show opposite trends. For efficiency calculations, the number of grid lines was optimized for each sheet resistance using the grid model described in Chapter 3. After establishing full area $J_{0e,pass}$ =11 fA/cm^2 and $J_{0e,metal}$ = 707 fA/cm^2 (Figure 55) for our 170 Ω/□ implanted homogeneous emitter, we estimated the total metallized J_{0e} using the metal-Si contact area fraction of 2.7% for our 40 μm wide 106 grid lines and five floating busbars according to:

$$J_{0e,metal} = 11 \times f_{dielectric} + 707 \times (1 - f_{dielectric})$$
$$= 11 \times 0.973 + 707 \times 0.027 \quad \textbf{(61)}$$
$$= 29.8\, fA/cm^2$$

This is very close to our target value of ~30 fA/cm^2 for the 23% efficient cell (Figure 31). In addition, this emitter has 3-5 mΩ-cm^2 contact resistance (Figure 50), which is also consistent with the requirement of the technology roadmap. Therefore, we decided to use 170 Ω/□ homogeneous emitter for our 23% efficiency target.

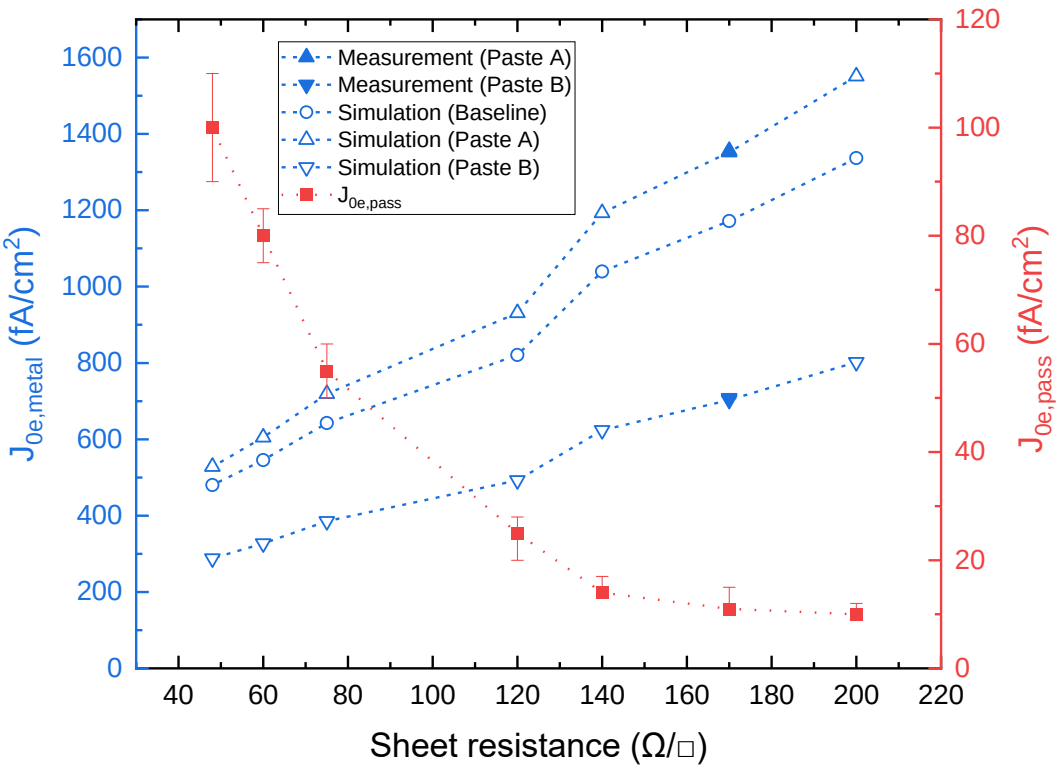


Figure 59: Measured $J_{0e,metal}$ at 170 Ω/□ boron emitter, and simulated $J_{0e,metal}$ for baseline, paste A (assuming emitter etch depth of 130 nm) and paste B (assuming unetched dielectric layers area fraction of 40%) as a function of boron sheet resistance from Sentaurus simulation.

5.5 Summary

In this task, optimization of doping profile, surface concentration, unmetallized and metallized recombination current density and sheet resistance of ion-implanted B emitter was investigated. Measured $J_{0e,pass}$ and contact resistances of various ion-implanted B emitters with R_{sheet} in range of 48-200 Ω/□ are reported. Some of the lowest $J_{0e,pass}$ values (< 15 fA/cm^2) were achieved for implanted textured B emitters with R_{sheet} > 140 Ω/□. Based on the SEM images of the metal/Si contact interfaces and measured J_0 values for different pastes, it was concluded that paste chemistry and firing affects the extent of emitter surface etching and the percentage of unetched dielectric islands under the metal contacts. This can increase or decrease the metallized J_0 of screen-printed contacts compared to an evaporated metal contact interface. It was found that Paste A increased the $J_{0e,metal}$ by 16% due to 0.13 μm etching of the emitter surface, while paste B resulted in 40 % reduction in $J_{0e,metal}$ due to the significant fraction of unetched or undissolved dielectric islands under the grid that result in the formation of local contacts. In this chapter, consistent with our technology roadmap for 23% cell efficiency, we succeeded in designing and fabricating a 170 Ω/□ ion-implanted homogeneous B emitter with Al_2O_3/SiN passivation and screen-printed contacts, using paste B and 2.67% metal-Si contact area, that gave a metallized J_{0e} of ~30 fA/cm^2 with contact resistivity of < 5 mΩ-cm^2.

CHAPTER 6. TASK 3: DEVELOPMENT, OPTIMIZATION AND FABRICATION OF REAR SIDE N-TOPCON WITH METALLIZED J_{0B}, OF 5 FA/CM^2 *

After developing the screen-printed B emitter on the front with metallized J_{0e} of 30 fA/cm^2, in this chapter we report on the development of rear side n-TOPCon with metallized J_{0b}, target of ~5 fA/cm^2 to attain 23% cell efficiency. As mentioned before, efficiency of current industrial silicon solar cells is largely limited by the recombination in the heavily doped regions in the absorber and at the metal/silicon contacts to them. Tunnel oxide passivated contacts (TOPCon) are a promising candidate for next-generation high-efficiency Si solar cells because they can eliminate high recombination at the metal/Si contacts and bypass the needs for heavily diffused regions inside the absorber. This is achieved by displacing the diffused and metallized regions outside the Si absorber by introducing a tunnel oxide in between. Therefore, in this task, we have replaced the traditional phosphorus diffused n^+ BSF on the rear side of PERT cell with n-TOPCon which is composed of ultra-thin tunnel oxide on top of a Si wafer capped with a heavily doped poly-Si layer. In this study, phosphorus-doped poly-Si layers are deposited by a low-pressure chemical vapor deposition (LPCVD) on top of a chemically grown tunnel oxide, followed by a high temperature anneal to crystallize and activate dopants in poly-Si. Somewhat thicker (100-200nm) poly-Si layers are deposited to prevent J_0 degradation due

* Experimental results in Section 6.1.1 to 6.1.3 courtesy of Ajay Upadhyaya and Dr. Young-Woo Ok in UCEP, Georgia Tech.

to metal penetration through poly-Si into the Si wafer during the subsequent formation of screen-printed contacts to n^+ poly-Si surface which are fired at high temperature (~775 ℃).

6.1 Experimental Development and Characterization of N-TOPCon Using Chemically Grown Tunnel Oxide and LPCVD Polysilicon

6.1.1 Development of Chemically Grown Ultra-Thin Tunnel Oxide for TOPCon

Tunnel oxide can be fabricated by nitric acid oxidation [115, 116], thermal oxidation [44], ozone oxidation [42, 44], and atomic layer deposition [117]. The thickness of the tunnel oxide is crucial, because it needs to be thick enough to block minority carrier transport from the bulk Si into poly-Si, but should be thin enough to allow the majority carriers to tunnel through without introducing appreciable contact resistance. Shewchun et al. showed that the tunnel oxide thickness needs to be less than 20 Å to obtain efficient tunneling [118]. In this research, we decided to use nitric acid oxidation (NAO) of Si for the tunnel oxide fabrication because the thickness of chemical oxide grown by this process saturates at ~15 Å and does not change appreciably after that [115, 116]. In addition, very good reproducibility of the SiO_2 thickness (± 0.05 nm) has been reported [116] , making this oxidation process simple and easy to control. Oxidation of c-Si surface with HNO_3 involves production of high concentration of atomic oxygen, with strong oxidizing ability, due to following decomposition process [116]:

$$2HNO_3 \rightarrow 2NO + H_2O + 3O \quad \textbf{(62)}$$

Therefore, during the NAO process, the atomic oxygen diffuses through the growing SiO_2 layer and reacts at the Si/SiO_2 interface. As a result, very stable and homogeneous ultra-

thin SiO_2 can be formed with the NAO process. Various temperatures and concentrations of HNO_3 have been used for this method and reported in the literature [116]. We found that the use of 68%$_{wt}$ HNO_3 at 100 ℃ gives a uniform oxide thickness that saturates at ~17 Å (Figure 60), which is nearly perfect for tunneling and carrier selectivity. Figure 61 shows the cross-section transmission electron microscopy image of our HNO_3 grown tunnel oxide in between n^+ poly-Si and n-Si base to validate its thickness and uniformity.

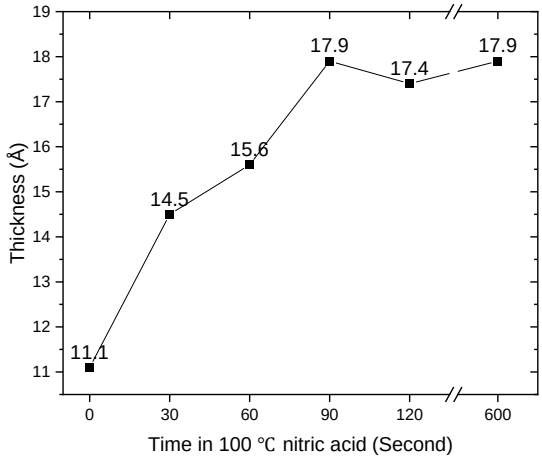


Figure 60: Oxide thickness as a function of time in 100 ℃ in nitric acid.

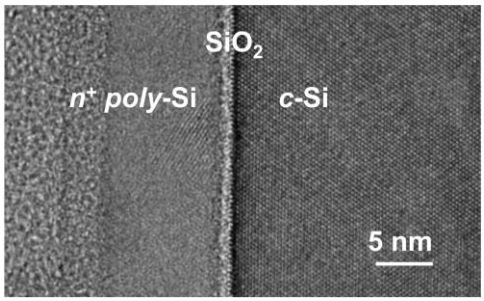


Figure 61: Transmission electron microscopy image of our tunnel oxide passivated contact structure.

6.1.2 Fabrication of Phosphorous-Doped Poly-Si by Low-Pressure Chemical Vapor Deposition

After tunnel oxide fabrication we focused on the development of doped poly-Si on top of it. Poly-Si layer can be formed by plasma-enhanced chemical vapor deposition (PECVD) or low-pressure chemical vapor deposition (LPCVD), followed by a high-temperature annealing for crystallization and dopant activation. PECVD is commonly used for deposition of SiN_x in the industry, and has the advantage of single-side deposition technology. However, because of the potential risk of blistering of thicker a-Si layer deposited at low temperatures, due to the large amount of hydrogen incorporated into PECVD films, it may restrict the maximum film thickness [67, 119]. That is what we observed in our PECVD tool. In addition, the ultra-thin tunnel oxide could also be damaged by ion-bombardment in PECVD [120, 121], resulting in inferior J_0 or surface passivation.

LPCVD has the advantage of producing highly conformal and pinhole-free layers, which ensures that the tunnel oxide is protected against the subsequent chemical and heat treatments [63], and allows for a larger number of wafers to be processed with better thickness and passivation uniformity [63, 122]. Therefore, we decided to use LPCVD for poly-Si deposition. A downside of LPCVD is that it grows poly-Si on both sides. The poly-Si wrap-around on the front side can be easily removed with an inline single side etching tool widely used in industrial setting [123, 124]. However, the single-side etching tool was not available in our lab, so a process sequence involving a dielectric mask had to be developed (Section 6.1.6) to retain the rear poly-Si and remove the front side poly.

6.1.3 Optimization of Crystallization and Dopant Activation Anneal of Poly-Si Layer

To characterize the LPCVD n-TOPCon structure in terms of passivation quality, symmetric LPCVD grown n-TOPCon structures (n^+ poly/tunnel oxide/Si/tunnel oxide/n^+ poly) on planar Si wafers were prepared, as shown in Figure 62. Lightly doped Cz wafers with resistivity of ~50 Ω-cm and high bulk lifetime (> 3 ms) were used in this study to ensure high level injection for J_0 determination by photoconductance decay measurements (Chapter 2). After growing the tunnel oxide by nitric acid oxidation for 10 minutes at 100 ℃, a phosphorous-doped polysilicon layer was deposited on both sides of the wafer in a LPCVD furnace at a temperature of 588 ℃ with SiH_4 and PH_3 gases. Detailed LPCVD recipe parameters are shown in Table 10. Since the as-deposited poly-Si layer at 588°C was found to be a mixture of amorphous and crystalline silicon [125], a crystallization anneal was performed to improve the properties of this layer and activate the dopants. The samples were annealed in the temperature range of 800~950 °C in N_2 ambient for dopant activation and crystallization. After a crystallization anneal above 800°C in N_2 ambient, the iV_{OC} and J_0 were measured at an injection level of ~1-3×10^{15}/cm^3 using the Sinton PCD tester (Chapter 2) and the photoconductance decay method proposed by Kane and Swanson [20]. Figure 63 shows that the increase in the annealing temperature from 800 to 875 ℃, increases the implied V_{oc} from less than 700 mV to ~725 mV and decreases unmetallized J_{0b}, significantly from 150 fA/cm^2 to ~5 fA/cm^2.

Table 10: Recipe parameters for phosphorus-doped poly-Si with LPCVD in this work.

Parameters	Value
Temperature (°C)	588
Deposition pressure (torr)	0.25
100% SiH_4 flow rate (sccm)	100
1% PH_3 in H_2 flow rate (sccm)	30

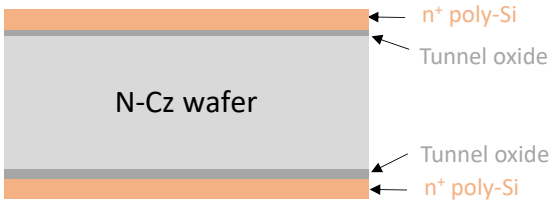


Figure 62: Symmetric structure to study $J_{0b'}$ and iV_{OC}.

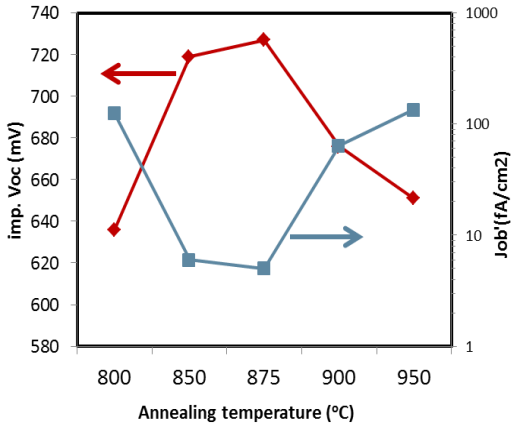


Figure 63: Implied V_{OC} and $J_{0b'}$ as a function of annealing temperature of n-TOPCon with NAO grown tunnel oxide and LPCVD poly-Si.

In order to understand and explain the effect of crystallization temperature on iV_{OC} and J_0 in Figure 63, SIMS (secondary ion mass spectrometry) analysis was performed as a function of polysilicon anneal temperature on mirror-polished wafers to study the extent of phosphorous activation and diffusion into Si through the tunnel oxide. Figure 64 shows the SIMS profile of the phosphorous-doped polysilicon in the as-deposited state as well as a function of annealing temperature. In this type of SIMS measurements, Argon sputtering can cause some phosphorous to diffuse into the silicon (black curve in Figure 64). Figure 65 reveals that phosphorous diffuses depth (>120nm) increases as the anneal temperature is increased from 800°C to 930°C. Note that heavy P diffusion in Si will hurt passivation, iV_{OC} and J_0 due to increased Auger recombination and bandgap narrowing but modest or low P diffusion may improve iV_{OC} by shielding the tunnel oxide interface defects without introducing significant Auger recombination.

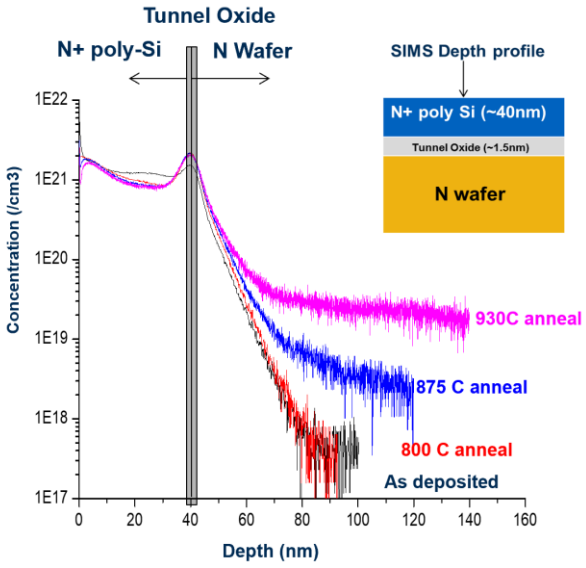


Figure 64: SIMS measurement of the phosphorous-doped polysilicon after annealing with different temperatures (courtesy of National NanoFab Center, Korea, [126]).

To further understand the degradation in iV_{OC} at higher anneal temperatures (> 900 °C), high-resolution transmission electron microscopy (HREM) was performed on our selected samples at Chonbuk National University, Korea. HREM is an imaging mode of the transmission electron microscope (TEM) that allows for direct imaging of the atomic structure of the sample. Figure 65 shows that the thin ~1.5nm chemical oxide can withstand moderate to high (875°C) anneal temperatures, because no disruption or breakdown was observed. However, after the 930°C anneal, the tunnel oxide is somewhat deformed as indicated by the arbitrary dashed red line in Figure 65 c, which shows larger poly-crystalline grains causing the tunnel oxide to thin in some regions, which may locally disrupt the oxide in extreme cases. This could enhance undesirable tunneling of holes from the bulk into the n^+ region and reduce the carrier-selectivity, accounting for increased recombination and the lower iV_{OC}. We believe a combination of interface disruption and excess P diffusion is the reason for degradation at anneal temperatures higher than 875 °C. At lower temperatures from 800 ℃ to 875 ℃, iV_{OC} increases gradually due to more dopant activation and band bending, improved crystallization and modest P diffusion into Si.

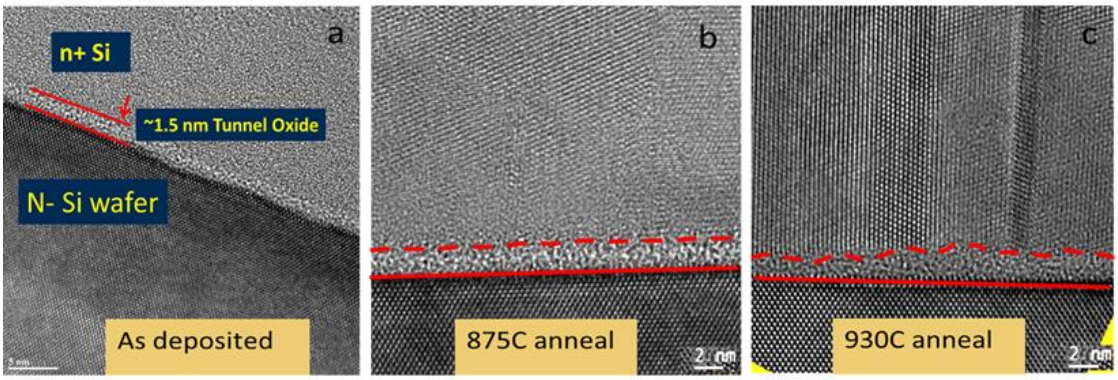


Figure 65: HREM images of the tunnel oxide interface between n-Si and n^+ poly-Si a) As deposited, b) Annealed at 875°C, c) Annealed at 930°C. (Courtesy of Chonbuk National University, Korea, [126].)

6.1.4 Investigation of the Effect of Surface Morphology on Recombination Current Density and Contact Resistivity of LPCVD TOPCon Structure

After the optimization of annealing temperature of poly-Si, the effects of the surface morphology (planar or texture) on recombination current density and contact resistivity on LPCVD TOPCon are investigated. The front side of solar cells requires textured surface for reduced reflection and efficient light trapping. However, it is more challenging to have good passivation and reduce carrier recombination on textured surface because of the presence of sharp edges and valleys [127] due to the pyramids and the higher Si/SiOx interface state density on the textured (111) surface relative to untextured or planar (100) surface [128]. To evaluate the surface morphology effect on the J_0 and contact resistivity of LPCVD grown n^+ poly-Si TOPCon structures, symmetric structures on textured and planar surfaces were made, as shown in Figure 66. After an acid clean and HF dip, a ~15 Å tunnel oxide layer was grown by nitric acid oxidation (NAO) at 100 °C for ~10 minutes,

followed by 200 nm LPCVD n^+ poly-Si deposition on both sides at the same time at 588 °C with in-situ phosphorus doping. The samples were then annealed at 875 °C for 30 minutes in N_2 ambient for poly-Si crystallization and dopant activation. The poly-Si was then capped with ~750 Å thick PECVD SiN_x layer. The J_0 and implied V_{OC} were measured by the photoconductance decay method proposed by Kane-Swanson [20].

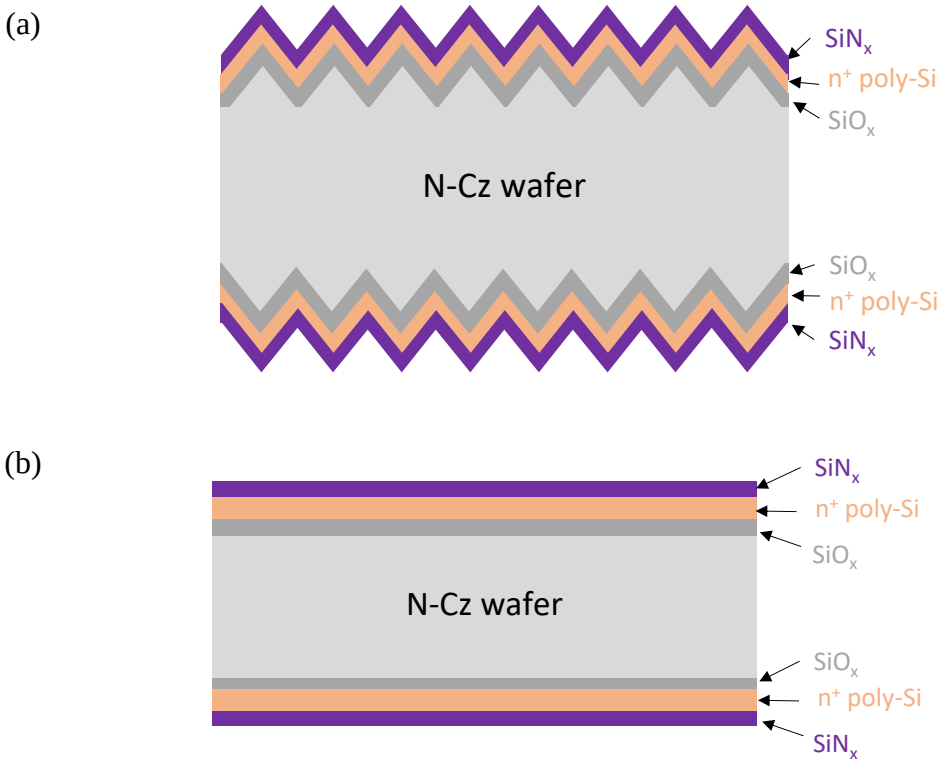


Figure 66: Schematic structures n-TOPCon symmetric structure with (a) texture surface and (b) planar surface to investigate the impact of surface morphology on passivation quality and metal contact resistivity.

In order to quantify the effect of screen-printed fire-through metallization on recombination current density of n-TOPCon ($J_{0b'}$), a special screen was designed (Figure 67) which can print four different metal fractions (0%, ~3%, ~6%, ~9%) on a single 6 inch

× 6 inch wafer to extract the metallized J_0. In addition, it had TLM metal patterns with different line spacing to extract contact resistivity. The patterns in Figure 67 were screen-printed using Ag paste (Dupont 17S) only on one side of the symmetric structures with planar and textured surfaces, and fired in a belt furnace at peak temperatures of 745±5 °C and 775±5 °C (Figure 68). The contact resistivity was measured with transfer length method (Section 4.5.1). After the TLM measurement, the bulk or excess Ag metal on the rear side was etched away in $HCl:H_2O_2:H_2O$ =1:1:1 solution, leaving only the embedded metal contact/crystallites and the glass layer on the surface for the metallized J_0 measurements.

Figure 67: Test screen with different metal fractions and TLM patterns for metallized J_0 and contact resistance measurements.

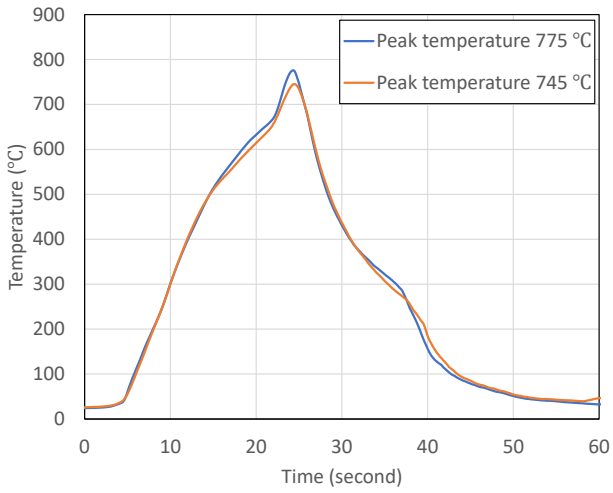


Figure 68: Measured temperature profile for firing screen-printed metal contacts in a belt furnace at peak temperature 775 ± 5 °C and 745 ± 5 °C.

Figure 69 shows the measured total resistance on TLM patterns as a function of contact spacing on n-TOPCon on the planar and textured surfaces after 745 °C and 775 °C simulated firing (Figure 68). From these plots we can extract the contact resistivity and sheet resistance, as described in Section 4.5.1 and Figure 41. The contact resistivities extracted from Figure 69 are summarized in Table 11. It shows that on planar surface, 745 °C peak firing temperature is too low to obtain a reasonable contact resistivity (< 10 mΩ-cm^2), however on textured surface, both 745 °C and 775 °C can give contact resistivity less than 10 mΩ-cm^2. Therefore, we selected 745 °C peak firing temperature for textured surface because lower firing temperature reduces metal-induced damage to the surface, and 775 °C temperature was used for planar surface to obtain a reasonably good contact resistivity.

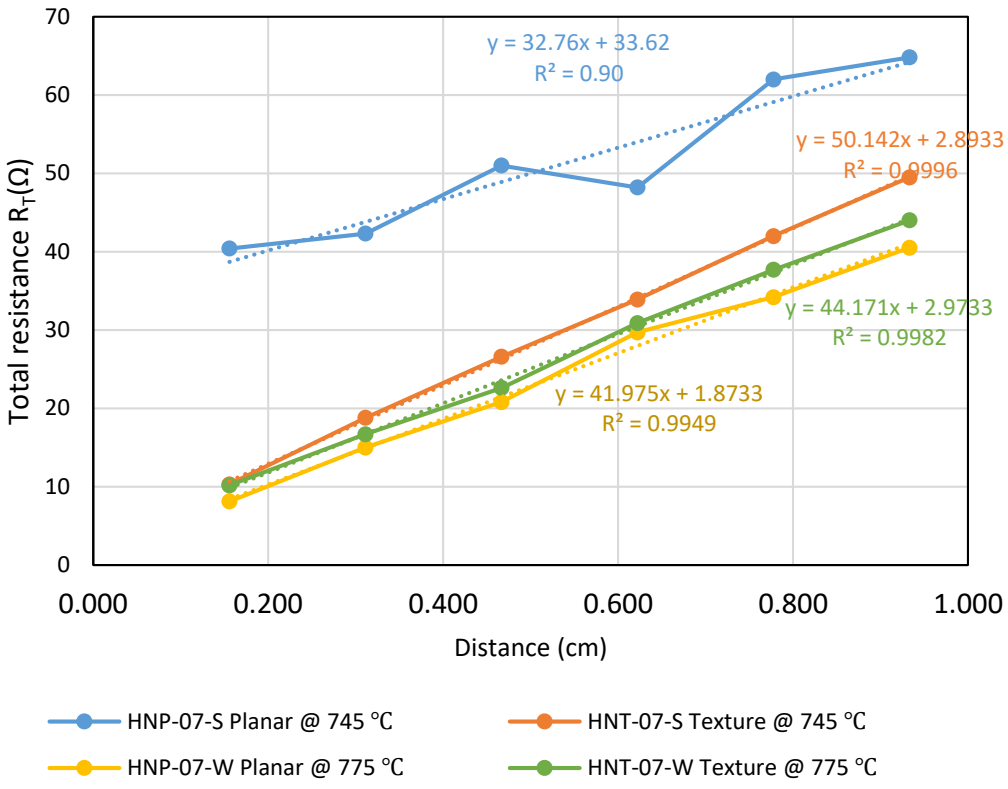


Figure 69: Plot of total resistance (R_T) as a function of contact spacing on planar and textured surfaces, with peak firing temperature at 745 ℃ and 775 ℃.

Table 11: Contact resistivity on n^+ poly-Si as a function of surface morphology and peak firing temperature.

	Contact resistivity (mΩ-cm^2)	
Peak firing temperature	**745 ℃**	**775 ℃**
Planar surface	84	**4.7**
Texture surface	**7.2**	7.4

The J_0 and implied V_{OC} values after different processing steps were measured for 200 nm n^+ TOPCon on planar and textured surfaces and the results are summarized in

Figure 70 and Figure 71, respectively. Note that for the TOPCon on planar surface, the unmetallized J_0 is only 3.3 fA/cm^2 and drops to 2.3 fA/cm^2 after SiN deposition, possibly due to SiN induced hydrogenation of the Si/SiO_2 interface defects. After screen-printing and firing, the J_0 increase to 6 fA/cm^2, which is very close to our target $J_{0b'}$= 5 fA/cm^2 for 23% efficiency (Task 1 Figure 31). However, for n^+ poly-Si on textured surface, the $J_{0b'}$ was 12.3 fA/cm^2 just after the annealing process, 4.6 fA/cm^2 after SiN deposition, and increase to an unacceptable level of 34.6 fA/cm^2 with 9.1%metal coverage. The higher TOPCon J_0 on textured surface than planar surface are also reported in [44, 63]. Therefore, in order to achieve the 23% efficiency target with metallized $J_{0b'}$ of ~5fA/cm^2, the planar back surface was used in this study for the rear n-TOPCon deposition.

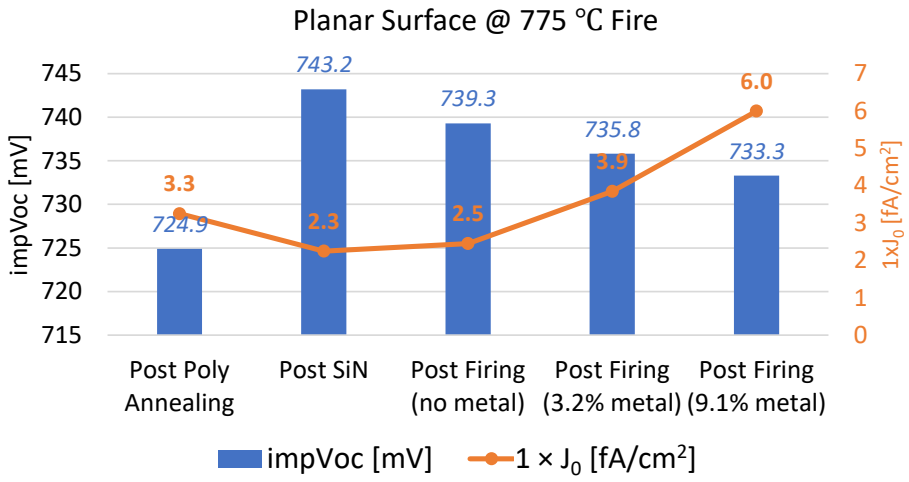


Figure 70: Metal effect to implied V_{OC} and 1×J_0 value at different process stages on planar surface at 775°C peak firing temperature.

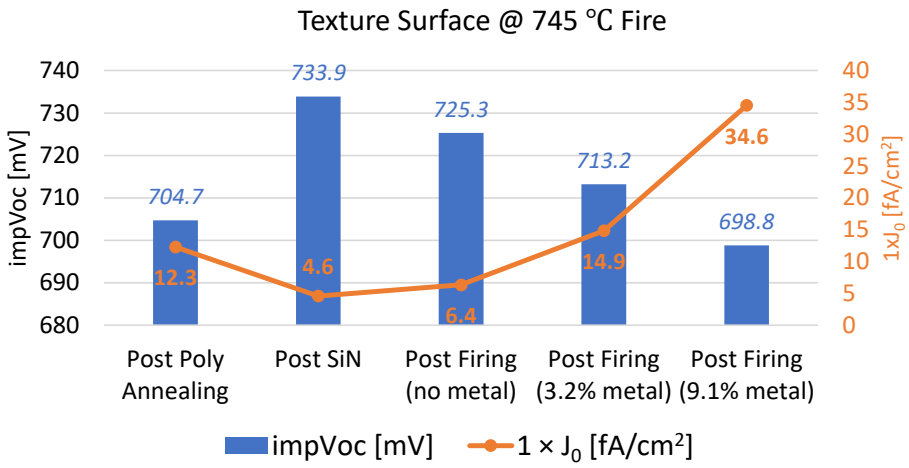


Figure 71: Metal effect to implied V_{OC} and $1\times J_0$ value at different process stages on texture surface at 745 ℃ peak firing temperature.

6.1.5 Investigation of the Impact of LPCVD Poly-Si Thickness on Recombination Current Density (J_0) of the N-TOPCon

Even though screen-printed contacts are fired through a SiN coating, some Ag crystallites may penetrate into the surface of poly-Si or aggressive glass frit may etch some poly-Si areas, resulting in undesirable local Ag contacts to the bulk Si through the tunnel oxide. This will increase metal-induced recombination or J_0. This effect can be mitigated by growing thicker poly-Si layer; however, this approach will increase absorption in rear poly and decrease the short circuit density. Therefore, poly-Si thickness and firing conditions were optimized for the selected paste in this study to achieve good passivation quality (low metallized J_0 and high V_{OC}) without appreciably sacrificing J_{SC} and FF due to parasitic absorption, sheet resistance and contact resistivity. This was done by first fabricating symmetric structures with tunnel oxide capped with LPCVD poly of different

thickness on both sides, and then measuring the unmetallized $J_{0b'}$ after (a) poly-Si anneal (b) SiN_x deposition, and (c) contact firing cycle. Detailed process sequence for making test structures involved surface damage removal and planarization of Si wafers in 80°C 9% KOH solution, followed by an acid clean and growth of a ~15Å tunnel oxide layer in 100 °C nitric acid (HNO_3). On top of the tunnel oxide, a 100 or 200 nm poly-Si layers were deposited at 588°C by LPCVD, followed by an 875°C/30 min anneal in N_2 for crystallization and dopant activation. Figure 72 shows the measured poly-Si thickness with Woollam M2000 ellipsometer for the two samples with thickness of 100 and 200 nm fabricated on 4-inch polished monitor wafers.

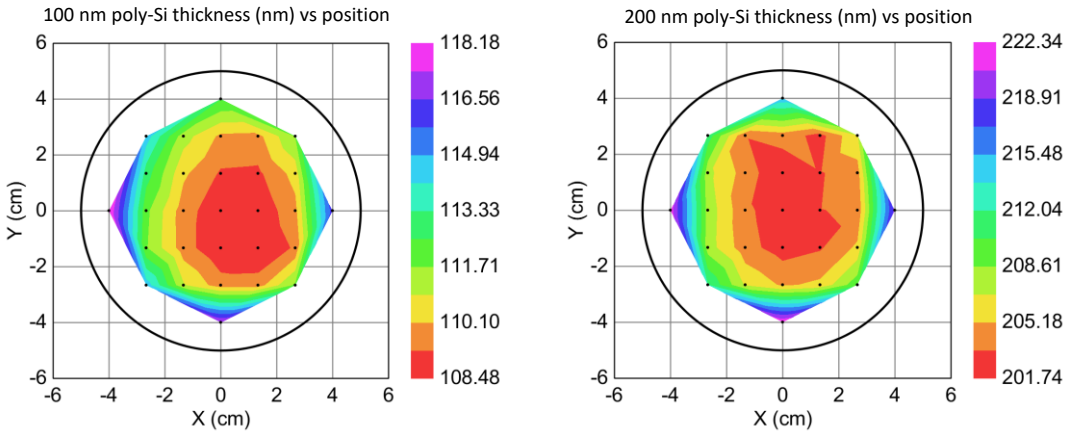


Figure 72: Poly-Si thickness measured with ellipsometer on 4-inch polished monitor wafers.

Figure 73 shows the $J_{0b'}$ and iV_{OC} for 100 nm and 200 nm thick poly-Si. Note that unmetallized $J_{0b'}$ gets better both after SiN_x deposition and simulated contact firing cycle, possibly due to SiN induced hydrogenation of the Si/SiO_2 interface defects. This resulted in an excellent median value of less than 2 fA/cm^2 for unmetallized $J_{0b'}$ for both 100 nm

and 200 nm thick poly-Si, which is comparable to the best values reported in the literature for planar n-TOPCon [55, 63]. This is also supported by very high unmetallized implied V_{OC} (~735 mV), which is inversely related to J_0.

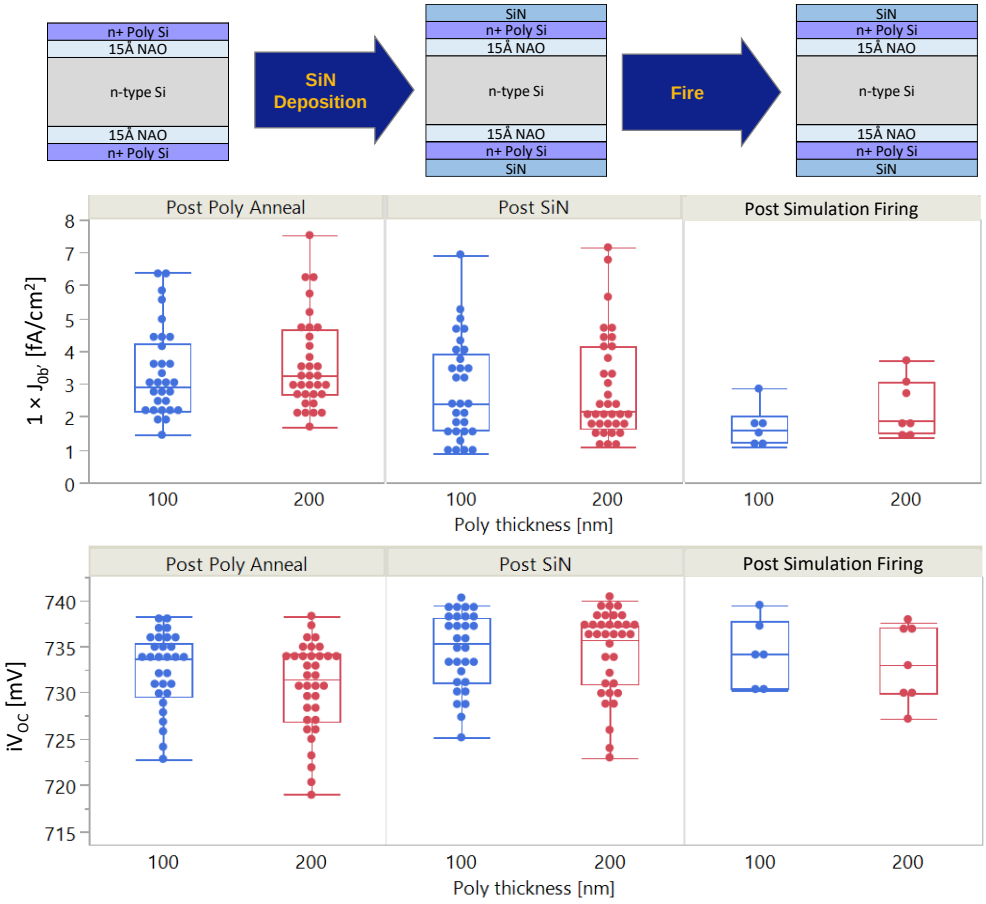


Figure 73: $J_{0b'}$ and iV_{OC} with different LPCVD poly-Si thicknesses at different stages. Data points are measured with 5 wafers for 100 nm poly, and 6 wafers for 200 nm poly-Si. Each wafer is measured with 5 positions at the post poly anneal stage, and the post SiN stage. For the post simulation firing stage, only the quarters without screen-printed metal are shown (1 point on each wafer).

Next, we investigated the impact of metallization by screen-printing the grid pattern prior to the firing cycle. As expected, we found that choice of metal paste and firing

condition play an important role in dictating the final metallized J_0 value. Note that optimized paste and firing must also achieve low metal-poly Si contact resistivity without appreciably sacrificing the passivation quality. The impact of metallization on J_0 was investigated with the help of asymmetric LPCVD TOPCon test structures with different silver metal pastes printed only on the rear side (Figure 74). After firing, the excess bulk Ag metal was removed in $HCl:H_2O_2:H_2O$ 1:1:1 solution. To conduct this study, a special screen with four different metal fractions (0%, ~3%, ~6%, ~9%) along with TLM patterns was printed on a single 6" × 6" wafer to extract the metallized J_0 and contact resistivity (Figure 67), as described in previous section. Figure 75 shows the measured total J_0 from the n-TOPCon test structures as a function of metal fraction on rear side. The total measured J_0 of the test structures with different metal fractions (f) on one side can be expressed as

$$\begin{aligned} Total\, J_{0b'} &= J_{0b'(no\ metal)} + J_{0b'(with\ metal\ fraction\ f)} \\ &= [J_{0b',pass} + 0]_{front} + [J_{0b',pass} \times (1-f) + J_{0b',metal} \times f]_{back} \\ &= (J_{0b',metal} - J_{0b',pass}) \times f + 2\, J_{0b',pass} \end{aligned} \quad \textbf{(63)}$$

where $J_{0b',pass}$ and $J_{0b',metal}$ are the full area (100% coverage) J_0 values for the un-metallized and metallized regions of n-TOPCon, which can be extracted from the intercept and slope values of the above linear relationship (Eq. (63)).

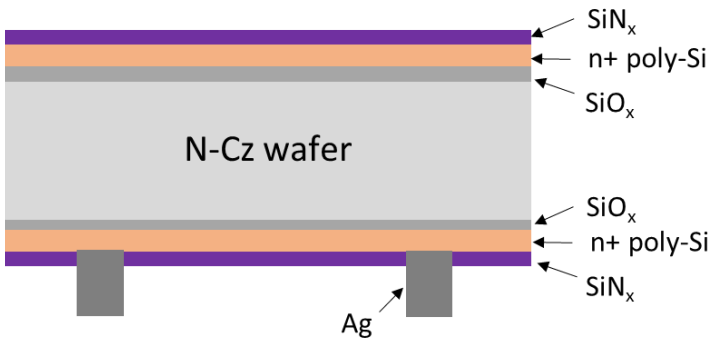


Figure 74: Schematic of n-TOPCon symmetric structure to investigate the impact of screen-printed metallization on J_0.

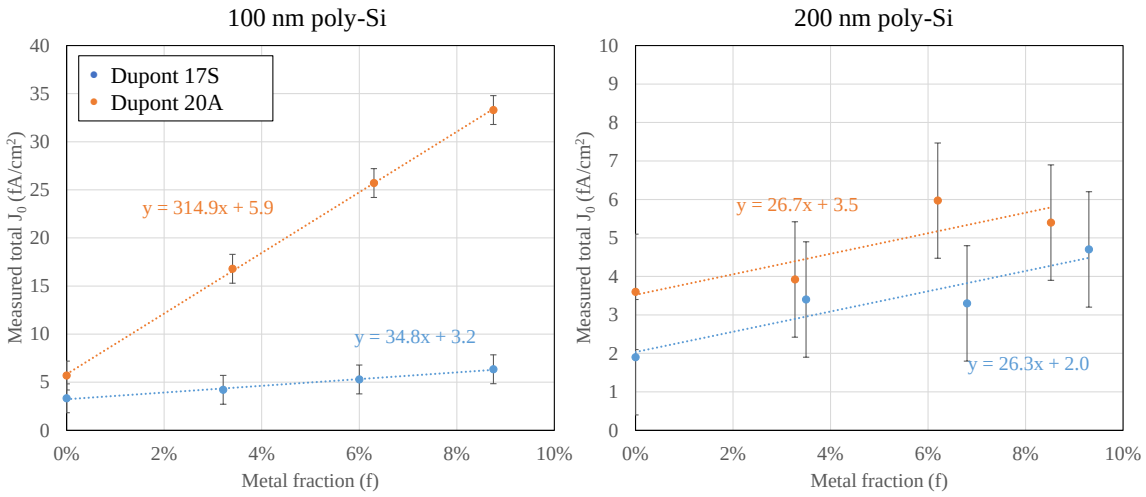


Figure 75: Full area $J_{0,poly}$ with different metal coverage. The left column is for 100nm thick poly-Si, and the right column is for 200 nm thick poly-Si.

Figure 75 shows that without any metal, the intercept or total J_0 (=2 × $J_{0b',pass}$) is ~2-6 fA/cm^2, which corresponds to a $J_{0b',pass}$ of ~1-3 fA/cm^2, indicating excellent passivation quality of our SiN_x capped unmetallized n-TOPCon after the simulated contact firing. However, total $J_{0b'}$ after metallization did show a slight increase with increased metal

fraction as indicated by the slope. Table 12 summarizes the metallized $J_{0b',metal}$ values and contact resistivity of the two Ag metal pastes investigated in this study on 100 and 200 nm thick poly-Si TOPCon structures. Ag paste 17S gave full area $J_{0b',metal}$ 0f ~30 fA/cm^2 for both 100 and 200 nm thick poly-Si, which corresponds to a total metallized $J_{0b'}$ of 5 fA/cm^2 (= 30 × 13.5% + 1 × 86.5%) for 13.5% back metal coverage (60 μm wide 300 grid lines with five busbars) designed for the bifacial solar cells. This study also reveals that selection of metal paste is very important for thinner poly-Si (100 nm because full area $J_{0b',metal}$ increases sharply to 316 fA/cm^2 for paste 20A. This corresponds to a total metallized $J_{0b'}$ of ~40 fA/cm^2 with ~13% back metal coverage, which is unacceptable for 23% cell efficiency.

Table 12 shows that we can obtain acceptable contact resistivity (< 5 mΩ-cm^2) and metallized J_0 (~5fA/cm^2) with 13% metal coverage on 200 nm thick poly with both metal pastes and a firing cycle that peaks at 775 ℃ temperature. Modeling in Figure 35 and Figure 36 showed that if J_0 and contact resistivity requirements are met simultaneously, then it is possible to get to 23% efficiency target. Note that in the case of thinner poly (100 nm), paste 17S will fail because of high contact resistivity and paste 20A will fail because of high metallized J_0 for this firing scheme. Since paste 20A gave slightly lower contact resistivity than 17S. Therefore, we decided to use paste 20A on rear n-TOPCon with 200 nm thick poly-Si for cell fabrication to satisfy the requirements of J_0 and contact resistivity simultaneously.

Table 12: Contact resistivity of different silver paste (fired at 775 ℃) on LPCVD poly and the poly sheet resistance with 100 nm and 200 nm thick poly-Si.

	100nm poly-Si			200 nm poly-Si		
Paste	$J_{0,metal}$ (100%) [fA/cm^2]	Contact resistivity - R_c [mΩ-cm^2]	Poly sheet resistance - R_{sh} [Ω/□]	$J_{0,metal}$ (100%) [fA/cm^2]	Contact resistivity - R_c [mΩ-cm^2]	Poly sheet resistance - R_{sh} [Ω/□]
Dupont 17S	~36	~7	~64	~27	~3	~37
Dupont 20A	~317	~4		~29	~2	

6.1.6 Process Development for Large Area Bifacial Screen-Printed Si Solar Cells with Rear Side LPCVD Grown TOPCon and Ion-Implanted Boron Emitter

In the previous section, we demonstrated the excellent passivation quality of our unmetallized and metallized LPCVD n-TOPCon structure. Since LPCVD grows poly-Si layers on both sides, and a single side etching tool was not available in this study, we developed a process using two masking layers to etch poly-Si from the front side. The cell fabrication process and the schematic diagram of the finished cell are shown in Figure 76 and Figure 77. We started with commercially available 200 μm thick industrial size (239 cm^2) 2 Ω-cm n-type Si Cz wafers with as-grown bulk lifetime of 1-2 ms. The wafers were subjected to saw damage removal etch and texturing, followed by boron implantation on the front side and 1050 ℃ / 30 minutes anneal, which resulted in a 180 Ω/□ boron emitter. Then, a 100 nm thick PECVD SiN mask was deposited on the front side to planarize the back. After an acid clean, a ~15Å tunnel oxide layer was grown by nitric acid oxidation at 100 °C for 10 minutes followed by LPCVD a-Si/poly-Si deposition at 588 ℃ in a tube furnace with in-situ phosphorus doping. Since doped poly is deposited on both sides, the

poly-Si on the backside was protected by depositing another 100 nm PECVD SiN_x masking layer, prior to front poly-Si removal by wet etching in a KOH solution. After the KOH etching, both front and back SiN_x masks were removed by HF etching. The samples were then annealed at 875 °C for poly-Si crystallization and dopant activation. After that, the front boron emitter was passivated by 100 Å ALD Al_2O_3 and 600 Å PECVD SiN_x stack, and the back poly-Si was passivated by 750 Å PECVD SiN_x. Finally, 50 µm wide 100 grid lines were screen-printed on the boron emitter side using Ag/Al paste, and Ag dots were screen-printed on the rear SiN_x/TOPCon and co-fired at 775 °C. The Ag dots had a diameter of ~120 µm and pitch of 400 µm, which is equivalent to ~9% metal coverage or metal-Si contact fraction.

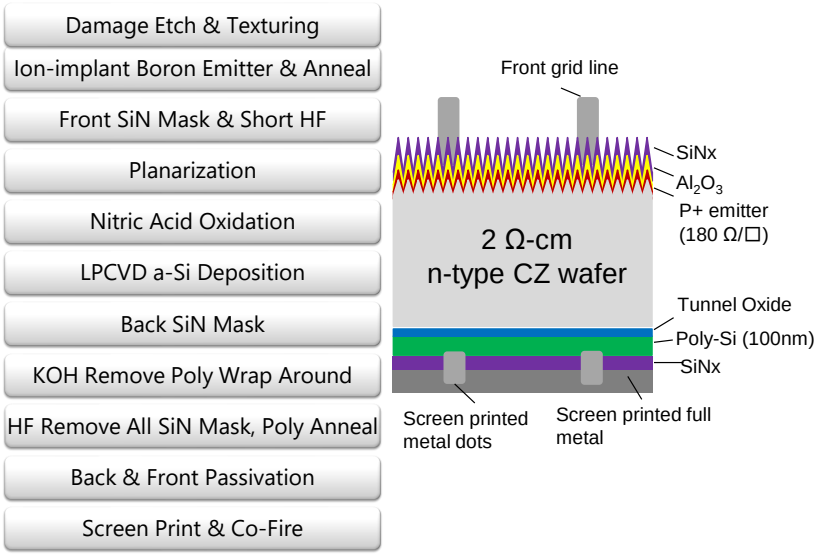


Figure 76: Schematic diagram of the cell process sequence and structure of the first 21.6% screen-printed TOPCon solar cell fabricated in this study.

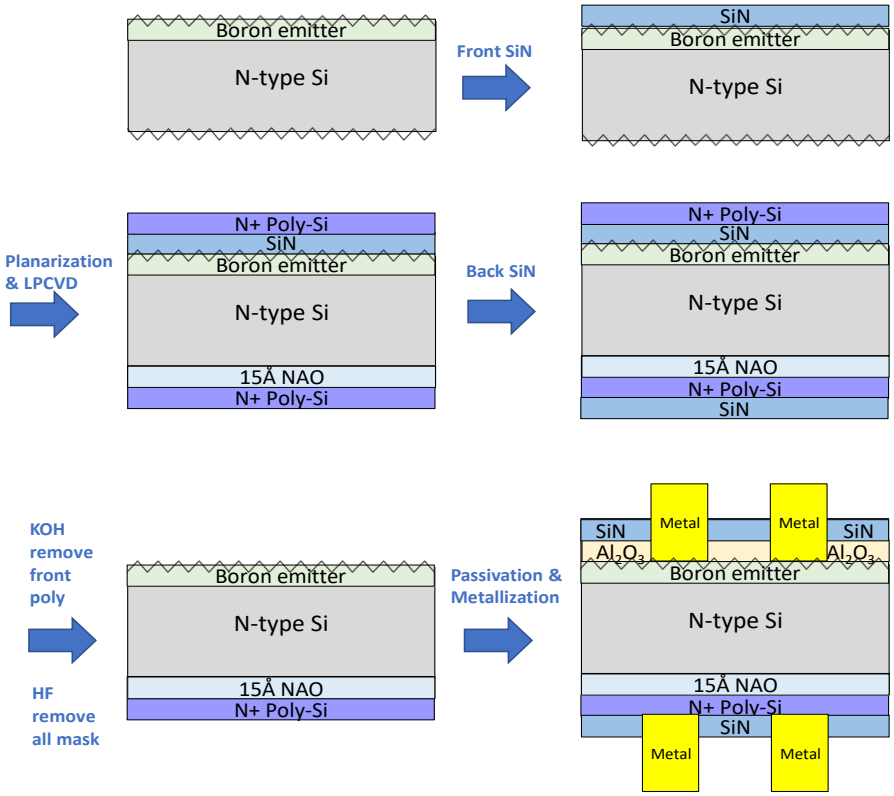


Figure 77: Schematic diagram of LPCVD TOPCon formation and metallization after processing of front B emitter wafer.

Table 13 shows the light IV data of a 21.6% cell (239 cm^2) achieved initially in this research with V_{OC} of 676mV, J_{SC} of 39.7 mA/cm^2, and FF of 80.4%. The measured light I-V curve is also shown in Figure 78. This cell confirmed the functionality of n-TOPCon, but its efficiency was low because of the absence of optimized B emitter and advanced screen printing developed in the previous chapters. This cell was characterized and modeled to understand the loss mechanisms followed by implementation all other technology enhancements to achieve ~23% efficiency in the following chapters.

Table 13: Measured illuminated I-V curve properties of 21.6% screen-printed TOPCon cell.

Area	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)	R_S (Ω-cm^2)	R_{SH} (Ω-cm^2)
239 cm^2	676	39.7	80.4	21.6	0.55	6090

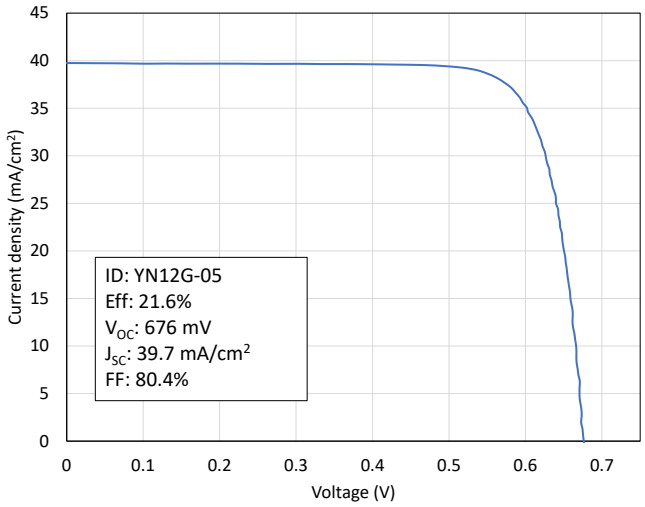


Figure 78: Measured current-voltage curve of 21.6% the first n-TOPCon cell in this study.

6.2 Summary

In this task, a high-quality n-TOPCon was developed with unmetallized J_{0b}, of ~2 fA/cm^2 and metallized J_{0b}, of ~5 fA/cm^2 with ~10% metal coverage. First a 15 Å tunnel oxide was grown on the back of a commercial grade n-type Cz Si wafers by nitric acid oxidation at ~100 ℃ followed by deposition of optimized phosphorus-doped polysilicon to form the n-TOPCon. This TOPCon was then capped with 750 Å PECVD SiN to facilitate

the formation of screen-printed Ag contacts, which were fired through SiN. Since low-pressure chemical vapor deposition (LPCVD) was used to deposit doped poly-Si at < 600 ℃ on top of the tunnel oxide, a high temperature anneal at 875 ℃ was performed to crystallize and activate dopants in poly-Si. Since LPCVD poly film grows on both sides of the wafer, a dielectric masking process was developed to obtain planar n-TOPCon only on the rear side. Poly-Si deposition conditions, thickness, doping, and annealing conditions were optimized in combination with screen-printing metal paste and firing conditions to minimize metallized J_{0b}, and achieve our technology roadmap target value of ~5 fA/cm^2. In addition, required contact resistivity of < 5 mΩ-cm^2 was achieved for this TOPCon structure. A process sequence was developed to make initial TOPCon cells to validate the functionality of n-TOPCon. Initial cells were fabricated without implementation of optimized B emitter, screen-printed contacts, and floating busbars reported in the previous chapters, which resulted in a cell efficiency of only 21.6%.

CHAPTER 7. TASK 4: FABRICATION OF HIGH-EFFICIENCY (~23%) N-TOPCON SOLAR CELLS BY PROCESS DEVELOPMENT AND INTEGRATION OF ADVANCED TECHNOLOGIES

7.1 Fabrication of 239 cm^2 High-Efficiency Screen-Printed Bifacial N-TOPCon Cell with Homogeneous B Emitter

After developing all the individual technology enhancements consistent with the technology roadmap, we developed and optimized a process sequence to fabricate commercial size screen-printed bifacial n-TOPCon cells with efficiency of ~23%. Figure 79 shows the process flow and structure of the n-type bifacial cells fabricated with an implanted homogeneous B emitter on front and LPCVD grown n-TOPCon on rear side of large-area (239 cm^2) 2 Ω-cm n-type Cz wafers. Since LPCVD grows poly-Si on both sides of the wafer, we had to implement a masking process to etch poly-Si from the front side because we did not have the single side etching tool widely used in industry. This added couple of extra steps. Process sequence starts with standard saw damage etching in KOH, surface texturing and cleaning. After that, wafers received B ion implantation on the front side with an ion energy of 10 KeV and dose of 1.2e15/cm^2 followed by an annealing and oxidation process (Chapter 5) at high temperature (~1050 °C), resulting in sheet resistance of 170-180 Ω/□. After the removal of thermally grown oxide during implant anneal, a PECVD SiN_x was deposited on the front side as a mask to protect the emitter during back planarization and front poly-Si etching. A heated KOH treatment was used to planarize the

back because planarized back reduces J_0 value (Section 6.1.4). After an acid clean and HF dip, a ~15 Å tunnel oxide layer was grown by nitric acid oxidation (NAO) at 100 °C for ~10 minutes, followed by 200 nm LPCVD n^+ poly-Si deposition at 588 °C with in-situ phosphorus doping. Next, a PECVD SiN_x masking layer was deposited on back poly-Si, and then the front poly-Si was removed by wet etching in KOH solution. After that, both front and back SiN_x masking layers were removed by HF treatment. The samples were then annealed at 855 °C for poly-Si crystallization and dopant activation. The B emitter was then coated with 3 nm Al_2O_3 by atomic layer deposition (ALD) for field-induced surface passivation followed by 450/920 Å PECVD SiN_x/SiO_x stack deposition for double layer anti-reflection coating. Next, the back poly-Si was capped with ~700 Å thick PECVD SiN_x layer for screen-printed contacts. For cells with non-floating busbars, 40 μm wide 106 grid lines in combination with 600 μm wide 5 busbars were screen-printed on B emitter using a fire through Ag/Al paste and single print. Front side metallization with floating busbars (FB) was done using dual-print to minimize the metallized J_{0e} by reducing the metal-Si contact area. For cells with floating busbars on emitter, the grid fingers were screen-printed first using the fire-through Ag/Al paste and then a fritless non-fire-through Ag paste was used to print the five busbars. Next, 60 μm wide 300 grid lines/600 μm wide 5 busbars were screen-printed on the rear n-TOPCon using fire-through Ag paste and single print. Finally, all samples were co-fired in an industrial-style belt furnace at peak firing temperature of 775 ±5 °C (Figure 68). Note that the second SiN_x masking step to remove front side poly-Si in our cell fabrication process can be eliminated by the single side etching tool used in industrial setting. Schematic of the process sequence and cell structure are shown in Figure 79 and the detailed process sequence is listed in Appendix B.

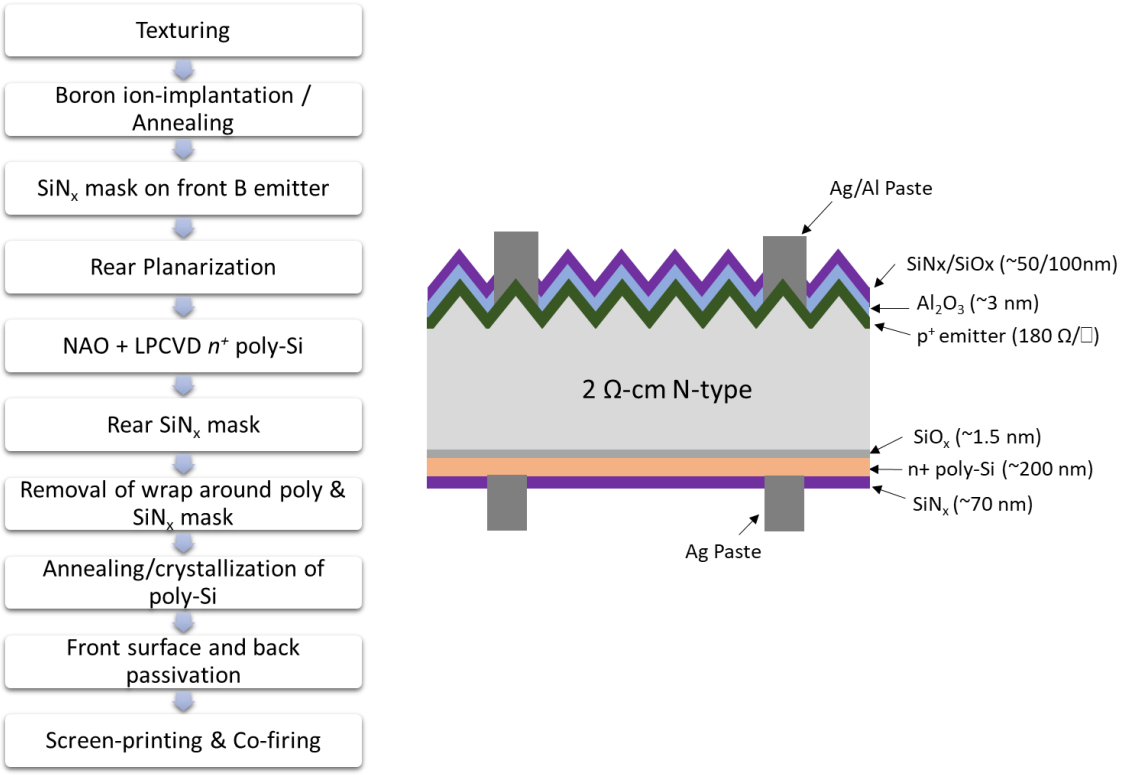


Figure 79: Process sequence and structure of the screen-printed bifacial N-type Si solar cell with front implanted boron emitter and rear tunnel oxide passivated contact.

Light I-V measurements were performed to assess the performance of these bifacial n-TOPCon cells under the 1000 W/m^2 AM 1.5G spectrum at 25 C. Figure 80 shows the light I-V curves, and Table 14 lists the key cell parameters extracted from light I-V measurements when the cells were illuminated from the front side. Cells were measured with respect to the Fraunhofer ISE certificated reference cell. The cell with fire-through busbars showed ~22% efficiency with V_{oc} of 687 mV, J_{sc} of 40.1 mA/cm^2, and FF of 79.7%. However, the cells with floating busbars showed ~15 mV higher V_{oc}, resulting in a V_{oc} of 702 mV and efficiency of ~22.6%. To the best of our knowledge, at that time this was among the highest cell V_{oc} on the large area (≥ 239 cm^2) single-side TOPCon cell with

homogeneous B emitter on n-type Cz wafer with industrial screen-printed fire-through metallization on both sides. Note that cells with and without the floating busbars gave similar FF (79.7%) even though floating busbar cell gave higher R_S due to reduced metal-Si contact, which was counterbalanced by slightly higher pFF for floating busbar cells (Table 14). Both cells showed reasonably high J_{SC} (> 40 mA/cm^2) due to high EQE, reduced reflectance from narrow lines and SiO_2/SiN_x two-layer AR coating on front. Since a bifacial cell can accept light from both sides, Table 15 shows the measured cell efficiency from the rear side with one sun illumination. Note that even with 13% metal coverage and planar back surface, rear side efficiency of this device is 16.6%. If the metal coverage was 5%, the efficiency would be 18.12%. Parasitic absorption on the rear side thick poly Si (200 nm) significantly reduced the performance during illumination from the rear side.

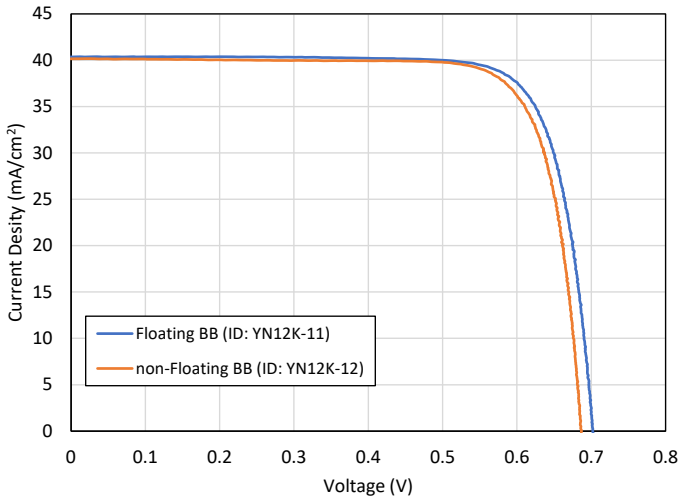


Figure 80: Light I-V curves of screen-printed, large-area n-TOPCon bifacial cells with non-floating and floating busbars.

Table 14: Measured I-V results of screen-printed, large-area n-TOPCon bifacial cells with non-floating and floating busbars.

Busbar	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]	n-factor	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]	pFF [%]
nFB	687	40.1	79.7	22.0	1.15	0.49	5520	82.0
FB	702	40.3	79.7	22.6	1.12	0.59	12800	82.7

Table 15: Measured I-V result of 22.6% floating busbar cell with illumination from the rear side.

Busbar	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]	n-factor	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]	pFF [%]
FB	691	30.8	77.9	16.6	1.17	0.56	8232	80.16

7.2 Fabrication of 100 cm^2 ~23% N-TOPCon Cells with Homogeneous B Emitter

With homogeneous B emitter and full area n-TOPCon on the rear, we achieved 22.6% efficiency, which is among the best for screen-printed single side bifacial TOPCon cells with 5 busbars (Table 3). However, detailed characterization showed that higher ideality or n-factor (n=1.12 instead of ~1.0) due to the edge leakage current contributed to some efficiency loss. Electroluminescence measurement in Figure 81 shows that edges light up when reverse bias is applied to the cell, indicating shunting or current leakage around edges [129]. This is also supported by sharp increase in current with increased reverse bias in Figure 82. Edge leakage may result from our wafer holders or some non-uniformity near the edges of such large area wafers in our deposition systems. High n-factor is known to reduce V_{OC}, FF and cell efficiency, therefore, an attempt was made to

fabricate somewhat smaller cells on the full size wafers to eliminate the edge effects and achieve higher efficiency.

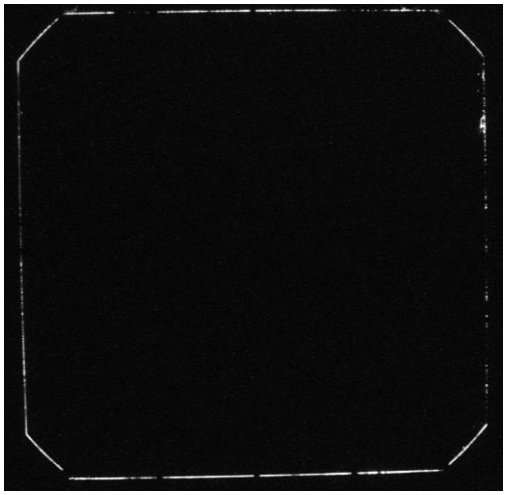


Figure 81: EL image of full area 239 cm^2 cell under reverse bias.

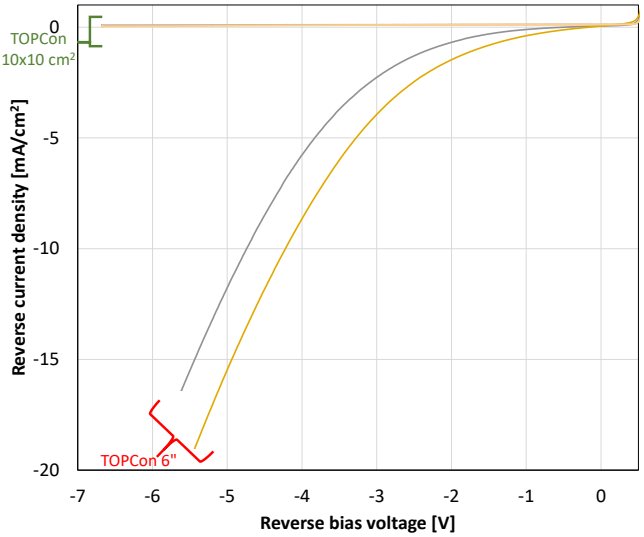


Figure 82: Comparison of reverse leakage current of laser isolated 100 cm^2 cell and full area 239 cm^2 cell.

In order to validate the above hypothesis, we fabricated 10 cm ×10 cm bifacial n-TOPCon cells with 120 Ω/□ and 170 Ω/□ ion-implanted B emitters on front and carrier-selective n-TOPCon contacts on the back of 2 Ω-cm ~200 μm thick 239 cm^2 n-type Cz wafers. Like in the case of 22.6% cell, we started with 239 cm^2 wafers followed by standard saw damage etching, texturing and cleaning. Then the wafers received 10 keV B ion-implantation on the front side with two different doses of $1.2\times10^{15}/cm^2$ and $2.0\times10^{15}/cm^2$ followed by our standard annealing at 1050 ℃ for 1 hour in N_2 ambient and 30 min in oxygen ambient, which resulted in emitter sheet resistances of 120 Ω/□ and 170 Ω/□, respectively. Next, 10 cm × 10 cm region was laser isolated, but was not removed from 6-inch pseudo square wafer to form 100 cm^2 cell on each wafer without the edge effects. The laser damage was removed by a 60 ℃ 10 minutes KOH treatment during which the emitter was protected by the thermal oxide grown during the post-implant anneal. After the removal of thermal oxide, same n-TOPCon structure was fabricated on the rear side by growing a 15 Å thick chemical oxide in HNO_3 solution followed by LPCVD growth of ~80 Ω/□ ~200 nm n^+ poly-Si. Similar to the 22.6% cell, the B emitter was then passivated by atomic layer deposition (ALD) of Al_2O_3 and PECVD SiN_x/SiO_2 stack while the back poly-Si was capped with ~700 Å thick PECVD SiN_x layer. Because of the smaller cell size, contact design was reoptimized using our grid model, and 40 μm wide 70 metal gridlines with only three busbars (total metal coverage ~3.8%) were screen-printed on the emitter side while 200 grid lines with three busbars (total metal coverage ~13%) were printed on the rear side (Figure 83). Front and back contacts were then co-fired with peak firing temperature of 775 ℃ and tested under AM 1.5G illumination. Cell image of laser isolated 10×10cm on 6 inch wafer is shown in Figure 83. Table 16 shows the data for the small area

n-TOPCon solar cells fabricated with 120 and 170 Ω/□ homogeneous B emitters. Consistent with the roadmap and model calculations (Figure 31, Table 5), without the edge leakage effect, 22.9% efficient fully screen-printed cells were achieved with both 120 and 170 Ω/□ homogeneous emitters.

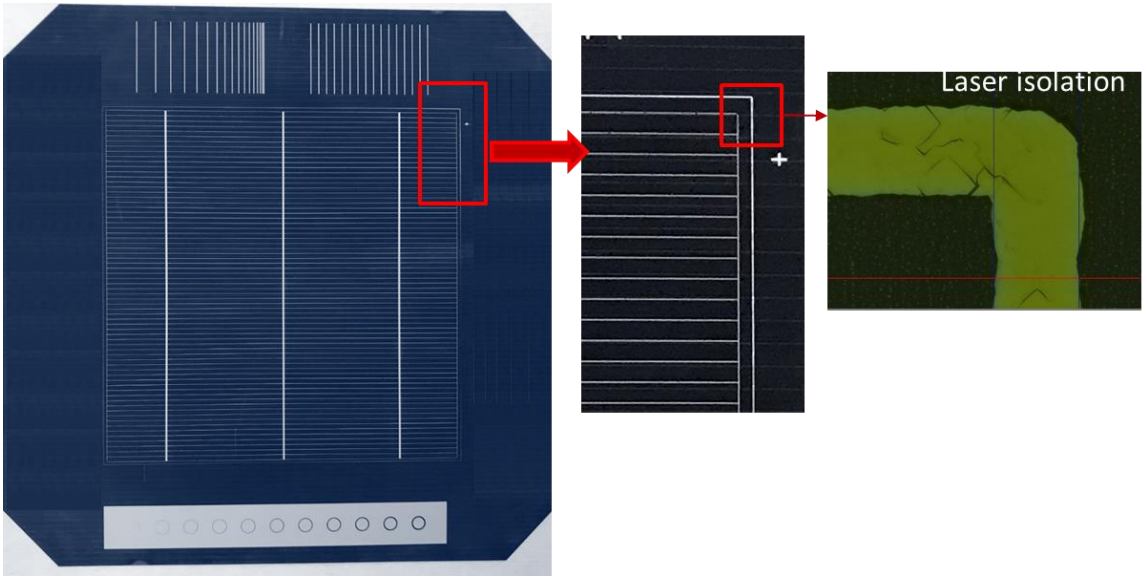


Figure 83: Cell image of 10×10 cm on 6-inch wafer with laser isolated edge.

Table 16: Light I-V measurement results of n-TOPCon solar cells with 170 Ω/□ and 120 Ω/□ implanted B emitters.

Boron emitter R_{sheet}	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Eff [%]	n-factor	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
170 Ω/□	693	40.9	80.7	22.9	1.04	0.47	7590
120 Ω/□	694	40.9	80.6	22.9	1.09	0.43	13900

7.3 Modelling the Impact of Selective Emitter, Improved Contacts and Higher Bulk Lifetime to Estimate the Efficiency Potential of ~23% Single-Side N-TOPCon Cells Fabricated in This Study

This section shows how the cell efficiency of ~23% cell fabricated in this research can be raised to 25% by implementing selective emitter in combination with improved contacts and higher bulk lifetimes reported in the literature. First the potential benefit of selective emitter alone is quantified and then the combined effect of the three advanced technologies is modeled.

Selective emitters (Figure 84 (b)) are often used in research and industry where a heavy diffusion in done underneath the metal grid to shield metal induced recombination by the field effect. In addition, much lighter diffusion is used in the field region, between the grid pattern, to reduce the recombination in the unmetallized or passivated region. Since metal contacts are formed on heavily doped region, contact resistance is lower, which can give higher FF to further improve the efficiency. The above ~23% cells were fabricated with 120-170 Ω/□ homogeneous B emitters which also introduces higher contact resistance. Even though selective emitter cells were not fabricated in this study, an attempt was made to quantify the potential efficiency gain from selective emitter on these cells by a combination of characterization and modelling. First, we characterized and modeled the 22.9% fabricated cell and then extended model calculations to predict the efficiency enhancement by replacing the 170 Ω/□ homogeneous emitter with 48/170 Ω/□ implanted p^{++}/p^{+} B selective emitter cell (Table 17). This was done by using the Sentaurus device model. Figure 85 shows the unit cell configuration for both homogeneous and selective emitters used in this model. Note that Contact resistivity, $J_{0e,pass}$ and $J_{0e,metal}$ values for the

implanted heavily-doped 48 Ω/□ emitter (p^{++} region) were taken from Task 2 (Figure 59). All the relevant input parameters used in modeling of the selective emitter cell are highlighted in Table 17, which revealed a gain of only ~0.2% in efficiency over the homogeneous emitter cell fabricated in this study.

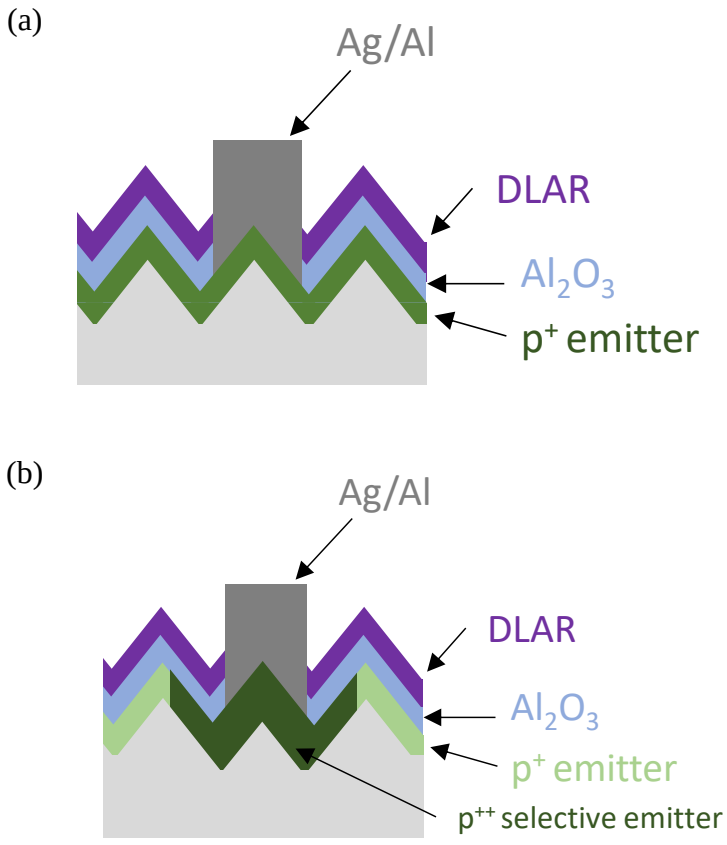


Figure 84: Schematic diagram of (a) homogeneous emitter and (b) selective emitter.

Table 17: Sentaurus Device modeling results and input parameters for the TOPCon cells with homogeneous 170 Ω/□ B emitter and selective B emitter.

Parameters	170 Ω/□ homogeneous boron emitter with Paste B	48 / 170 Ω/□ Selective boron emitter with Paste B
Voc [mV]	698	700
Jsc [mA/cm^2]	40.9	40.8
FF [%]	79.9	80.7
Efficiency [%]	22.8	23.0
Cell size (cm^2)	100	100
Front finger width W_f (μm)	40	40
Front shading/metal contact coverage	3.7%	3.7%
Busbar number / width (μm)	3 / 300	3 / 300
Wafer Thickness (μm)	180	180
Front Contact Resistivity (mΩ-cm^2)	5	0.1
Selective emitter sheet resistance (Ω/□)	N/A	48
Selective emitter junction width (μm)	N/A	200
Substrate resistivity (Ω-cm)	2	2
Substrate doping (cm^{-3})	2.38×10^{15}	2.38×10^{15}
Front passivated FSRV (cm/s)	297	297
Wing FSRV (cm/s)	NA	5366
Front contact FSRV (cm/s)	10^7	10^7
Lifetime (ms)	1	1
Back Contact Resistivity (mΩ-cm^2)	2	2
Back contact hole SRV at n+ Si/tunnel oxide interface (cm/s)	328	328

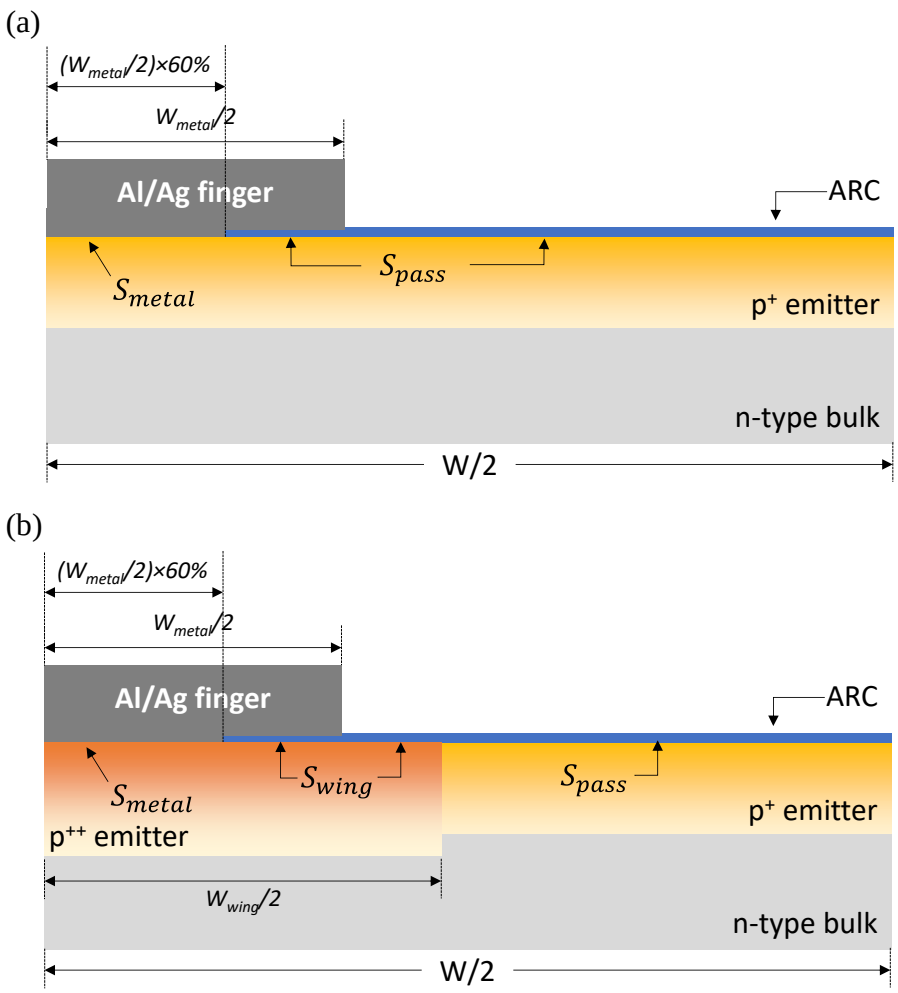


Figure 85: Unit cells in Sentaurus Device modeling for (a) Homogeneous emitter with paste B (b) Selective B emitter with Paste B.

Next, we modeled the impact of adding improved contacts (finer grid lines with busbarless contact) and higher bulk lifetimes (5-20ms) which have already been achieved and reported by some investigators. A new technology roadmap in Figure 86 was developed by device modeling which shows that this cell design with single side rear TOPCon has the potential to achieve 24-25% efficiency with the above three practically achievable and commercially viable technology enhancements.

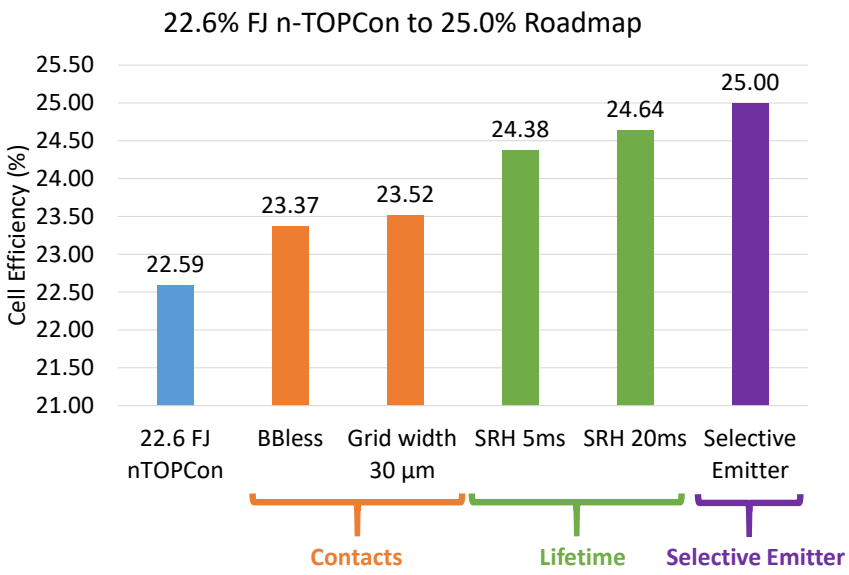


Figure 86: Roadmap to 25.0% efficiency with single-side TOPCon on rear side.

According to Figure 86, if we implement more advanced scree-printed contacts with 30 µm wide grid lines [130] in combination with busbarless contacts (a new industry standard used by several research institutes, which ignores shading from external busbars [131-134]), our 22.6% cell efficiency will rise to 23.5%. This is because of reduced shading, smaller metal-Si contact area, and reduced busbar to busbar spacing or resistance. The second technology enhancement involves 15-20 ms bulk lifetime in n-base material, compared to ~1 ms lifetime in our current cells, which has been also been reported by few investigators in starting material as well as finished n-base cells [87]. These two modifications will raise the efficiency to 24.6%. Finally, replacing our homogeneous B emitter with a p^{+}-p^{++} selective emitter with full area $J_{0e,metal}$ = 210 fA/cm^2 with contact resistivity ~1 mΩ-cm^2, compared to 706 fA/cm^2 and 3 mΩ-cm^2 in our current

homogeneous emitter cell, will raise the cell efficiency to ~25.0%. Table 18 summarizes all the relevant input parameters required to attain 25% efficiency from this cell design.

7.4 Summary

In this task we achieved screen printed 239 cm^2 n-TOPCon bifacial cells with efficiency of 22.6%. Modeling and analysis showed slightly higher n-factor (~1.1) because edge leakage effects lowered the FF and efficiency. To eliminate the edge effects, we fabricated 10×10 cm cell within the 6-inch pseudo square wafer by laser isolation and modified the grid design with three busbars for the 100 cm^2 cells. This resulted in 22.9% efficiency, entirely consistent with our technology roadmap for homogeneous B emitters. Based on the experimental and theoretical understanding developed in this research, we extended model calculations to establish a new roadmap to ~25% cell efficiency n-TOPCon cells which involves practically achievable and commercially viable busbarless contacts, higher bulk lifetime ($\geq$ 5 ms) and selective emitter.

Table 18: Quokka 2 modeling results and input parameters for the roadmap from 22.6% to 25%.

Parameters	22.6% n-TOPCon	Busbar-less	Grid width 30 µm	SRH 5ms	SRH 20 ms	Selective emitter
Voc [mV]	704	705	708	713	715	719
Jsc [mA/cm^2]	40.3	41.2	41.4	41.5	41.5	41.5
FF [%]	79.4	80.4	80.0	82.2	82.9	83.7
Efficiency [%]	22.59	23.37	23.52	24.38	24.64	25.00
Cell size (cm^2)	239	239	239	239	239	239
Front finger width W_f (µm)	40	40	30	30	30	30
Front shading coverage	4.49%	2.56%	1.92%	1.92%	1.92%	1.92%
Front metal contact coverage	2.56%	2.56%	1.92%	1.92%	1.92%	1.92%
Busbar number / width (µm)	5/600	0/0	0/0	0/0	0/0	0/0
Wafer Thickness (µm)	170	170	170	170	170	170
Front Contact Resistivity (mΩ-cm^2)	3	3	3	3	3	0.8
Selective emitter sheet resistance (Ω/□)	NA	NA	NA	NA	NA	30
Selective emitter junction width (µm)	NA	NA	NA	NA	NA	100
Substrate resistivity (Ω-cm)	2	2	2	2	2	2
Front passivated J_0 (fA/cm^2)	12	12	12	12	12	12
Wing J_0 (fA/cm^2)	NA	NA	NA	NA	NA	90
Front contact $J_{0,metal}$ (fA/cm^2)	706	706	706	706	706	210
Bulk SRH Lifetime (ms)	1.2	1.2	1.2	5	20	20
Back Contact Resistivity (mΩ-cm^2)	2	2	2	2	2	2
Rear passivated J_0 (fA/cm^2)	1	1	1	1	1	1
Rear contact $J_{0,metal}$ (fA/cm^2)	30	30	30	30	30	30
Rear contact percentage	13.5%	13.5%	13.5%	13.5%	13.5%	13.5%

CHAPTER 8. TASK 5: MODELLING AND UNDERSTANDING OF > 25% REAR JUNCTION DOUBLE-SIDE PASSIVATED CONTACT SOLAR CELLS WITH SELECTIVE AREA TOPCON ON FRONT

The screen-printed, large-area single-side n-TOPCon bifacial cells fabricated in the previous task achieved 22.6% efficiency on 239 cm^2 wafers and 22.9% efficiency on 100 cm^2 cell area. Detailed cell analysis and modelling showed that due the very low metallized recombination current density J_{0b}, of ~5 fA/cm^2 on the rear TOPCon with 13% metal coverage, the boron emitter and metal-induced recombination on the front (metallized J_{0e} = 30 fA/cm^2) becomes a major efficiency limiting factor in these cells. One possible solution is to replace B emitter by p-TOPCon structure on the front side. However, poly-Si layer on the front side acts as a strong light absorber, which will significantly decrease the J_{SC} and cell efficiency because currently thicker poly-Si ($\geq$ 100 nm) layers are needed to avoid degradation and metal penetration during screen-printed metallization. To minimize parasitic absorption in poly-Si and enable the use of thicker poly-Si on front to mitigate the traditional screen-printed contact-induced degradation, a new rear junction device structure is proposed in this task to achieve > 25% efficient industry-compatible rear junction solar cell. This cell design has full-area p-TOPCon on the rear side of a n-type wafer but selected area (6.4%) thick n-TOPCon on the front only under the front grid pattern (selective TOPCon) to avoid appreciable absorption in the front poly-Si as well as contact induced degradation. Because of the grid alignment challenge to poly-Si fingers, the proposed cell design has wider poly-Si TOPCon fingers (~100 μm) compared to the

grid width (~40 μm). Device modelling is performed to establish the efficiency potential of this cell design using practically achievable material and device parameters and provide guidelines for future research in this area.

The proposed small area coverage (6.4%) by the poly-Si fingers, this cell design (Figure 88) enables the use of thicker TOPCon (> 100nm) on the front without incurring metal-induced damage and high parasitic absorption loss. Modelling showed that for the proposed rear junction design with appropriate bulk lifetime and resistivity combination eliminates the need for any heavy doping in the front field region between the grid lines because carriers can flow through the bulk Si to front grid contacts without introducing appreciable resistance or FF loss. High V_{OC} is achieved because high-quality undiffused Si surface passivation by dielectric stacks, like Al_2O_3/SiN, in the field region can give J_0 comparable to the TOPCon without any absorption in the dielectrics. Our device modeling establishes the practically achievable properties and parameters for each region, including full area rear p-TOPCon, selective area front n-TOPCon, bulk Si properties and contacts, to achieve > 25% efficiency screen-printed bifacial rear junction selective TOPCon cells.

8.1 Literature Review on Double-Side TOPCon Solar Cells

Very little work has been published on modeling and fabrication of practically achievable double-side or selective-area TOPCon cells. This task explores the possibility of using TOPCon on both sides of the Si wafer by incorporating selective-area thick TOPCon (~ 100 μm wide) underneath the front grid to minimize parasitic absorption and eliminate screen-printed contact-induced degradation of passivation quality. Larionova et al [135] achieved 728 mV V_{OC} on a finished cell with full area TOPCon on both sides

(Figure 87) but reported a significant loss in short-circuit current density due to parasitic absorption even with the very thin (10-12 nm) full-area poly-Si layer on the front side, resulting in only 22.3% efficiency. Also, due to the very thin poly-Si used on the front, the metallization was limited to low temperature processes to prevent metal punch-through during high-temperature firing process, which increases the manufacturing costs and limits cell performance. Young et al [136] attempted to fabricate selective area TOPCon cells by reactive ion etching (RIE) of the passivated field region with metal grid fingers serving as etch masks. However, they reported loss of performance due to non-uniform etching and RIE induced degradation of surface passivation. Attempts have also been made to fabricate selective area TOPCon using shadow masks for deposition of poly [137] and lithography-defined [138] patterns, but they are not industrially compatible. Therefore, in this task, we have performed 2D device modeling to establish the cell design including all the practically achievable material and device parameters, that can or have been achieved using industrial processes, to achieve >25% efficient manufacturable screen-printed rear junction bifacial cell with selective TOPCon on front.

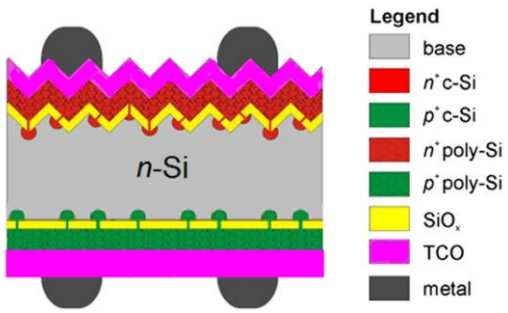


Figure 87: Schematic drawing of a full-area double-side contacted TOPCon solar cell with TCO and low-temperature Ag screen-print metallization on both sides (adapted from [135]).

8.2 Modeling and Understanding of Proposed Rear Junction Cell Structure on N-Base with Selective Area Front TOPCon

8.2.1 Proposed Structure of Rear Junction Solar Cell with Selective Front TOPCon

Figure 88 shows the schematic diagram of the proposed double-side TOPCon solar cell with selective n-TOPCon on the front side and full area p-TOPCon on the rear side. The selective TOPCon on front side can be fabricated with several industry-compatible patterning techniques involving wet etching in combination with protecting poly fingers by and screen-printed or inkjet-printed pastes that can serves as mask for etching poly in the field region, similar to the procedure for the formation of selective diffused emitter [139]. To achieve this proposed cell design, full area front and back TOPCon regions can be first formed on the planar (100) surfaces instead of the traditional (111) textured surfaces to minimize J_0 [55, 140]. Since lateral charge carrier transport on front takes place through Si bulk, it eliminates the need for any heavy diffusion in the field region between the grid. This desensitizes cell efficiencies with respect to front sheet resistance [43, 141] and allows the application of selective area TOPCon structure on the front with high quality dielectric passivation of bare Si wafer in the field region (Figure 88).

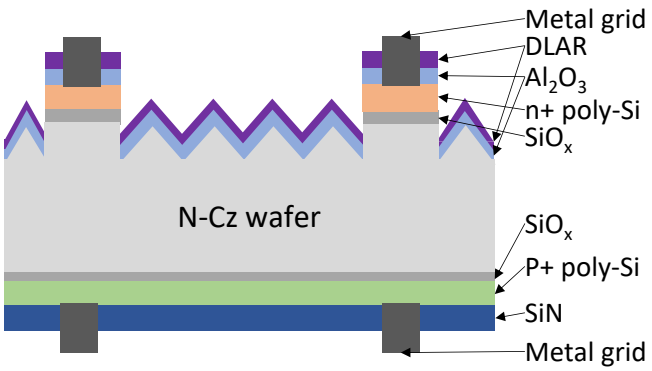


Figure 88: Schematic diagrams of double-side TOPCon solar cell with selective area TOPCon the front side.

8.2.2 Optical Simulation of Absorption Loss as a Function of Thickness of Full-Area and Selective TOPCon on the Front

The optical simulator OPAL 2 [142] is used in this study to simulate the parasitic light absorption loss in the poly-Si fingers on the front side. The wavelength-dependent refractive index and extinction coefficient for poly-Si are extracted from [143, 144]. Practically achievable 1.56 mm pitch for 40 μm wide screen-printed metal grid lines on top of 100 μm wide selective TOPCons fingers are assumed in these simulations, which results in 3.85% selective TOPCon area on the front that is not shaded by 40 μm wide metal grid lines and can contribute to absorption loss in poly-Si.

In order to quantify the benefit of using thick selective TOPCon on front instead of full area thin TOPCon, we simulated loss in J_{SC} as a function of poly thickness for both full-area and proposed selective TOPCon structures on the front side (Figure 89). To the best of our knowledge, the thinnest reported screen-printed TOPCon without appreciable

degrading in J_0 is ~40 nm [75], however, our modeling in Figure 89 shows that even at this thickness, full-area TOPCon will result in > 2mA/cm^2 current loss. Figure 89 also shows that the proposed selective thick TOPCon structure on the front will not only reduce the current loss to < 0.3 mA/cm^2 but will also allow the use of ≥ 100nm poly-Si layer to avoid metal-induced degradation of J_0. This should increase both V_{OC} and J_{SC}.

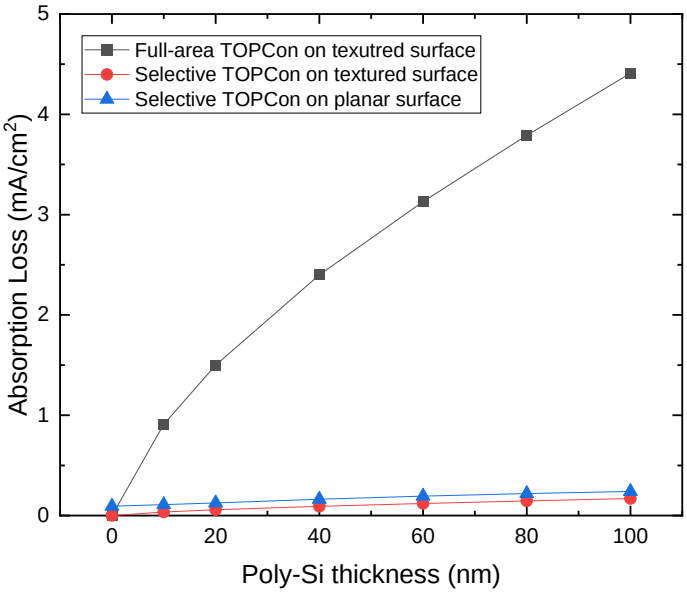


Figure 89: Simulated absorption loss from the front poly-Si as a function of front poly-Si thickness. Selective poly-Si is simulated by assuming that 3.85% of area is covered by poly-Si and not shaded by metal contacts.

8.2.3 Simulation of Efficiency Potential of Proposed Selective TOPCon Cell Design

In order to assess the efficiency potential of the proposed rear junction bifacial selective TOPCon cell, 2D device simulations were performed with Quokka 2 [79] with full area rear p-TOPCon on the back side and selective thick n-TOPCon on the front. The details of all the practically achievable input parameters are summarized in Table 19

starting with 23% baseline cell to >25% advanced cells. The baseline cell represents the current measured values of J_0, bulk lifetime and contacts parameters on n and p-TOPCon in our lab [68, 145], and the advanced cell simulation is performed using the best reported parameters in the literature to date to the best of our knowledge. Note that six parameters, shown in red, in Table 19 are changed to simulate the advanced cell. These parameters have been achieved and reported in the literature and their corresponding reference is also shown in Table 19. These six altered parameters include 1) reduction in passivated J_0 value of n-TOPCon from 1 to 0.4 fA/cm^2 2) reduction in metallized full area n-TOPCon J_0 from 30 to 24 fA/cm^2 3) increase in bulk lifetime from 1 to 20 ms 4) reduction in full area passivated p-TOPCon J_0 from 4.6 to 1 fA/cm^2 5) reduction in front contact resistivity from 2 to 0.5 mΩ-cm^2 and 6) reduction in rear contact resistivity from 3 to 2 mΩ-cm^2 Since most commercial cells currently use floating busbars but more advanced busbarless cells are recently being attempted and reported, we have simulated both screen-printing schemes for baseline and advanced cells: (1) 600 μm wide 5 floating busbars and (2) busbarless cell which are tested with external multiple narrow conductive wires that act like busbars but shading from the wires is neglected in efficiency calculation [131]. Table 19 summarizes the cell simulation results (V_{OC}, J_{SC}, FF and efficiency) along with all the important input parameters and their corresponding references. Table 19 shows that the baseline selective TOPCon structure can currently achieve 23.1% efficiency with five floating busbars and ~23.9% efficiency with busbarless contacts. However, it has the potential to achieve commercially viable ~25.4% efficiency if we integrate the best reported J_0, lifetime and contact parameters in the literature. It is also important to note that this is only possible with the proposed rear-junction cell design which permits the use of Al_2O_3/SiN passivated

field region between the metallized thick poly fingers without introducing appreciable resistive losses. In addition, it eliminates the front poly-Si absorption or recombination in the heavily doped field regions. Based on our absorption loss calculations in Figure 89, even if a full area 40nm n-TOPCon is used on the front side, J_{SC} will drop by ~2.5 mA/cm^2, resulting in efficiency below 24%. Front poly thickness for full area double side TOPCon needs to be ~20 nm to achieve > 24.5% efficiency with the risk of screen-printed metallization induced damage to J_0 and FF. Back junction cell design with full area rear p-TOPCon and selective area front n-TOPCon can eliminate both the problems and achieve > 25% efficiency.

Table 19: Detailed parameters for Quokka 2 simulation.

	Parameter	Baseline		Advanced		References (Baseline/Adv.)
		5 Busbar	Busbarless	5 Busbars	Busbarless	
Cell Data	V_{OC} [mV]	715	716	729	730	
	J_{SC} [mA/cm^2]	40.5	41.3	40.9	41.8	
	FF [%]	79.5	80.6	82.1	83.2	
	Efficiency [%]	23.1	23.9	24.5	25.4	
	Total J_0 [fA/cm^2]	33	33	19	19	
Front Selective TOPCon	Front Poly Type	N		N		
	Selective area width [μm]	100		100		
	Front Poly thickness [nm]	200		150		
	Front field SRV [cm/s]	3.8		3.8		[146]
	$J_{0frontpoly,pass,100\%}$ [fA/cm^2]	1		0.4		[68]/[44]
	$J_{0frontpoly,metal,100\%}$ [fA/cm^2]	30		24		[68]/[147]
Bulk	Bulk Type	N		N		
	Bulk thickness [μm]	170		170		
	Bulk resistivity [Ω-cm]	1		1		
	SRH lifetime [ms]	1		20		[68]/[87]

Table 19 (continued)

Rear TOPCon	Rear Poly Type	P		P		
	Rear Poly thickness [nm]	250		250		
	Rear Poly sheet resistance [Ω/□]	200		200		In-house
	$J_{0rear,pass,100\%}$ [fA/cm^2]	4.6		1		[145]/[148]
	$J_{0rear,metal,100\%}$ [fA/cm^2]	112		112		[145]
Front grid	Number of lines	100		100		
	Pitch [mm]	1.56		1.56		
	Line thickness [µm]	40		40		
	Number of busbars	5	30	5	0	
	Metal coverage	2.56%		2.56%		
	Busbar contacts	Floating	Busbarless	Floating	Busbarless	
	Busbar width [µm]	600	0	600	0	
	Contact resistivity [mΩ-cm^2]	2		0.5		[68] /[147]
Rear grid	Number of lines	200		200		
	Pitch [mm]	0.52		0.52		
	Line thickness [µm]	40		40		
	Number of busbars	5	0	5	0	
	Metal coverage	7.69%		7.69		
	Busbar contacts	Floating	Busbarless	Floating	Busbarless	
	Busbar width [µm]	600	0	600	0	
	Contact resistivity [mΩ-cm^2]	3		2		[145]/[148]

8.2.4 Modelling the Impact of Si Bulk Material Properties on Cell Performance of Rear Junction Selective Front TOPCon Cell

Since the minority charge carriers are collected at the rear junction, the electrical quality (resistivity, mobility and lifetime) of the Si bulk absorber material becomes more important than in the case of front junction cells [141]. Therefore in Figure 90 we have generated a cell efficiency contour map by device modeling as a function of bulk resistivity

and SRH lifetime. It shows that any given target efficiency can be achieved with several lifetime and bulk resistivity combinations, but for a fixed SRH lifetime there is an optimum resistivity for achieving the highest cell efficiency, indicated by the white dashed line in Figure 90. The contour map suggests that > 25 % efficiency cannot be achieved for bulk lifetimes below 3 ms for this cell design but a base material with ≥ 3 ms lifetime and 0.6 Ω-cm bulk resistivity can exceed 25% efficiency. To further understand the loss mechanisms, advanced busbarless cell parameters were plotted as a function of bulk resistivity and SRH lifetime in Figure 91. Note that fill-factor in the rear-junction cells drops significantly when the bulk resistivity exceeds 0.7 Ω-cm, and the drop is more pronounced for a lower bulk lifetime. This is because both low resistivity and high lifetime are important for lateral charge carrier transport in Si bulk for the rear-junction design. Due to the intrinsic Auger recombination, V_{OC} and J_{SC} decrease appreciably when bulk resistivity falls below 0.4 Ω-cm (Figure 91 (c), (d)). The trade-off between lateral carrier transport (high FF) and low bulk Auger recombination (high V_{OC} and J_{SC}) results in an optimum bulk resistivity at a fixed SRH lifetime, indicated by the white dashed line in Figure 90. However, this trade-off becomes less significant at high lifetime as the efficiency curve becomes flatter, as shown in Figure 91 (a). This is because bulk conductivity is dictated by high injection level in high lifetime material rather than the initial resistivity. Model calculations in Figure 91 also show that for 0.8 Ω-cm n-type Si wafer with bulk lifetime approaching 20 ms, which has been reported by some investigators in Cz Si cells [85-87], efficiency of 25.4% can be achieved using the proposed selective TOPCon design with rear junction cell structure.

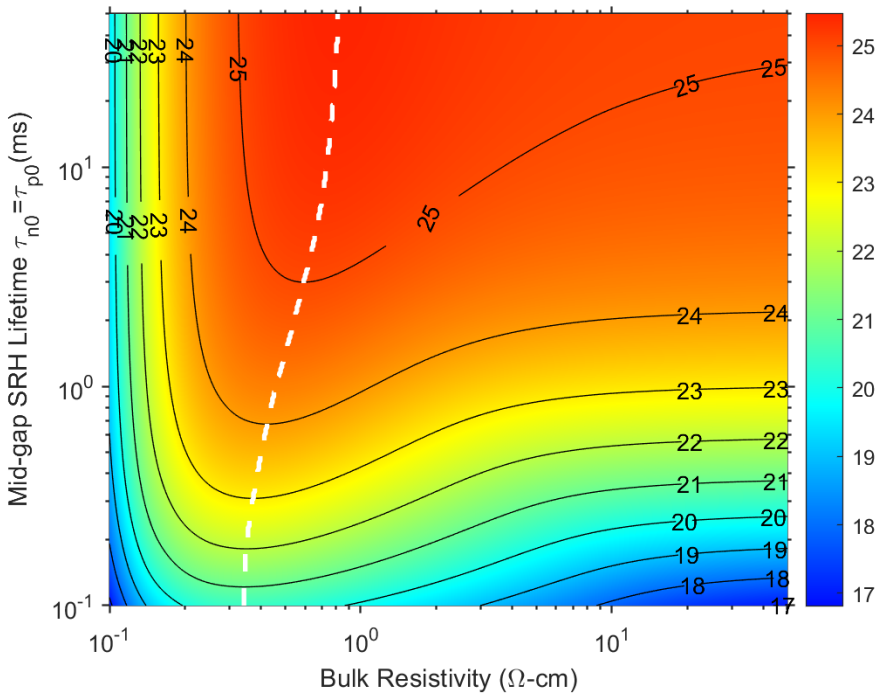


Figure 90: Efficiency contour map as a function of bulk resistivity and mid-gap SRH lifetime for the advanced busbarless selective TOPCon cell. The white dashed line corresponds to the optimum bulk resistivity that results in the highest cell efficiency at a given mid-gap SRH lifetime.

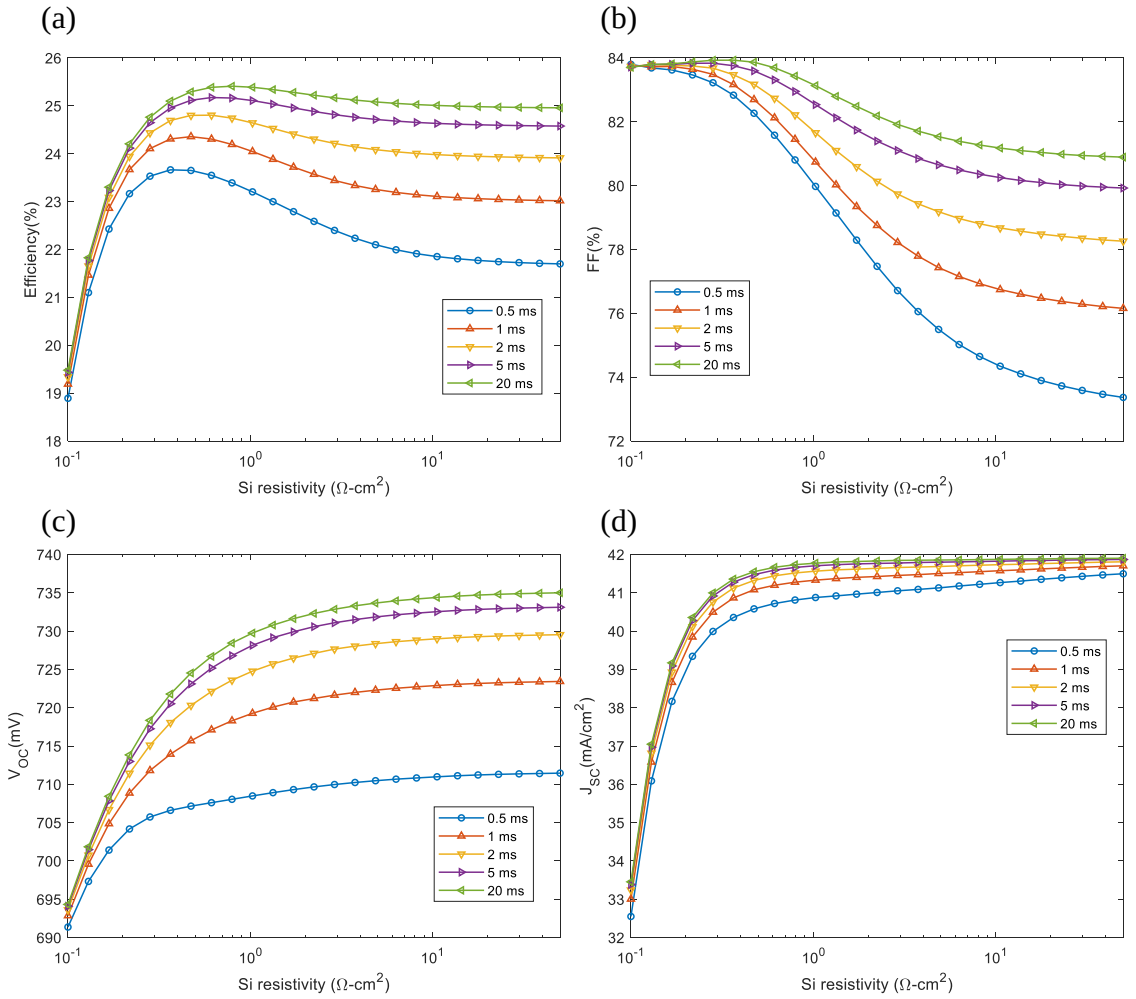


Figure 91: Efficiency and IV data of the rear-junction advanced busbarless cell in Table I as a function of Si bulk resistivity and SRH lifetime.

8.3 Summary

A quantitative understanding and efficiency potential of a screen-printed bifacial rear junction cell with selective TOPCon on the front is presented. This cell structure is composed of full area p-TOPCon on the rear and selective area n-TOPCon on the front side of an n-type Si wafer. Detailed modeling using practically achievable material and device

parameters shows that ~25.4% efficiency is achievable with this design using traditional screen-printing. This is because selective n-TOPCon on the front minimizes parasitic absorption and rear junction design allows the use of thicker poly under the front grid without the need for any diffusion in the field region. The undiffused field region is passivated with Al_2O_3/SiN coating to provide a J_0 comparable to TOPCon passivated Si surface without any absorption loss. Modeling reveals that this structure does not require any front diffusion because lateral conduction to the front grid takes place through Si bulk without appreciable resistive or FF loss. Because bulk material properties are very important for such a rear junction device, an efficiency contour map is generated through numerical modeling to show that a given target efficiency can be achieved by several combinations of bulk lifetime and resistivity. However, to achieve the highest efficiency for a fixed bulk lifetime, there is an optimum resistivity. For the proposed design and structure, bulk lifetime needs to be $\geq$ 3ms to achieve > 25% cell efficiency.

CHAPTER 9. CONCLUSIONS

9.1 Conclusions

In this dissertation, ~23% low-cost high-efficiency commercial ready bifacial screen-printed silicon solar cells have been developed by a combination of computer modeling, cell design, technology developments, cell fabrication and characterization. First, a technology roadmap to drive the efficiency of traditional 21% n-PERT cell to 23% was developed by establishing the properties and requirements for each layer or region of solar cells. This was accomplished through extensive 2D device simulations using advanced Sentaurus and Quokka 2 models. These models are used throughout this research to analyze the fabricated cells and understand the loss mechanisms. The technology roadmap involved identifying and quantifying necessary and practically achievable improvements in J_0, doping profile, contact resistivity and surface passivation of B emitter and rear n-TOPCon, lifetime and resistivity of bulk Si, optical properties of anti-reflectance, shading and contact parameters of the metal grid that can lead to 23% n-TOPCon cell efficiency. Recombination loss in each region was quantified by recombination current density $J_{0.}$ First, an ion-implanted B emitter was designed by profile engineering and advanced screen-printed metallization that can reduce metallized emitter recombination current density J_{0e} to ~30 fA/cm^2 compared to ~150 fA/cm^2 for our PERT cell. Next, it was shown by modeling that replacing full area N^+ back surface field (BSF) in the n-PERT cell with n-TOPCon can lower the metallized rear side recombination current density $J_{0b,}$ from ~120 fA/cm^2 to < 10 fA/cm^2. In addition, required bulk lifetime and resistivity combinations were established by modelling to minimize bulk

recombination (J_{0bulk}) and resistive losses that can produce J_{0bulk} of ~13-17 fA/cm^2. It was found that this can be achieved by 0.5-1 Ω-cm n-type Si material with a bulk lifetime of ~2 ms. Finally, design of antireflection coating as well as front and back metal contact grids were optimized using computer modeling to minimize reflection and metal-induced recombination losses. It was found that for our proposed 120-170 Ω/□ homogeneous B emitters and 60 Ω/□ rear n-TOPCon, 100-120 gridlines on front and 300 gridlines on the rear side will be optimum for the 5 busbar cells.

The technology roadmap showed that all the above improvements can reduce the total J_0 to ~50 fA/cm^2, compared to 315 fA/cm^2 in the starting n-PERT cell, and produce ~23% cell efficiency. This roadmap was used to guide the experimental work and validate the technology development. Each layer of the device was investigated and optimized individually, and then integrated into a process sequence to achieve the target efficiency.

In Chapter 5, ion-implanted emitters on textured Si surfaces were fabricated and characterized in the sheet resistance range of 48-200 Ω/□ by tailoring the implantation dose, energy, and annealing conditions. These emitters were passivated with Al_2O_3 and SiN dielectrics prior to contact formation. Nearly record low unmetallized J_0 values ($J_{0e,pass}$ < 15 fA/cm^2) were achieved in this study for R_{sheet} > 140 Ω/□. These emitters were metallized by screen-printing metal gridlines followed by rapid firing through the dielectric stack at ~770 °C. It was found that screen-printed contacts can increase or decrease the metallized J_0 compared to an evaporated metal contact interface. It was shown that Paste A increased the $J_{0e,metal}$ by 16% due to 0.13 μm etching of the emitter surface, while a more advanced Ag-Al paste B resulted in 40 % reduction in $J_{0e,metal}$ due to the significant fraction of unetched or undissolved dielectric islands under the metal grid that resulted in the

formation of local contacts. Consistent with our technology roadmap, we succeeded in achieving metallized J_{0e} of ~30 fA/cm^2 and contact resistivity of < 5 mΩ-cm^2 on 170 Ω/□ B emitter with 2.67% metal-Si contact area.

In Chapter 6, a high-quality n-TOPCon was developed with unmetallized $J_{0b'}$ of ~1 fA/cm^2 and metallized $J_{0b'}$ of ~5 fA/cm^2 with ~10% metal coverage which are close to the best values reported in the literature. First a 15 Å tunnel oxide was grown on the back of a commercial-grade n-type Cz Si wafers by nitric acid oxidation at ~100 ℃ followed by LPCVD deposition of optimized phosphorus-doped polysilicon to form the n-TOPCon. Poly-Si deposition conditions, thickness, doping, and annealing conditions were optimized in combination with screen-printing metal paste and firing conditions to achieve our technology roadmap target value of ~5 fA/cm^2.

In Chapter 7, a complete process sequence was developed to achieve screen-printed 239 cm^2 n-TOPCon bifacial cells with efficiency of 22.6%. Detailed analysis showed slightly higher ideality or n-factor (~1.1) due to edge leakage which lowered the FF and efficiency. To eliminate the edge effects, we fabricated 10×10 cm cell within the 6-inch pseudo square wafer which resulted in 22.9% efficiency. These are among the highest efficiency screen-printed cells with three to five busbars. Our modeling showed that busbarless contacts can improve the cell efficiency by ~0.7% by reducing shading and resistive losses, as recently reported by some investigators. In order to validate that and provide guidelines for future research, model calculations were extended to establish a new roadmap for achieving ~25% cell efficiency using this front junction single side n-TOPCon cell design. Simulations revealed that this can be accomplished by incorporating commercially viable busbarless contacts in combination with practically achievable higher

bulk lifetime (≥ 5 ms) Si wafers and boron selective emitter. Finally, a next-generation rear junction bifacial double-side TOPCon structure was proposed and modeled, involving full area p-TOPCon on the back and selective area n-TOPCon on the front. Detailed modeling showed that this structure can achieve ~25.4% efficiency with practically achievable material parameters and screen-printed contacts.

APPENDIX A INPUT FILES FOR QUOKKA 2 FOR SINGLE-SIDE N-TOPCON SOLAR CELL SIMULATION

Quokka 2 code to simulate the single-side n-TOPCon solar cell with advanced metallization in Chapter 4 (corresponding to bar 4 in Figure 31 and Table 5):

```
% Script Author: Ying-Yuan (Peter) Huang
% yingyuanhuang@gatech.edu
% N-TOPCon solar cells with advanced metallization


version.design='FRC';
lumi.enable=0; % switch luminescence on (1) or off (0)
optim.enable=0;


geom.dimensions=2; % set to 1, 2 or 3
geom.rearcont.position=[1];


geom.Wz=180; % [μm] thickness


% ==== Front Contact ====
geom.frontcont.shape='line'; % 'circle' 'rectangle' 'line'
'full'
geom.frontcont.wx=40/2; % [μm] half front contact
```

```
geom.Wxfront=1500/2; % [µm] front unit cell width (half
spacing)
    % ==== Shading ====
    Peter.busbarWidth = 600/2 ; % [µm] half busbar width,
(Not Quokka parameter!)
    Peter.busbarNumber = 5 ; % how many busbars (Not
Quokka parameter!)
    % Half shading width =  (busbar metal coverage * unit
cell width = effected busbar width) + front metal width
    generation.shading_width= (Peter.busbarWidth *
Peter.busbarNumber *2) / 156e3 * geom.Wxfront +
geom.frontcont.wx;  % half shading width by metal fingers
% Front homogeneous emitter
bound.conduct{1}.location='front'; % 'front' 'rear'
bound.conduct{1}.shape='full'; %
'full' 'line' 'rectangle' 'circle' 'contact'
bound.conduct{1}.Rsheet=170; % Sheet resistance
bound.conduct{1}.noncont.rec='J0'; %'J0' 'S' 'expr'
bound.conduct{1}.noncont.J0=12e-15; % J0e,pass A/cm², NOT
fA/cm²
bound.conduct{1}.cont.rec='J0';
bound.conduct{1}.cont.J0=700e-15; % J0e,metal A/cm², NOT
fA/cm²
```

```
bound.conduct{1}.cont.rc=3e-3; % [ohm-cm2] Contact
resistivity of contacted area
bound.conduct{1}.jctdepth=1.5; % [μm] junction depth
bound.conduct{1}.colleff=1.00; % [0-1] fixed value for
collection efficiency


% ==== Rear Contact ====
geom.rearcont.shape='line'; % 'circle' 'rectangle' 'line'
'full'
geom.rearcont.wx=70/2; % [μm] half rear contact ; 60 μm +
2 % fire-through busbar ~ 70 μm
geom.Wxrear = geom.Wxfront/3; % [μm] back unit cell width
(half spacing), can be different with front, but LCM need
to be small
% TOPCon
% ========================================
bound.conduct{2}.location='rear';
bound.conduct{2}.shape='full';
bound.conduct{2}.Rsheet= 60; % Sheet resistance
bound.conduct{2}.cont.rec='J0';
bound.conduct{2}.cont.J0=30e-15; % metallized J0
bound.conduct{2}.noncont.rec='J0';
bound.conduct{2}.noncont.J0=1e-15; % field J0
```

```
bound.conduct{2}.cont.rc=2e-3; % [ohm-cm2] Contact
resistivity of contacted area
bound.conduct{2}.colleff=1;


% ==== Bulk ====
bulk.T=300; % temperature in K
bulk.type='n-type'; % 'p-type' 'n-type'  doping type
bulk.rho=2; % [Ohm.cm]
bulk.taubfixed=1e20;  % [µs] taub bulk


% ==== Mesh ====
geom.meshquality=2; %    1: coarse (sufficient for most
simulations), 2: medium, 3: fine
geom.dxmin=5;      % minimum element size in x-direction
geom.dzminfront=0.5; % element size in z-direction at the
front surface
geom.dzminrear=0.5;
geom.scale=5;
geom.inflation=2.5;       % maximum allowable ratio of
neighboring element sizes; effectively controls how fast
mesh sizes are increased away from feature edges


% ==== Bulk other ====
```

```
bulk.Auger='Richter2012'; % 'Richter2012'* 'Altermatt2011'
'Kerr2002' 'Sinton1987' 'off'
bulk.mobility='Arora'; % 'Klaassen'* 'Arora' 'Fixed'
bulk.nieff='default'; % 'default'* 'fixed'
% bulk.nieffvalue=10000000000; % default value
% bulk.nieffvalue=8.6e9;  % Sinton's value
bulk.Brad=4.73E-15; % radiative recombination coefficient
bulk.SRH.BO.Nt=0;
bulk.SRH.BO.m=2;
bulk.SRH.midgap.taup0=1.5e3;
bulk.SRH.midgap.taun0=1.5e3;


% ==== Circuit LIV / single point Simulation ====
circuit.terminal='light_IV_auto'; % 'light_IV_auto':
automated algorithm to quickly but accurately derive light
IV-curve and parameters (Voc, Jsc, FF, eta)
circuit.Voc_guess=0.68;
circuit.IV_accuracy=5;
circuit.IV.init_previous=0;


% ==== Resistance ====
circuit.Rseries=0.215; % External Series resistance (Rs
ext)
```

```
circuit.Rshunt=100000; % External shunt resistance


% ==== Light Generation ====
generation.type='1D_model'; %   '1D_model' 'ext_file'
generation.Jgen_correction=1; % 0 or 1;  use this to math
Jsc!
      generation.Jgen=42.34; % use this to math Jsc!
42.34
generation.suns= 1; % 1 sun,
generation.Z='limit_Green02';
generation.Z_value=1;  % fixed value for pathlength
enhancement
generation.Z_filename=''; % load pathlength enhancement
data from external fil
generation.facet_angle=54.74; % 0 or 54.7    facet angle
of illuminated surface texture; set to 0 for planar
surface
generation.transmission='fixed'; %how (wavelength
dependent) transmission at the illuminated surface is
defined 'fixed': fixed value for all wavelengths
generation.transmission_value=1.0; % fixed value for front
transmission
```

```
generation.transmission_filename='';  % 'ext_file'
transmission only
generation.spectrum='AM1.5g'; %
'AM1.5g' 'monochromatic' 'custom'
generation.ext_file='';
generation.illum_side='front'; % 'front' 'rear'


% ==== Sweep ====
% sweep.param_1{i} sweep.param_2{i} are independent
% Index {i} stands for the i-th dependent sweep parameter
%
============================================================
sweep.enable=0;


sweep.param_1{1}='bulk.SRH.midgap.taun0';
sweep.values_1{1}=linspace(0.1,20, 10);
sweep.param_1{2}='bulk.SRH.midgap.taup0';
sweep.values_1{2}=linspace(0.1,20, 10);


sweep.param_2{1}='';
sweep.values_2{1}=[]; % sweep.value_2{1}=[]; to turn off
the second group
```

APPENDIX B DETAILED PROCESS SEQUENCE FOR SINGLE SIDE N-TOPCON SOLAR CELL FABRICATION

1. Starting Wafers

1.1. Phosphorus-doped N-type Cz Si wafers with textured surfaces on both sides.

2. Ion-Implantation

2.1. Boron implantation with selected implantation energy on the front side at Suniva.

3. Clean Wafers in Falcon Clean Bench

3.1. Deionized water (DI) rinse 3 cycles.

3.2. 5% by wt. HF dip for 90 seconds.

3.3. DI rinse 3 cycles.

3.4. Place the cassette in 2:1:1 (by volume) H_2O: H_2O_2 (30%): H_2SO_4 (96%) solution for 10 minutes.

3.5. DI rinse 3 cycles.

3.6. 5% by wt. HF dip for 90 seconds.

3.7. DI rinse 3 cycles.

3.8. Place the cassette in 5:1 (by volume) H_2O: HCl (100%) solution at 50 °C for 10 minutes.

3.9. DI rinse 3 times.

3.10. 5% by wt. HF dip for 90 seconds.

3.11. DI rinse 3 times.

3.12. Dry wafers in the hot air dryer at 150°C for 15 minutes.

4. Post Implantation Anneal in Centrotherm Oxidation Tube

4.1. Anneal at 1050 ℃ for 1 hour in N_2 ambient and 30 minutes in O_2 ambient (Recipe name: N1050NO.prz).

4.2. Implanted emitter side should face implanted side. Because the wafers are not labeled at this time, the user may need to take a note on the wafers' slot numbers.

5. Determine the P/N Type and Labeling

5.1. Connect the manual four-point probe to the P/N type hot-probe unit (Jandel Model PN01).

5.2. Use the four-point probe to probe the wafer, and then press "Test/Clear" key on the P/N type unit. You should see a solid P-type light on emitter side. If it shows solid N-type light or flashing light, try probe on the wafer again or probe on another side. Notice this measurement is only accurate after B anneal. Before B anneal there is not enough active B concentration to get an accurate measurement.

5.3. The sharp-pointed contacts on four-point probe can make small damage to the sample surfaces, so for the P/N type testing, unless for troubleshooting or failure analysis, usually one point per wafer is enough.

5.4. Label the wafer ID on the B emitter side with a diamond scribe.

6. Measure boron sheet resistance with four-point probe after B anneal

7. Clean Wafers in Falcon Clean Bench

7.1. DI rinse 3 cycles.

7.2. 5% by wt. HF dip for 90 seconds.

7.3. DI rinse 3 cycles.

7.4. Place the cassette in 2:1:1 (by volume) H_2O: H_2O_2 (30%): H_2SO_4 (96%) solution for 10 minutes.

7.5. DI rinse 3 cycles.

7.6. 5% by wt. HF dip for 90 seconds.

7.7. DI rinse 3 cycles.

7.8. Place the cassette in 5:1 (by volume) H_2O: HCl (100%) solution @ 50°C for 10 minutes.

7.9. DI rinse 3 cycles.

7.10. 5% by wt. HF dip for 90 seconds.

7.11. DI rinse 3 cycles.

7.12. Dry wafers in the hot air dryer at 150°C for 15 minutes.

8. SiN Mask on Front Emitter Side for Planarization & Wrap-Around Poly Removal in Centrotherm PECVD

8.1. Horizontal boat recipe: n_hor_np, 1200 sec.

9. Planarize rear side at Falcon Bench Tank 5 (KOH)

9.1. Prepare fresh KOH solution (1 large glass bottle KOH used) at Tank 5.

9.2. Set temperature to 80C (it takes ~2 hours to heat up).

9.3. Load wafers in texturing cassette with top net to keep wafers contained in KOH solution.

9.4. Di rinse for 3 cycles.

9.5. HF (10%) Falcon texturing side till rear hydrophobic (~30s).

9.6. Di rinse for 3 cycles.

9.7. Place the cassette in KOH 80 ℃ for 13 minutes.

9.8. Di rinse for 3 cycles.

9.9. Dry (15min).

9.10. Measure wafer thickness. ~10-15 μm is etched from the rear side.

10. Clean wafers without HF in Falcon Clean Bench

10.1. DI rinse 3 times

10.2. Place the cassette in 2:1:1 (by volume) H_2O: H_2O_2 (30%): H_2SO_4 (96%) solution for 10 minutes

10.3. DI rinse 3 times

10.4. Place the cassette in 5:1 (by volume) H_2O: HCl (100%) solution @ 50°C for 10 minutes

10.5. DI rinse 3 times

10.6. Dry wafers in the hot air dryer @ 150°C for 15 minutes

11. Nitric Acid Oxidation in Pettit CMOS Clean Wet Bench

11.1. Make new HNO_3 solution (3 full bottles, no water) in Nitric Acid tank.

11.2. Heat HNO_3 to 100 ℃.

11.3. Make new HF solution (~1%) in HF tank.

11.4. Submerge the wafer cassette into HF solution for 10 seconds. The rear side should be hydrophobic.

11.5. DI Rinse the wafers 3 times.

11.6. Submerge the wafer cassette into 100 ℃ HNO_3 solution for 10 minutes.

11.7. DI Rinse the wafers 3 times.

11.8. Dry each wafer one by one by air gun on the wet bench.

12. LPCVD N-Poly Deposition in Tystar Poly Tube 3

12.1. N-Poly recipe name: DPOLY.007. Parameters used are shown in Table 20. Deposition time 150 minutes deposits ~ 200 nm poly; 75 minutes ~ 100 nm.

Table 20: Parameters of n-type poly-Si deposition recipe in Tystar poly tube.

	Comment				VARIABLE
STEP TEMP:	Variable temps	TEMPL	(250.0 - 1250.0)	DEGC	0588.0
STEP TEMP:	Variable temps	TEMPC	(250.0 - 1250.0)	DEGC	0588.0
STEP TEMP:	Variable temps	TEMPS	(250.0 - 1250.0)	DEGC	0588.0
STEP STBP:	Stable pressure	PRCPR	(.000 - 2.000)	SCCM	00.250
STEP PSIH:	Pressure SiH4	SIH4	(0. - 200.)	SCCM	00100.
STEP PSIH:	Pressure SiH4	PH3	(.00 - 50.00)	SCCM	030.00
STEP DEPO:	Deposition	STEPTIME	(hh.mm.ss)		**02.30.00**

12.2. Put the prepared polished wafer with thermal oxide on the cantilever, beneath the boat for thickness monitor. Put wafers in the slots of horizontal boats, as shown in Figure 92. There are 8 slots in the boats (7 slots inside and the 8th one on top of the 4 pillars). Each slot can put 2 cell structure wafers with poly side facing out, or 1 symmetric structure. Notice the deposition thickness is affected by loading effect (the poly-Si growth rate depends on the number of wafers). Always fill the all 8 slots to ensure the poly-Si thickness is repeatable.

(a) (b)

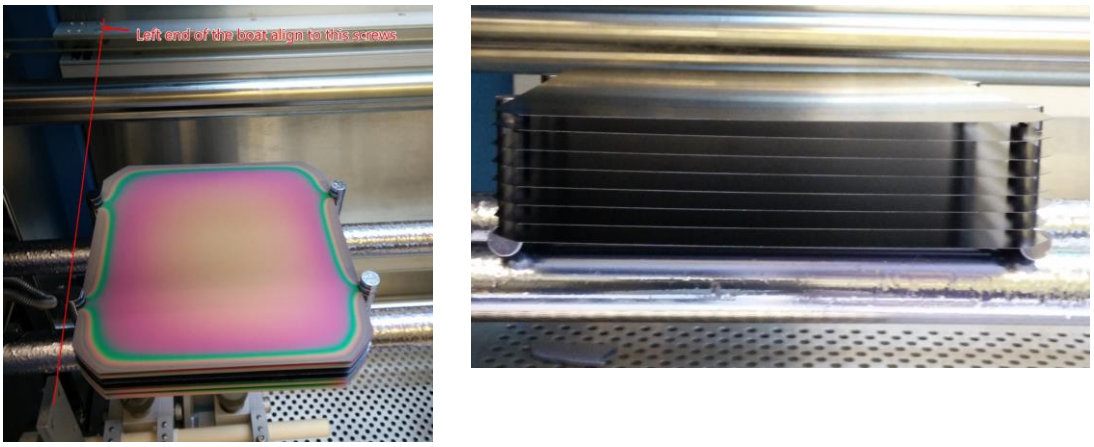


Figure 92: Photo of the quartz boat for poly-Si deposition: (a) top view (b) side view.

13. Rear SiN Mask in Centrotherm PECVD

13.1. Deposit the same SiN mask on the front side on the rear side.

14. Front poly wrap-around removal

14.1. Heat Falcon bench KOH tank to 40 ℃.

14.2. Dip wafers in HF (10%) till the edges on the front and the wrapped around poly on the front becomes hydrophobic (~30sec – 2 minutes)

14.3. DI rinse 3 times.

14.4. Dip in KOH at 40 ℃ in the damage etch bath for 4 minutes. Shake the cassette during the KOH bath to ensure wafer edge is not sticking to the cassette.

14.5. DI rinse 3 times.

14.6. Dry wafers in the hot air dryer at 150°C for 15 minutes

14.7. Check if poly-Si are fully removed on the front emitter side. You should only see SiN blue color on the emitter side now. If there is still rainbow color remain on the front side, it means there are poly-Si residue remain on the front side. If

not sure, dip the wafer in to HF solution for 1 second and the surface should be all hydrophilic. If part of it is hydrophobic it means some poly-Si is remained and the need additional KOH etching.

15. Mask Removal

15.1. Dip wafers in HF 10% in Falcon bench Tank 2, until wafers are all hydrophobic.

15.2. Fresh HF solution is highly recommended. HF etching drops fast after a couple SiN etching. Usually this step takes 30-40 minutes, depends on how fresh the chemical is.

16. Boron sheet resistance measurement

16.1. Pick 1-2 wafers every 5 wafers and measure 5 points of B emitter sheet resistance. Compare this sheet resistance with the values that was measured after Boron anneal and will be measured after poly anneal.

16.2. If the sheet resistance is very different with previous measurement, use the P/N units (hot probe) to make sure B emitter is still exist on the front side.

17. Clean wafers in Falcon Clean Bench

17.1. DI rinse 3 times.

17.2. Place the cassette in 2:1:1 (by volume) H_2O: H_2O_2 (30%): H_2SO_4 (96%) solution for 10 minutes.

17.3. DI rinse 3 times.

17.4. 5% by wt. HF dip for 10 seconds.

17.5. DI rinse 3 times.

17.6. Place the cassette in 5:1 (by volume) H_2O: HCl (100%) solution @ 50°C for 10 minutes.

17.7. DI rinse 3 times.

17.8. 5% by wt. HF dip for 10 seconds, wafers should be hydrophobic on both sides.

17.9. DI rinse 3 times.

17.10. Dry wafers in the hot air dryer at 150°C for 15 minutes.

18. Poly-Si anneal at MRL oxidation tube

18.1. MRL oxidation tube recipe: 875 ℃ for 30 minutes in N_2 ambient (Recipe name: **110- 875 N2 anneal**)

18.2. Put the poly-Si side face to poly-Si side during anneal.

19. Measure Poly-Si Thickness on Thickness Monitor Wafer at with Woollam M2000 ellipsometer

19.1. Recipe: yyhuang/ Tystar poly4 a-Si-with oxide on top.mod

20. ALD Al_2O_3 deposition at Cambridge NanoTech Plasma ALD - Oxide (right)

20.1. HF dip for 30 seconds to remove native oxide before ALD. If wafers stay in cabinet for a long time, do a full clean instead.

20.2. Use Recipe/Moon Hee/Plasma Al2O3 at 200℃, do a dummy run for 100 cycles.

20.3. Place a clean dummy wafer on the platform and then place the real sample on it.

20.4. Deposit Al_2O_3 at 200C, for 30 cycles on front emitter side.

21. Front SiN/PDO double layer anti-reflection (DLAR) deposition at Centrotherm PECVD

21.1. Recipe name: 156_DLAR. 500sec for SiN, 380 sec for PDO.

21.2. Notice that the deposition rate changes with the coating on the boat. A discussion with previous users for a more accurate timing for DLAR, or deposition of some dummy runs to confirm the deposition time is needed.

22. Rear SiN Deposition at Centrotherm PECVD.

22.1. Recipe: 156-npc, 700sec

23. Lifetime Measurement at Sinton WCT-120 QSSPC

24. Screen Print Front Grid Line

24.1. Screen: 106 lines, 40 μm

24.2. Paste: Heraeus 1614

25. Screen Print Front-Side Floating Busbar

25.1. Screen: 5 busbar 600 μm wide

25.2. Paste: Heraeus 1074

26. Screen Print Rear Side

26.1. Screen: 300 lines, 60 μm wide with 5 hollow busbars

26.2. Paste: Dupont 20A (Notice that the green strength of Dupont 20A is very low, which means the metal lines can be damaged easily before firing. Do not touch the printed line before firing!)

27. Co-Fire at Despatch Belt Furnace

27.1. Target peak temperature is ~775 ± 5 ℃. Measured temperature profile is shown in Figure 68.

27.2. Recipe name: UCEP-Peter_PERC_05. Parameters are shown in Table 21. If measured peak temperature is not expected, vary the set temperature in Zone 6 (FRN6) to achieve the targeting firing profile and peak temperature.

Table 21: Parameters of Despatch belt furnace recipe.

Recipe name	Conveyor speed [IPM]	FRN1	FRN2	FRN3	FRN4	FRN5	FRN6
UCEP-Peter_PERC_05	210	530	630	650	700	730	905

27.3. Put the wafer with boron side faces down, and poly-Si side faces up during the co-firing. Because of the low green strength of Dupont 20A, metal line can be damaged by contact points to the belt furnace, and the firing recipe is optimized with boron side facing down.

28. Light IV measurement

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PUBLICATIONS FROM THIS WORK

Journal Paper:

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[1] **Y.-Y. Huang**, A. Jain, W. Choi, K. Madani, Y.-W. Ok, and, A. Rohatgi, "Modeling and Understanding of Rear Junction Double-Side Passivated Contact Solar Cells with Selective Area TOPCon on Front " IEEE 48th Photovoltaic Specialists Conference (PVSC) 2021.

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