MIXED MATERIAL INTEGRATION FOR HIGH SPEED APPLICATIONS

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MIXED MATERIAL INTEGRATION FOR HIGH SPEED APPLICATIONS

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DEDICATION

To Tina, a soul taken far too soon from this earth. My heart reaches out to her parents, my aunt and uncle, in their time of sorrow. Tina, since you left this world before you completed yours, this thesis is dedicated to you.

Christina Lachenmann
1970 - 1998

A CHILD LOANED

"I'll lend you for a little time a child of Mine," He said,
"for you to love the while he lives and mourn for when he's dead.
It may be six or seven years or twenty-two or three, but will you,
till I call him back, take care of him for Me?
He'll bring his charms to gladden you, and should his stay be brief, you'll
have his lovely memories as solace for your grief."

"I cannot promise he will stay, since all from earth return, but there are
lessons taught down here I want this child to learn. I've looked this wide
world over in My search for teacher true, and from the throngs that
crowd life's lanes I have selected you.
Now will you give him all your love, not think the labor vain, or hate
Me when I come to call and take him back again?"

I fancied that I heard them say, "Dear Lord, Thy Will be done. For all the
joy the child shall bring, the risk of grief we'll run.
We'll love him while we may, and for the happiness we've known,
forever grateful stay.
But should the Angels call for him much sooner than we planned
we'll brave the bitter grief that comes and try to understand."

DON LARSON 1974

ACKNOWLEDGEMENTS

My thanks goes out to all those whose help, support and guidance has given me the strength to complete this chapter in my life. I would also like to thank those who have ever doubted my ability to succeed, for without them I would never have continued to push myself, constantly reaching for higher goals.

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SUMMARY

A great demand for portable and highly integrated high speed electronic components and systems has recently surfaced as a result of the vast expansion of personal communications and other wireless applications. As more and more applications in personal communications require frequencies between 1 and 100 GHz, a reduction in the cost of III-V technology is necessary for a wide distribution of wireless products in the consumer market. III-V technology provides improved and unique functionality compared with silicon CMOS integrated circuit (IC) technology, yet current III-V technologies cannot meet all the demands of low cost, high levels of integration, low power, and performance because of high material costs and low yield compared with the current silicon technology.

In this thesis, thin film mixed material integration is investigated as a method to increase functionality at lower cost. InP active devices are removed from the growth substrate and integrated onto other host substrates such as silicon via substrate removal. Characterization of these devices is performed. Also, thin film passive components via deposition on free standing polyimide are evaluated for lower cost and increased design freedom. By optimizing the passives and III-V active components separately and then integrating the two opens a new realm in mixed material integration.

CHAPTER I

INTRODUCTION

A great demand for portable and highly integrated high speed electronic components and systems has recently surfaced as a result of the vast expansion of personal communications and other wireless applications. As more and more applications in personal communications require frequencies between 1 and 100 GHz, a reduction in the cost of III-V technology is necessary for a wide distribution of wireless products in the consumer market. III-V technology provides improved and unique functionality compared with silicon CMOS integrated circuit (IC) technology, yet current III-V technologies cannot meet all the demands of low cost, high levels of integration, low power, and performance because of high material costs and low yield compared with the current silicon technology. Although silicon ICs possess the benefits of low cost material, high yield, and high component density, conventional silicon circuitry cannot provide the higher frequencies for emerging wireless communication. The need to reduce the cost of wireless technology can be solved through multi-material integration, which is the hybrid integration of III-V high speed components bonded directly to silicon circuitry. RF/microwave applications can be implemented with the high performance III-V components, while the remaining functions can be realized in the silicon circuit,

which also serves as the hybrid integration substrate. Cost is optimized through the sparse distribution of the relatively costly III-V components, by moving the large area components and low performance functions to the low cost, standard silicon circuitry. Each individual high speed component can be optimized for cost and performance independent of the silicon circuit design and fabrication and then the devices of choice can be integrated with the conventional, low cost silicon circuit.

Thin film semiconductor device integration has the advantage of integrating a variety of materials onto a single host substrate without concern for growth nucleation and growth compatibility. The direct growth approach of compound semiconductor material onto Si circuitry has constraints because of lattice and coefficient of thermal expansion mismatches between the Si and the compound semiconductor. Because of these mismatches, III-V material structures grown on silicon have been of worse quality than the growth of the structure on a lattice matched substrate. For example, the peak-to-valley ratio (PVR) of the negative differential region (NDR) of a resonant tunneling diode (RTD) is extremely sensitive to the growth conditions of the material structure. A ten times reduction is seen in the PVR of the same device grown on silicon instead of InP.[1]

Si/SiGe growth is another alternative to mixed material integration for resonant tunneling devices and high speed devices. An RTD grown by IBM using chemical vapor deposition yielded at room temperature a PVR of 1.2.[2] This is a factor of 25 smaller than III-V RTDs grown on lattice matched substrates.[1,2] Progress has been made in the area of high speed electronics using Si/SiGe, but at this time there is not a significant cost

advantage, especially when taking into consideration that substrates on which the Si/SiGe structures are grown are incompatible with the low resistivity substrates used for conventional low cost silicon circuitry.

Mixed material integration has also been achieved by use of flip-chip or bump bonding. One of the disadvantages of using flip-chip instead of thin film integration is that one is not able to process both sides of the devices. Also, it is much easier to planarize thin film devices with polyimide or benzocyclobutene (BCB) since they are on the order of 600 Å to 10 μm thick. After planarization a second layer of devices/interconnects can be stacked on top creating a three dimensional circuit. As for the thermal advantage of flip-chip heterojunction bipolar transistors (HBTs), or field effect transistors (FETs), it is mitigated by the fact that the solder must connect the device to the ground plane.

Successful demonstration of thin film device integration on host substrates establishes the feasibility of mixed-material integration for Si-based electronics. The ability to fabricate any type of high speed device with top and bottom processing bonded to virtually any type of substrate will enable significant increases in circuit performance and functionality. Mixed material integration represents a form of wafer scale packaging, in which the thin film devices, the host substrates, and the bonding and processing of these components produce an integrated package.

Thin film semiconductor device integration to host substrates such as Si circuits has already been successfully applied to an optical receiver[3] and an optoelectronic integrated circuit (OEIC)[4] using thin film GaAs-based MESFETs and a 10 GHz

amplifier[5] using a pseudomorphic thin film GaAs-based HEMT device. A thin film HBT has been successfully integrated which produced record high power-gain cutoff frequency in excess of 400 GHz.[6] These thin film devices are created by either substrate removal or epitaxial lift-off (ELO) of the device active layers from the growth substrate. Both of these processes utilize single crystal device epilayers that are grown lattice matched (or near lattice matched) on a growth substrate to ensure high material quality. Between these epilayers of interest and the growth substrate, selective or stop etch layers are grown if necessary, to facilitate removal of the substrate from the epilayers of interest. This material is then generally partially or fully processed into devices, the substrate is removed through selective chemical etching, and the thin film devices are transferred, aligned, and bonded to an arbitrary host substrate (such as a Si circuit). This process has yielded thin film devices that are comparable to or better than (due to removal of the substrate) conventional devices.

The thin film device integration process can be performed before or after the devices of interest have been fabricated. The devices in this study were all pre-processed for higher density of devices fabricated per unit area, thereby lowering cost. Also, all pre-processing of the thin film compound semiconductor device is separate from the manufacture of the host substrate (for example, a complex silicon circuit or a high thermal conductivity, high resistance substrate). Thus, the processes prior to integration can be separately optimized and neither compromises the other.

To complement this work, characterization of thin film deposited passive components on free standing polyimide held taut by a 4 or 6 inch titanium frame

hereinafter termed "flex" were also evaluated. Much interest has been shown in thin film passive devices as an alternative to more conventional passive components.[7-17] This study concentrates on thin film passive components on free standing flex provides an alternative to silicon passives which are frequency limited by the lossy substrate and to the III-V passives components which occupy large amounts of area on costly substrates. These thin film passives on flex have the ability to be integrated via lamination on any host substrate of choice. This gives an added flexibility to integrate mixed materials in a variety of packages ranging from silicon substrates to ceramic or even plastic packages.

The work presented in this thesis is divided into two parts, the Chapters 1 through 5 deal with fabrication, integration and characterization of the active components for use in mixed material integration while Chapter 6 consists of all the passive component fabrication, testing and evaluation. Chapter 7 gives a summary of the completed work, and finally, Chapter 8 will outline future directions.

ENDNOTES

[1] N. Evers, O. Vendier, C. Chun, M. R. Murti, J. Laskar, N. M. Jokerst, T. S. Moise, and Y.-C. Kao, *38th Electronic Materials Conference*, (1996).

[2] N. Evers, O. Vendier, C. Chun, M. R. Murti, J. Laskar, N. M. Jokers t, T. S. Moise, and Y.-C. Kao, *IEEE Electron Device Letters*, **17**(9) (1996).

[3] T. Morf, C. Brys, P. De Dobbelaere, P. Van Daele, P. Demeester, T. Martinson, and W. Bachtold, *IEEE GaAs IC Symposium 1995*, 189 (1995).

[4] I. Pollentier, P. Demeester, P. Van Daele, D. Rondi, G. Glastre, A. Enard, and R. Bondeau, *3rd Int. Conf. of InP and Rel. Mat. 1991* , 268 (1991).

[5] P. G. Young, R. R. Romanofsky, S. A. Alterovitz, R. A. Mena, and E. D. Smith, *IEEE Microwave and Guided Wave Lett.*, **3** 107 (1993).

[6] R. Pullela, Q. Lee, B. Agarwal, D. Mensa, J. Guthrie, L. Saoska, and M. Rodwell, *1997 IEEE Device Research Conference*, III.B-2 (1997).

[7] H. Yoshino, T. Ihara, S. Yamanaka, and T. Igarashi, *IEEE/CHMT '89 Japan IEMT Symposium*, 156 (1989).

[8] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, *IEEE IEDM*, 6.5.1 (1996).

[9] P. K. Singh, R. S. Cochrane, J. M. Borrego, E. J. Rymaszewski, T. M. Lu, and K. Chen, *1994 IEEE MTT-S*, 1457 (1994).

[10] T. Lenihan, L. Schaper, Y. Shi, G. Morean, and J. Parkerson, *1996 Electronic Components and Technology Conference*, 119 (1996).

[11] H. Okabe, H. Yamada, M. Yamasaki, O. Kagaya, K. Sekine, and K. Yamashita, *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, **21**(3) 269 (1998).

[12] K. Chen, M. Nielsen, S. Soss, E. J. Rymaszewski, T.-M. Lu, and C. T. Wan, *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, **20**(2) 117 (1997).

[13] S. Byeon and Y. Tzeng, *IEEE Transactions on Electronic Devices*, **37**(4) 972 (1990).

[14] R. R. Kola, M. Y. Lau, S. Duenas, H. Y. Kumangai, P. R. Smith, R. C. Frye, K. L. Tai, and P. A. Sullivan, *1997 International Symposium on Advanced Packaging Materials*, 71 (1997).

[15] P. Chahal, R. R. Tummala, M. G. Allen, M. Swaminathan, *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, **21**(2) 184 (1998).

[16] J. Crols, P. Kinget, J. Craninckx, and M. Steyaert, *1996 Symposium on VLSI Circuits Digest of Technical Papers*, 28 (1996).

[17] H. Kapadia, H. Cole, M. Nielsen, and N. Krishnamurthy, *ATW 1998 Chateau Elan*, (1998).

CHAPTER II

THIN FILM INP-BASED SEMICONDUCTOR DEVICE INTEGRATION PROCESS

Hybrid integration through the bonding of thin film devices to arbitrary host substrates is a powerful emerging tool for mixed material integration. The thin film devices and host substrate can be independently grown, processed, and optimized and joined in the bonding process without concern for lattice matching. The thin film epitaxial structure of interest, as grown, includes a sacrificial or stop etch layer grown between the epitaxial devices of interest and the growth substrate, and sometimes the bottom active layer of the device can be used as the stop etch layer. The thin film epitaxial devices of interest (and any associated metals, dielectrics, etc. used in the pre-bonded device formation) are separated from the growth substrate either by selectively laterally etching the sacrificial layer (called epitaxial lift-off, ELO), or by selectively etching away the substrate, stopping at the stop etch layer (called substrate removal).

Using handling layers and transfer techniques, these thin film materials can be transferred after separation, processed on both sides of the device, aligned, and bonded onto host substrates of arbitrary composition, including silicon circuits, polymers, and high thermal conductivity ceramics. Processing of these thin film materials and devices can be performed without degradation of the quality of the material or the circuit, and, in fact, some devices benefit from the direct top and bottom contact options when the growth substrate is removed. The thin film devices can range from hundreds of angstroms to tens of microns thick, and, after bonding to the host substrate, the integrated host substrate is

nearly planar, thus enabling the use of standard microelectronic processing techniques to complete the integration.

In the InP system, selective etching of the InP growth substrate can be accomplished using an HCl or $HCl:H_3PO_4$ ((3:1) or (4:1)) solution to remove the thin film device from the host substrate. There is a high degree of selectivity between InP and undoped InGaAs for these etch solutions, so InGaAs can be used as a stop etch layer. Devices grown and fabricated at Raytheon/TI Systems for the substrate removal process utilize the same growth procedure and processing steps as the conventional devices.

The InP-based devices such as the resonant tunneling diode (RTD), the tunneling hot electron transfer amplifier (THETA), and the heterostructure bipolar transistor (HBT) in this study have a highly doped InGaAs layer as the first growth layer, which may be used as the stop etch layer. However there is a decrease in the selectivity of the etch when the InGaAs is highly doped, which causes the InGaAs to be etched slightly during the substrate removal process. This can be eliminated by the growth of a thin (100 -2000Å) undoped InGaAs layer between the thin film device and the growth substrate.

2.1 Standard Substrate Removal and Bonding

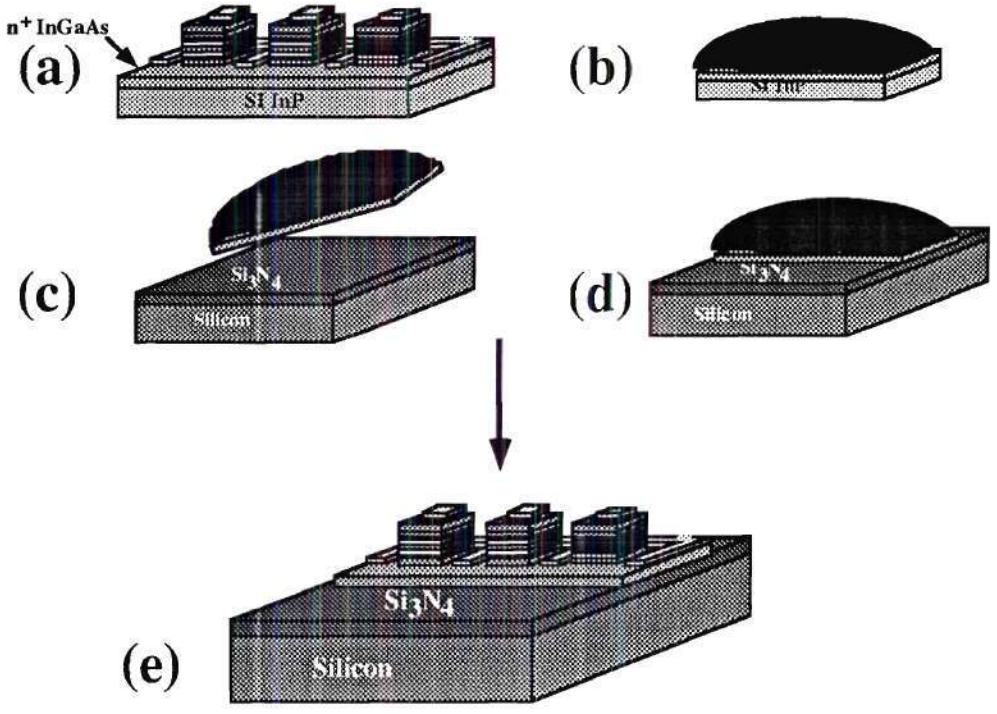


Figure. 2.1 Substrate removal and bonding of RTDs onto silicon host substrates.

Figure 2.1 illustrates the basic steps for substrate removal and bonding to a host substrate. A handling layer is used to preserve the integrity and relative spatial orientation of the thin film devices. This Apiezon W handling layer is applied before the substrate removal and also serves to protect the devices from the substrate removal etch. After the substrate is fully removed, the samples are placed in DI water and then transferred and bonded to the host substrate. The thin film devices can be bonded to the host substrate through either a contact bond of semiconductor-semiconductor or semiconductor-metal, or

a bond using a partially cured epoxy, BCB, or polyimide. The disadvantages of this process are the inability to align, to process both sides of the device, and to flip devices if desired. Also, since the contact bond is not a metal-metal bond, the bond is not as strong and adhesion becomes an issue. Therefore, epoxy or partially cured BCB or polyimide is necessary for a reliable bond.

2.2 Modified Substrate Removal and Bonding

Efforts have been made to study the feasibility of processing both sides of the thin film device and aligning the device using a variety of techniques. Figure 2.2 shows one possible alternative thin film semiconductor integration technique.

The substrates were bonded to a thin glass slide using a small amount of black wax to be used as a rigid handling layer. Removal of the host substrate was performed by placing the devices in a $HCl:H_3PO_4$ (4:1) etch. The etch uniformity was improved by the weight of the glass slide keeping the substrate inverted in the etch solution. Metal was deposited onto the backside of the devices using an e-beam evaporator. The devices were then bonded to a metal pad using a hot plate anneal. After the anneal, the devices were submersed in TCE overnight for removal of the black wax and the glass slide was removed. This process kept the devices under constant rigid support while still maintaining the ability to evaporate contacts on both sides of the devices. The adhesion of the devices to the pad on the host substrate was excellent. Issues of alignment are currently being investigated including use of photoresist in place of the black wax layer.

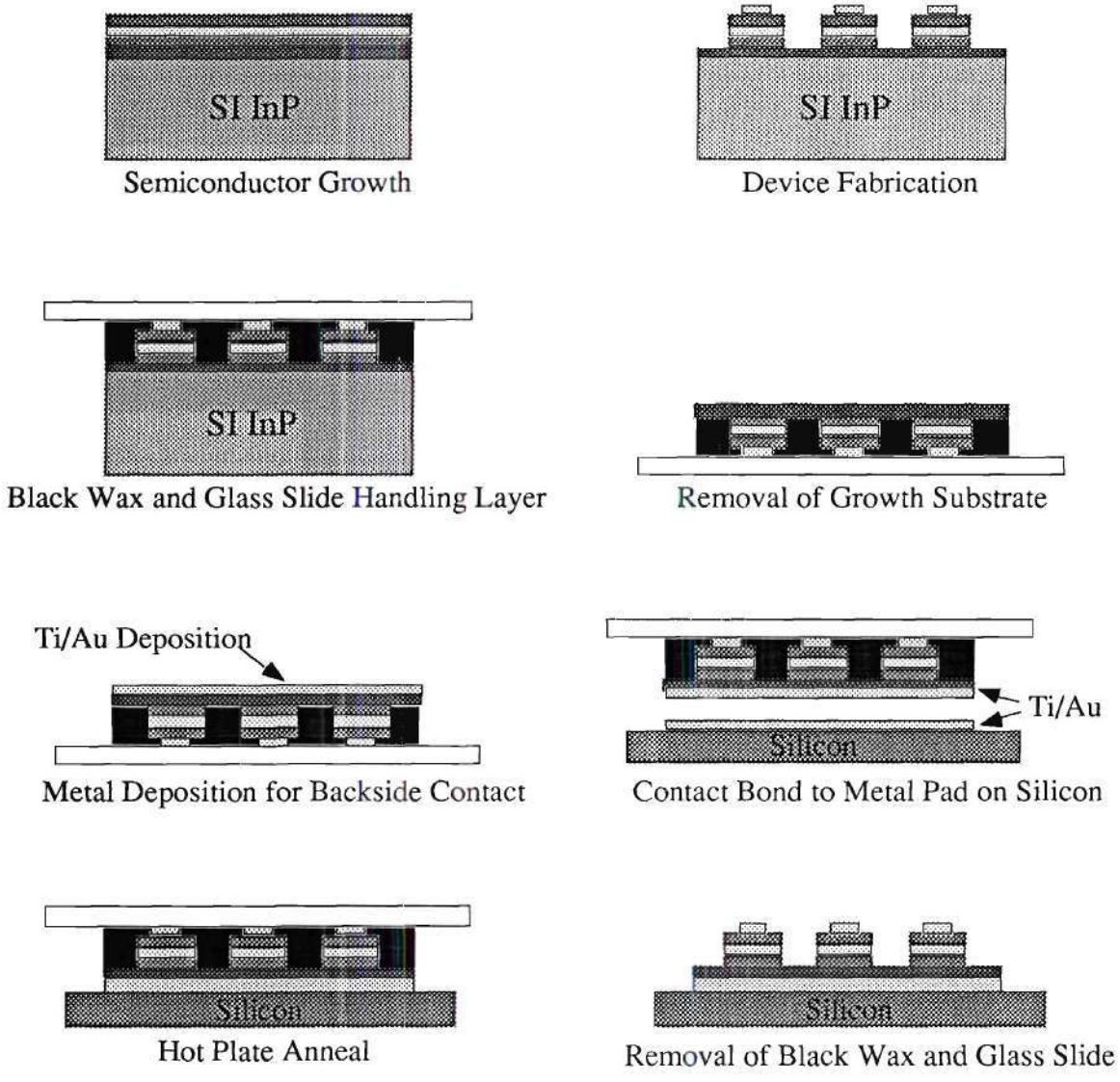


Figure. 2.2 Transfer of thin film devices to host substrate without use of transfer diaphragm. Contacts are made on both sides of the device.

2.3 Integration Utilizing a Transfer Diaphragm

A drawback to the techniques illustrated in Figure 2.1 and 2.2 was the inability to precisely align the thin film devices with respect to features on the host substrate. This causes difficulty in the manufacturable final metallization that may be necessary, in some applications, to connect the thin film devices to a host silicon circuit. An approach that is more consistent with post processing masking steps involves transferring the thin film devices to the host substrate using a transparent transfer diaphragm. [1-3] Thus, the thin film devices can be aligned with respect to features on the host substrate, and there is the versatility to pick and place optimized devices, as shown in Figure 2.3. The devices or arrays of devices are bonded to the silicon circuit using the standard transfer techniques with a transfer diaphragm. This involves the application of the black wax handling layer and removal of the growth substrate as shown in Figure 2.1. The thin film devices are then contact bonded to the transfer diaphragm. After bonding to the transfer diaphragm the handling layer is removed using TCE. The diaphragm is then inverted and lowered into contact with the host substrate. The bond to the host substrate is made so that the metal pads of the device that were deposited on top of the device, but now inverted, are aligned with the pads on the host substrate removal of the handing layer. This enables a thermally and electrically conductive, and mechanically stable metal/metal bond to be realized between the thin film devices and the host substrate (such as a silicon circuit). Finally, this method enables the processing of both sides of the thin film devices while under substrate (either growth or host) support.

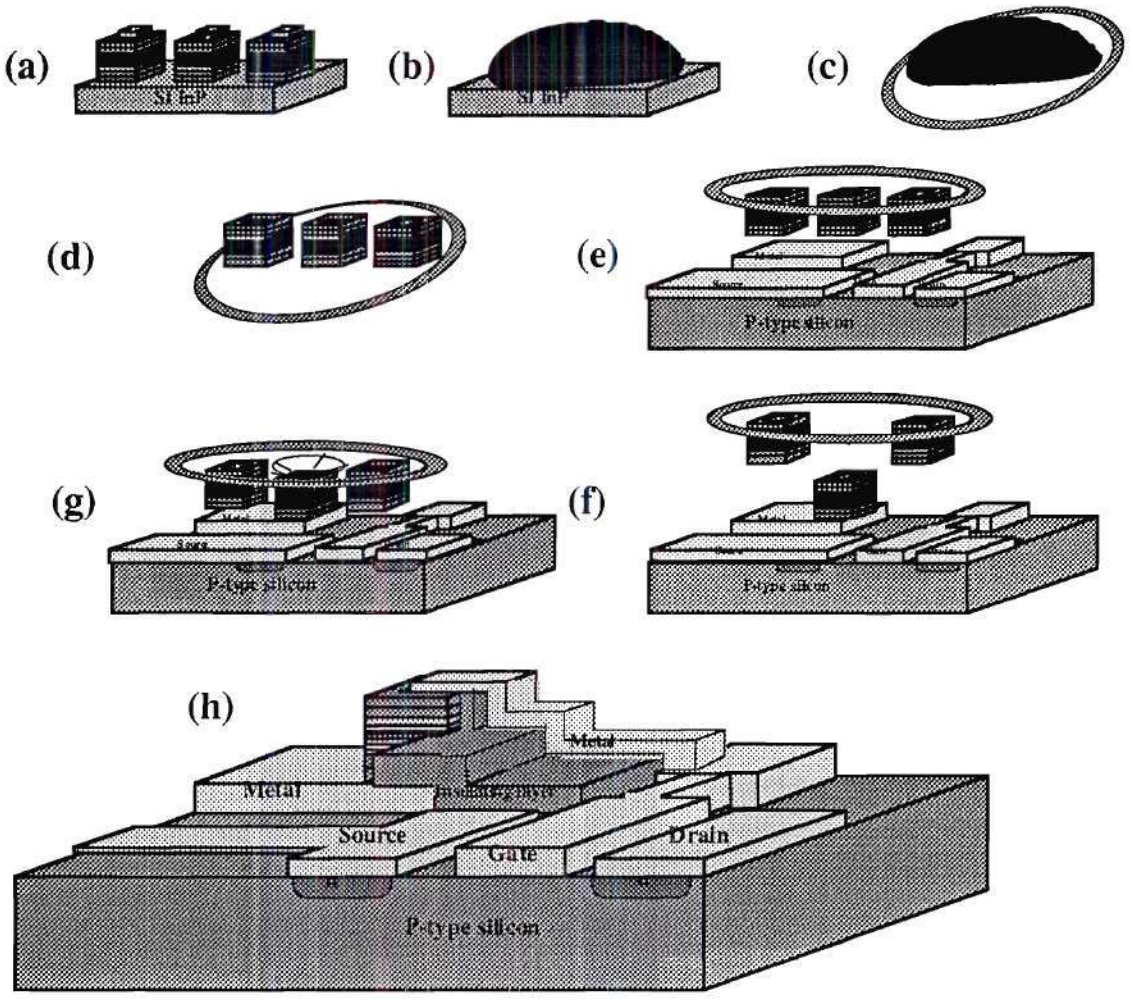


Figure. 2.3 Substrate removal and bonding using a transfer diaphragm. The transfer diaphragm enables the alignment and bonding of the thin film devices to the host substrate as well as the ability to process both top and bottom of the device. Post-processing of top contact pads is done after device has been contact bonded to the host substrate.

ENDNOTES

[1] K. H. Calhoun, C. B. Camperi, and N. M. Jokerst, *IEEE Photonics Tech. Letters*, **5**(2), (1993).

[2] S. Fike, B. Buchanan, N. M. Jokerst, M. A. Brooke, T. G. Morris, and S. P. Deweerth, *IEEE Photonics Tech. Letters*, **7**(10), 1168 (1995).

[3] O. Vendier, N. M. Jokerst, and R. P. Leavitt, *IEEE Photonics Tech. Letters*, **8**(2), (1996).

CHAPTER III

THIN FILM RESONANT TUNNELING DIODES

Resonant tunneling was first proposed by Tsu and Esaki in 1973.[1] Their theoretical analysis of one-dimensional superlattices with periods shorter than the electron mean free path concluded that interesting transport properties such as negative differential resistance (NDR) would occur in such structures. In 1974, this resonant tunneling producing an NDR region was first observed.[2] The main factor in realizing such a structure was the ability to precisely control the thickness, composition, and quality of the such thin layers. With the technique of growing such thin multilayer structures using molecular beam epitaxy (MBE), resonant tunneling in these structures was finally detected.

A resonant tunneling diode (RTD) in its simplest form consists of an undoped well sandwiched between two higher conduction band undoped barriers and heavily doped emitter and collector regions. The heavily doped emitter and collector regions are degenerate states in which the donors are present in such high concentrations that they are no longer considered to be composed of discrete non-interacting states. Instead, they are considered to form a band. The Fermi level in these regions may lie within the conduction band if the conduction band electron concentration exceeds the effective density of states. In the well between the barriers and these degenerate regions, there are quasi-bound, or resonant, states that are formed. These resonant states will accommodate electrons when the energy of the electrons in the degenerate region are the same as the resonant state. Figure 3.1 shows the different bias conditions of the RTD: (a) zero bias, (b) threshold bias, (c) resonance, and (d) off-resonance. At (a) zero bias, the energy of the electrons in the emitter is below the energy of the first resonant (or quasi-bound state) in the well. At (b),

threshold, the energy of the local Fermi level in the emitter is equal to the energy of the first resonant well. At (c), resonance, there are electrons in the emitter conduction band that are equivalent to the first resonant state energy and these electrons tunnel through the barriers via this resonant state. At (d) off-resonance, the conduction band edge in the emitter is at a higher energy level than the first resonant state.[3] Resonant tunneling diodes are well known for their high speed switching characteristics and several prototype circuits that take advantage of their unique electrical characteristics have been demonstrated. For example, room temperature operation of a full-adder integrated circuit that uses resonant-tunneling bipolar transistors and conventional transistors has been demonstrated.[4] In related experiments, RTDs have been vertically integrated to achieve a multiple negative-differential resistance characteristic for use in frequency multiplication[5], multistate memory[6], analog-to-digital conversion[7], and static access memory circuits.[8] By successfully separating prefabricated pseudomorphic AlAs/$In_{0.53}Ga_{0.47}As$/InAs RTDs from their host InP substrate followed by bonding to silicon, the feasibility of future integration of quantum device technology with conventional silicon circuitry may be realized. This future integration offers the possibility of high-speed, enhanced functionality circuits which take advantage of the multistate characteristics of the RTD and the high-integration density and high thermal conductivity associated with silicon technology.[9, 10] Further, multi-stack RTDs integrated with silicon electronics provide high packing density and eliminate the necessity for interconnects between the RTDs after substrate removal.[11] Finally, through this approach, both the RTD and silicon device structures can be separately optimized prior to integration.

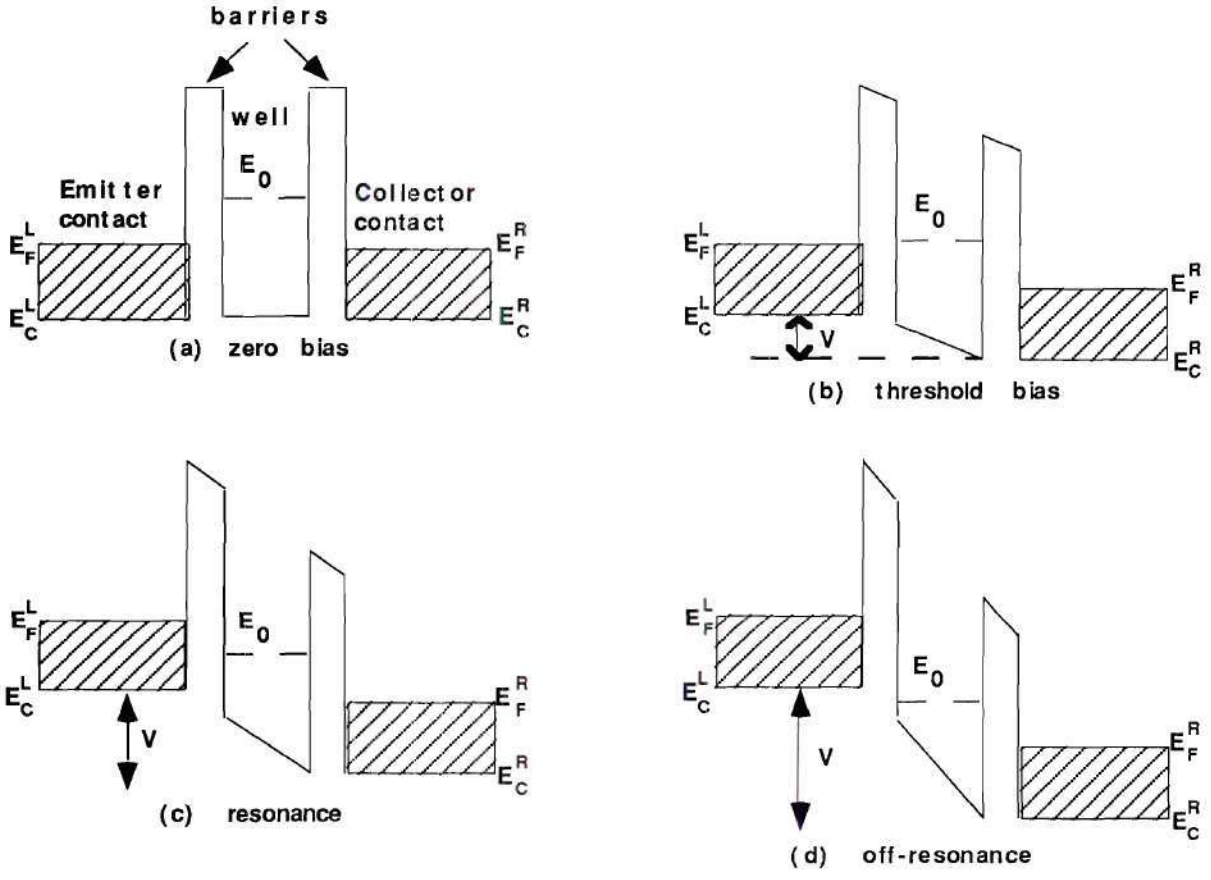


Figure 3.1 Conduction band profiles of the RTD under the conditions of (a) zero bias, (b) threshold bias, (c) resonance, and (d) off-resonance. At (a) zero bias, the energy of the electrons in the emitter are below the energy of the first resonant (or quasi-bound state) in the well. At (b), threshold, the energy of the local Fermi level in the emitter is equal to the energy of the first resonant well. At (c) resonance, there are electrons in the emitter conduction band that are equivalent to the first resonant state energy and these electrons tunnel through the barriers via this resonant state. At (d), off-resonance, the conduction band edge in the emitter is at a higher energy level than the first resonant state.[3] The local Fermi levels in the emitter and collector are E_F^L and E_F^R, and the energies of the conduction-band edge in the emitter and collector are E_C^L and E_C^R.[3]

3.1 Growth and Fabrication

For this work, the high PVR RTD layers were grown by Raytheon/TI using molecular beam epitaxy using group III and group V elemental sources. A cross-sectional layer schematic of the as-grown RTD sample is shown in Figure 3.2(a). The 20 Å AlAs RTD barrier layers are under a tensile strain of 3.2% when deposited on the larger lattice-constant $In_{0.53}Ga_{0.47}As$ crystal. The RTD quantum well consists of 30 Å of InAs, which is compressively strained by 3.5%, sandwiched between symmetric 5 Å $In_{0.53}Ga_{0.47}As$ layers. The InAs layer serves to increase the PVR by decreasing the ground state energy of the quantum well while increasing the energy separation between the quantum-confined bound states as a result of the reduced electron effective mass.[12, 13]

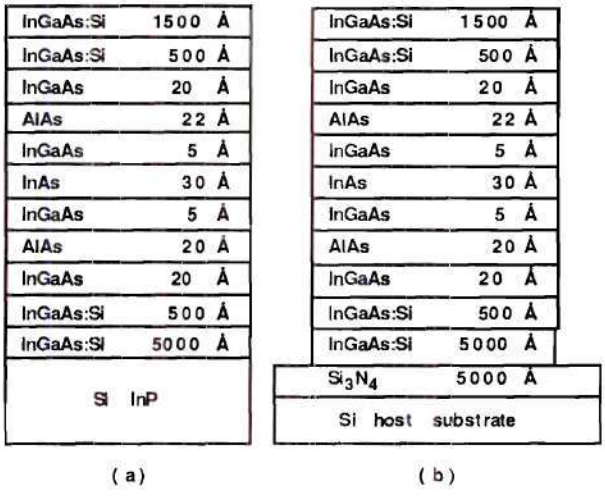


Figure 3.2 Structure of the high PVR RTD (a) before and (b) after substrate removal and bonding to the host substrate.

The thin film devices were bonded to silicon using the standard substrate removal and bonding process explained in Section 2.1. The cross-sectional schematic after bonding to the host substrate is shown in Figure 3.2(b).

3.2 Experimental Results of Thin Film RTDs on Silicon

Following the bonding procedure shown in Figure 2.1, the thin film RTDs were placed in a scanning electron microscope (SEM) for inspection. Consistent with the results of previous bonding demonstrations,[14-16] the RTDs exhibited no signs of structural degradation, as shown by the electron micrograph in Figure 3.3. A comparison of the current-voltage characteristics for the as-grown and bonded 256 μm^2 area RTD is shown in Figure 3.4 The peak current and PVR are very similar, indicating that the pseudomorphic RTD retains its high quality during the separation and bonding process. Similar trends were observed for all five of the samples investigated independent of device area (16 μm^2 - 256 μm^2). The highest measured PVR for the thin film RTD integrated onto Si was 30, as seen in Figure 3.4.

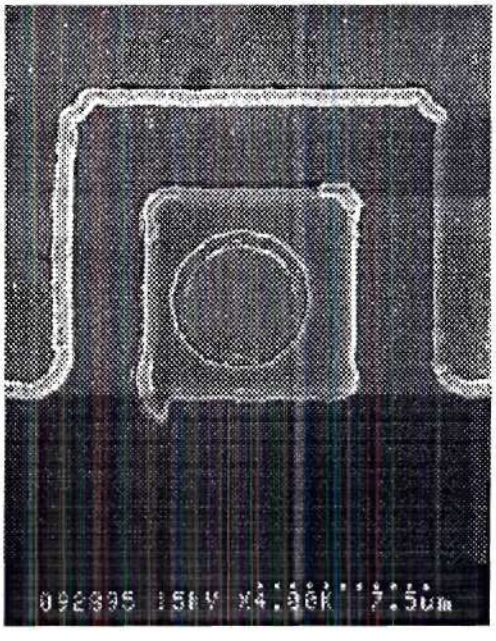


Figure 3.3 SEM of a 64 μm^2 high PVR RTD after substrate removal and bonding.

A comparison of the current-voltage characteristics for the as-grown and bonded thin film four-stack resonant tunneling diode heterostructure (16 μm^2 area) is shown in Figure 3.5. Although the PVRs remain nearly constant before and after integration, some deviations from the as-grown current-voltage characteristics were observed. Since these structures were not optimized for substrate removal and bonding, these deviations from the as-grown structures may be due to the variations in the adhesion of the RTD structure to the host substrate and the non-uniform removal of the InP substrate, which may have caused some areas of the highly doped InGaAs to be partially etched. The combination of spatial variation in etching and bonding quality may have resulted in slight non-uniform variations in the I-V characteristics for different devices. RTD structures optimized for substrate removal and bonding may eliminate the variation in adhesion and etching.

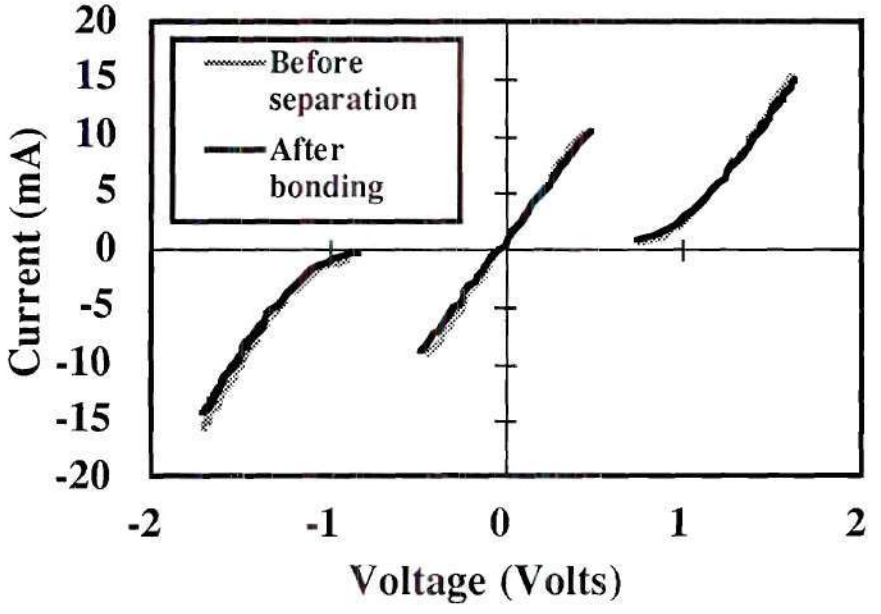


Figure 3.4 256 μm^2 high PVR RTD before and after substrate removal and bonding. The corresponding positive and negative PVRs were 13 and 21, respectively.

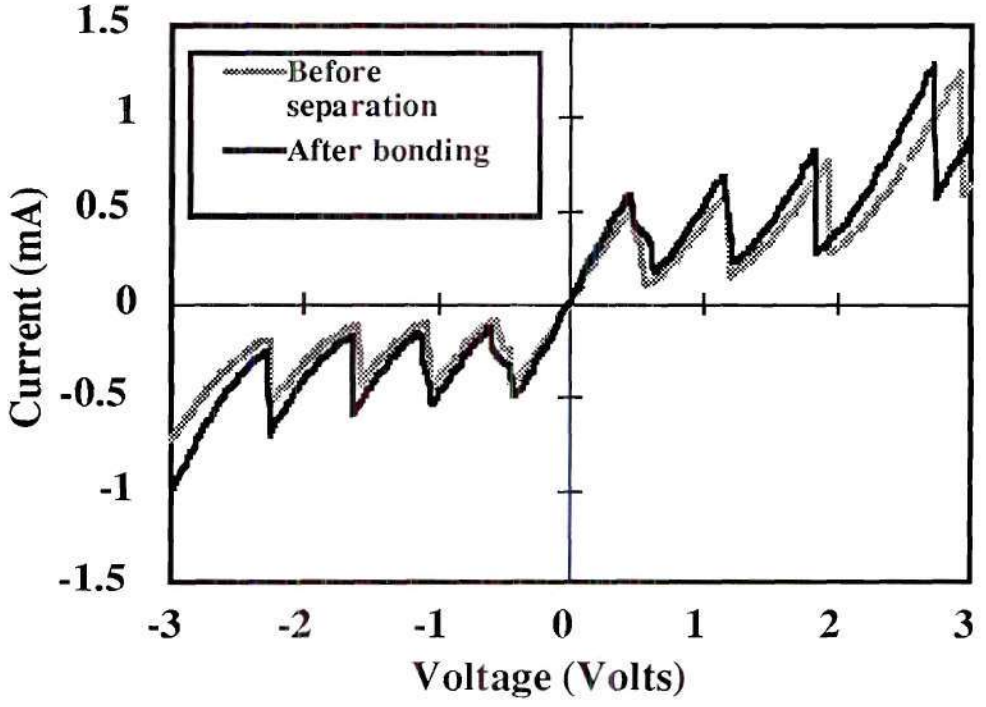


Figure 3.5 Four vertically stacked 16 μm^2 RTDs before and after substrate removal and bonding.

3.3 Empirical SPICE Model and MDS Diode Model

In an effort to better understand the slight variations in the DC characteristics of the RTDs before and after substrate removal and bonding, and for modeling of device performance for design of silicon circuitry utilizing the thin film devices, a simplified empirical SPICE model was used. The Tsu-Esaki formula for current utilizing an effective mass approximation is[1]

$$J = \frac{em^* kT}{2\pi^2 \hbar^3} \int_0^\infty dE T(E,V) \bullet \ln\left[\frac{1+e^{(E_F - E)/kT}}{1+e^{(E_r - E - eV)/kT}}\right], \qquad (3.1)$$

where m^* is the effective mass, k is Boltzmann's constant (1.38×10^{-23} J/K), T is the temperature in Kelvin, $\hbar$ is Planck's constant (1.054×10^{-34} J-s), and Γ is the resonance width.

The transmission coefficient for this simplified analysis is approximated by a Lorentzian,[17]

$$T(E,V) = \frac{\left(\frac{\Gamma}{2}\right)^2}{\left[E - \left(E_r - \frac{eV}{2}\right)\right]^2 + \left(\frac{\Gamma}{2}\right)^2}, \qquad (3.2)$$

where E is the energy measured up from the emitter conduction band edge, E_r is the energy of the resonant level to the bottom of the well at its center and Γ is the resonance width.[17]

The assumptions made are (1) the barriers are equal widths and (2) half the voltage drop falls from the emitter to the center of the well. Since (2) is not always valid, $eV/2$ can be replaced by eVn with n determined from fitting or analysis. For small Γ, T(E,V) is negative except when E is close to resonance, $E \approx E_r - eV/2$. Since Γ is approximately 1 meV or less for even extremely thin barriers, $\Gamma << kT$, so substituting $E = E_r - eV/2$ gives[17]

$$J = \frac{em^* kT\Gamma}{4\pi^2\hbar^3} \ln\left[\frac{1 + e^{(E_F - E_r + eV/2)/kT}}{1 + e^{(E_F - E_r - eV/2)/kT}}\right] \bullet \left[\frac{\pi}{2} + \tan^{-1}\left(\frac{E_r - \frac{eV}{2}}{\frac{\Gamma}{2}}\right)\right]. \qquad (3.3)$$

This formula gives the proper form for the lineshape, but the physical values may depart from their actual values. This is due to an oversimplified model which is effective for circuit model applications, but not for physical modeling of an RTD device. By using the Tsu-Esaki current density formula, a separation of variables approximation was utilized to reduce the current density formula to a one dimensional integral. In any device in which multiple sub-bands are coupled unphysical results such as current spikes can occur in the model. The Lorentzian approximation for the transmission coefficient has a delta-function-like nature which selects out only electrons very close to the resonance, but the dependance of the transmission peak on voltage was neglected. To make the model more realistic, voltage dependance of the transmission coefficient, multiple bands, band bending, as well as a more physical approach to incorporate the voltage drop across the collector spacer layer which physically causes voltage spreading, and a more intense numerical integration of the current density formula must be incorporated.[17,18]

The simplified equation for circuit modeling can be written in the following form[17] :

$$J_1(V) = A \ln\left[\frac{1+e^{(B-C+n_1 eV)/kT}}{1+e^{(B-C-n_1 eV)/kT}}\right] \bullet \left[\frac{\pi}{2} + \tan^{-1}\left(\frac{C-n_1 eV}{D}\right)\right], \qquad (3.4)$$

where $A = \frac{em^* kT\Gamma}{4\pi^2\hbar^3}$, $B = E_F$, $C = E_r$, $D = \frac{\Gamma}{2}$, and $n_1 = \frac{1}{2}$ or determined from fitting or analysis. A and D are determined by the value of Γ assuming temperature remains constant.

Formula (3.4) gives the resonant tunneling current and the negative differential resistance for the first resonance, but the increasing valley current resulting from inelastic scattering, non-resonant tunneling through higher lying quasi-continuum levels, and the

thermionic current that flows over barriers still need to be included. The increasing valley current can be represented by a simple diode form[17] :

$$J_2(V) = H\left(e^{n_2 eV/kT} - 1\right). \qquad (3.5)$$

If second or higher resonances are desired, the addition of more components in the form of J_1 can be used. So the sum of the external and tunneling current give the total current,

$$J(V) = J_1(V) + J_2(V). \qquad (3.6)$$

A SPICE simulation was used to investigate the changes in the current-voltage characteristics resulting from the changes in the device structure. The program is shown in Figure 3.6. By varying the parameters A, B, C, and D in J_1, one can fit the peak height, peak width and valley current to give an understanding of what parameters can cause a shift in the current-voltage curves.

```
*DC SWEEP OF 1-PEAK RTD
.PARAM A = 0.0011
.PARAM B = 0.034
.PARAM C = 0.067
.PARAM D = 0.0009
.PARAM n1=0.10, n2=0.110
.PARAM H = 1.6E-5
.PARAM VT0 = 0.0259  ; = kT/q
.PARAM PI = 3.1415926
.FUNC NLG(B,C,n1,X) {1+exp((B-C+n1*X)/VT0)}
.FUNC DLG(B,C,n1,X) {1+exp((B-C-n1*X)/VT0)}
.FUNC ATA(C,D,n1,X) {PI/2 + atan((C-n1*X)/D)}
G1 1 0 VALUE={A*log(NLG(B,C,n1,V(1,0))/DLG(B,C,n1,V(1,0)))*ATA(C,D,n1,V(1,0))}
G2 2 0 VALUE = {H * (exp(n2*V(2,0)/Vt0) - 1)}
R1 3 1 100
R2 1 2 65
VA 3 0 1VOLT
.DC VA 0 2 .01
.probe
.END
```

Figure 3.6 SPICE program for physics-based DC curves

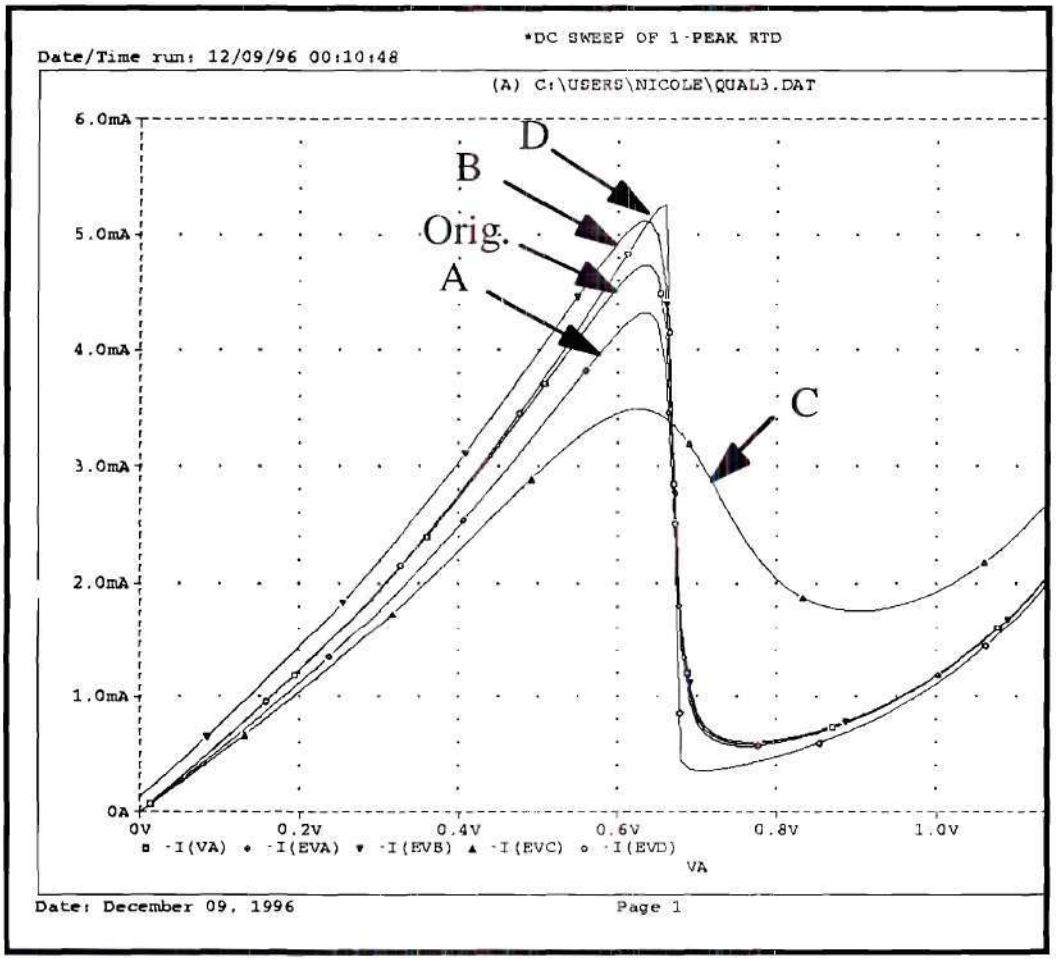


Figure 3.7 Variations in DC response of the RTDs resulting from changes in the parameters in the resonant tunneling current equation.

Parameters	Fitted Values	Varied Values
A	0.0011	0.0010
B	0.034	0.038
C	0.067	0.071
D	0.0009	0.0001

Table 3.1 Fitted and varied parameter values for the resonant tunneling current equation. Fitted values were used for the InP-based RTD for circuit simulations. Varied values were used to show how the DC characteristics change with changes in E_F (B), E_r (C), and Γ (A and D).

Changes were made in the peak and valley currents by the variation of the parameters as shown in Table 3.1. There was little to no shift seen in the voltage where the peak current occurred as the parameters were varied. It had been observed that there was little change in the peak-to-valley ratio of the RTDs before and after substrate removal and bonding, yet there was a shift in the voltage where the peak occurred and some slight changes in the peak and valley current. Changes in the active device because of relaxation of strain after substrate removal and bonding could cause some of the effects observed, or the shift in voltage that is being seen may partially be because of a change in resistance of the contacts due to nonuniform adhesion of the thin film devices on the host substrate.

Using MDS, a circuit consisting of diodes was used to simulate the current-voltage characteristics of the RTD as shown in Figure 3.8.

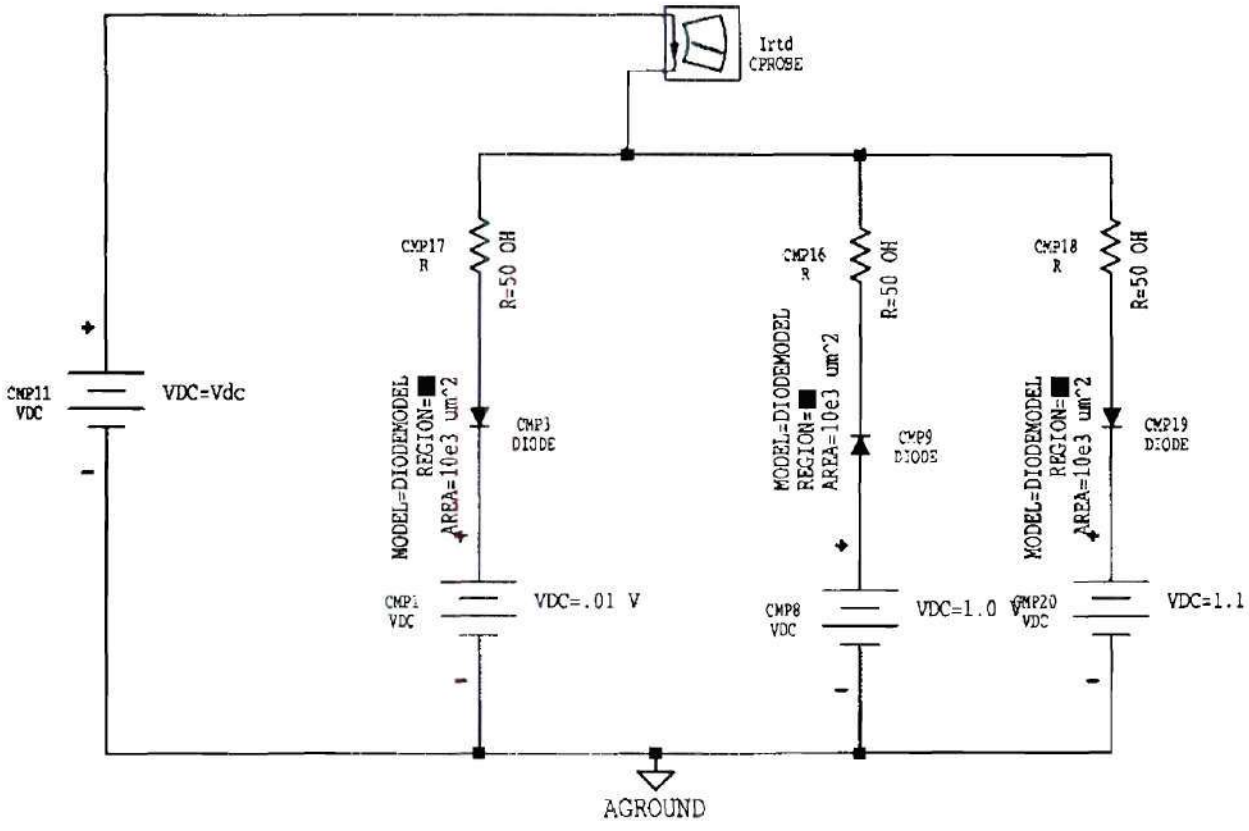


Figure 3.8 A large signal model in MDS for simulation of current-voltage characteristics of RTD.

In Figure 3.9, a resistor is put in series with the RTD model to simulate an increase in series resistance after substrate removal and bonding.

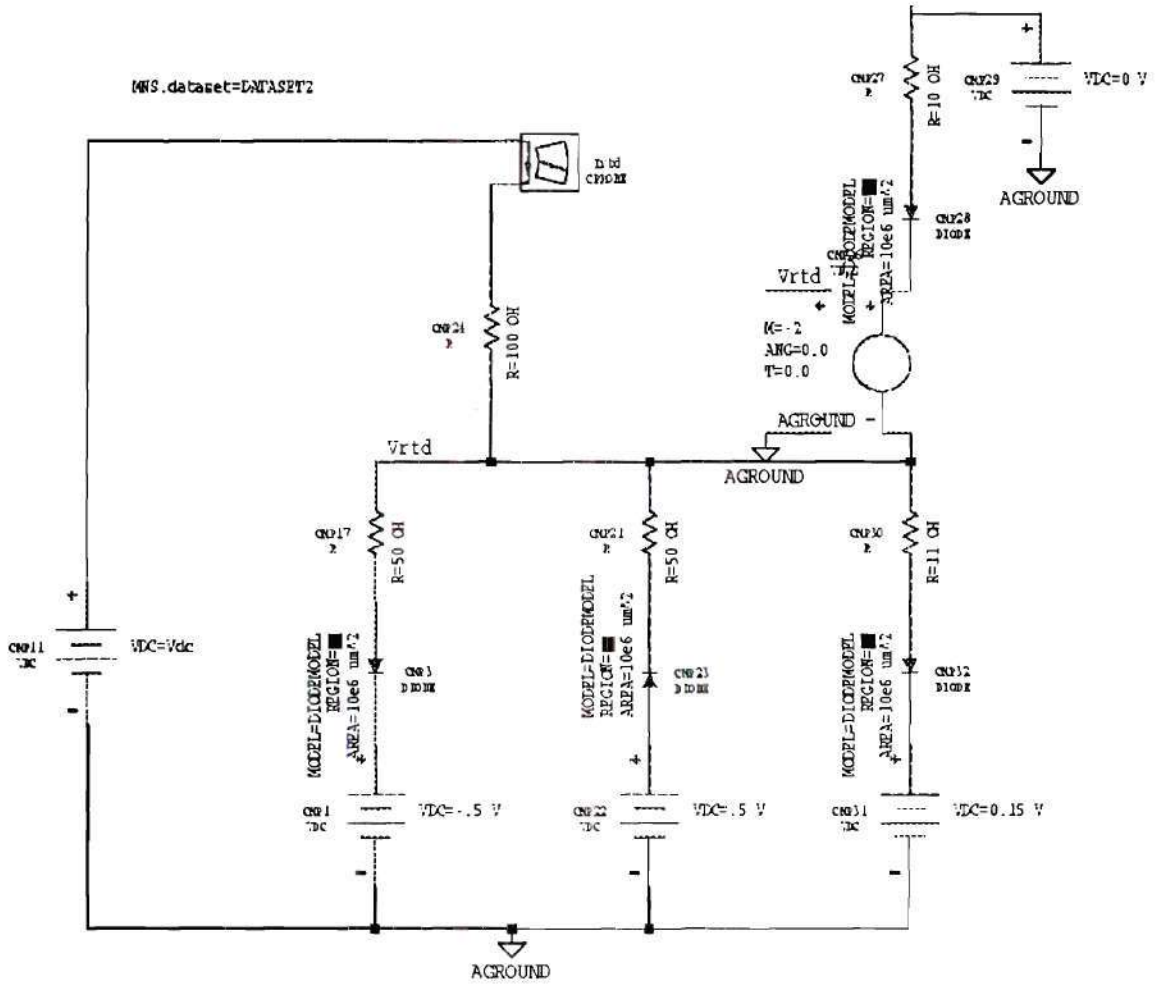


Figure 3.9 A resistor is added in series with the model for simulation of the voltage shift which occurred for the thin film RTDs.

Figure 3.10 shows the DC characteristics of the RTD with increased series resistance. An increased series resistance causes the peak and valley current to shift to the right as well as increasing the valley current and lowering the rise of the extrinsic current. The changes in the DC characteristics before and after substrate removal and bonding differ slightly from device to device. All effects are within the difference of DC characteristics

from device to device on-wafer. An interplay between some relaxation of the strain intentionally incorporated into the device and some stresses induced from nonuniform bonding of the contact pads may have caused the changes in the DC characteristics between the on-wafer and thin film device. Thin film RTDs that were bonded utilizing a semiconductor-metal bond and those utilizing an annealed metal-metal showed more consistent results between the on-wafer and thin film devices. The semiconductor-metal bond maintained the same or a slightly increased voltage for the peak current showing uniform bonding with little to no increased series resistance, while the annealed metal-metal bond consistently showed a decreased series resistance. There were still decreases in the peak and valley currents, which may have been caused by slight changes in the strain of the active layers of the device after substrate removal and bonding.

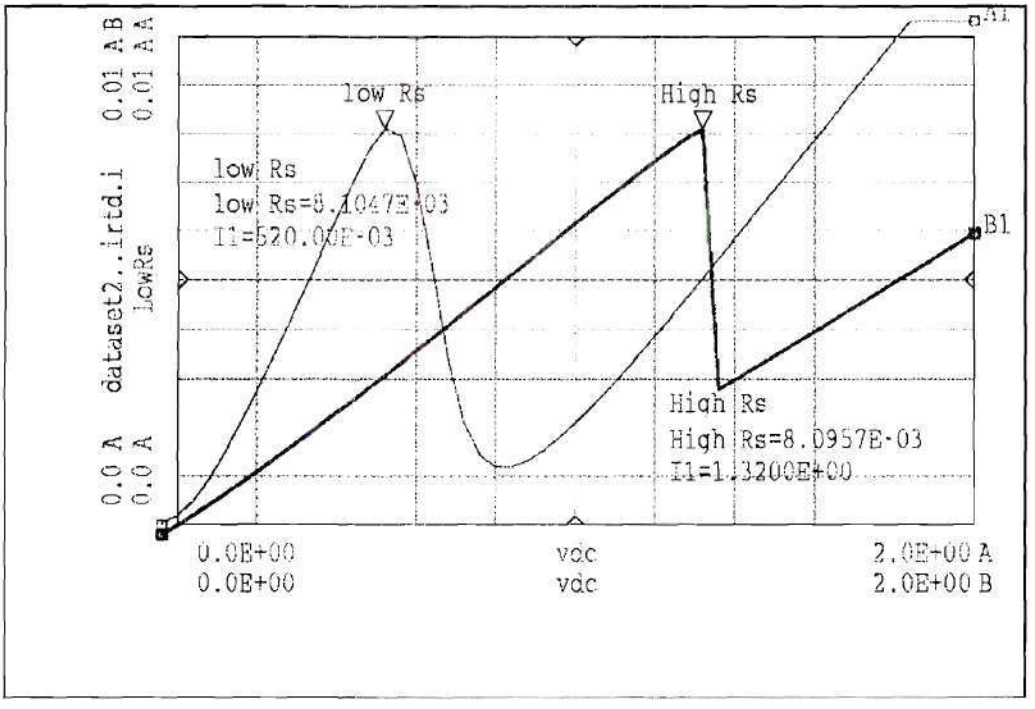


Figure 3.10 DC characteristics of low and high series resistance RTDs modeled using MDS.

3.4 Process Optimization for Circuit Integration

Before integrating resonant tunneling diodes (RTDs) into a silicon circuit, an experiment was performed to determine the most precise way to integrate thin film RTDs which would maintain the DC characteristics. The devices of interest were low current RTDs which had been fabricated with a thick planarizing nitride on-wafer. 6 μm devices were chosen for the initial integration since these were the lowest current devices on wafer that had yielded close to 100% on wafer. Initial integrations of thin film RTDs on silicon using the higher current RTDs with a thinner planarizing nitride had produced a slight shift in the I-V characteristics. This shift had been within the range of shift of the on-wafer devices. For the lower current, thicker nitride, the shift after substrate removal and bonding was more significant and could no longer be ignored. I-V characteristics of on-wafer 6 μm RTDs is shown in Figure 3.11.

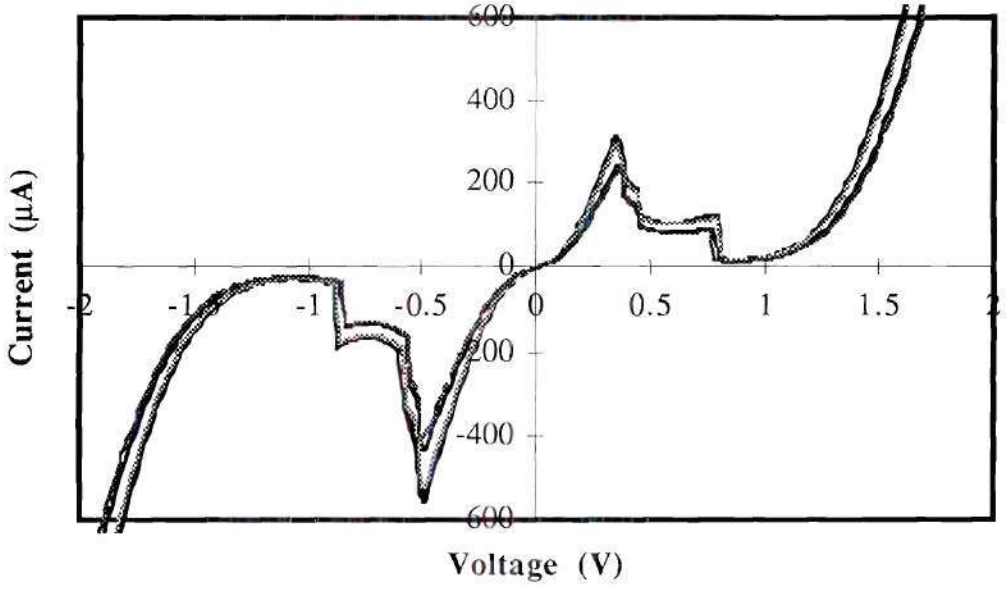


Figure 3.11 On wafer DC characteristics of low current 6 μm RTD's with thick planarizing nitride.

After substrate removal and bonding, the DC characteristics of these devices is shown below in Figure 3.12.

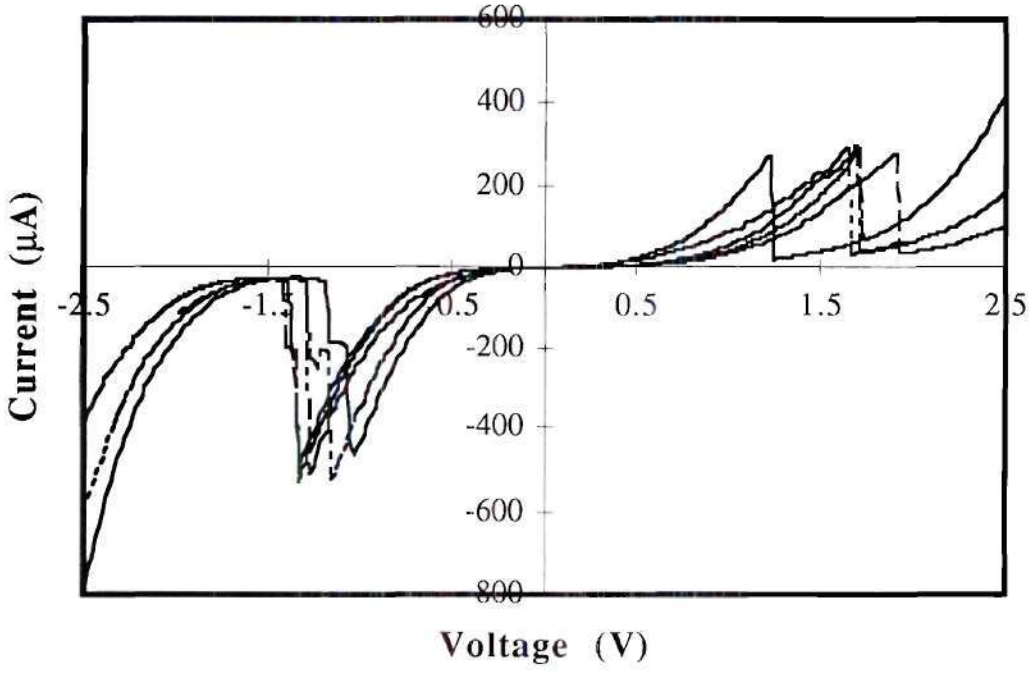


Figure 3.12 Low current 6 μm RTD's with thick planarizing nitride after substrate removal and bonding.

To reduce the strain of the nitride on the thin film devices, the nitride which was not underneath the contact pads were removed. Two different samples were used in this process. On one sample the nitride was removed using a wet etch while the other was removed by a reactive ion etch (RIE). The sample which under went the wet etch maintained the DC characteristics on-wafer while the RIE sample showed degradation in the DC response of the devices on-wafer, as shown in Figure 3.13.

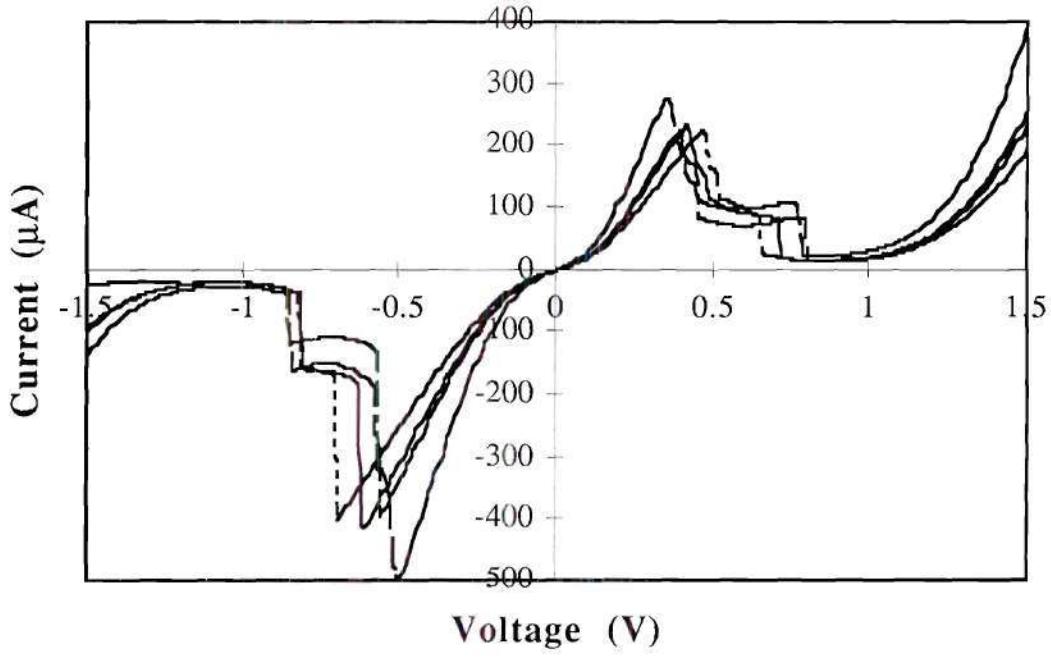


Figure 3.13 Current-voltage characteristics of on wafer low current 6 μm RTD's after RIE nitride removal.

The devices with the wet etch of nitride on wafer proceeded with substrate removal and bonding onto silicon. Figure 3.14 shows the DC characteristics of these thin film devices.

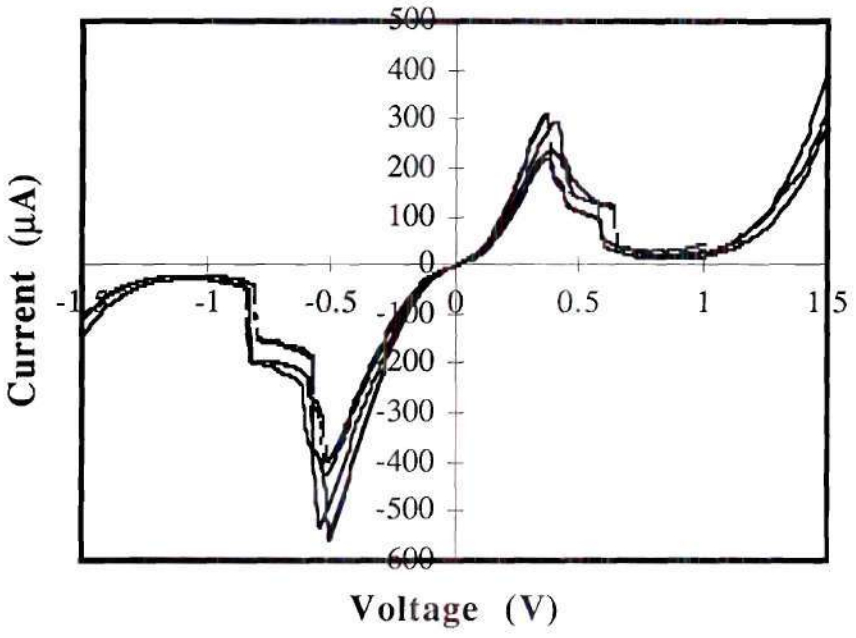


Figure 3.14 Low current 6 μm RTD's after wet etch of nitride and substrate removal.

The statistics of the peak current and the voltage at which it was recorded is given in Tables 3.2 and 3.3.

Table 3.2 Statistics of the peak voltage for the negative NDR.

	On Wafer	Integrated with Thick Nitride	On Wafer after RIE of Nitride	Integrated after Wet Etch of Nitride
Mean	-0.5	-1.23	-0.6	-0.52
Median	-0.5	-1.28	-0.59	-0.51
Standard Deviation	0.0	0.13	0.08	0.01
Minimum	-0.5	-1.34	-0.70	-0.54
Maximum	-0.5	-1.04	-0.51	-0.51

Table 3.3 Statistics of the peak current for the negative NDR.

	On Wafer	Integrated with Thick Nitride	On Wafer after RIE of Nitride	Integrated after Wet Etch of Nitride
Mean	-488.34	-499.66	-425.08	-490.14
Median	-517.20	-506.90	-405.60	-527.60
Standard Deviation	65.06	24.62	45.78	74.25
Minimum	-557.60	-524.60	-493.00	-554.90
Maximum	-403.70	-464.20	-396.10	-396.10

The devices integrated with the thick planarizing nitride maintained their peak current, yet there was a large shift in the voltage corresponding to the peak current. Since the use of the RIE to remove the nitride also degraded the peak voltage of the RTDs, the wet etch of the nitride was used. These RTDs integrated onto silicon after wet etch on the planarizing nitride maintained their current-voltage characteristics.

3.5 Thin Film RTD Integrated with a Si Circuit

After process optimization of the thin film RTD, circuit integration was ready to begin. Below in Figure 3.15 is a circuit diagram of the silicon comparator circuit designed using an InP RTD. Appendix A gives a detailed step-by-step process of the actual circuit integration process.

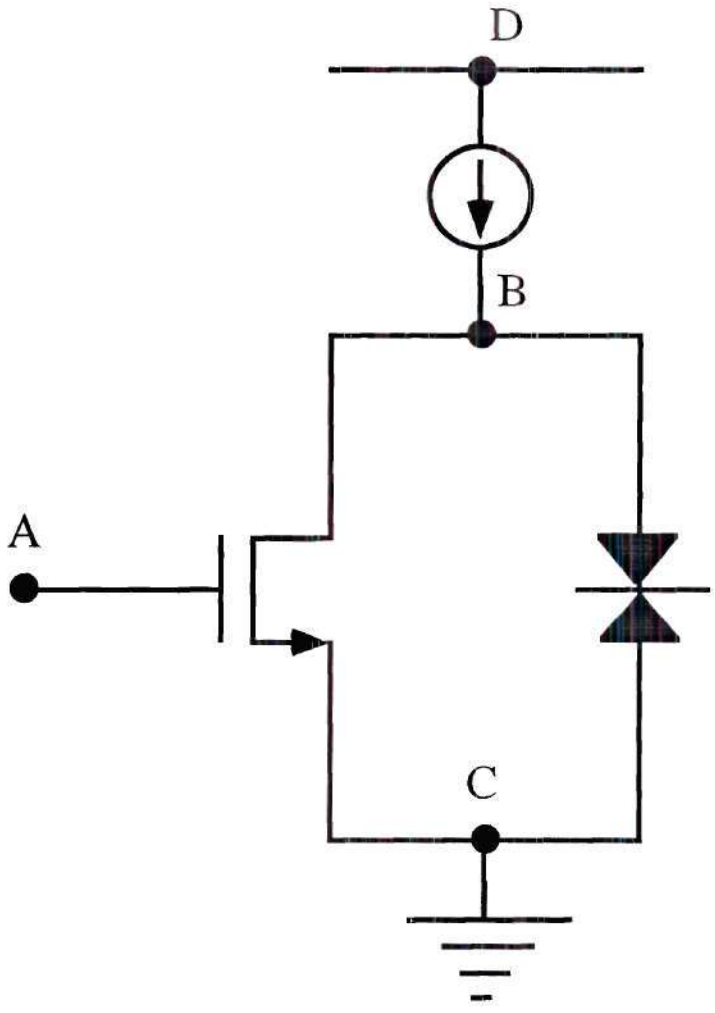


Figure 3.15 Silicon comparator circuit with integrated InP RTD.

Figures 3.16 and 3.17 shown a 6 μm RTD after successful integration with a silicon comparator circuit. The mesa defined before substrate removal, which defined the area of the entire thin film area after substrate removal, was approximately 200 μm by 300 μm and included the RTD and the original bonding pad. A contact pad the size of the area of the thin film area was created by metal lift-off in the region provided for circuit integration. After substrate removal, the thin film device was contact bonded to the bottom

pad. Polyimide was spun over the device to encapsulate it. A via was etched down to the contact pad of the RTD and a top contact was again defined by metal lift-off. Figure 3.17 gives a close-up of the RTD after integration.

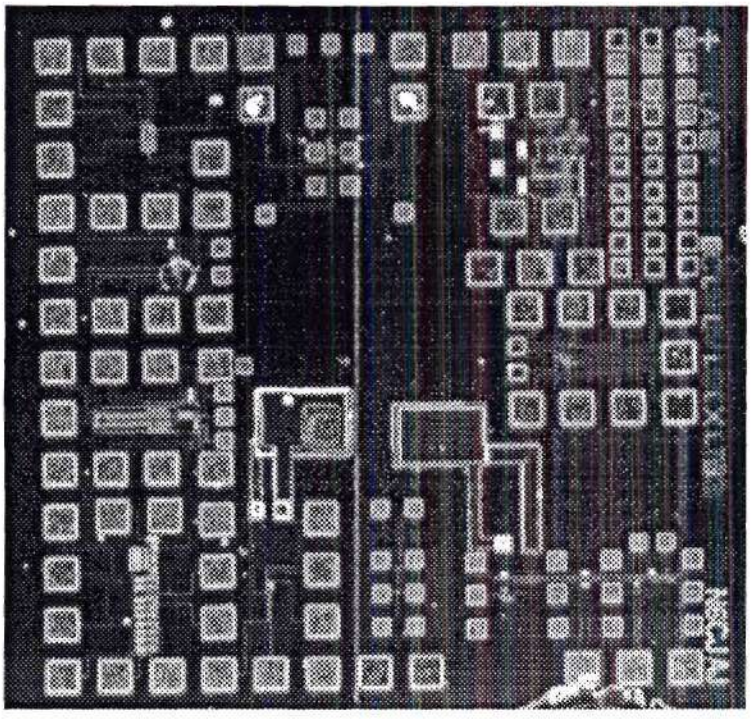


Figure 3.16 Photograph of RTD integrated with Si comparator circuit.

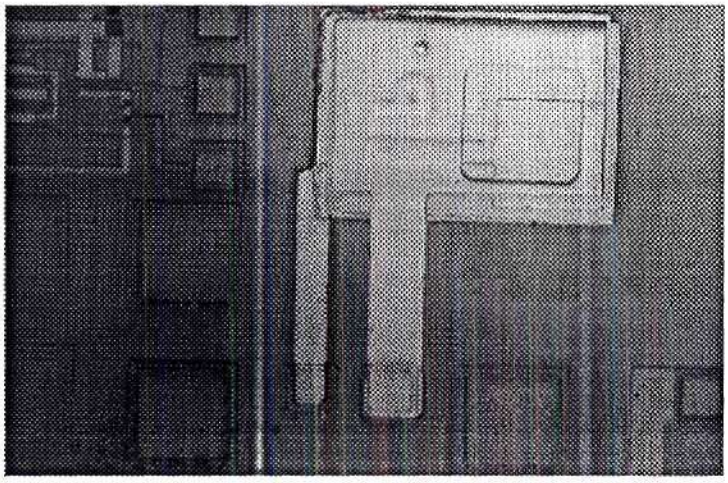


Figure 3.17 Close-up of RTD integrated with a Si comparator circuit.

After the top contact was made, the RTD was separately tested to make sure there were no open contacts between the top and bottom contacts due to a break in the metal in the via for the top contact. The negative current voltage characteristics of the RTD which is used by the circuit in this particular configuration are shown in Figure 3.18.

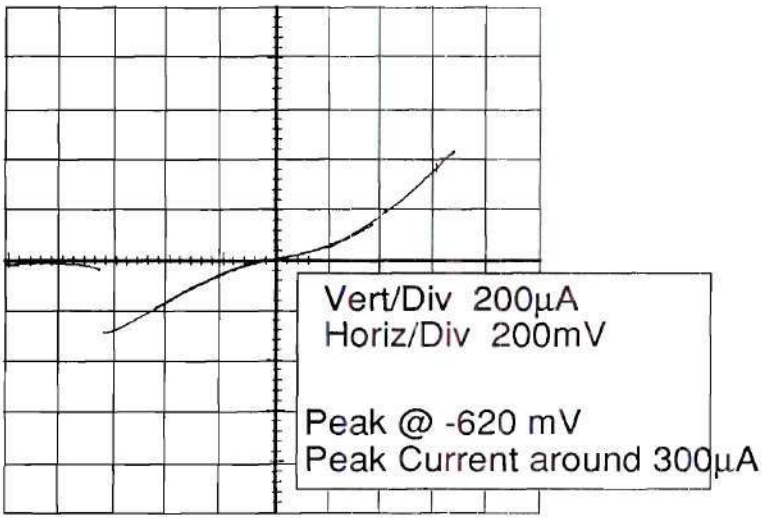


Figure 3.18 Negative region current-voltage characteristics of RTD after integration with comparator circuit.

Simulations utilizing the Pspice model of the RTD were performed before testing of the circuit. The simulated RTD current voltage characteristics and the actual characteristics matched well. The modeled RTD characteristics and the circuit characteristics with and without the RTD are shown in Figures 3.19 - 3.21.

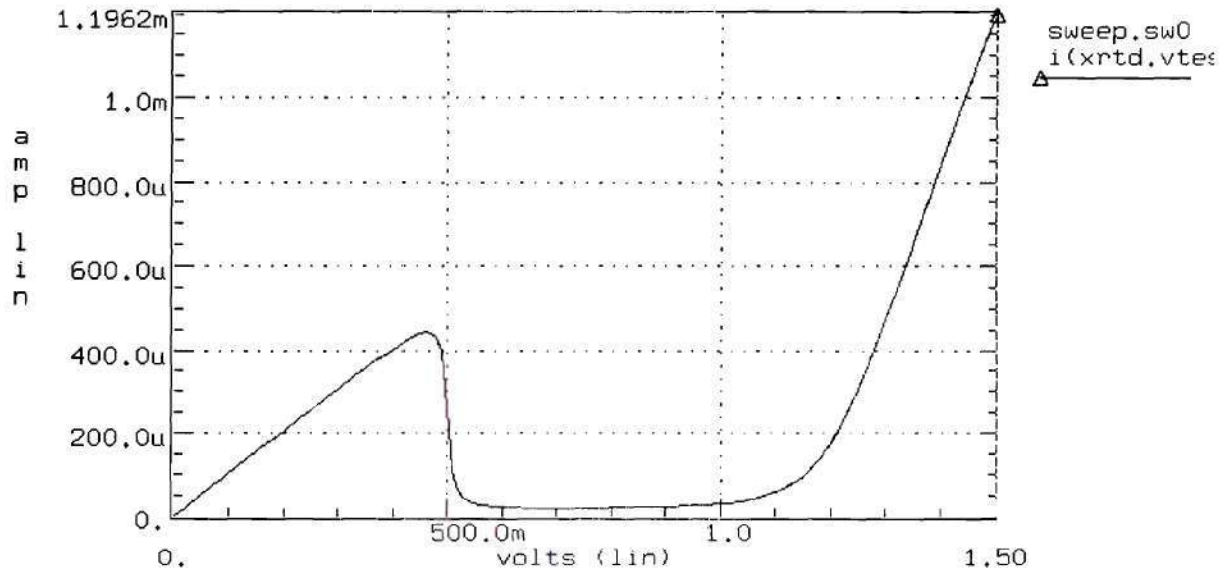


Figure 3.19 Modeled current-voltage characteristics of RTD for circuit simulations.

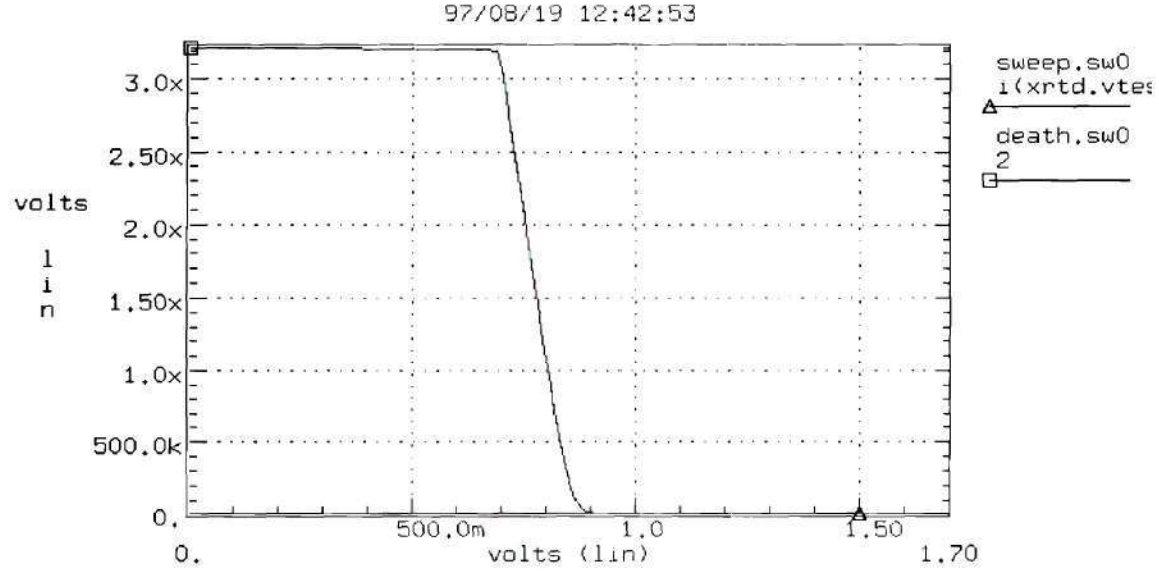


Figure 3.20 Simulated current-voltage characteristics of comparator circuit without RTD.

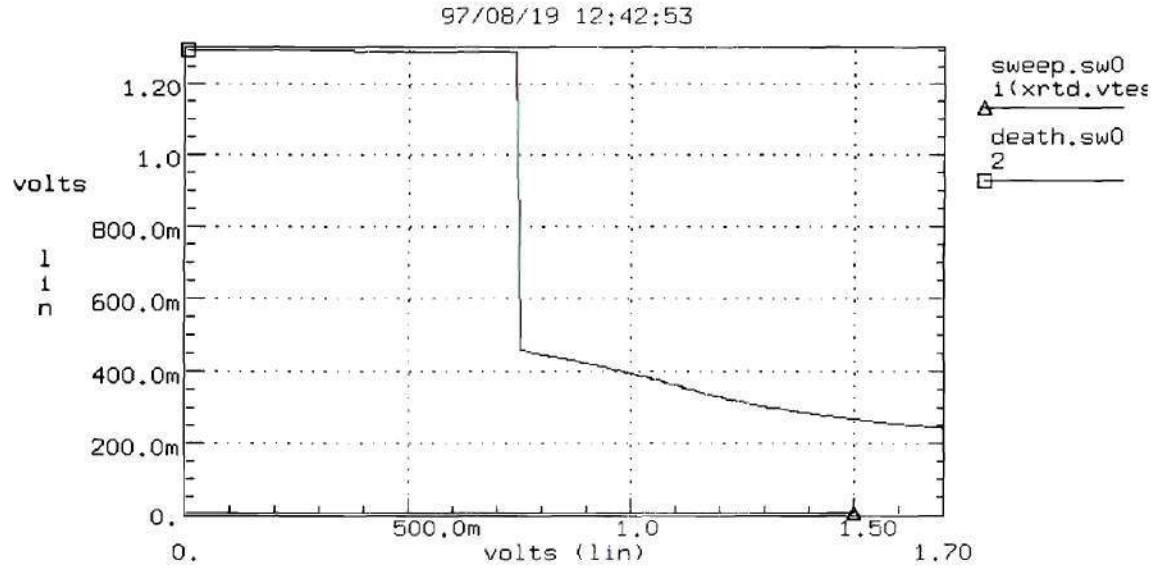


Figure 3.21 Simulated current-voltage characteristics of comparator circuit with RTD.

Finally, the comparator circuit was tested with and without an RTD integrated with it to compare the actual circuit performance with the simulated results. To test the circuit, a HP4145 was used. Figure 3.22 shows the bias conditions of the circuit.

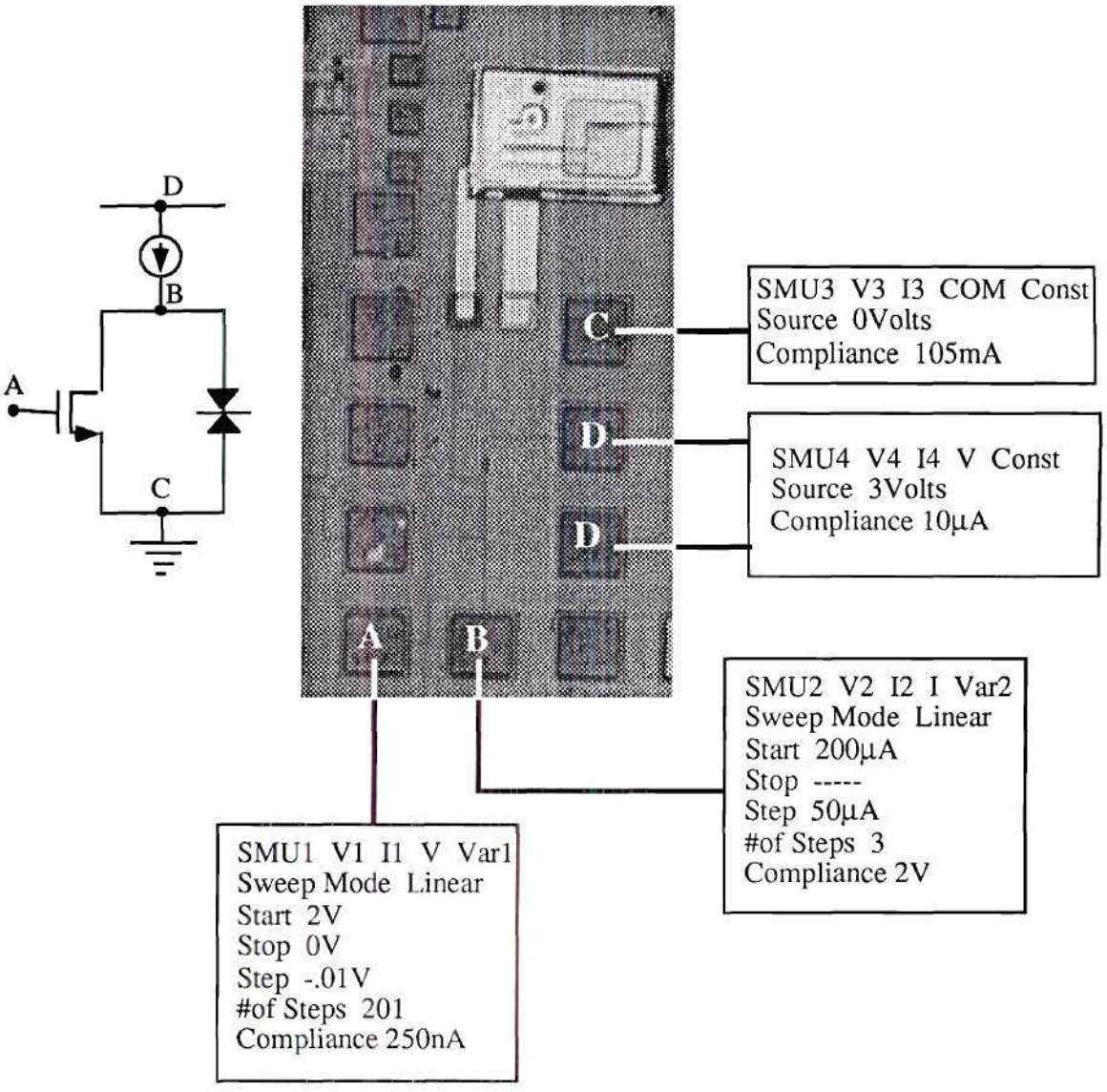


Figure 3.22 Bias conditions for testing of comparator circuit with InP-RTD.

Performance of the comparator circuit without the RTD is shown in Figure 3.23. The comparator circuit with the RTD characteristics are shown in Figure 3.24. The RTD switches when the current defined as I_2 reaches 300 μA. The switch occurred at a voltage difference of 0.6 volts since the sweep was in the negative direction, starting at 2 volts.

The performance of the circuit agreed well with the modeled circuit as well as what was expected after initial measurements on the I-V characteristics of the RTD device which had been integrated.

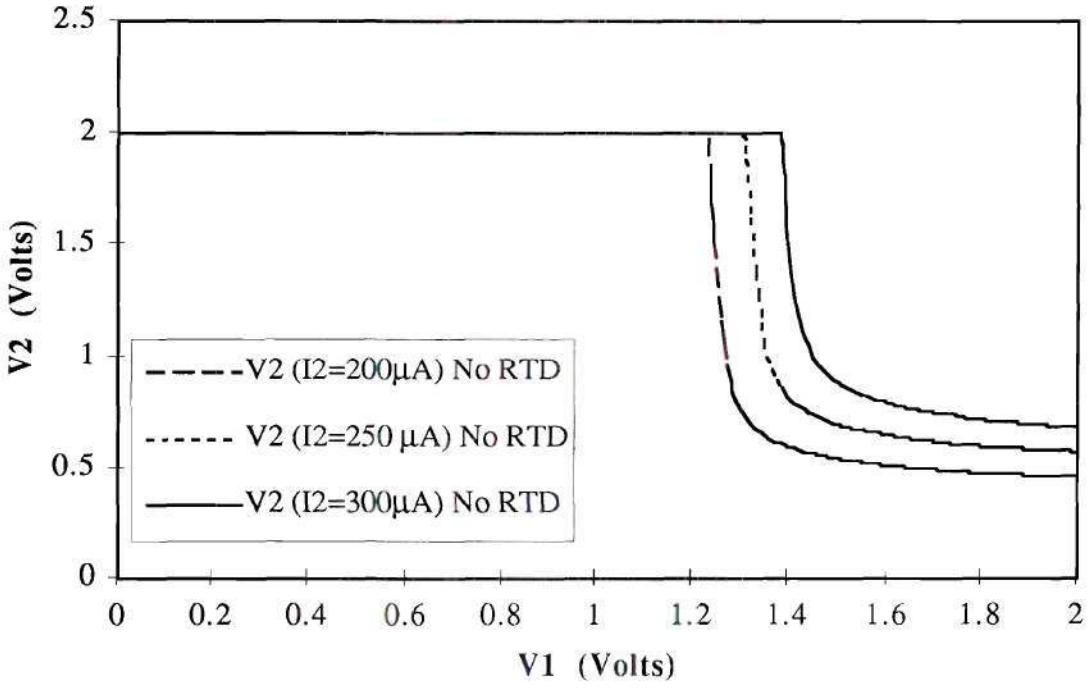


Figure 3.23 Measured current-voltage characteristics of comparator circuit without RTD.

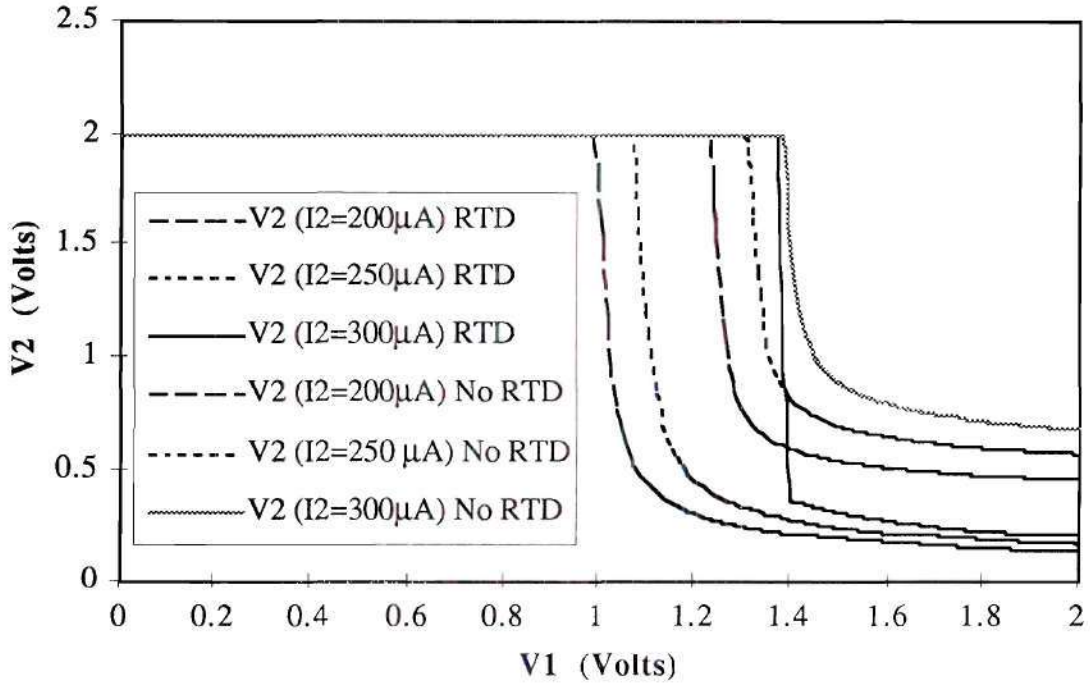


Figure 3.24 Measured current-voltage characteristics of comparator circuit with and without RTD. When the current reached 300 μA, the RTD switched.

In conclusion, the PVR of the RTDs represented the highest reported to date on silicon. Substrate removal and bonding provided an effective approach for the integration of high PVR resonant tunneling diodes with silicon electronics. After thin film process optimization, a thin film InP-based high PVR RTD was successfully integrated with a silicon comparator circuit. These results are the first successful demostration of InP based electronics bonded to a silicon host substrate and integrated with a conventional silicon circuit.

ENDNOTES

[1] R. Tsu and L. Esaki, *Appl. Phys. Lett.*, **22**(11), 562 (1973).

[2] L. L. Chang, L. Esaki, and R. Tsu, *Appl. Phys. Lett.*, **24**(12), 593 (1974).

[3] H. Mizuta and T. Tanque, *The Physics and Applications of Resonant Tunnelling Diodes*. Cambridge University Press, (1995).

[4] A. C. Seabaugh, A. H. Taddiken, E. A. Beam III, J. N. Randall, Y.-C. Kao, and B. Newell, *IEDM Tech. Dig.*, 419 (1993).

[5] F. Capasso, S. Sen, and F. Beltran, *High Speed Semiconductor Devices*. New York: Wiley, (1990).

[6] S. Sen, F. Capasso, A. Y. Cho, and D. L. Sivco, *IEEE Electron Device Lett.*, **9**, 533 (1988).

[7] R. C. Potter, A. A. Lakhani, D. Beyea, H. Hier, E. Hempfling, and A. Fathimulla, *Appl. Phys. Lett.*, **52**, 2163 (1988).

[8] T. Mori, S. Muto, H. Tamura, and N. Yokoyama, *Japan. J. Appl. Phys.*, **33**, 790 (1994).

[9] N. Evers, O. Vendier, C. Chun, M. R. Murti, J. Laskar, N. M. Jokerst, T. S. Moise, and Y.-C. Kao, *38th Electronic Materials Conference*, (1996).

[10] N. Evers, O. Vendier, C. Chun, M. R. Murti, J. Laskar, N. M. Jokerst, T. S. Moise, and Y.-C. Kao, *IEEE Electronic Device Letters*, **17**(9), (1996).

[11] Y.-C. Kao, A. C. Seabaugh, and H. T. Yuan, *4th Int. Conf. on InP and Rel. Mat.*, 489 (1992).

[12] T. P. E. Broekaert, W. Lee, and C. G. Fonstad, *Appl. Phys. Lett.*, **53**, 1545 (1988).

[13] J. H. Smet, T. P. E. Broekaert, and C. G. Fonstad, *J. Appl. Phys.*, **71**, 2475 (1992).

[14] O. Vendier, N. M. Jokerst, and R. P. Leavitt, *IEEE Photonics Tech. Letters*, **8**(2), (1996).

[15] C. Camperi-Ginestet, Y. W. Kim, N. M. Jokerst, G. Augustine, M. G. Allen, and M. A. Brooke, *IEEE Photon. Tech. and Lett.*, **4**(9), 1003 (1992).

[16] S. M. Fike, B. Buchanan, N. M. Jokerst, M. A. Brooke, T. G. Morris, and S. P. DeWeerth, *IEEE Photon. Tech. Lett.*, **7**(10), 1168 (1995).

[17] J. N. Schulman, H. J. De Los Santos, and D. H. Chow, IEEE Electron Device Letters, **17**(5), 220 (1996).

[18] R. C. Bowen, G. Klimeck, R. K. Lake, W. R. Fresley, T. Moise, submitted to *J. Appl. Physics*.

CHAPTER IV

TUNNELING HOT ELECTRON TRANSFER AMPLIFIER

The Tunneling Hot Electron Transfer Amplifier (THETA) is a three-terminal unipolar device whose ballistic transport properties have been extensively studied.[1] More recently, the effort to understand and improve the RF performance of these devices has increased because of their potential use in high speed applications.[2-4] To eventually integrate THETAs, or other three-terminal InP-based electronic devices with standard silicon circuitry, the characteristics of these devices before and after substrate removal and bonding to various host substrates were studied. The DC and RF performance of the thin film THETAs to develop direct high frequency interfaces with various host substrates were also analyzed.

4.1 Device Structure and Characteristics

The devices were fabricated by Raytheon/TI.[2, 3] The device layers were grown on semi-insulating InP by MBE. The layers from top to bottom consisted of a 500 Å n+ ($5x10^{18}$ cm^{-3}) InGaAs cap layer, a 2000 Å n-type $In_{0.52}Al_{0.4}Ga_{0.08}As$ emitter, a 20 Å AlAs tunnel barrier, a 400 Å n-type ($1x10^{18}$ cm^{-3}) InGaAs base, a 2500 Å $In_{0.52}Al_{0.3}Ga_{0.18}As$ collector barrier, and an 8000Å n+ InGaAs sub-collector. Through a self-consistent solution to Poisson's Equation, a conduction band energy profile for the THETA structure was calculated, as shown in Figure 4.1.[2] Electrons tunnel through the 20 Å AlAs barrier from the emitter into the base region of the device.[1,2] A fraction of these electrons thermalize within the base while the remainder travel ballistically over the

base/collector potential energy barrier and contribute to the collector current. The current gain is determined by the ratio of the collector current to the base current.

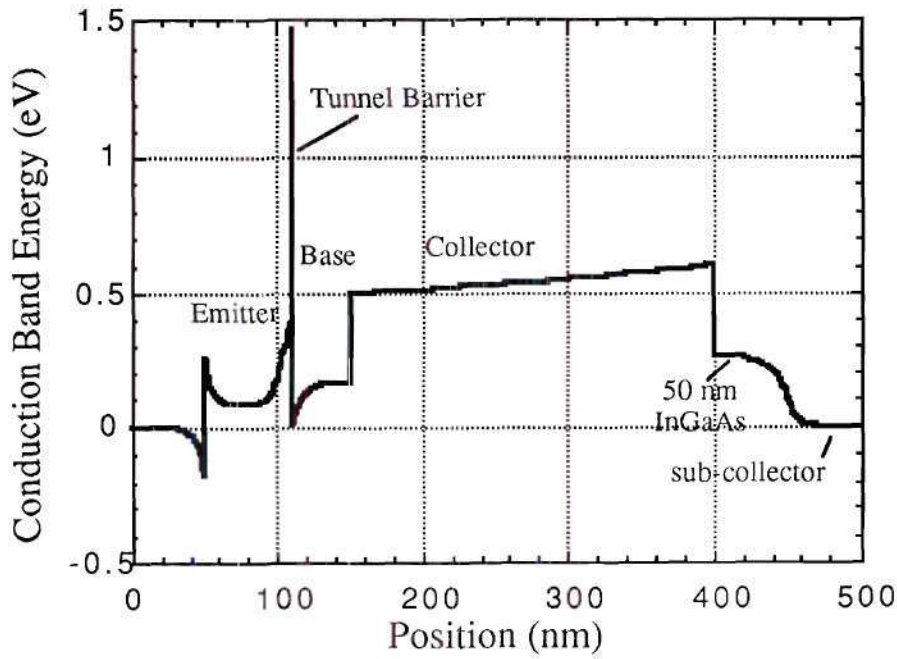


Figure 4.1 Computed conduction band profile for the Tunneling Hot Electron Transfer Amplifier. The emitter thickness has been reduced in the simulation so that the entire structure can be seen in one plot.

The THETAs were fabricated for a common emitter configuration and employed an air bridge contact structure. These air bridges remained intact during the substrate removal and bonding process, as shown in Figure 4.2 To protect the devices from the substrate removal etch and to give mechanical support to the 1.3 μm thick devices after substrate removal, a black wax handling layer was applied to the devices. The devices were submersed in an $HCl:H_3PO_4$ (3:1) etch solution to remove the InP substrate and were subsequently contact bonded to the host substrate as explained in Chapter 2.

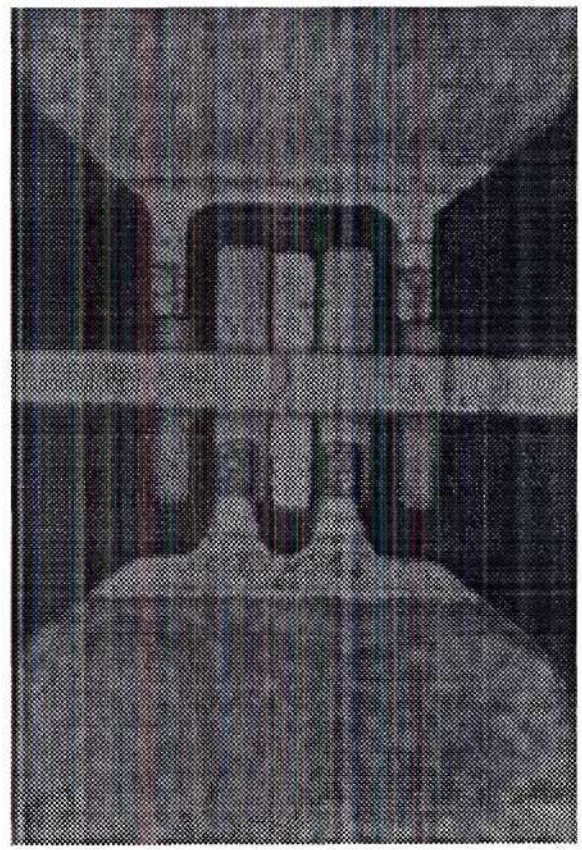


Figure 4.2 Close-up of thin film, 1.3 μm thick THETA device on silicon coated with 0.5 μm of silicon nitride.

Over 0.5 cm by 2 cm areas consisting of THETA devices and some test circuits have been bonded to silicon coated with 5000 Å of Si_3N_4, as shown in Figure 4.3. To study the effects of the substrate on the high frequency performance of the devices, a variety of host substrates including silicon, quartz, alumina, and sapphire were used in this experiment.

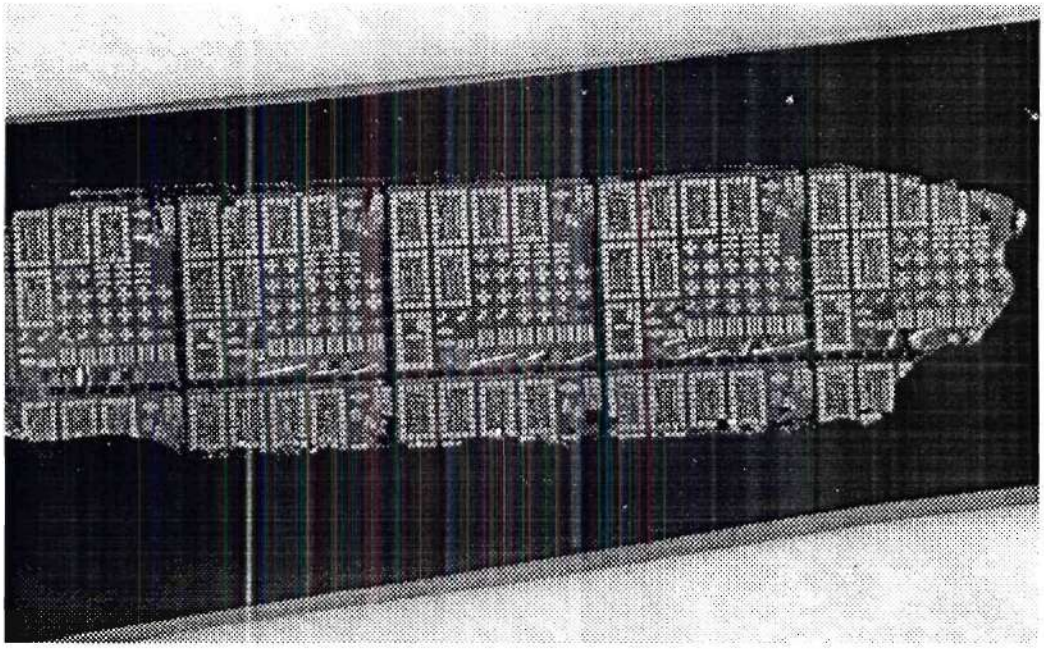


Figure 4.3 Thin Film THETAs bonded to Silicon Coated with 5000 Å Silicon Nitride.

4.2 Comparison of DC and RF Performance

DC and RF measurements of the THETAs were taken before and after substrate removal and bonding. Figure 4.4 shows the DC characteristics of a THETA device before and after substrate removal and bonding to a silicon wafer coated with 0.5 μm thick Si_3N_4. At the lower bias points (V_{CE} < 1.5 V), the current-voltage characteristics are nearly identical for the two cases. At the higher voltage, a slight collector current increase for the thin film device was seen. This change may be attributed to partial etching of the highly doped InGaAs collector during the substrate removal process and/or the non-optimized thickness of the dielectric between the thin film device and the host substrate. Other bonding and substrate removal techniques were investigated in Chapter V to optimize the DC and RF performance of the thin film device.

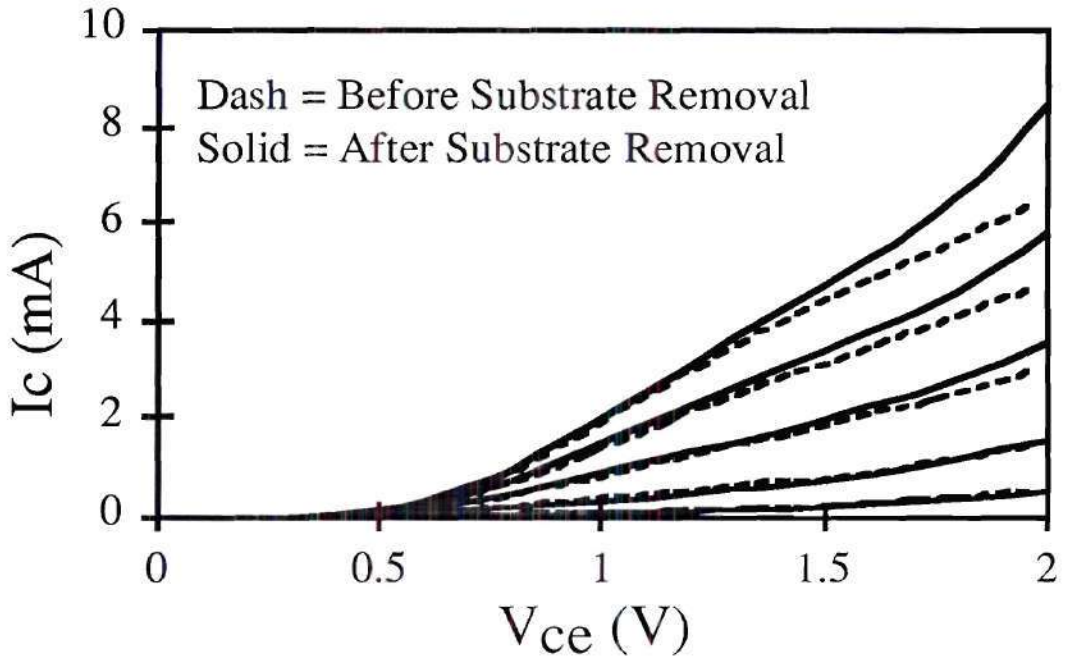


Figure 4.4 DC characteristics of a THETA before and after substrate removal and bonding to silicon coated with 0.5 μm of silicon nitride.

To separate the effects of varying substrates from those associated with the substrate removal and bonding process, we studied THETAs bonded to sapphire, quartz, and alumina host substrates as well as the Si_3N_4/Si substrates. For all cases, the DC current-voltage characteristics were similar to those shown in Figure 4.4 for the Si_3N_4/Si substrate sample. For all comparable DC operating points before and after substrate removal, the device cut-off frequencies, f_t in excess of 20 GHz and f_{max} of 17 GHz, were preserved for the thin film device on sapphire, quartz, and alumina.

Two of the most commonly used gain definitions are the maximum unilateral transducer power gain, GTU_{max}, and the short-circuit current gain, $/h_{21}/^2$. The maximum unilateral transducer power gain is defined as:

$$GTU_{max} = \frac{|S_{21}|^2}{\left(1+|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} \qquad (4.1)$$

when $\Gamma_S = S_{11}^*$, $\Gamma_L = S_{22}^*$ and Roller's stability factor,

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}S_{12}|} \leq 1 \quad (4.2)$$

where Γ_S is the source reflection coefficient, Γ_L is the load reflection coefficient, and the scattering (S) parameters for a two-port network are: S_{11} is the input reflection coefficient when the output port (port two) has a matched termination; S_{21} is the forward transmission coefficient when the output port (port two) has a matched termination, S_{12} is the reverse transmission coefficient when the input port (port one) has a matched termination, and S_{22} is the output reflection coefficient when the input port (port one) has a matched termination. The short circuit current gain is defined as:

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \qquad (4.3).$$

GTU_{max} provides an accurate estimate of maximum frequency of oscillation, F_{max}, and h_{21} extrapolated out to unity gain gives the current gain cut-off frequency, F_T.

Representative curves of the unity power gain, GTU_{max}, and short-circuit current gain, h_{21}, are shown in Figures 4.5 and 4.6, respectively. For all substrates, we observed

a small drop in gain for h_{21} and a larger drop for GTU_{max} at the lower frequencies. The only degradation in cut-off frequencies occurred in the 0.5 μm Si_3N_4/Si samples because of the conductivity of the silicon substrate. However, by increasing the dielectric thickness to several microns, the effect of the conductive silicon was eliminated, as presented in Chapter V.

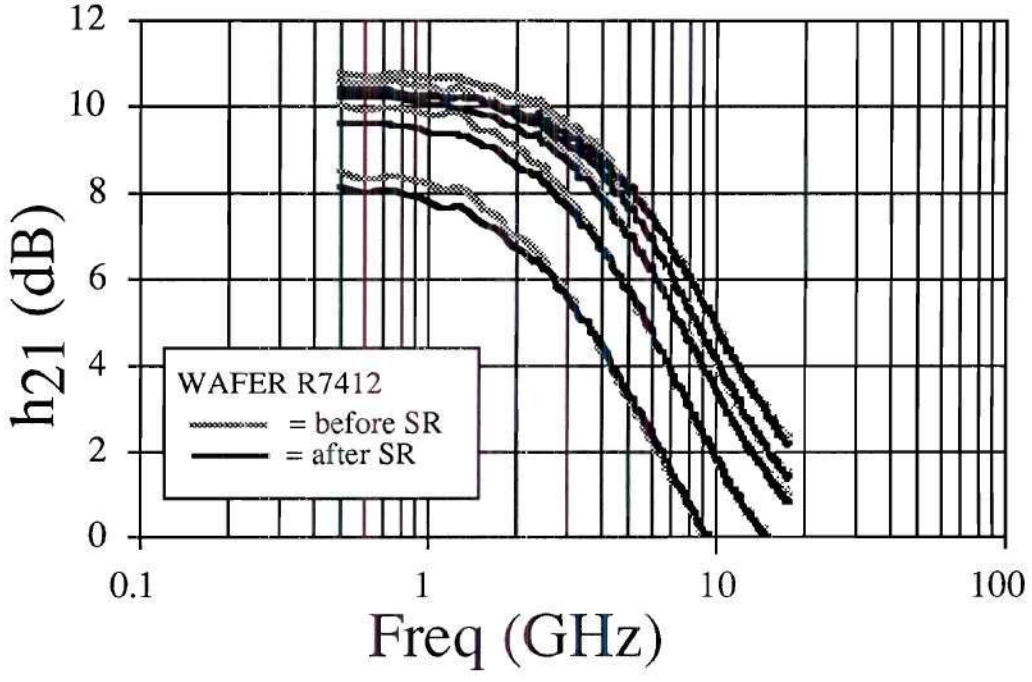


Figure 4.5 H_{21} of the THETA for V_{ce}=1.5V, I_b from 0.5 to 2.5 mA (0.5 mA steps), and I_c from 2.8 to 11.5 mA before and after substrate removal and bonding to sapphire. F_t exceeded 20 GHz for I_b>1.5 mA (I_c>6.8 mA). Similar characteristics were observed for the alumina and quartz host substrates.

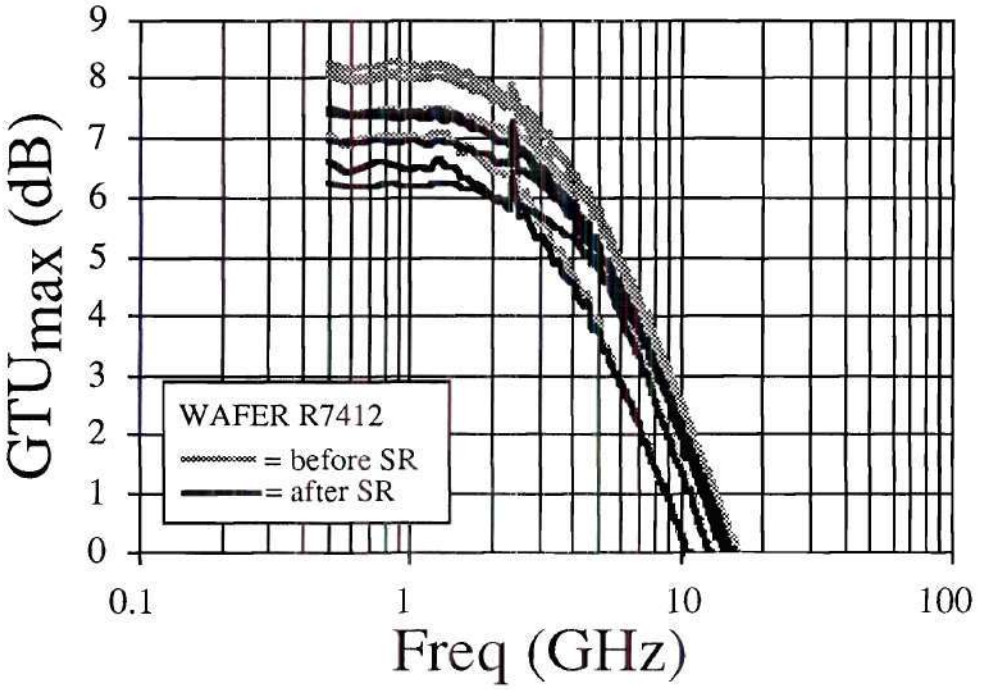


Figure 4.6 GTU_{max} of a THETA for V_{ce}=1.5V, I_b from 0.5 to 2.5 mA (0.5 mA steps), and I_c from 2.8 to 11.5 mA before and after substrate removal and bonding to sapphire. F_{max} was around 17 GHz for I_c=11.5 mA. Similar characteristics were observed for alumina and quartz host substrates.

ENDNOTES

[1] M. Heiblum, Solid State Electron. **31**, 617 (1988).

[2] T. S. Moise, Y.-C. Kao, and A. C. Seabaugh, Appl. Phys. Lett. **64**, 1138 (1994).

[3] T. S. Moise, Y.-C. Kao, A. C. Seabaugh, and A. H. Taddiken, IEEE Electron Device Lett. **15**, 254 (1994).

[4] M. R. Murti, J. Laskar, T. S. Moise, and Y. C. Kao, Proc. IEEE Cornell Conf. Adv. Concepts High Speed Semicond. Device Circuit, 234 (1995).

CHAPTER V

HETEROJUNCTION BIPOLAR TRANSISTORS

In 1957, H. Kroemer first proposed the heterostructure bipolar transistor (HBT).[1] The band structure diagram of the emitter-collector transition region of the device is shown in Figure 5.1. The bandgap offsets enhance electron flow from the wide bandgap n-type emitter to the low bandgap p-type base while inhibiting the flow of holes from the base to the emitter. Therefore, the efficiency of the emitter is higher than that of the homojunction in conventional bipolar transistors. Parasitic resistances and capacitances in the base can also be decreased by increasing the base doping in the HBT without any harmful effects to the emitter efficiency.[2]

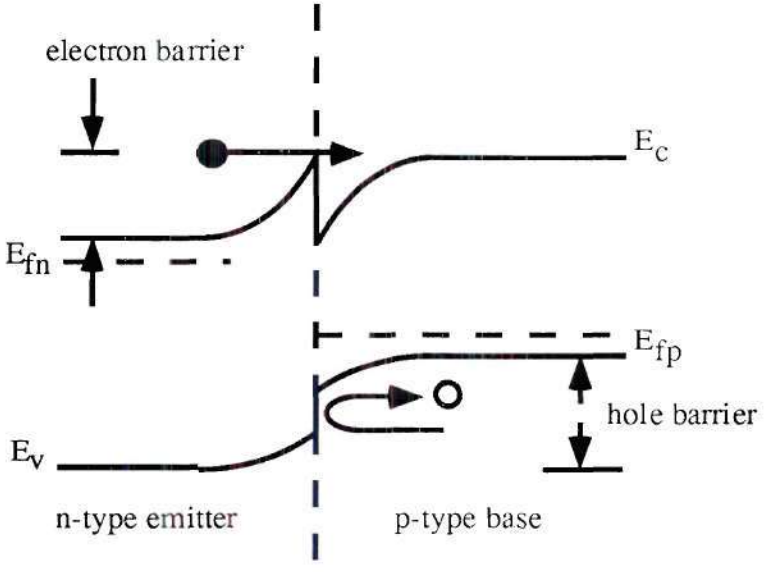


Figure 5.1 Energy band diagram of the emitter-base transition region of the HBT.[2]

5.1 InP-Based Single Heterojunction Bipolar Transistors

The HBT's in this study were InP-based single heterojunction bipolar transistors (SHBTs). The structure of these devices is shown in Figure 5.2. InP-based HBT's have an intrinsic advantage over GaAs-based HBT's for high-speed, low power, and high-gain digital, microwave, and optoelectronic applications. The smaller bandgap InGaAs reduces power consumption and produces a lower turn-on voltage. Also, the larger Γ-L separation of InGaAs (0.55) compared with GaAs (0.28) improves the high speed characteristics because of better velocity overshoot. The smaller surface recombination velocity of the InGaAs ($S_0 = 10^3$) compared with GaAs ($S_0 = 10^6$) is responsible for lower phase and 1/f noise, and no degradation of current gain resulting from device scaling. It was also believed that these devices would have improved reliability, reduced thermal hysteresis, and allow for lower chip operating temperatures than GaAs based devices since the thermal conductivity of InP (0.68 W/cm-K) is 50% higher than GaAs (0.46 W/cm-K). Since InP-based electronics are still in their infancy, the higher thermal conductivity of the InP substrate has not been utilized to its fullest advantage. This is due to the use of thick low thermal conductivity InGaAs in the single-heterojunction bipolar transistor (SHBT). The use of the InGaAs offsets any advantages from the higher thermally conductive InP substrate by significantly increasing the device junction temperature and the base-collector reverse saturation current. Since in the GaAs-based HBTs, the collector and subcollector consist of GaAs, this problem does not arise.[3]

The typical material structure of an InP-based SHBT consists of a n^+ InGaAs emitter cap, an n-type InP, InAlAs, or quaternary alloy such as InGaAsP and InAlGaAs emitter layer, a p^+ InGaAs base layer, a n^- collector layer, and a n^+ InGaAs subcollector. Advantages of InP-based double heterojunction bipolar transistors (DHBT's) over the SHBTs can be found in reference 3. The devices in this study were exclusively common-

emitter SHBT's with an InP emitter layer that were grown and fabricated at Raytheon/TI Systems. The high doping of the emitter cap, base, and subcollector layers are used for small emitter, base, and collector resistances, respectively. The lightly doped InGaAs collector layer is for small base-collector capacitance.

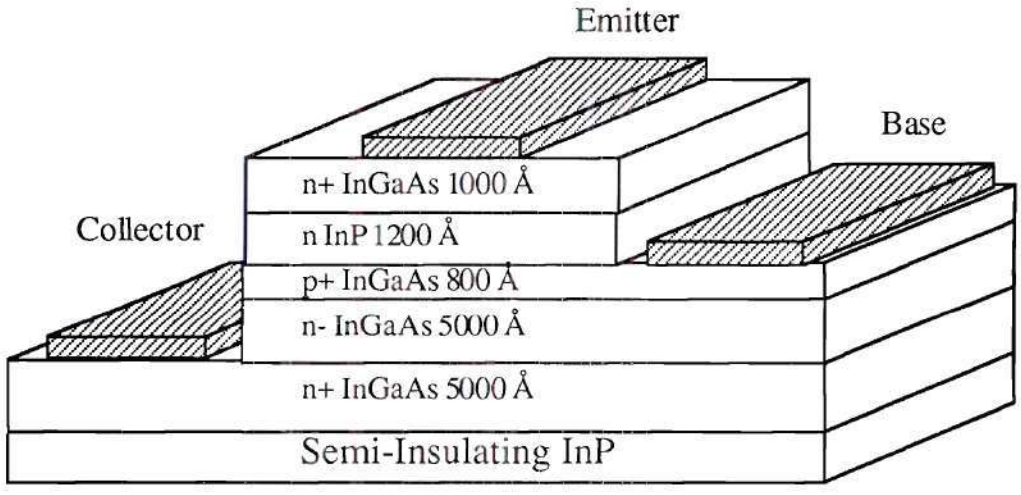


Figure 5.2 SHBT device structure used in this study.

The RF characteristics of an HBT depend largely on doping concentrations, base thicknesses, and collector thicknesses. Record high cut-off frequencies for InP-based HBTs of over 200 GHz have been achieved by utilizing very thin base (420 Å) and collector (1500 Å) layers.[4] Even though record high cut-off frequencies were achieved for thin collector layers, the corresponding open-base collector-emitter breakdown voltages were substantially lower.[4]

5.2 DC and RF Performance of Thin Film HBTs

In this study, thin (nominal thickness of 1.3 μm) InP-based HBTs were integrated onto silicon host substrates. The ability to eliminate the effects of the highly conductive and

lossy silicon substrate by utilizing a low loss polymer such as benzocyclobutene (BCB) between the thin film transistor and the silicon was investigated. The BCB was utilized instead of an epoxy because of its low dielectric loss at high frequencies.[5] The thin film device can be fully integrated with other on-wafer components using conventional integrated circuit (IC) processing techniques.

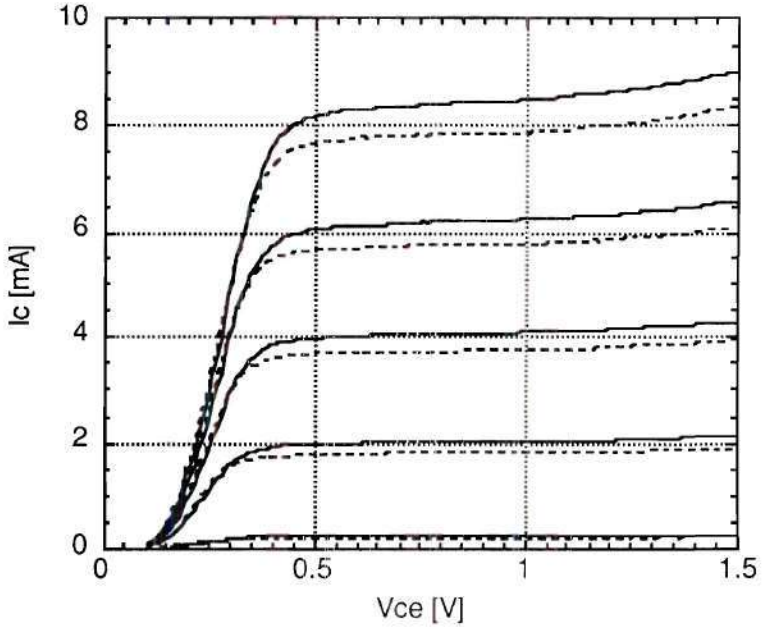


Figure 5.3 IV characteristics of HBT on-wafer (solid) and bonded to BCB on Si (dashed).

The S-parameters and I-V curves of an InP HBT before and after thin film integration were measured with a HP8510C network analyzer, HP4145 semiconductor parameter analyzer, and a Cascade on-wafer probe station. The DC performance of the devices, as seen in Figure 5.3, shows a slight drop in the collector current, which may be due to the partial etching of the highly doped InGaAs collector of the device during substrate removal. The more the device collector layer seemed to have been etched, the

larger the difference in collector current and the lower the break-down voltage of the device before and after bonding to the host substrate. This is consistent with numerous studies by Hughes on the result of variation of the thickness of the collector layer.[6] The breakdown voltage of the device may also have been affected by the bonding techniques used in this study. An increased junction temperature of the device after substrate removal resulting from the low thermal conductivity of the BCB and a weak adhesive bond may also have caused the break-down voltage to occur at lower biases.

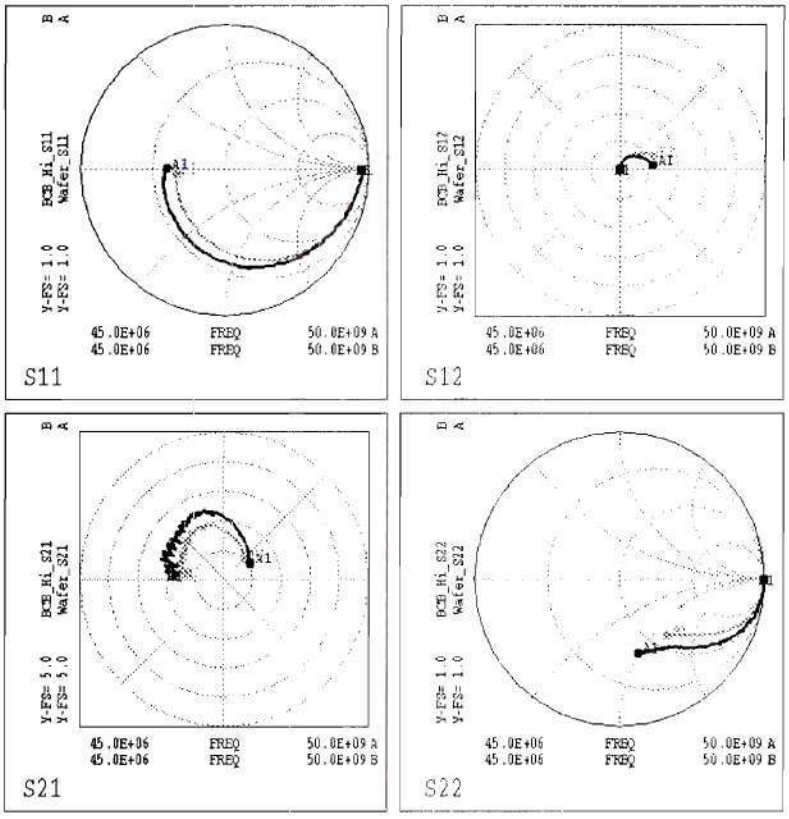


Figure 5.4 Comparison of S-parameters of HBT on-wafer (dark line) and HBT on BCB insulated Si substrate (gray line).

The S-parameters of the HBT are shown in Figure 5.4. They vary slightly, as do the curves of the unity power gain, GTU_{max}, and short-circuit current gain, h_{21}, as shown in Figures 5.5 and 5.6. Table 5.1 gives the different dielectric coatings and thicknesses used in this experiment to determine the optimum thickness and choice of dielectric between the thin film device and the lossy silicon substrate.

Table 5.1 Various Si host substrates and dielectric layers to which the HBTs were bonded.

Name	Material	Resistivity	Dielectric Layers
S1	Si	.375-.625 Ω cm	15 μm BCB
S2	Si	500-1000 Ω cm	15 μm BCB
S3	Si	0.01-0.02 Ω cm	0.5 μm Si_3N_4 15 μm BCB
S4	Si	.375-.625 Ω cm	7 μm BCB

The best performance was on the high resistivity silicon with 15 μm of BCB. The performance of this device was better than the on-wafer device. Since all of the devices measured were the same emitter area and were from same wafer, there was expected to be only a slight variation in the DC and RF characteristics between the devices. Considering the possible slight variations between devices, the trend was towards the high frequency characteristics including the cut-off frequencies, f_{max} and f_t , being preserved and possibly

slightly improved because of the thinner collector linked with the better isolation on the BCB/high resistivity silicon than the other host substrates.

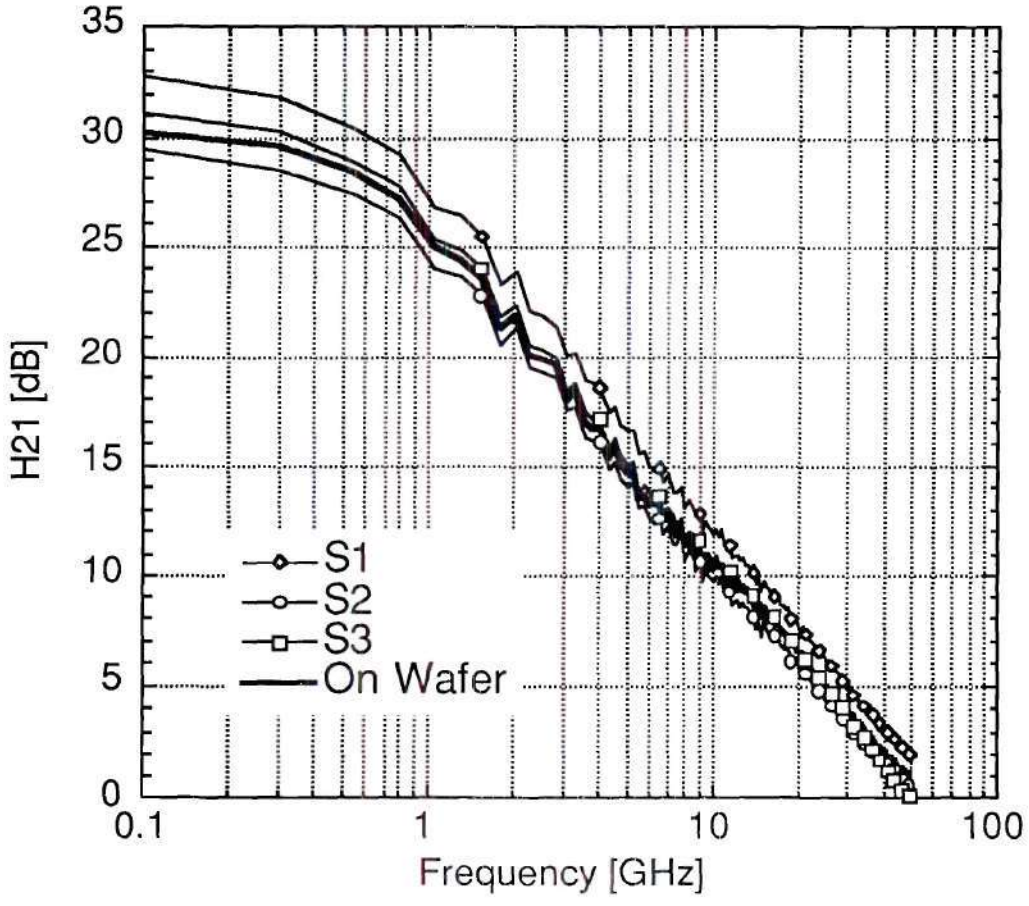


Figure 5.5 H_{21} **of HBT at Vce=1.5V Ic=2mA on various substrates.**

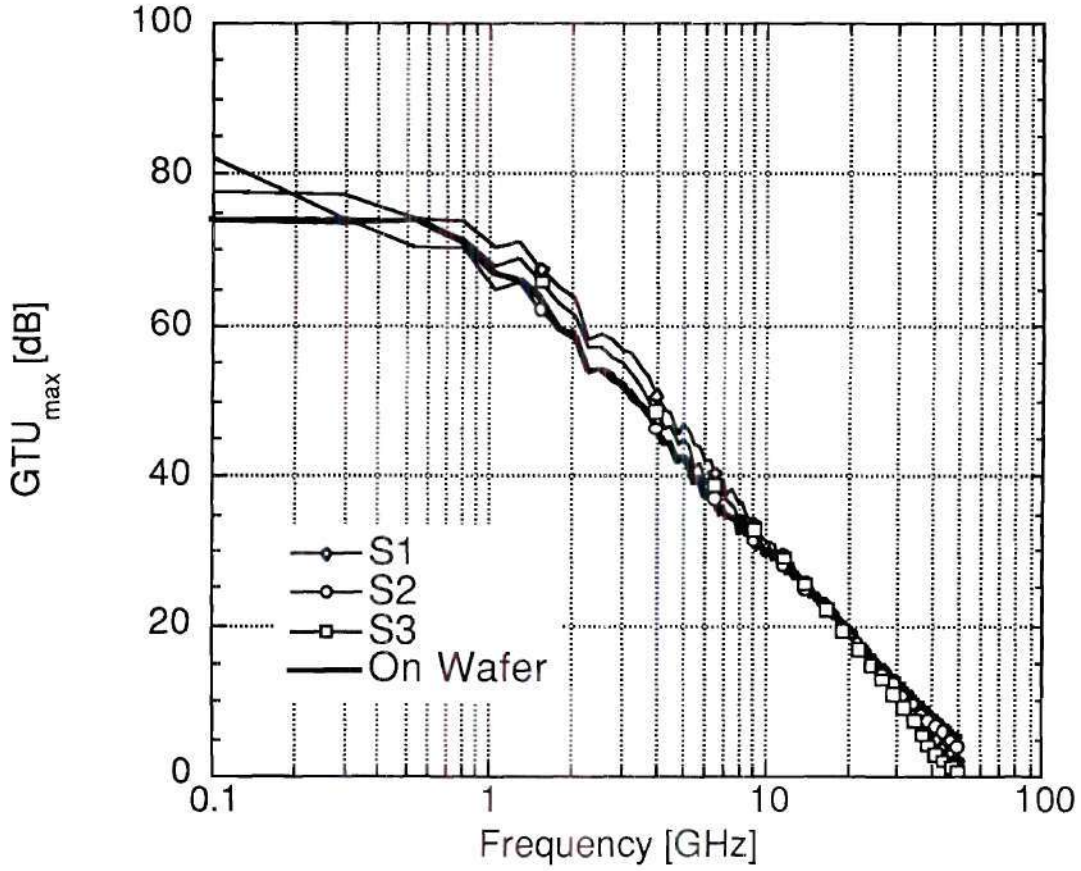


Figure 5.6 GTU_{max} of HBT at V_{ce}=1.5V and I_c=2mA on various substrates.

Since the evaluation of device performance is a combination of the DC and RF characteristics, a plot of DC β versus collector current and a plot of f_t versus I_c are shown in Figures 5.7 and 5.8.

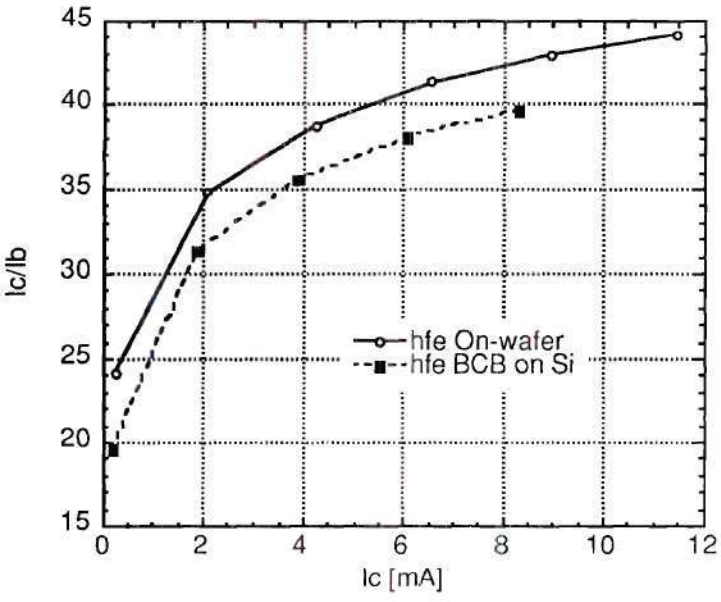


Figure 5.7 DC β vs. collector current plot of HBT before and after bonding to BCB on Si.

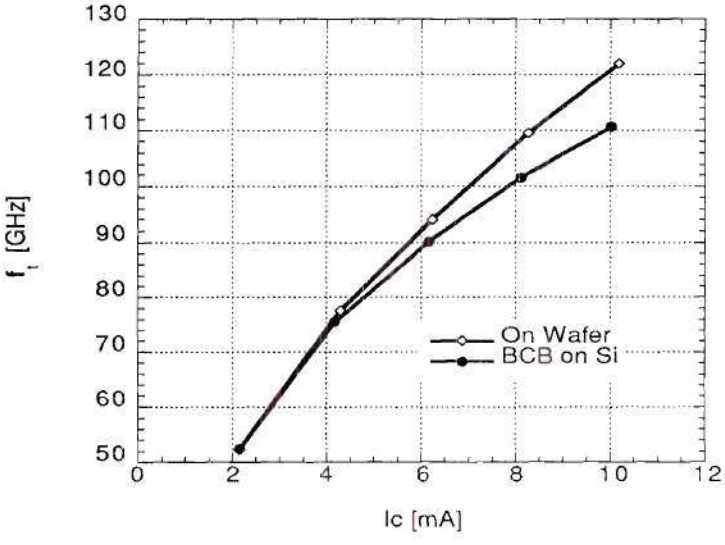


Figure 5.8 Comparison of HBT cutoff frequency verses I_c before and after integration to Si.

In conclusion, InP-based HBTs were removed from their growth substrate and bonded to various host substrates. By use of a layer of BCB over the conductive silicon substrate, the high frequency response of the device was preserved. A small degradation in the DC current was observed. This was believed to be due to partial etching of the InGaAs collector and could be eliminated by growth of a thin undoped InGaAs stop etch layer before the actual growth of the collector layer. These results represent the first step in the direction of thin film InP device integration with other host substrates for highly integrated systems.

ENDNOTES

[1] H. Kroemer, *Proc. IRE*, **45**(11), 1535 (1957).

[2] F. Ali and A. Gupta, HEMTs and HBTs: Devices, Fabrication, and Circuits, Artech House, 5 (1991).

[3] H.-F. Chau, W. Liu, and E. A. Beam III, *Microwave and Optical Tech. Lett.*, **11**(3), 114 (1996).

[4] J.-I. Song, K. B. Chough, C. J. Palmstrom, B. P. Van der Gaag, and W.-P. Hong, *IEEE Device Research Conf.*, IVB-5 (1994).

[5] V. B. Krishnamurthy, H. S. Cole and T. Sitnik-Nieters, *IEEE Trans. on Comp., Packaging, and Manufacturing Tech. - Part B*, **19**(1), (1996).

[6] K. R. Elliot, *Advanced Heterostructure Workshop*, Kona, Hawaii, (1996).

CHAPTER VI

THIN FILM INTEGRAL PASSIVES

The wireless communications market has been expanding exponentially, increasing the demand for high frequency analog circuits. The backbone behind most high frequency analog circuits are the integral passive components which can consume up to 70% of the real estate. The need for miniaturization, decreased weight, and full integration into a "chip-scale" package has become increasingly important to contend in this highly competitive market by reducing size and lowering cost. Thin film passive components are showing great promise in fulfilling these requirements.[1-13]

One option to lower cost is by transferring the passive components to cheaper substrates. Other options in mixed material integration include the use of low cost lossy substrates such as silicon or a free standing thin film device which can be laminated onto any substrate of choice. The direction of this investigation is into deposited thin film passive components on free standing polyimide, focusing on the characterization of these thin film passives before full integration into a multi-layer package.[1-3] The thin film inductors, capacitors, and resistors in this study were formed by deposition of the metals and dielectrics necessary to form the passive component of interest. A cross section of a free standing polyimide (flex) with two-sided integrated passives is seen in Figure 6.1

and a picture of resistor test element groups (TEGs) on flex is shown in Figure 6.2. Vias through the polyimide connect the passive components.

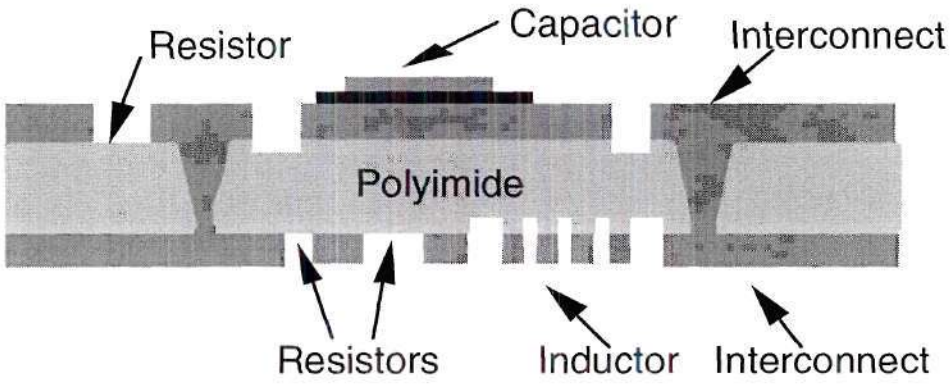


Figure 6.1 Cross-section of two-sided integrated passives on flex.

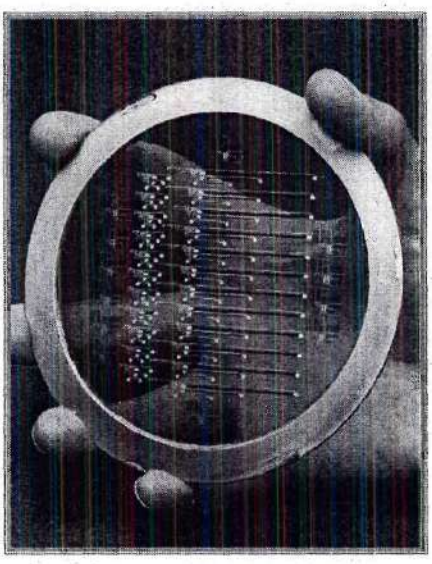


Figure 6.2 One of the smaller area flex consisting of resistor TEGs supported by a titanium frame.

For optimum performance, these devices need to be characterized from the microscopic view of the inherent material properties to macroscopic view of the actual device in a multi-layer module. This is necessary to determine the actual material limitations and the performance of a device which is processed to meet requirements for General Electric's (GE's) standard high density interconnect (HDI) technology. Solid state electronics is continuously pressing for smaller packages and it is, therefore, essential to determine the performance of the device not only as stand alone, but also when inserted into packages in which ground planes and other devices are densely packed together.

Characterization of the devices in this study is performed at DC, low frequency, and high frequency to evaluate the inherent material parameters, the device design, the

performance of the fabricated device before and after standard HDI passivation, and the effect of ground planes on the device microwave performance at near field distances.

6.1 Testing of Integral Passives

6.1.1 DC Testing of Thin Film Resistors

Initial measurements of the thin film resistors were made on a manual probe station. For yield measurements, resistors designed with only a single launch for DC measurements were automatically probed. The suite of equipment used to automatically probe the resistors was (1) a HP4062B parametric test system, (2) a Pacific Western Probe II semi-automatic probe station, (3) a Cerprobe ceramic blade probe card, (4) a HP3457A Multimeter with improved voltage resolution, and (5) the GE Supertest software.

The main algorithm used to measure the thin film resistors was a program named RES4T. When executed, the RES4T test connects the specified current source pin to a source measurement unit (SMU), the ground pin to a different SMU and the high sense and low sense pins to the terminals of the digital volt meter (DVM). The routine, Measure_r4t which is a general purpose four point kelvin measurement routine, is called, and the resulting resistance is stored in the database. The specified force current (Iforce) and voltage compliance (Vlimit) are passed to Measure_r4t which runs as follows:

1. Set the hold time between forcing current and measuring voltage (Thold) according to the current range:

- 10 seconds if I < 5 nA,
- 5 seconds if 5 nA < I <= 30 nA,
- 0.4 seconds if 30 nA < I <= 20 μA,
- 0.01 seconds if I > 20 μA,

2. Make connections.
3. Force Iforce on Hiforce pin.
4. Wait Thold.
5. Measure Vmeas.
6. Measure Imeas on Loforce.
7. Force 0 amps on Hiforce.
8. Measure V at 0 amps for thermal EMF correction. Thermal EMF, also known as thermoelectric voltage is voltage resulting from temperature differences within a measuring circuit or when conductors of dissimilar materials are joined together.
9. Subtract (8) from (5) to get corrected Vmeas.
10. If Iforce is more than 1% different than (6), in other words, input and output current are not equal, an error message is given.
11. Calculate resistance, R=Vmeas/Imeas.

Results from these measurements will be presented in section 6.2.2.

6.1.2 DC and Low Frequency Testing of Thin Film Capacitors

Initial capacitor values and dissipation factors were recorded using a HP4275A Multi-Frequency LCR Meter at 10 kHz. These values were used as comparisons to the 45 MHz data to determine the value of the parasitics at low frequency. After recording these initial values, a HP4083A switching matrix was used to switch to a HP4140A pA Meter and DC Voltage Source for destructive testing of the capacitor. Destructive testing of capacitors was performed at DC to determine breakdown voltage and leakage current of the thin film capacitors before and after top passivation. The devices were tested up to a 100 volts and breakdown was defined to be when the leakage current reached 1mA.

A Labview program was used to make the measurements up to 100 volts. The hold time was set to 4 seconds and the step delay time was set to 3 seconds. Measurements were varied between devices using the cathode high on one and the anode high on the next as defined in Figure 6.3 below to determine whether the devices behaved differently under different bias conditions.

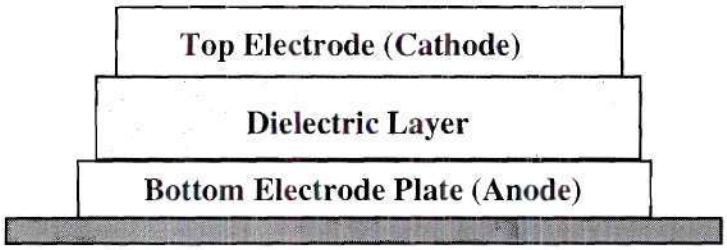


Figure 6.3 Cathode and anode definitions of the thin film capacitor.

Results from these tests will be presented in Section 6.4.1.

6.1.3 Microwave Testing of Integral Passive Components

An HP8510C Network Analyzer, Alessi probe station, 3.5 mm flexible cables, and 250 μm pitch ground-signal-ground probes custom designed by GGB to give a higher clearance were used to characterize the thin film components from 45 MHz up to 7 GHz. Data was collected by utilizing a PC with a customized C++ program which controlled the HP8510C. The program stored the Microsoft Excel® compatible s-parameter data in either magnitude or dB and phase, real and imaginary.

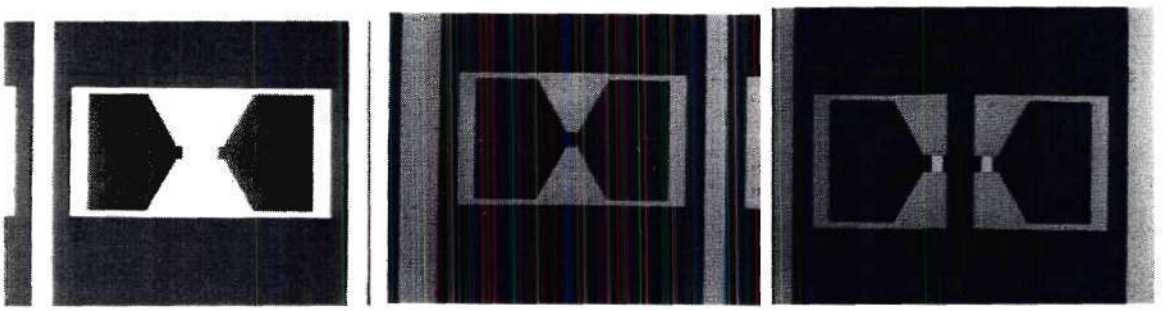
The frequency range was chosen primarily to support applications ranging from wireless communications to military radar systems. A total of 201 frequency data points were chosen for each frequency sweep, thus providing adequate frequency resolution over the frequency sweep.

To insure a good signal-to-noise (S/N) ratio for the measurements of these passive components, both power sources on the 8510C were set to 10 dBm and averaging was used. Line-reflect-match (LRM) calibration was performed using a C-5 calibration substrate from Picoprobe for off-wafer calibrations. The LRM calibration is based on test structures designed for reflects, a thru line, and a symmetric pair of resistors. The LRM calibration was chosen because it is more accurate at the higher frequencies than the short-open-load-thru (SOLT) calibration. Even though it has its weaknesses, it is similar to the thru-reflect-line (TRL) calibration when coupling between probes, and repeatability errors and multiple modes of propagation are not an issue.[14]

An off-wafer calibration is a calibration where the test structures used for the calibration are different than the launches in which the device under test (DUT) is

embedded. Therefore, the off-wafer calibration is less accurate than on-wafer calibration since accurate corrections for the transition between the launches and the DUT cannot be made unless one de-embeds through additional testing or modeling. Due to an absence of designed on-wafer calibration structures and since most of the launches were designed to 50 ohms, the errors in the transition between the launches and the DUT were not de-embedded from most of the devices under test. Therefore, there are some losses associated with the transition which lower the values of the quality factor from the actual value for the inductors and capacitors tested.

For the single-sided resistors composed of deposited TaN onto 1 mil thick polyimide, large launch pads were required. These coplanar launches without a ground plane could not be designed to a Z_0 of 50 Ω due to area limitations. Therefore, an on-wafer calibration was required. The on-wafer calibration corrected for the losses associated with the less than optimum launch pads. Pictures of the on-wafer test structures of an open, a 50 ohm match using thin film TaN as the resistor, and a thru can be seen in Figure 6.4. Verification of the on-wafer calibration was performed by first performing an off-wafer calibration and characterizing the on-wafer calibration structures. Since the launches were large, measurements would become invalid at a lower frequency point compared to the smaller 50 ohm launch pads with a ground plane. The 50 ohm calibration load was used to characterize its frequency limit by defining it to be accurate as long as the return loss remained below -20 dB. This was the case for the 45 MHz to 7 GHz frequency band.



(a) (b) (c)

Figure 6.4 (a) Open, (b) through, and (c) matched load on-wafer LRM calibration designs for de-embedding the resistor launches and transition region from one-side TaN resistors.

6.2 Thin Film Ta_2N Resistors on Flex

6.2.1 Design of Thin Film Resistors

Ta_2N was reactively deposited on free standing flex which was adhesively laminated taut on a 4 inch diameter titanium ring. Copper 3000 A thick was then sputter deposited and then electroplated to 4 μm. An optional top sputter deposition of 1000 A Ti was then deposited. The resistor was then patterned by a two step process: first, an oversized active area is opened and the Ti/Cu metal is selectively etched, thereby defining the resistor length. Then the interconnect lines and resistor width are patterned and etched.

Two different designs were fabricated using the ground-signal-ground launches for microwave testing of thin film resistors. One design shown in Figure 6.5 is a two

sided resistor design where the ground launches have vias through the flex to a ground plane on the back of the flex.

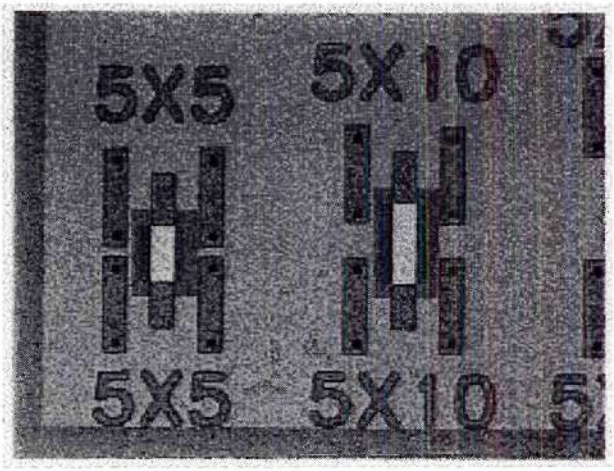


Figure 6.5 Mayo design of two-sided resistors with vias from top ground pads of microwave launches thorough the polyimide to the ground plate on the back of the free standing flex.

The second design was generated to determine the parasitic effects of the ground plane spacing on the thin film resistor performance. It was, therefore, designed without a back ground plane. This proved to be more complicated than expected since the ground-signal-ground launch pads that were required to obtain an impedance near 50 Ω launches were quite large. It is necessary to design as close to 50 Ω as possible in order to reduce the losses due to reflection of the launches. The launches were designed using the Maxwell finite element modeling tool and were not quite 50 ohms. Since the launches were large, approximately 1000 μm wide with 50 μm spacing, they were not accurate for use in measurements above 7 GHz. On-wafer calibration structures were fabricated to extract the effects of the non-optimized launches. This was also useful since the ground

plane distance from the resistors would vary depending on the final high density interconnect (HDI) design. The distance of the ground plane from the resistor also caused variations in the impedance of the launches, which ranged from about 40 Ω with the ground plane 1 mil away to about 60 Ω where the ground plane was an infinite distance away.

Serpentine and linear resistors, shown in Figure 6.6, were designed utilizing different lengths, line widths, and spacing to determine the limits of the designs. Designs similar to these were fabricated for DC testing of the resistors. These designs had a standard 100μm test pad in place of the large microwave launches.

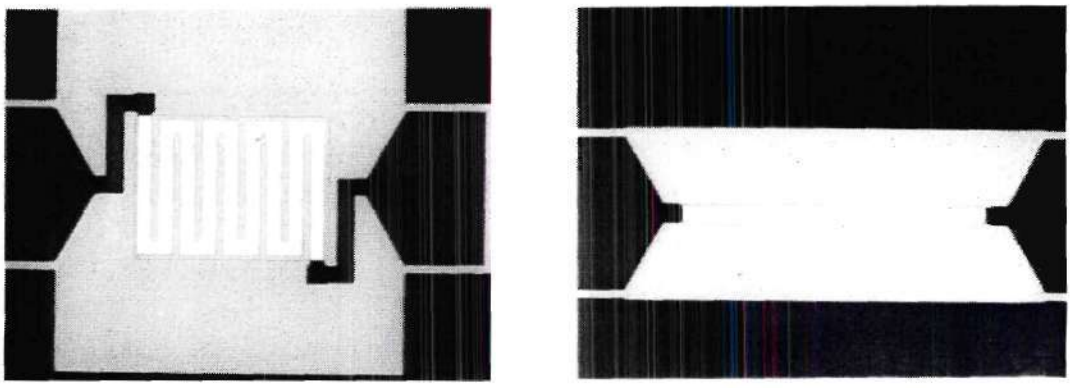


Figure 6.6 Serpentine and linear resistor designs for the single-sided resistors. To evaluate the design limits, length, width, and number of squares were varied.

6.2.2 Overview of DC testing of Thin Film Ta_2N Resistors

Using the structure and test methodologies outlined in previous sections, the following results were consistently achieved. Thin films, 250 and 1000 Angstroms, of

Ta_2N yielded 125 and 25 Ohms per Square. Excellent yields of greater than 98% were routinely demonstrated over numerous samples where the pass tolerance was less than 5% off target in resistance value. Thermal coefficient of resistance, TCR, for the material was found to be -100 to -75 ppm/°C, which is consistent with independent evaluation of Ta_2N on silicon substrates. Using the structure areas and power inputs, maximum power densities of 51 W/cm^2 were achieved with minimal drift in resistance over the two week evaluation period.[3]

Table 6.1 Summary of DC testing of some of the Ta_2N resistors.[3]

	250A Films	**1000A Films**
Resitivity (Ω/sq)	125	25
0603 Footprint **0402 Footprint**	**30K Ohms** **10K Ohms**	**6K Ohms** **2K Ohms**
Yield (%)	> 98%	> 98%
Tolerance (%)	< 5%	< 5%
TCR (ppm/°C)	-100	-75
Power Density (W/cm^2)	51	51

6.2.3 One- and Two-Port Resistor Extractions from S-Parameters.

The 1-port resistance measurement was performed by shunting one port of the resistor to ground. Therefore,

$$S_{11} = \frac{Z_L - Z_0}{Z_L + Z_0}. \qquad (6.1)$$

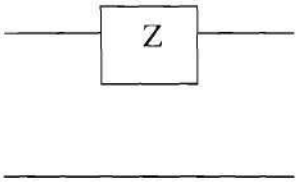
Solving for Z_L we get

$$Z_L = Z_0 \frac{(1 + S_{11})}{(1 - S_{11})}. \qquad (6.2)$$

Substituting in $Z_L = R + jX$ and $S_{11} = Re + jIm$ and solving for R,

$$R = Z_0 \frac{1 - Re^2 - Im^2}{(Re - 1)^2 + Im^2}. \qquad (6.3)$$

R was also extracted from S_{11} and S_{21} from the 2-port measurement using the same equations for R from the ABCD Matrix for series impedance between port 1 and port 2 to verify the results from the resistor shorted to ground. [15]



A=1 B=Z

C=0 D=1

For this ABCD Matrix S_{11} and S_{22} reduce to be equal.

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} = \frac{Z/Z_0}{2 + Z/Z_0}. \qquad (6.4)$$

Solving for Z,

$$Z = \frac{-2 \cdot Z_0 \cdot S_{11}}{(S_{11} - 1)}. \qquad (6.5)$$

Substituting in S_{11} = Re + jIm and Z = R + jωX:

$$R = -2 \cdot Z_0 \left[\frac{\mathrm{Re}^2 - \mathrm{Re} + \mathrm{Im}^2}{(\mathrm{Re} - 1)^2 + \mathrm{Im}^2} \right]. \qquad (6.6)$$

To check the resistance value from the 1-port extraction, a 2-port extraction was performed for S_{21}. For the same ABCD matrix given above, $S_{21}=S_{12}$.

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} = \frac{2}{2 + Z/Z_0}. \qquad (6.7)$$

Proceeding as before:

$$Z = \frac{2 \cdot Z_0 (1 - S_{21})}{S_{21}} \qquad (6.8)$$

Substituting in $S_{21} = \mathrm{Re} + j\mathrm{Im}$ and $Z = R + j\omega X$ to get:

$$R = 2 \cdot Z_0 \left[\frac{\mathrm{Re} - \mathrm{Re}^2 - \mathrm{Im}^2}{(\mathrm{Re}^2 + \mathrm{Im}^2)} \right]. \qquad (6.9)$$

The resistance values for the one and two port extractions correlated well.

6.2.3 Results

Figure 6.8 shows the resistance versus frequency for a set of resistors from the two-sided Mayo Foundation design shown in Figure 6.5. The values of the resistors shown varied from 100 Ω to 800 Ω and did not decrease significantly in the 1-2 GHz

range of interest. There was a significant drop in resistance at the higher frequency values for the 800 Ω resistor.

Since these designs did not have on-wafer calibration structures, the parasitics from the launches could not be extracted. Also, since the ground plane was 1 mil away, determination of parasitics associated with the near field ground plane was also an issue. To eliminate the effects of the ground plane and the launches, the one-sided resistor design was used.

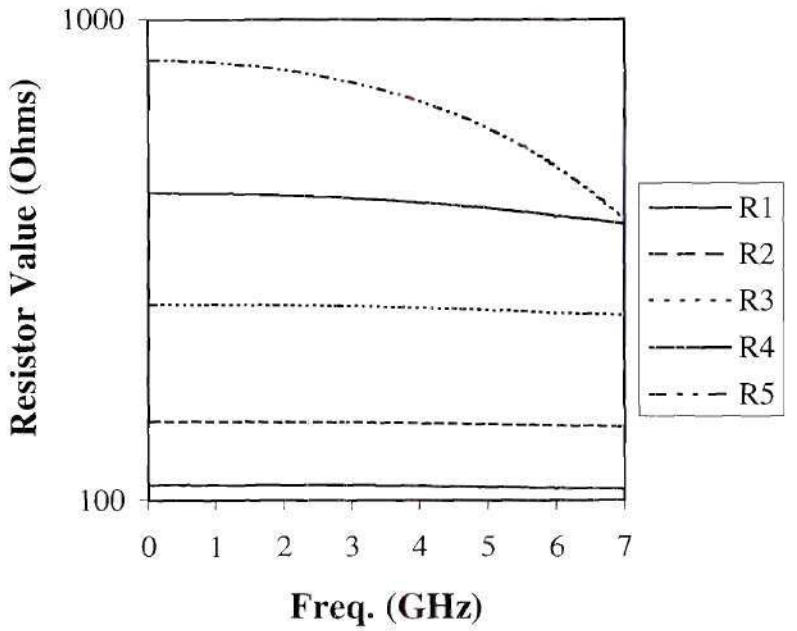


Figure 6.7 Two-sided resistor design results. Ground plane is on the back of the 1 mil flex.

The designs of the one-sided resistors varied in width and length of the lines for both linear and serpentine structures. The designs were analyzed from 45 MHz to 2

GHz. Tables 6.2 gives the size and length of the different designs, the impedence at 45 MHz, 1 GHz, and 2 GHz and Table 6.3 gives the percent off from the target value for each frequency point and the percent change of the resistor between these frequency points. The resistors beginning with "R" are linear resistors, "RN" are the same linear designs rotated 90 degrees, and "RS" are the serpentine resistors.

Table 6.2 Resistor designs for one sided resistors.

Resistor	number of squares	line width (um)	Rs (ohms/sq.) Target	Est. Rs (ohms/sq.) Obtained	Rs ohms Target	Rs @ 45MHz ohms	Rs @ 1 GHz ohms	Rs @ 2 GHz ohms
R1	50	42	93	91.2	4650	4479	4500	4699
R2	50	42	93	91.2	4650	4658	4681	4913
R3	50	60	93	91.2	4650	4792	4733	4590
R4	50	78	93	91.2	4650	4806	4581	3833
R5	50	60	93	91.2	4650	4656	4602	4473
R6	50	78	93	91.2	4650	4751	4534	3744
RS1	100	60	93	91.2	9300	9401	10468	7361
RS2	100	60	93	91.2	9300	9375	10497	7628
RS3	100	42	93	91.2	9300	9154	9317	7002
RS4	100	42	93	91.2	9300	9196	9356	6831
RS5	100	78	93	91.2	9300	9182	10975	9517
RS6	100	78	93	91.2	9300	8491	10260	9469
RS7	100	78	93	91.2	9300	8817	9300	9762
R7	20	42	93	91.2	1860	1815	1814	1824
R8	20	60	93	91.2	1860	1878	1879	1898
R9	20	78	93	91.2	1860	1932	1933	1959
R10	20	96	93	91.2	1860	1791	1785	1781
RN1	20	96	93	91.2	1860	1999	2001	2061
RN2	20	42	93	91.2	1860	1804	1804	1817
RN3	20	60	93	91.2	1860	1771	1772	1795
RN4	20	78	93	91.2	1860	1822	1824	1865
R12	10	42	93	91.2	930	848	846	846
R13	10	60	93	91.2	930	906	905	905
R14	10	78	93	91.2	930	909	909	911
R15	10	96	93	91.2	930	939	939	943
RN6	10	42	93	91.2	930	933	931	929
RN7	10	60	93	91.2	930	948	946	946
RN8	10	78	93	91.2	930	961	959	961
RN11	10	96	93	91.2	930	972	972	978
R11	1	60	93	91.2	93	83	83	83
R16	1	96	93	91.2	93	90	90	90
R17	1	78	93	91.2	93	87	87	87
RN5	1	60	93	91.2	93	85	85	85
RN9	1	96	93	91.2	93	95	95	95
RN10	1	78	93	91.2	93	90	90	89
R18	0.5	96	93	91.2	46.5	46	46	48
R19	0.5	156	93	91.2	46.5	48	48	48
R20	0.5	198	93	91.2	46.5	48	48	46
RN12	0.5	96	93	91.2	46.5	48	48	48
RN13	0.5	156	93	91.2	46.5	49	49	49
RN14	0.5	198	93	91.2	46.5	50	50	50

Table 6.3 Percentage off from target value and percent change for the single-sided resistor designs.

Resistor	number of squares	line width (um)	Rs ohms Target	% off Target 45 MHz	% off Target 1GHz	% off Target 2 GHz	45 MHz-1GHz % change	45 MHz-2GHz % change
R1	50	42	4650	3.7	3.2	1.1	0.5	4.9
R2	50	42	4650	0.2	0.7	5.7	0.5	5.5
R3	50	60	4650	3.1	1.8	1.3	1.2	4.2
R4	50	78	4650	3.4	1.5	17.6	4.7	20.2
R5	50	60	4650	0.1	1.0	3.8	1.2	3.9
R6	50	78	4650	2.2	2.5	19.5	4.6	21.2
RS1	100	60	9300	1.1	12.6	20.8	11.3	21.7
RS2	100	60	9300	0.8	12.9	18.0	12.0	18.6
RS3	100	42	9300	1.6	0.2	24.7	1.8	23.5
RS4	100	42	9300	1.1	0.6	26.5	1.7	25.7
RS5	100	78	9300	1.3	18.0	2.3	19.5	3.6
RS6	100	78	9300	8.7	10.3	1.8	20.8	11.5
RS7	100	78	9300	5.2	0.0	5.0	5.5	10.7
R7	20	42	1860	2.4	2.5	2.0	0.0	0.5
R8	20	60	1860	1.0	1.0	2.0	0.1	1.1
R9	20	78	1860	3.9	3.9	5.3	0.1	1.4
R10	20	96	1860	3.7	4.0	4.2	0.3	0.6
RN1	20	96	1860	7.5	7.6	10.8	0.1	3.1
RN2	20	42	1860	3.0	3.0	2.3	0.0	0.7
RN3	20	60	1860	4.8	4.7	3.5	0.1	1.4
RN4	20	78	1860	2.0	1.9	0.3	0.1	2.3
R12	10	42	930	8.8	9.0	9.1	0.2	0.3
R13	10	60	930	2.6	2.7	2.6	0.1	0.0
R14	10	78	930	2.2	2.3	2.1	0.1	0.1
R15	10	96	930	1.0	0.9	1.4	0.0	0.4
RN6	10	42	930	0.3	0.1	0.2	0.2	0.5
RN7	10	60	930	1.9	1.7	1.7	0.1	0.2
RN8	10	78	930	3.3	3.2	3.3	0.1	0.0
RN11	10	96	930	4.5	4.5	5.1	0.0	0.6
R11	1	60	93	10.5	10.5	10.7	0.0	0.2
R16	1	96	93	3.6	3.6	3.5	0.0	0.1
R17	1	78	93	6.0	6.0	5.9	0.0	0.1
RN5	1	60	93	8.6	8.5	8.8	0.1	0.2
RN9	1	96	93	2.0	2.0	1.8	0.0	0.2
RN10	1	78	93	3.8	3.7	3.9	0.1	0.2
R18	0.5	96	46.5	2.0	1.9	2.6	0.1	4.7
R19	0.5	156	46.5	2.2	2.3	3.6	0.1	1.4
R20	0.5	198	46.5	3.2	3.3	1.6	0.1	4.6
RN12	0.5	96	46.5	3.0	3.1	2.9	0.1	0.0
RN13	0.5	156	46.5	6.1	6.2	6.1	0.1	0.1
RN14	0.5	198	46.5	6.6	6.9	6.7	0.3	0.1

For the linear resistors over the frequency range of 45 MHz to 2 GHz, only three resistors fell outside the allocated +/- 5% change over the frequency range. The two resistors that showed a large change between 45 MHz and 2 GHz were the 50 square resistors with a line width of 78 μm. Due to the thicker line width, the length of the resistors were much larger than the other designs. Increased parasitics due to the longer length caused significant changes in the impedence. Resistance versus frequency for the linear resistors can be seen in Figures 6.8 and 6.9.

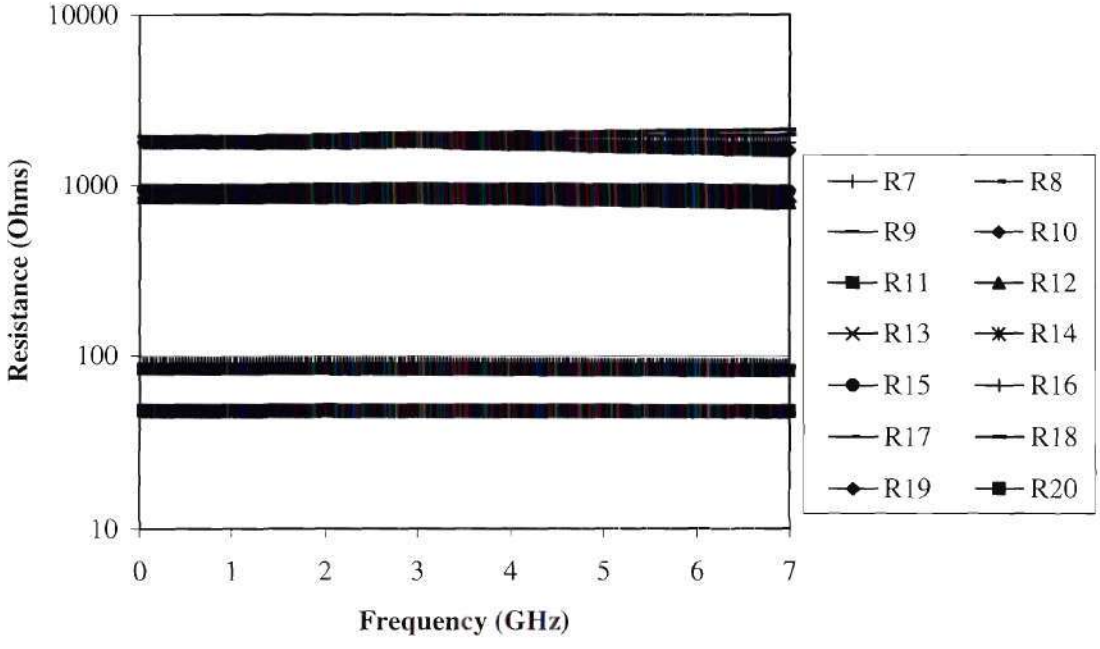


Figure 6.8 Linear resistors on flex.

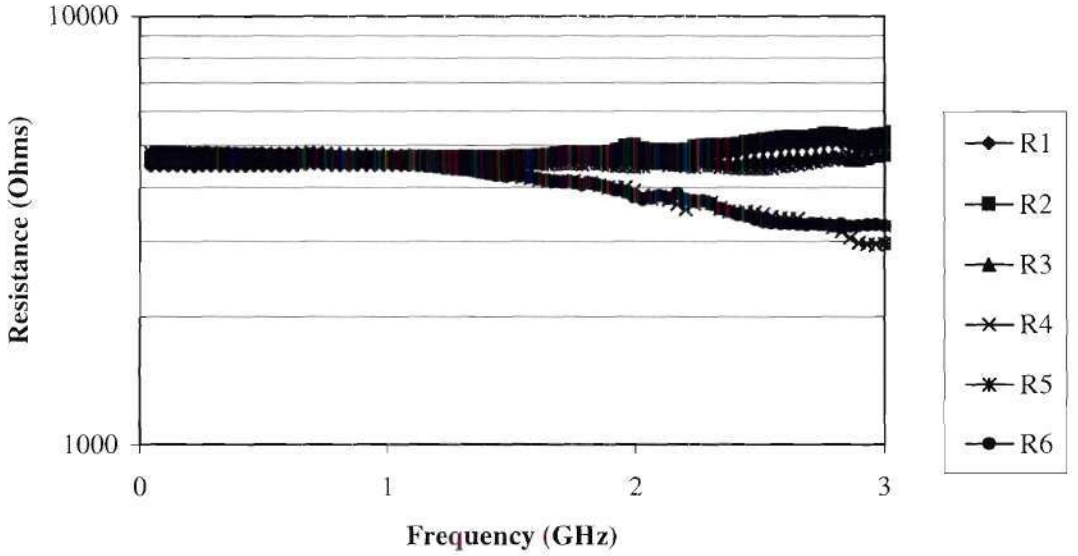


Figure 6.9 Linear long length resistors on flex. Higher parasitics are due to increased length of resistors.

The linear resistors rotated 90 degrees showed better agreement with the targeted values for most of the resistors over the frequency range of 45 MHz to 2 GHz, as shown in Figure 6.10. Since the resistors were patterned using direct write laser, these devices were used to evaluate the precision of the laser in both horizontal and vertical directions as well as determining any differences in impedence as a function of the direction patterned on the Kapton H ® polyimide material used for the free standing flex. A discrepancy in the vertical patterned direction on some of the linear resistors which were not rotated 90 degrees may have contributed to a small increase off of the target value. For tighter tolerance on resistor values, photolithographic patterning is necessary.

Overall, the direction of patterning on the Kapton H ® did not seem to show any consistent differences.

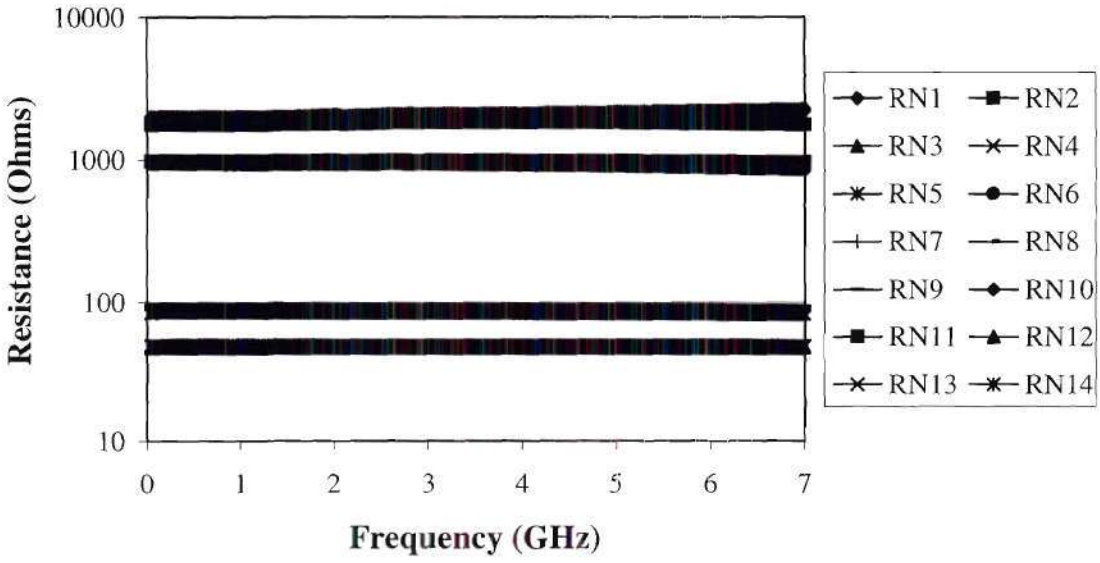


Figure 6.10 90 degree turned linear resistors on flex.

The serpentine resistors showed good agreement between the target value and actual value, well within the +/- 10% tolerance given for these higher value resistors. Increased parasitics for these resistors caused degradation of these resistors at lower frequencies when compared with the linear resistors. The increased parasitics can be partially attributed a to the higher resistive value of the resistor and due to capacitive coupling between lines.

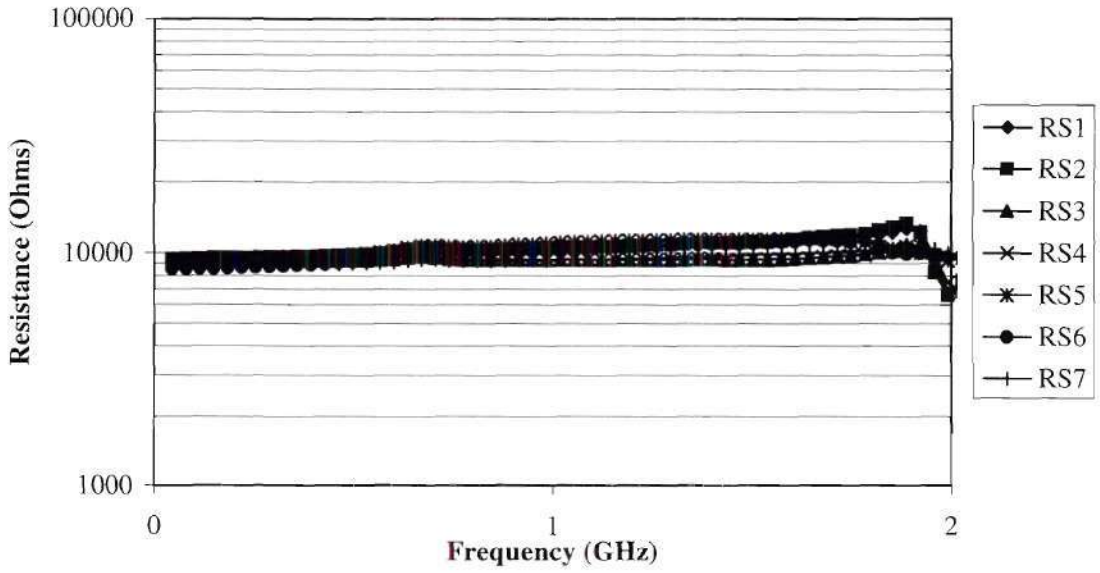


Figure 6.11 Serpentine resistors on flex. Higher parasitics than the linear resistors can be observed, partially due to capacitive coupling between lines.

6.3 Thin Film Inductors

Cu spiral inductors were fabricated on flex by laser patterning 3000 A of deposited copper, the sample then placed in a copper bath to yield a final copper thickness of 8 μm. Through vias in the polyimide were used to connect the inner port of the inductor. A picture of a 4 turn, 13.5nH inductor is shown below in Figure 6.12.

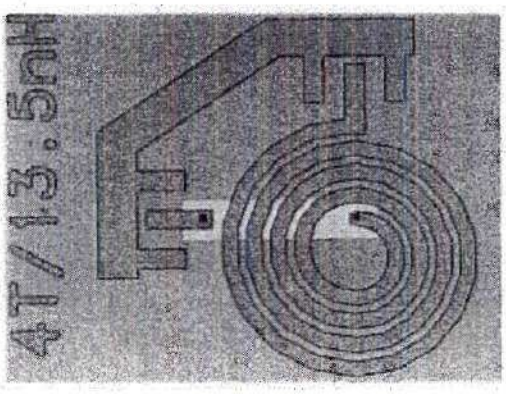
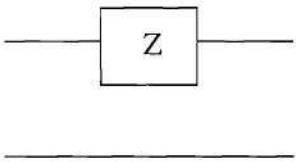


Figure 6.12 A 4 turn, 13.5 nH inductor fabricated on flex.

Inductor values in the TEG were designed to range from 3.4 nH to 208 nH. Inductance values measured at 45 MHz were found to be slightly higher than the designed values, ranging from 6.5 nH to 229 nH. This difference was expected since this is the first fabrication on flex with these designs. The models utilized were used to determine the trend and a first fabrication returns information so that a more accurate prediction can be made.

Section 6.3.1 Inductance and Parasitic Resistance Extraction from S-Parameters

One-port (S_{11}) extractions were performed from 2-port measurements utilizing the ABCD Matrix for a 2-port network consisting of a series impedance Z between ports 1 and 2, which is given below:



A=1 B=Z

C=0 D=1

For this ABCD Matrix, S_{11} and S_{22} reduce to be equal. This is a good approximation, but since the input and output parasitic inductance and resistance are not equal, S_{11} and S_{22} do vary slightly from one another. The difference in parasitics is a product of the variation in transitions between the input and output launches to the device under test. An on-wafer calibration which would remove the parasitics of the launches from the measurements would have produced more accurate and lower parasitic results. S_{11} is given by

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} = \frac{Z/Z_0}{2 + Z/Z_0}. \qquad (6.10)$$

Solving for Z,

$$Z = \frac{-2 \cdot Z_0 \cdot S_{11}}{(S_{11} - 1)}. \qquad (6.11)$$

Substitute in S_{11} = Re + jIm and Z = R + jωL:

$$R = -2 \cdot Z_0 \left[\frac{\mathrm{Re}^2 - \mathrm{Re} + \mathrm{Im}^2}{(\mathrm{Re} - 1)^2 + \mathrm{Im}^2} \right] \text{ and} \qquad (6.12)$$

$$L = \frac{2 \cdot Z_0}{\omega} \left[\frac{\mathrm{Im}}{(\mathrm{Re} - 1)^2 + \mathrm{Im}^2} \right]. \qquad (6.13)$$

Resonance is defined where ωL = 1/ωC or where Im = 0.

Q for a series resonant circuit is defined as

$$Q = \frac{\omega \cdot L}{R} = \frac{-\mathrm{Im}}{\mathrm{Re} - \mathrm{Re}^2 - \mathrm{Im}^2} \qquad (6.14)$$

To check the inductance value from the 1-port extraction, a 2-port extraction was performed for S_{21} where for the same ABCD matrix given above, S_{21}=S_{12}.

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} = \frac{2}{2 + Z/Z_0}. \qquad (6.15)$$

Proceeding as before:

$$Z = \frac{2 \cdot Z_0 (1 - S_{21})}{S_{21}} \qquad (6.16)$$

Substitute in $S_{21} = Re + jIm$ and $Z = R + j\omega L$ to get:

$$R = 2 \cdot Z_0 \left[\frac{Re - Re^2 - Im^2}{(Re^2 + Im^2)} \right] \qquad (6.17) \text{ and}$$

$$L = \frac{-2 \cdot Z_0}{\omega} \left[\frac{Im}{Re^2 + Im^2} \right]. \qquad (6.18)$$

Q values extracted from 2-port calculations have been found to be less accurate than the Q from a 1-port calcuation.[16] Since the parasitics are slightly different because the terminations of S_{11} and S_{22} are not the same, the Q was measured as a function of the input, S_{11}, 1-port measurements. Q's from the output, S_{22}, port yielded similar, but slightly lower Q's due to the parasitics of the vias and the return on the back of the flex. Q's measured from the output port were found to be on the average about 10% to 20%

lower at peak Q than the Q's measured from the input port. In other words, an inductor with a Q of 35 from S_{11} port yielded a Q between 28 and 31.5 from the output port.

Because of the more accurate determination of the inductor parasitics at the frequencies of interest from the 1-port measurement using the simplified extraction model, only the value of the inductance was checked using the 2-port measurement, while all parasitics were extracted from 1-port measurements. The 2-port measurement is very useful for determination of the value of the passive component to high frequency since it is more sensitive in the high frequency range that the 1-port measurement.

Section 6.3.2 Results

Initial results for the Q and the inductance were done under ideal circumstances. The measurements were performed assuming a far field ground plane. This was defined as a ground plane at least 500 mils away. These measurements were performed to separate the degradation of Q due to a near field ground plane from the actual Q of the inductor under ideal conditions. Measurements made with the ground field 90 mils away produced similar results.

To obtain an accurate Q value of the inductor it was necessary to bring the probes down into the metal of the launches. Since these probes required a steeper angle for added clearance, they traveled across the launch more than regular probes. This caused some damage after repeated measurements and caused some degradation in the Q of the inductor. Some differences in Q after repeated measurements on the same inductor can be attributed to this damage.

Figures 6.13 and 6.14 show the results from one-port extractions of the inductance and Q verses frequency for the far field (ground plane more than 90 mils away) measurements.

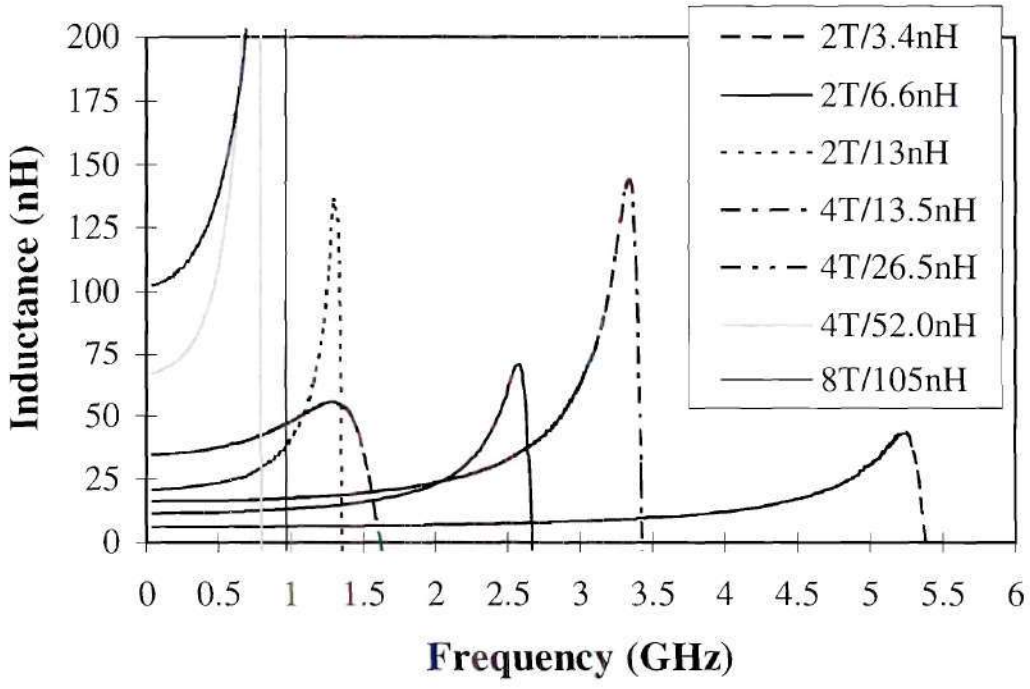


Figure 6.13 Inductance verses frequency for different inductance values and designs for ground plane over 90 mils away.

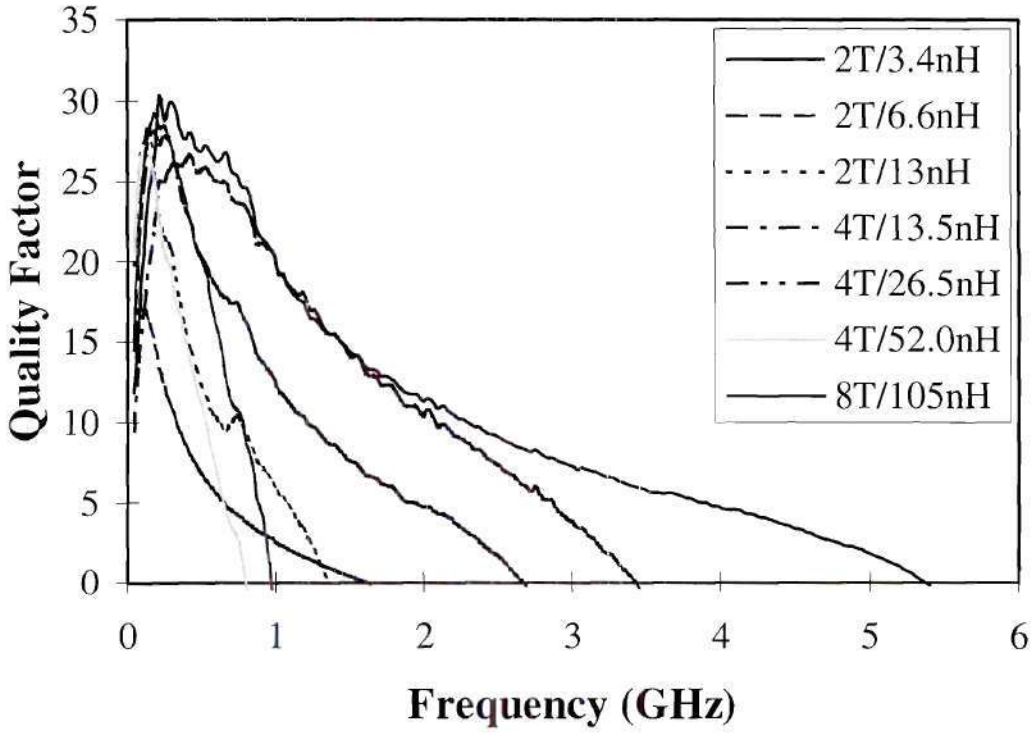


Figure 6.14 Quality Factor, Q, of thin film inductors on flex with far-field (over 90 mils away) ground plane.

The resonant frequency, peak Q value and frequency varied not only because of inductance value, but also because of the particular design. Designs varied in number of turns, line widths, and line spacing of the inductors. Also, the launches and line width of the return was varied. A summary of the high frequency response for some of the inductors is given in Table 6.4. Design parameters are shown in Table 6.5.

Table 6.4 Summary of high frequency response for some inductors with ground plane over 90 mils away. * notes these structures were not tested.**

Ref	Structure	Inductance (nH @45MHz)	Quality (Qmax)	Qmax Freq.	Resonant Frequency
hu586f3/11	2T/3.4nH	6.3	30.3	220 MHz	5.4 GHz
hu586f3/11	4T/13.5nH	16.3	26.5	428 MHz	3.45 GHz
hu586f3/11	2T/6.6nH	11.6	28.1	185 MHz	2.7 GHz
hu586f3/11	4T/26.5nH	34.7	17	116 MHz	1.65 GHz
hu586f3/11	8T/105nH	102.4	29.2	185 MHz	985 MHz
hu586f3/11	4T/52.0nH	66.8	26.8	116 MHz	811 MHz
hu586f3/11	2T/13nH	20.7	28.3	150 MHz	1.37 GHz
hu586f3/11	8T/208nH	***	***	***	***
hu586f3/11	2T/XXXnH	***	***	***	***
hu586f3/22	2T/13nH	18.7	26.8	81 MHz	880 MHz
hu586f3/11	2T/XXXnH	13.7	9.9	428 MHz	1.68 GHz
hu/21	2T/3.4nH	6.4	34.4	289 MHz	5.47 GHz
hu/21	4T/13.5nH	16.6	26.8	428 MHz	3.45 GHz

Table 6.5 Specifications of inductor designs, and predicted and measured inductance.

L_{Design} (nH)	Number of Turns	Line Width (μm)	Line Spacing (μm)	Diameter (μm)	$L_{Meas.}$ (nH)
3.4	2	200	50	1648	6.3
6.6	2	451	50	3333	11.6
13	2	1000	50	6728	20.7
13.5	4	100	50	1590	16.3
26.5	4	224	50	3204	34.7
52	4	501	50	6486	66.8
105	8	113	50	3150	102.4
208	8	250	50	6348	

The predicted value and measured value of the inductors did not correlate well. To try to determine more accurately the value of the inductor without an initial lot fabrication to establish the trend, other models were evaluated. Many have modeled thin film inductors.[5,8,13] Many of these models are based on the derivations established in Greenhouse's paper on the design of planar inductors which gives the basic mathematical concepts and the effects of film thickness and frequency on the mutual-inductance

parameter of planar inductors.[17] By using these derivations, models were developed for the smaller inductor designs. Crols et. al. introduced a model for planar inductors on low doped silicon.[13] Utilizing this model we were able to accurately fit the inductance values, parasitic resistance and Q at the lower frequencies, but the model's parasitic resistance, increased substantially with frequency. For example, the 6.6 nH designed inductor with measured value of 11.6 nH was modeled. At 45 MHz the model's inductance was 11.7 nH and it's parasitic resistance was 0.12 Ω giving a Q of 27.4. Unfortunately, the model's reduced line width formula to compensate for skin effect was found to be extremely inaccurate. At 1 GHz, the model predicted an increase in series resistance by over 100, giving a Q of 3. The measured Q at 1 GHz was 20 which is almost a factor of 10 hiher than the model predicts. The inductance values matched the measured inductance values within 10% for all the smaller 2 turn inductors and was able to accurately predict the trend, but was inaccurate for the higher value 4+ turn inductors.

A factor of note for the thin film planar inductors when placed in densely packed and multiple stacked modules is the effect of the distance of the ground plane or other conductive structures close to the inductor on the quality factor of the inductor. The closer the ground plane distance to the inductor, the lower the quality factor due to increased parasitic coupling capacitance and resistance. When the ground plane is on the back side of the 1 mil flex, the inductance value and Q are reduced as seen in Figures 6.15 - 6.18. Therefore, for these inductor designs, a trade-off between Q and density of packing must be made.

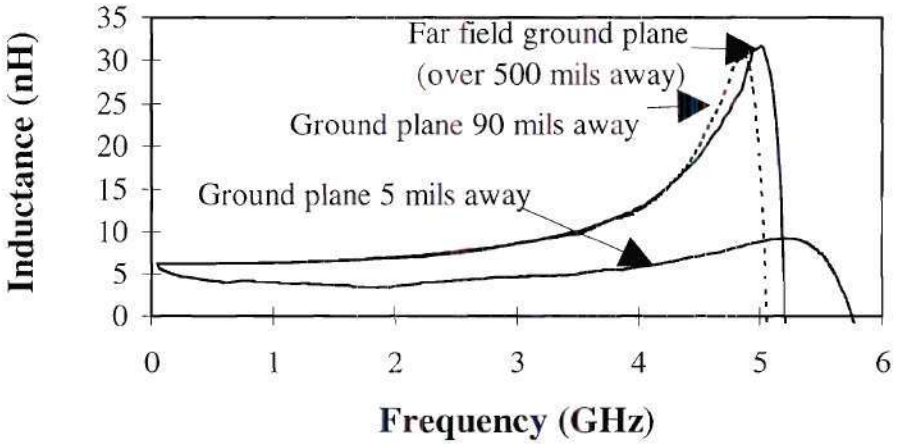


Figure 6.15 Measured inductance vs. frequency for the 3.4 nH inductor design with the ground plane distance varied. Measured inductance value was 6.3 nH.

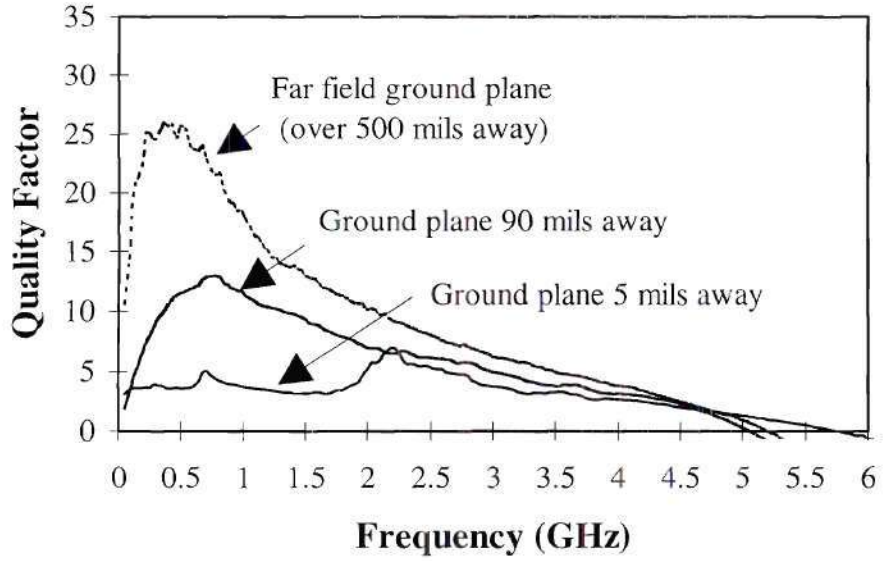


Figure 6.16 Changes in quality factor vs. frequency for the 3.4 nH inductor design as a function of distance of ground plane.

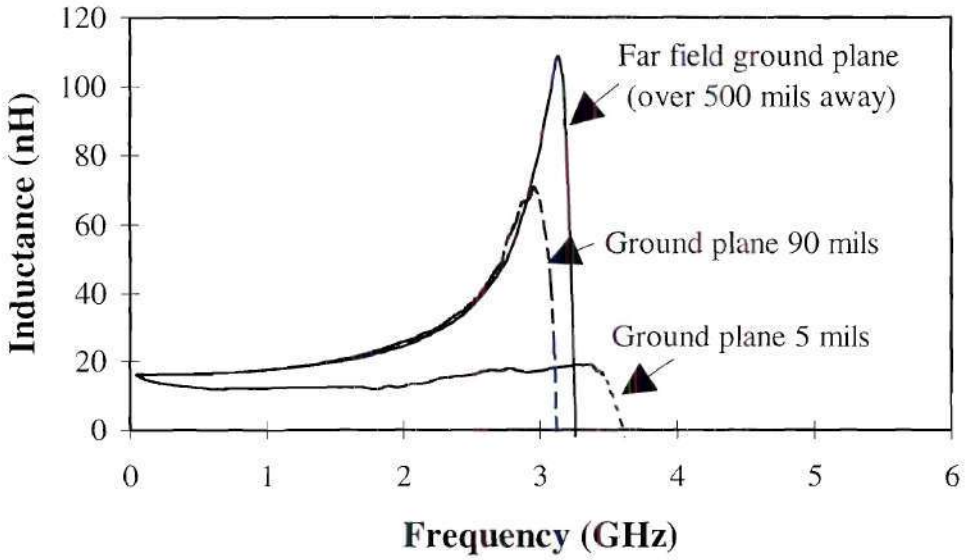


Figure 6.17 Measured inductance verses frequency for 13.5 nH inductor design with the ground plane distance varied. Measured inductance was found to be 16.6 nH with far field greater than 90 mils away.

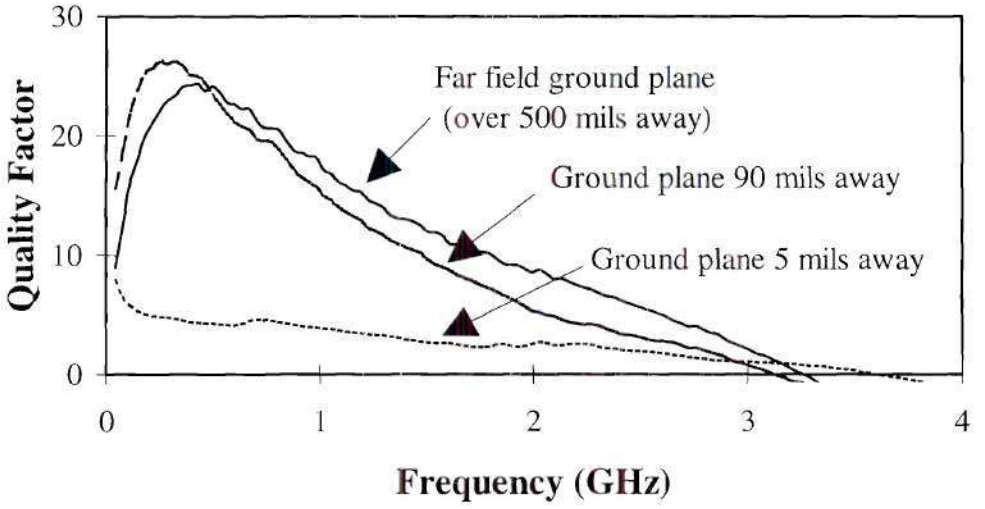


Figure 6.18 Changes in quality factor vs. frequency for a 13.5 nH inductor design as a function of distance of ground plane.

Section 6.4 Thin Film DLC and Ta_2O_5 Capacitors

Thin film capacitors were fabricated on silicon and on free-standing polyimide (flex) using the following processing steps. First, a bottom electrode was created by deposition of 1000 A Ti / 3000 A Cu with subsequent electroplating of 4 to 8 μm thick brite Cu. The brite copper was used since it created a smoother surface for the capacitor dielectric, which in turn reduced the defect density of the deposited dielectric and enhanced the capacitor performance on flex. A thin top layer of Ti or Mo was sputter deposited to promote the adhesion of the dielectric to the metal. Deposition of the Diamond Like Carbon (DLC) was composed of a hard/soft/hard sandwich structure.[1] For example, a 2000 A thick DLC capacitor would be composed of 200 A hard DLC / 1600 A soft DLC / 200 A hard DLC. Deposition of the Tantalum Oxide (Ta_2O_5) was performed at RPI.[2] Sputter deposition of 200 A Ti or Mo, followed by 3000 A Cu and 1000 A Ti was used to create the top dielectric. After all the layers were deposited, the capacitor was patterned and etched beginning with the top plate, then the dielectric, and finally, the bottom dielectric.[1,2] A top passivation was performed to simulate these capacitors, since they would be in an integrated multi-layer circuit. Vias were created from the top ground-signal-ground pads to the respective plates of the capacitor. The high frequency parallel and floating plate capacitors were designed at the Mayo

Foundation and at GE. A final Mayo design of a parallel plate capacitor is shown in Figure 6.19.

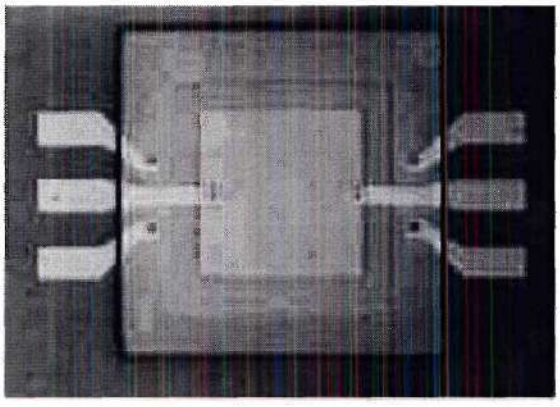


Figure 6.19 Mayo design of high frequency parallel plate capacitor.

The parallel plate capacitors on silicon were used as a control to determine ideal characteristics of these capacitors on a rigid, smooth surface. Even though the silicon is a very lossy substrate for microwave characteristics, the capacitor bottom ground plate shielded these effects from the microwave measurements. Since the final product was the capacitors on free-standing polyimide for molding to any substrate of choice with a top passivation, the data shown will be in reference to this. Capacitors without the top passivation yielded higher breakdowns in excess of 100 volts due to the enhanced ability of the capacitor to self-heal.[1,3] Improvements in the bottom plate roughness and optimized dielectric deposition has improved the capacitor characteristics to reduce the defects that are current annealed out in the self healing process. This, in turn, has improved the characteristics of the capacitors with top passivation. Test and

characterization played a key role in understanding the factors affecting the capacitor parameters such as yield, breakdown, leakage current, and high frequency response. Therefore, great care was taken to again ensure a statistically significant sample size with a variety of structure sizes ranging from $3x10^{-3}$ mm^2 to 40 mm^2 for the parallel plate capacitors and $2.6x10^{-2}$ to 1.26 mm^2 for the floating plate capacitors. A table of the various sizes in this study are shown in Table 6.6 Sizes not shown are the Mayo designs, which included the 40 mm^2 capacitor.

Table 6.6 Different Capacitor sizes for GE designed capacitors.

Name		X	Y	AREA
	cap name	mm	mm	mm^2
GROUP 1				
cap54x54	4B	0.054	0.054	0.0029
cap72x72	4C	0.072	0.072	0.0052
cap117x117	4D	0.117	0.117	0.0137
cap72x192	2A	0.072	0.192	0.0138
cap84x198	2B	0.084	0.198	0.0166
cap105x225	2C	0.105	0.225	0.0236
cap222x225	2D	0.222	0.225	0.0500
cap330x333	2E	0.330	0.333	0.1099
cap405x408	2F	0.405	0.408	0.1652
cap708x708	2G	0.708	0.708	0.5013
cap1533x1533	3E	1.533	1.533	2.3501
cap2235x2235	4A	2.235	2.235	4.9952
GROUP2				
cap90x90	1A	0.090	0.090	0.0081
cap147x147	1B	0.147	0.147	0.0216
cap96x225	1C	0.096	0.225	0.0216
cap117x225	1D	0.117	0.225	0.0263
cap168x225	1E	0.168	0.225	0.0378
cap282x285	1F	0.282	0.285	0.0804
cap420x420	1G	0.420	0.420	0.1764
cap630x420	1H	0.630	0.420	0.2646
SMT Sizes				
cap0201	3A	0.255	0.510	0.1301
cap0402	3B	0.510	1.014	0.5171
cap0603	3C	0.762	1.524	1.1613
cap0805	3D	1.269	2.031	2.5773
Floating Plate				Area/plate
capf252x102	5C	0.252	0.102	0.0257
capf1002x252	5B	1.002	0.252	0.2525
capf2502x504	5A	2.504	0.50	1.2620

Section 6.4.1 DC and Low Frequency Characterization

Manual probing of the structures was used to evaluate the materials at low frequency and DC by destructive testing of the devices. Breakdown voltage, which was defined as 1 μA leakage current when subjected to a ramped electric field, and leakage current were measured at DC and capacitance value and dissipation factor (loss tangent) at 10 kHz. The sequence of extracting the data employed a HP 4275A LCR meter and a HP 4140A pA meter/DC voltage source controlled via the HPIB interface using Labview. The voltage across the capacitor was stepped in 1 volt increments on 5 second intervals.

To verify that there was not any difference in electrical characteristics depending on bias conditions, half the capacitors were biased with the cathode (top electrode) high and half were biased with anode (bottom electrode) high. No bias dependence was observed in the electrical characteristics of either dielectric. Shown in Figure 6.20 are values of leakage current verses area for different thicknesses of Ta_2O_5 and for DLC with top passivation at 5 Volts. Figures 6.21 and 6.22 show the values of breakdown voltage for these same devices across the flex as a function of area. Devices with data points at 100 volts for DLC and 50 volts for Ta_2O_5 did not breakdown. Over 40 devices varying in area were tested across each part. These results are initial results for the high frequency design with top passivation coupons, and their performance is currently being optimized by use of the brite copper bath for the bottom electrode and in-house deposition of Ta_2O_5.

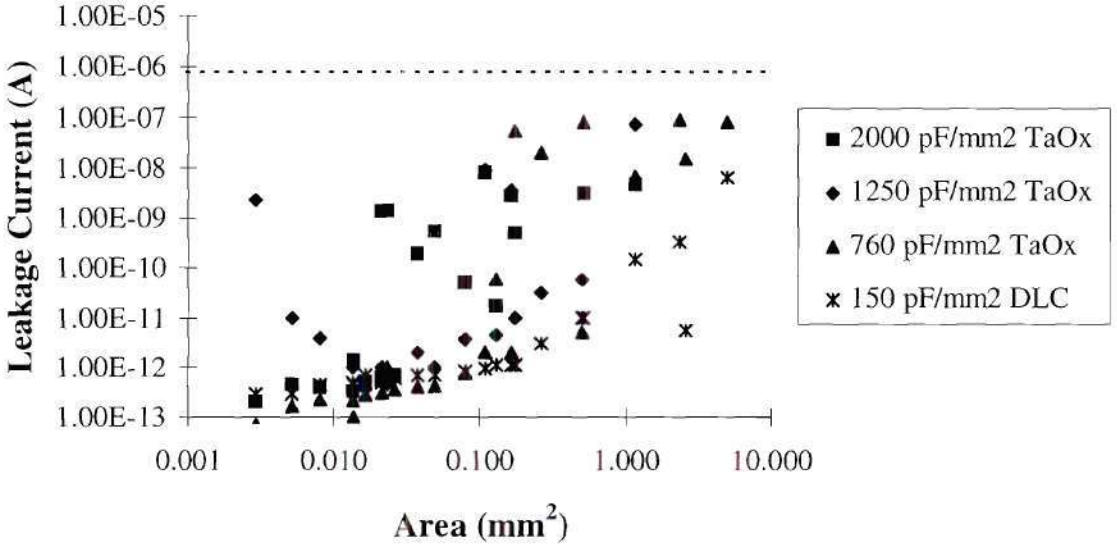


Figure 6.20 Leakage current at 5 volt bias verses area.

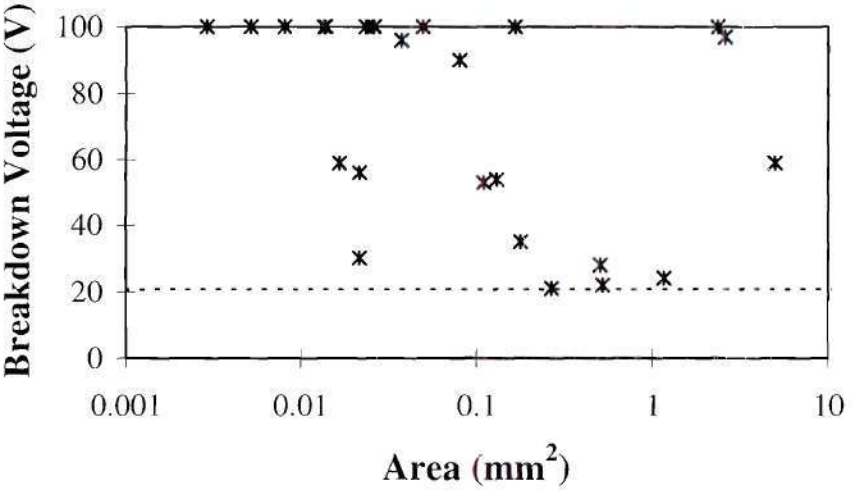


Figure 6.21 Breakdown voltage verses area for different thicknesses of DLC after top passivation. Values at 100 volts did not break down.

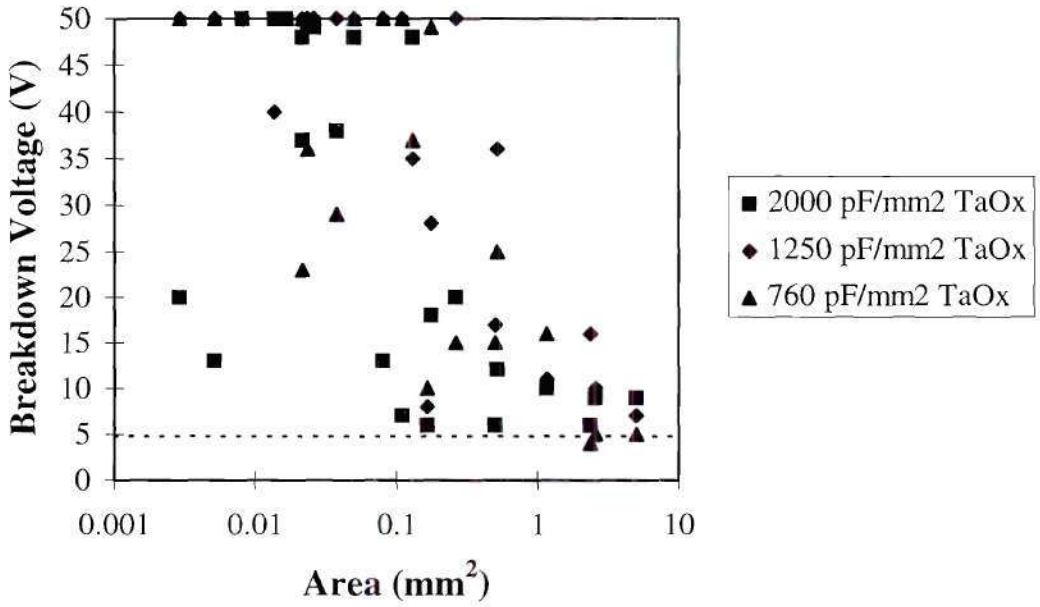


Figure 6.22 Breakdown voltage verses area for different thicknesses of Ta_2O_5 after top passivation. Values at 50 volts did not break down.

Measurements of the capacitance per unit area (CPUA) was performed at 10 kHz on all the parts to determine how close to target the values were and to evaluate the scaling of the capacitance with area. Figure 6.23 shows the percentage off target for the different lots as a function of area, while Figures 6.24 through 6.27 show the scaling of the capacitance verses area for the different lots. As can be seen, the smaller capacitors were found to be off target by a larger percent than the larger capacitors. This was expected due to the smaller capacitors having more sensitivity to the small capacitance variations caused by fringing capacitance and small differences in the actual patterned capacitor size compared to the designed size.

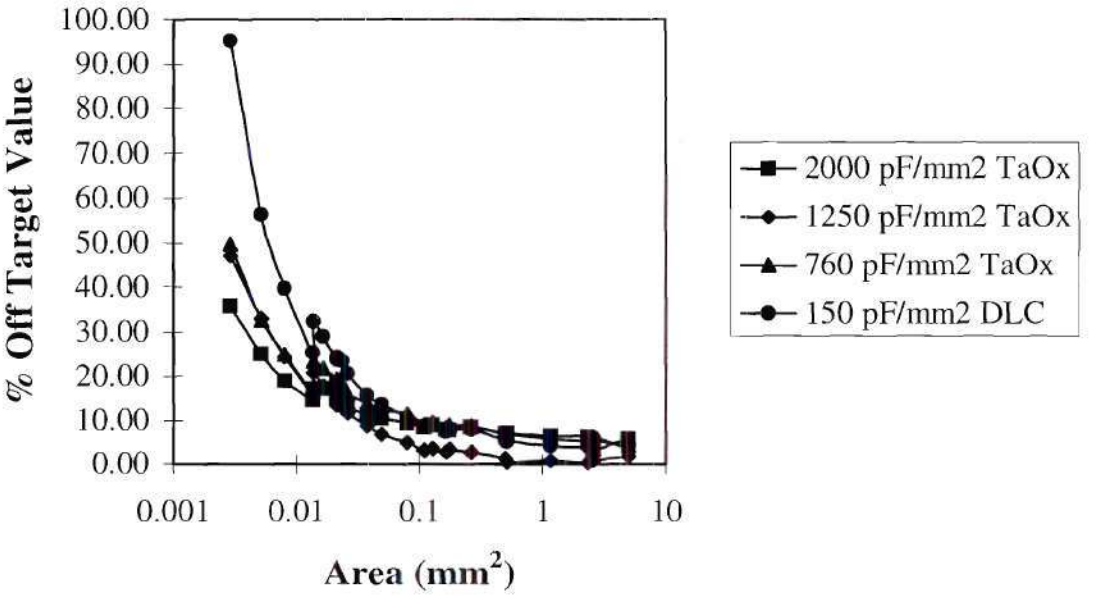


Figure 6.23 Percentage off target verses capacitance.

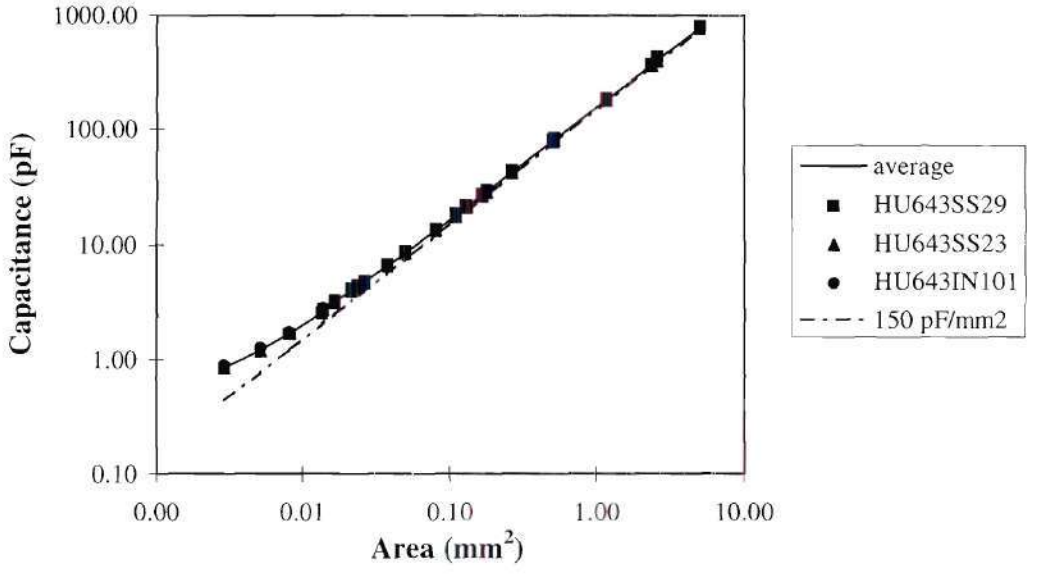


Figure 6.24 Capacitance verses area for 2kA DLC on flex at 10kHz for parallel plate capacitor design. Dashed (150pF/mm^2) and dotted (200pF/mm^2) lines give the theoretical values of capacitance for the stated capacitance per unit area (CPUA).

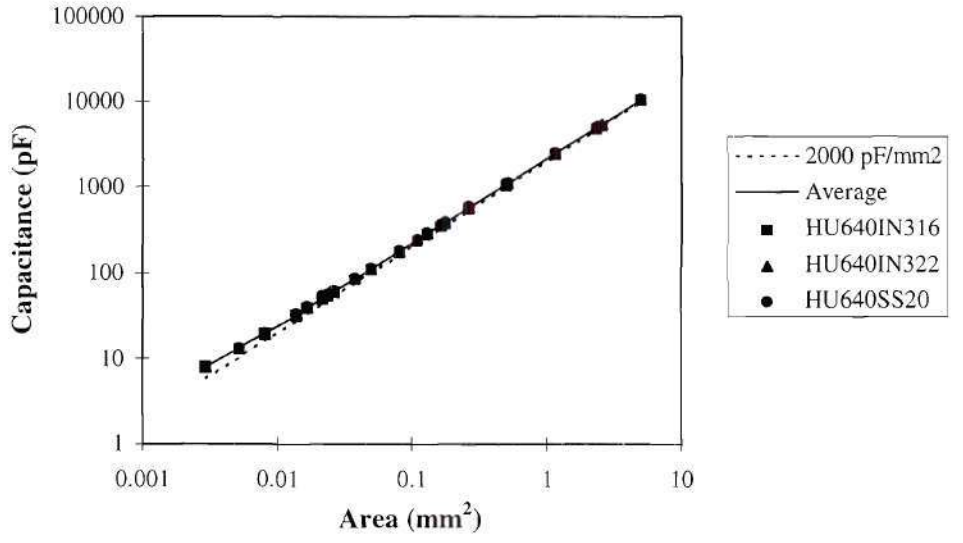


Figure 6.25 Capacitance verses Area for 1kA Ta_2O_5 on Flex at 10kHz for parallel plate capacitor design. Dotted (2000 pF/mm2) line gives the theoretical values of capacitance for the stated capacitance per unit area (CPUA).

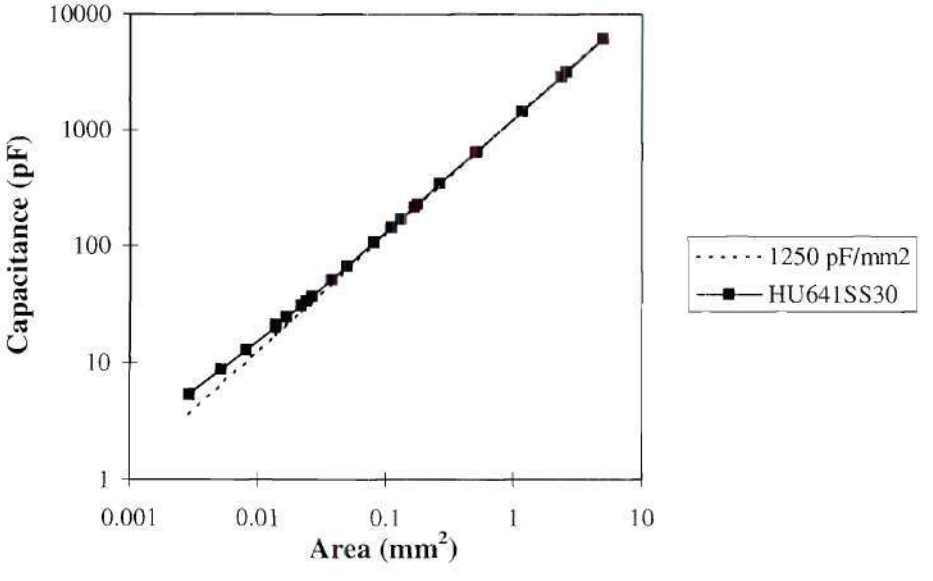


Figure 6.26 Capacitance verses Area for 1.5kA Ta_2O_5 on Flex at 10kHz for parallel plate capacitor design. Dotted (1250 pF/mm^2) line gives the theoretical values of capacitance for the stated capacitance per unit area (CPUA).

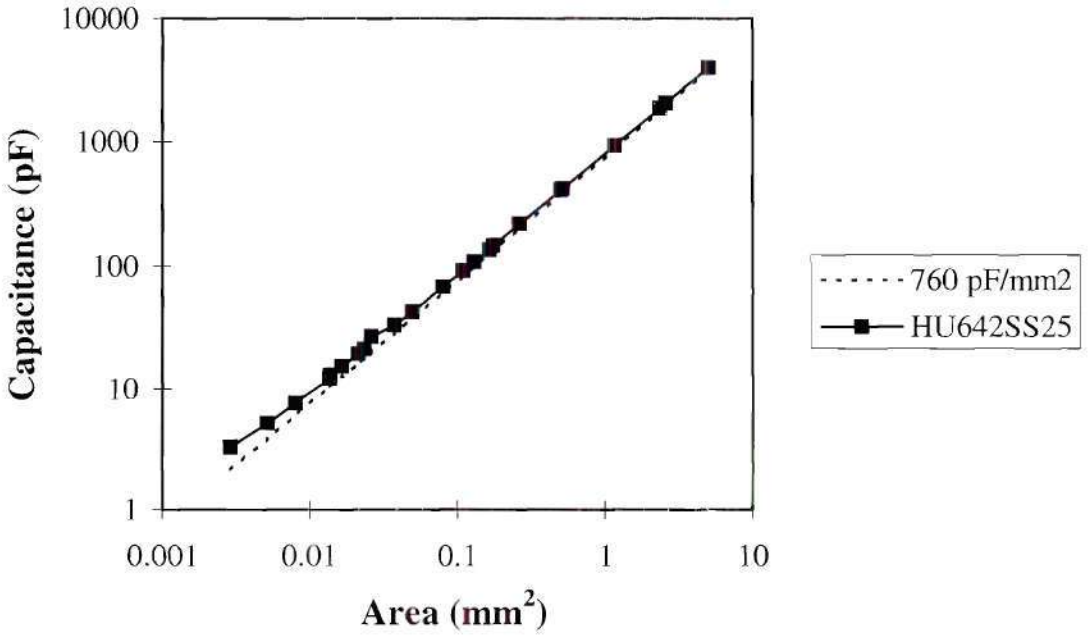
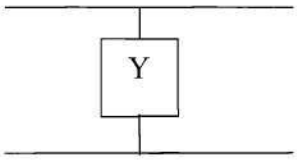


Figure 6.27 Capacitance verses Area for 2.3kA Ta_2O_5 on Flex at 10kHz for parallel plate capacitor design. Dotted (760 pF/mm^2) line gives the theoretical values of capacitance for the stated capacitance per unit area (CPUA).

Section 6.4.2 High Frequency One and Two Port Extractions of Thin Capacitors.

Two-port (S_{21}) extractions were performed from 2-port measurements utilizing the ABCD Matrix for a 2-port network consisting of a shunt admittance Y between ports 1 and 2 which is given below:



A=1 B=0

C=Y D=1

For this ABCD Matrix S_{21} and S_{12} reduce to be equal.

$$S_{21} = \frac{2}{A + BY_0 + C/Y_0 + D} = \frac{2}{2 + Y/Y_0}. \qquad (6.19)$$

solve for Y:

$$Y = \frac{2 \cdot Y_0 \cdot (1 - S_{21})}{S_{21}}. \qquad (6.20)$$

Substitute in S_{21} = Re + jIm and Y = G + jB = G + jwC:

$$G = 2 \cdot Y_0 \left[\frac{\mathrm{Re} - \mathrm{Re}^2 - \mathrm{Im}^2}{\left(\mathrm{Re}^2 + \mathrm{Im}^2\right)} \right] \qquad (6.21) \text{ and}$$

$$C = \frac{-2 \cdot Y_0}{\omega} \left[\frac{\mathrm{Im}}{\mathrm{Re}^2 + \mathrm{Im}^2} \right]. \qquad (6.22)$$

To check the capacitance value from the 2-port extraction, a 1-port extraction was performed for S_{11} where port 2 is left open. Again,

$$S_{11} = \frac{Z_L - Z_0}{Z_L + Z_0}. \qquad (6.23)$$

Solving for Z_L,

$$Z_L = Z_0 \frac{(1 + S_{11})}{(1 - S_{11})}. \qquad (6.24)$$

Substituting in $Z_L = R + jX$, $S_{11} = Re + jIm$, $Y_L = 1/Z_L$, and $Y_L = G + jB$ and solving for G and B,

$$G = Y_0 \frac{1 - Re^2 - Im^2}{(Re+1)^2 + Im^2} \qquad (6.25) \text{ and}$$

$$B = \omega \cdot C = -2 \cdot Y_0 \frac{Im}{(Re+1)^2 + Im^2} \quad (6.26) \text{ so } C = \left(\frac{-2 \cdot Y_0}{\omega}\right)\left(\frac{Im}{(Re+1)^2 + Im^2}\right), \quad (6.27)$$

where $\tan\delta = G/B$ and $Q = 1/\tan\delta$ (6.28) for a parallel resonant circuit.

Section 6.4.3 Results

High frequency measurements on the capacitors were performed from 45 MHz to 7 GHz, as stated in Section 6.1.3. One-port extractions of the capacitance and quality factor were performed for three die per lot. The capacitance and quality factor for the thinnest Ta_2O_5 and the DLC are shown in Figures 6.28 through 6.31. Resonant frequencies are determined from the one-port extraction, and are defined as the zero crossing since this is where the parasitic inductance equals the capacitance, producing an overall zero value for the imaginary part of the impedance. As expected, resonant frequencies were higher for the smaller capacitors, which were in excess of 7 GHz. The Q's for the Ta_2O_5 were still in excess of 100 at 45 MHz for the smaller capacitors, yet degraded more quickly than the Q's for the DLC. The smallest DLC capacitor had a Q of 50 at 45 MHz which remained above 20 up to 7 GHz. Optimization of the Ta_2O_5 deposition will help with maintaining the Q over frequency. Q's in excess of 400 have been measured at 10 kHz for the Ta_2O_5 material. These high Q's were attained partially due to the higher capacitance per unit area of the Ta_2O_5 compared to the DLC.

Figure 6.32 gives the CPUA of the first row of capacitors in the die for each lot. Consistency of the CPUA over the frequency sweep is seen for the smaller capacitors. Some losses in extracted CPUA associated with the increased parasitics of the larger footprint and higher capacitance of the larger capacitors is seen at the higher frequencies. The highest CPUA was determined to be in excess of 2000 pF/mm (200 nF/cm) for the thinnest Ta_2O_5.

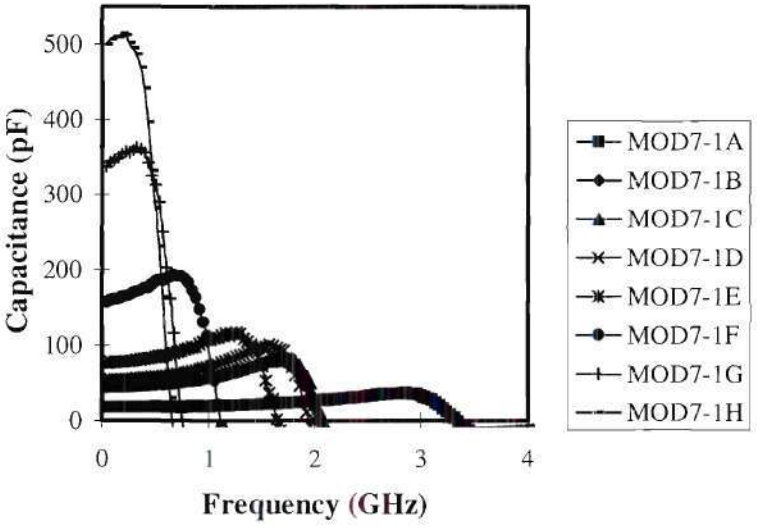


Figure 6.28 One port measurements showing resonant frequency for 1000A Ta_2O_5 parallel plate capacitors. See Table 6.6 for areas.

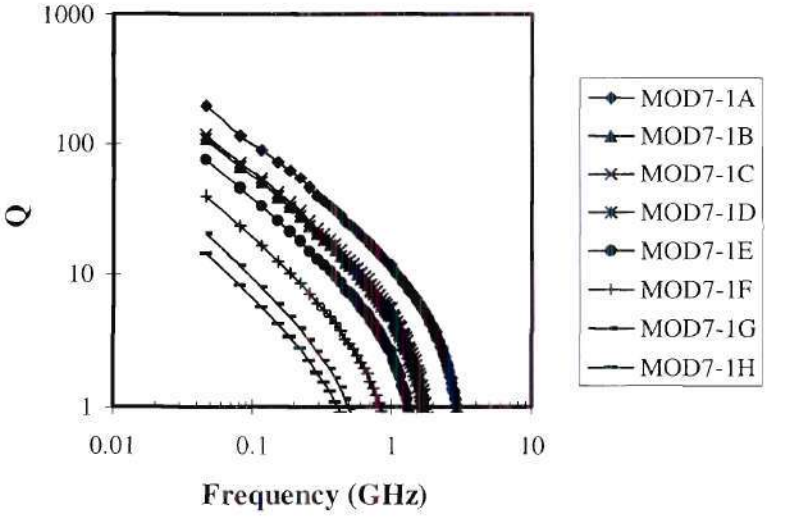


Figure 6.29 Quality factor vs. frequency for 1000A Ta_2O_5 parallel plate capacitors with different areas. See Table 6.6 for area for particular capacitor.

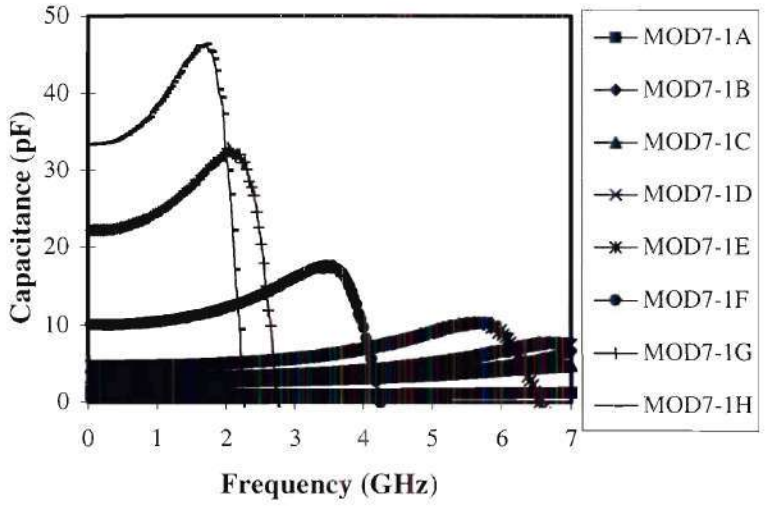


Figure 6.30 Capacitance verses frequency of some of the 150pF/mm^2 DLC parallel plate capacitors extracted from 1-port measurements.

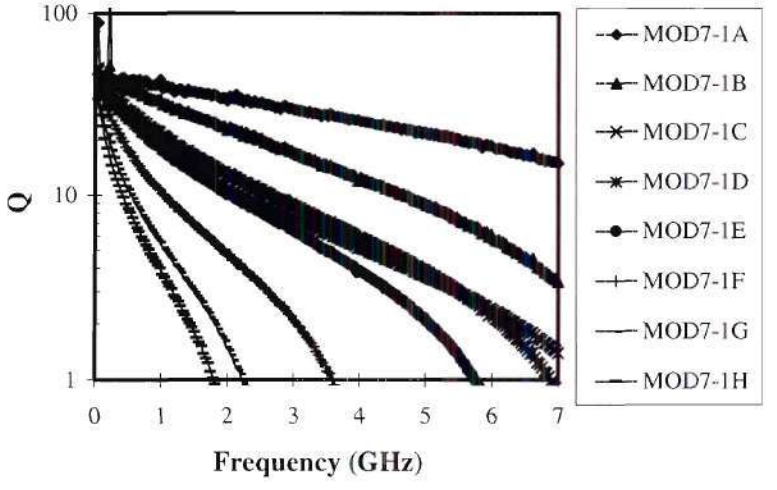


Figure 6.31 Quality factor verses frequency of some of the 150pF/mm^2 DLC parallel plate capacitors extracted from 1-port measurements.

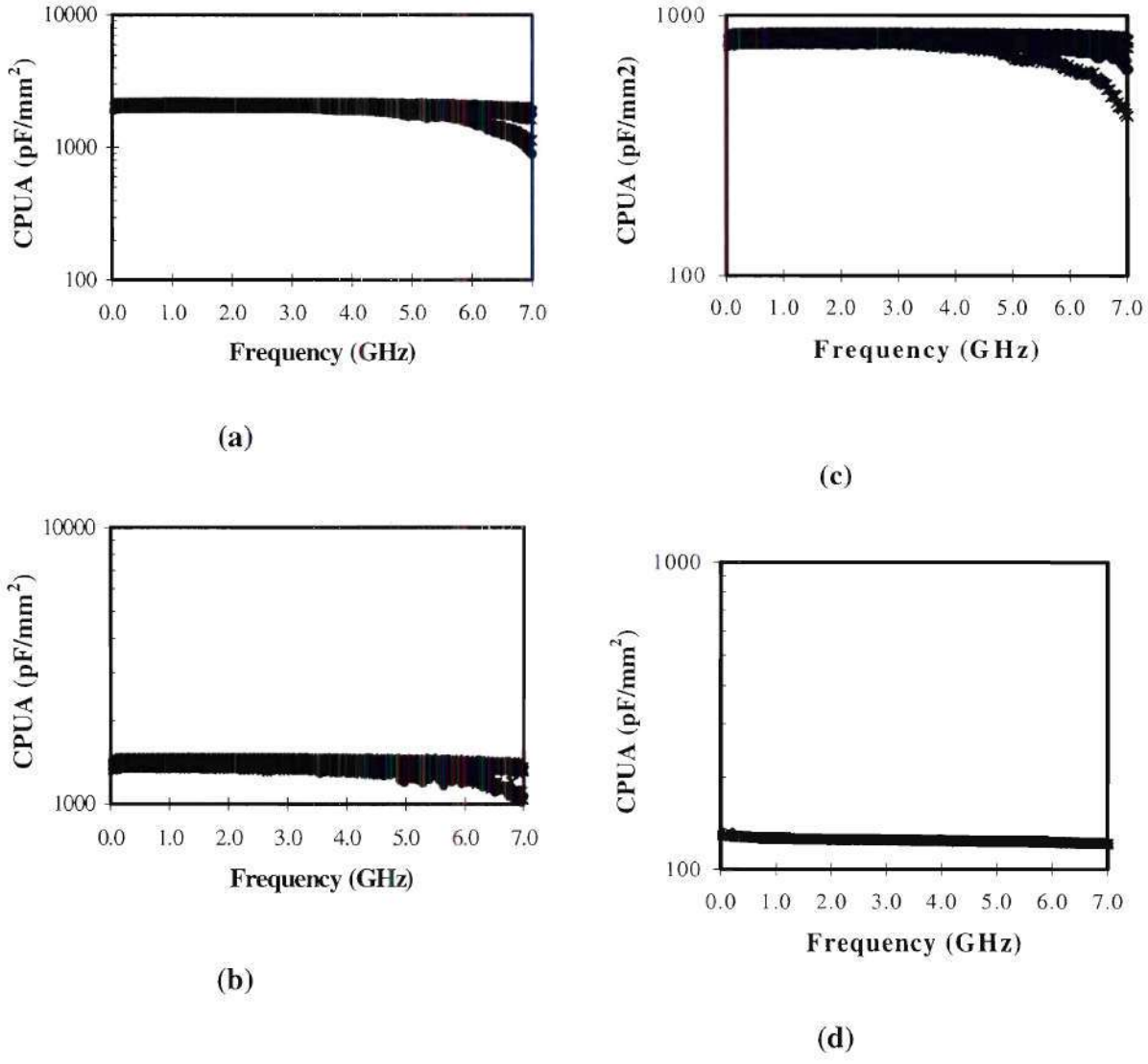


Figure 6.32 Capacitance per Unit Area (CPUA) verses frequency for the first row of the (a) 1000A Ta_2O_5, (b) 1500A Ta_2O_5, (c) 2500A Ta_2O_5, and (d) 2000A DLC parallel plate capacitors. The CPUA remains constant for the smaller footprint devices while the larger footprint devices, show a drop due to larger parasitics which were not included in the extraction.

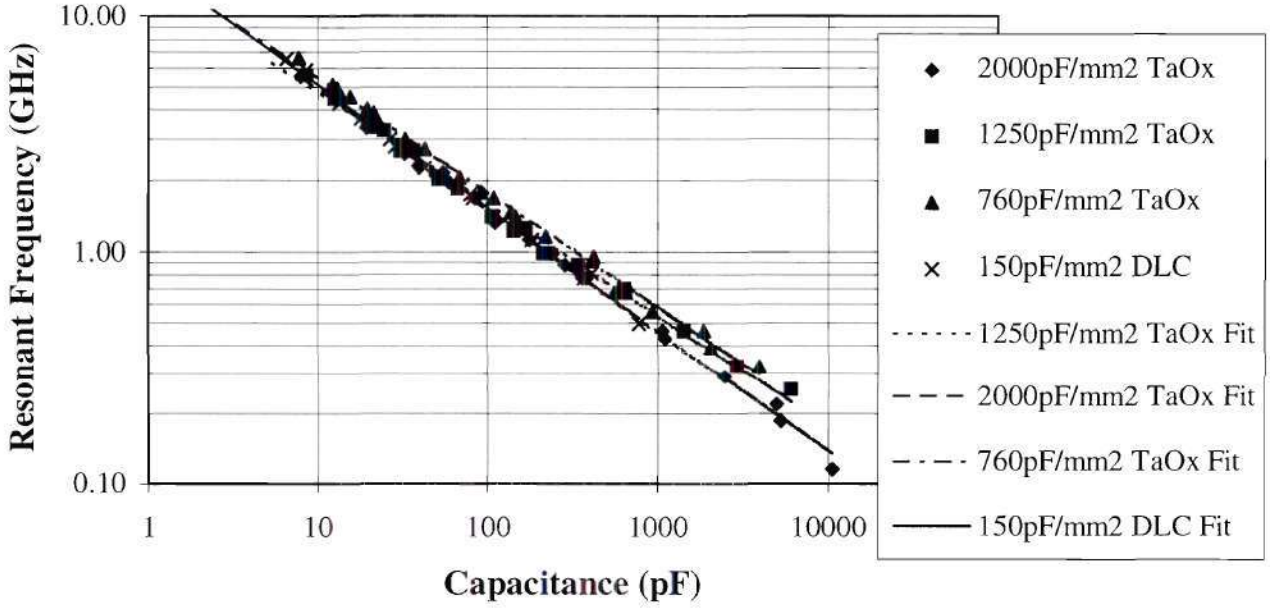


Figure 6.33 Resonant frequency verses capacitance for different CPUA Ta_2O_5 and DLC.

Figure 6.33 shows resonant frequency as a function of capacitance. It was hypothesized that the higher CPUA materials would yield higher resonant frequencies since the smaller footprint would produce reduced parasitics. For the areas of the capacitors which were designed, this was not the case. The parasitics due to thinner material deposited seemed to negate any reduction of parasitics due to the decrease in area. The best results were seen with the thickest Ta_2O_5 material, 760 pF/mm^2 (2344A),

while the 150 pF/mm^2 (2000A) DLC and the 2000 pF/mm^2 (987A) Ta_2O_5 showed lower resonant frequencies at the higher capacitance values.

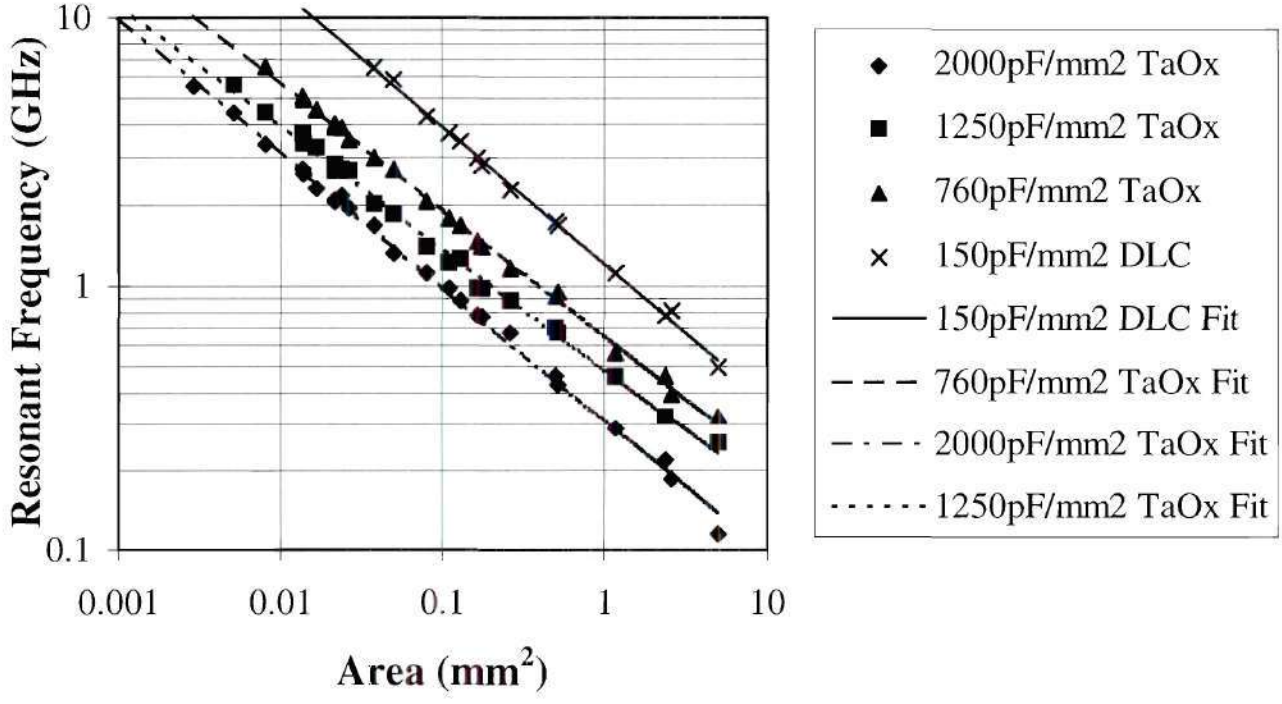


Figure 6.34 Resonant Frequency vs. Area for Different CPUA of Ta_2O_5 and DLC.

From Figure 6.34, for the resonant frequency verses area, the DLC yields the highest resonant frequency for a particular area, while the thickest Ta_2O_5 yields the highest resonant frequency of all the Ta_2O_5. This is to be expected due to lower parasitics associated with the thicker material, but also since the capacitance is lower for the same size device. When comparing only the value of capacitance and it's resonant frequency, the thickest Ta_2O_5 seems to be the best candidate since the CPUA is too low for the DLC to see the overall improvement.

Choice of capacitor material and size is dependent on the device specifications and the order in which they take priority. There is give and take on each device parameter. Therefore, there is no easy answer which dielectric thickness or material is best. Choice of the thickness and dielectric depend on the application which defines the overall device requirements. An interplay between these will determine what is best suited for a particular application. Rules of thumb for the thin film materials in this study were found to be: (1) For higher Q, smaller area and higher CPUA were desired. (2) For higher breakdown and lower leakage, smaller area and thicker material were desired. DLC outperformed Ta_2O_5 on breakdown and leakage parameters in this study because of optimized deposition. It is believed that Ta_2O_5, when optimized, will yield similar results to the DLC. (3) For higher resonant frequency, smaller area and thicker material are again preferred. The thickest Ta_2O_5 seemed to be the best candidate in this study, since due to it's high CPUA, large capacitance values could still be reached with the thicker material. Overall, the Ta_2O_5 once fully optimized will be a great candidate for high frequency thin film capacitors for integration with the Chip-on-Flex (COF) process.

REFERENCES

[1] R. J. Saia, H. S. Cole, K. M. Durocher, and M. C. Nielsen, *Int'l Conf. On Multichip Modules and High Density Pkg. in Denver, CO*, (1998).

[2] R. J. Saia, H. S. Cole, and K. M. Durocher, *Proceedings of the Fourth Int'l. Conf. on Flex Circuits*, (1997).

[3] H. Kapadia, H. Cole, M. Nielsen, N. Krishnamurthy, *ATW 1998 Chateau Elan*, (1998).

[4] H. Yoshino, T. Ihara, S. Yamanaka, and T. Igarashi, *IEEE/CHMT '89 Japan IEMT Symposium*, 156 (1989).

[5] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, *IEEE IEDM*, 6.5.1 (1996).

[6] P. K. Singh, R. S. Cochrane, J. M. Borrego, E. J. Rymaszewski, T. M. Lu, and K. Chen, *1994 IEEE MTT-S*, 1457 (1994).

[7] T. Lenihan, L. Schaper, Y. Shi, G. Morean, and J. Parkerson, *1996 Electronic Components and Technology Conference*, 119 (1996).

[8] H. Okabe, H. Yamada, M. Yamasaki, O. Kagaya, K. Sekine, and K. Yamashita, *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, **21**(3) 269 (1998).

[9] K. Chen, M. Nielsen, S. Soss, E. J. Rymaszewski, T.-M. Lu, and C. T. Wan, *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, **20**(2) 117 (1997).

[10] S. Byeon and Y. Tzeng, *IEEE Transactions on Electronic Devices*, **37**(4) 972 (1990).

[11] R. R. Kola, M. Y. Lau, S. Duenas, H. Y. Kumangai, P. R. Smith, R. C. Frye, K. L. Tai, and P. A. Sullivan, *1997 International Symposium on Advanced Packaging Materials*, 71 (1997).

[12] P. Chahal, R. R. Tummala, M. G. Allen, M. Swaminathan, *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, **21**(2) 184 (1998).

[13] J. Crols, P. Kinget, J. Craninckx, and M. Steyaert, *1996 Symposium on VLSI Circuits Digest of Technical Papers*, 28 (1996).

[14] D. F. Williams, *1996 MTT-S Workshop WMFE*, 42 (1996).

[15] D. M. Pozar, Microwave Engineering, Addison-Wesley Publishing Company, (1993).

[16] Verbal discussion with Tim Schaefer from Mayo Foundation.

[17] H. M. Greenhouse, *IEEE Trans. On Parts, Hybrids, and Packaging*, 101 (1974).

CHAPTER VII

CONCLUSIONS

The work contained in this thesis examines mixed material integration using thin film devices for high speed electronic applications. In this work, the impact of thin film semiconductor integration of InP-based high performance electronic devices onto silicon and other substrates has been demonstrated, as well as the use of a dielectric such as benzocyclobutene (BCB) between the high performance device and the highly conductive silicon for isolation from the lossy silicon substrate. To wrap up this work, thin film passive devices were also designed, fabricated, and evaluated on free standing flex for integration with any host substrate of choice.

The work that has been completed as part of this thesis includes the first integration of an InP-based thin film device onto silicon. The first two terminal InP-based device integrated with silicon was an RTD. Characterization of the device before and after substrate removal and bonding was performed and process optimization was performed to preserve the current voltage characteristics of the devices through the integration process. This resulted in the first successful demonstration of an InP-based RTD with a silicon circuit.

The first successful demonstration of a three terminal high speed InP-based thin film device was also integrated onto silicon and a variety of other host substrates. The thin film Tunneling Hot Electron Transfer Amplifier maintained it's dc performance except for a slight reduction in collector current resulting from partial etching of the collector during substrate removal. The process was optimized to minimize the etching of the collector

region without having to modify the device growth. As was expected, the high frequency performance of the device was effected by the lossy silicon substrate. This lead to an investigation of InP-based thin film Heterojunction Bipolar Transistors (HBTs) on silicon utilizing a layer of benzocyclobutene (BCB) between the thin film device and the lossy silicon. Comparisons were made on different resistivity silicon substrates with varying BCB thickness to find the best compromise between shielding from the effects of the silicon and maintaining a realistic BCB thickness for fabrication of vias for continued circuit integration.

Acknowledging the amount of real estate occupied by passive components in many high frequency analog circuits, an investigation of thin film passive components on free standing polyimide for high frequency applications was performed. The investigation consisted of modeling and design of the devices as well as characterization and parameter extraction of the devices. The material, processing, and device design were evaluated and processing variations were made according to results. Also, the components were characterized while varying the ground planes to determine what reduction in performance one could expect as the distance between components is reduced. The results reported here are the first high frequency passive components evaluated on free standing polyimide.

The work performed in this thesis was divided into four separate, yet related, experiments. The first experiment performed was integrating resonant tunneling diodes (RTDs) on silicon coated with 5000 Å of silicon nitride and characterizing their DC performance before and after substrate removal and bonding. A decrease in etch selectivity between the InP substrate and the highly doped InGaAs layer of the RTD used as a stop etch layer as opposed to an undoped InGaAs layer was detected. Also, a shift in the IV characteristics were observed. An empirical SPICE model was used to analyze how different device parameters may affect the DC characteristics. An MDS model was also used to observe the effect of an additional resistance in series with the device. Possible

changes in resistance, non-uniform adhesion, and relaxation of the strain of the RTD layers may have caused these changes in the DC performance of the devices. Since the changes from comparable on-wafer devices was within the same amount of variation of one device before and after substrate removal and bonding, the shift was considered to be minimal.

Thin film RTDs with contacts on the top and bottom of the device on silicon were fabricated. An RTD with contacts on the top and bottom of the device was also integrated onto a silicon circuit and was shown to exhibit an NDR region. A summary of these integrations were given. Also an investigation of some variations in integration of the thin film devices utilizing the transfer diaphragm were summarized.

In the second experiment, three-terminal, high frequency tunneling hot electron amplifiers (THETAs) were integrated onto silicon coated with 5000 Å silicon nitride, sapphire, quartz, glass, and alumina. Both the DC and the RF performance of these devices were investigated before and after substrate removal and bonding. The DC performance of the devices was similar for all host substrates. As expected, the RF performance of the THETA was affected by the lossy silicon substrate. To evaluate the effects of the lossy silicon, thin film devices bonded to different host substrates that were thermally conductive, yet electrically insulating, were investigated. The RF performance of the thin film THETAs was similar to the on-wafer results, yet there was still a slight drop in the unity power gain, GTU_{max}, and short-circuit current gain, h_{21} at the lower frequencies. The cut-off frequencies, f_{max} and f_t, were similar before and after bonding. Since GTU_{max} was degraded far more than h_{21}, there may have been an increase in the parasitics of the thin film device. The break-down voltages of the devices were found to occur at lower biases, which may have been due to a slightly thinned collector.

In the third experiment, integration of high frequency HBTs with conventional silicon, a layer of BCB was spun onto the host substrate and a low temperature cure was performed. Analysis of the DC and RF performance was made for different thicknesses of

BCB. The RF performance of the devices before and after substrate removal and bonding to silicon was found to be similar. As with the RTDs and the THETAs, there was still the problem of the highly doped InGaAs collector being etched slightly during substrate removal. Lapping of the substrate down to 100 μm and attachment of a glass slide to the black wax handling layer to keep the substrate inverted in the etch solution produced more etch uniformity over the surface of the wafer.

Finally, a thorough study of thin film passive components was performed. These components were fabricated on free standing flex for flexibility of lamination of these devices on any host substrate of choice. DC and low frequency characterization was performed to determine yield. High frequency evaluation was performed on these devices to determine performance, parasitics due to design and variations in the thickness of the deposited materials, and the quality factor as it varied with the distance of the ground plane. Simplified models of the passive components were extracted from the low and high frequency measurements to predict the trends in the designs for future optimization of these devices on flex.

In conclusion, the results presented in this thesis include many firsts. These firsts include: integration of an InP-based RTD onto a silicon host substrate and with a silicon circuit; InP-based THETA integrated on a variety of host substrates; InP-based HBT integrated onto silicon with BCB; and high frequency passive components on flex which are laminated to any substrate of choice. These integrations and process optimizations are the fundamental building blocks for the integration of various materials for a low cost, high performance, self-contained three dimensional packages.

CHAPTER VIII

FUTURE DIRECTIONS

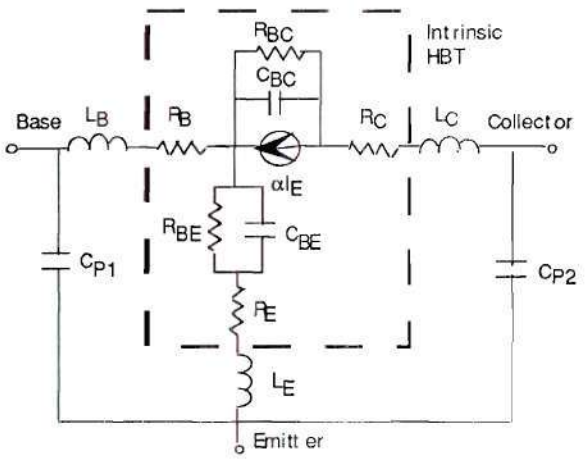
Research is continuing in the areas of integrated thin film RTDs and HBTs at Georgia Tech. Also, the thin film passive components on free standing flex reported here are progressing at a rapid pace at GE's Corporate Research and Development Center. In the following sections, a quick summary of the continuing research is given.

8.1 Thin Film RTDs

Circuit integration is continuing with the thin film RTDs. Plans to integrate multiple peak RTDs as well as multiple single RTDs with a Si circuit is planned.

8.2 Thin Film HBTs

To try to fully understand what parameters are changing between the on-wafer HBT and the thin-film HBT on BCB/Si, a small signal equivalent circuit model is needed for the thin film device. By modeling the changes, optimization of the thin film device and the bonding technique is possible. An equivalent circuit of the HBT which is determined by the physical operation of the device is needed. Since there are two different physical approaches to modeling the bipolar transistors, there are two different small signal equivalent circuit topologies used, the T-topology and the π-topology. The T-topology circuit model and element values are shown in Figure 8.1 for the on-wafer InP HBT at a collector current of 8.5 mA.



V_{BE} (mA)	0.78	V_{CE} (mA)	1.50
a_0	0.99	f_T (GHz)	90
$f_{max,G}$ (GHz)	98	$f_{max,U}$ (GHz)	166
t_B (ps)	0.52	t_C (ps)	0.52
R_E (W)	4.2	C_{BC} (fF)	27
R_B (W)	4.6	C_{P1} (fF)	11
R_C (W)	1.5	C_{P2} (fF)	19
R_{BE} (W)	3.9	L_E (nH)	0.047
R_{BC} (W)	56000	L_B (nH)	0.020
C_{BE} (fF)	122	L_C (nH)	0.018

Figure 8.1 T-topology small signal equivalent model and element values of an on-wafer InP HBT for I_c = 8.5 mA and emitter area of 11μm².[1]

There have been numerous techniques for calculating the parasitics of an HBT by utilizing test structures that short the transistor.[2] By shorting the transistor and measuring the test patterns which consists of the short, the pads, and the device feeds, it was hypothesized that accurate values for the device parasitics could be calculated. It was shown by Gobert et al. that when using this technique, there was a strong disagreement between the measured and fitted values for the parasitics, particularly the parasitic capacitances.[3] This is believed to be due to the fringing capacitances and inductances along

the "fingers" of the device that are ignored. Even though the S-parameters appeared to be correct, the Z-parameters did not agree well, especially at the low frequencies. Also, the final values of the pad parasitics, dc current gain, and the access resistances were strongly dependent on the initial starting values. To eliminate these inaccuracies, Gobert et al. established a direct extraction method for the parasitics of the HBT similar to the one used for the field effect transistor (FET).[3]

To model the intrinsic device a simple lumped element circuit is usually used, but by ignoring the distributed effects under the emitter and between the base and collector, the accuracy for the model can be reduced. For an accurate model, a number of RC distributed circuits are required, as shown in Figure 8.2 But to keep the circuit simple, the RC circuit between the base and the collector is replaced by a simple π-RC circuit. Once the parasitic elements are de-embedded from the s-parameter data, the values for the small signal circuit can be fit to the data using MDS.

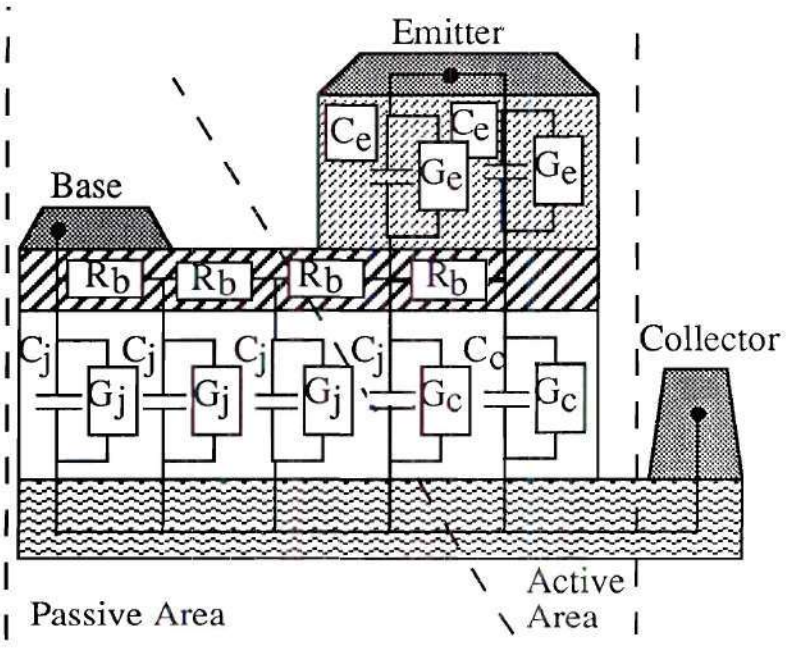


Figure 8.2 Lumped element circuit for the HBT.[3]

The equivalent circuit model of the HBT when normally biased is shown in Figure 8.3.

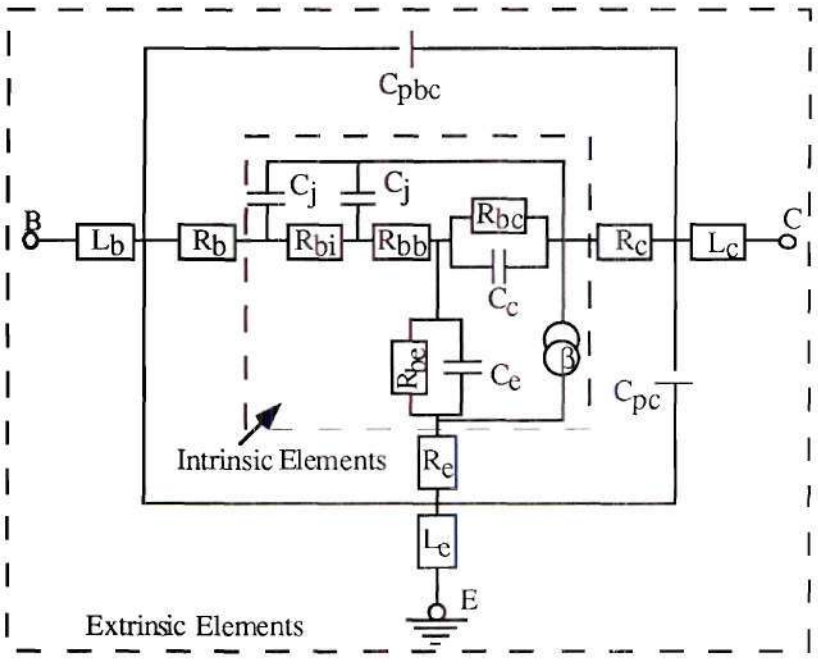


Figure 8.3 Equivalent circuit of HBT when normally biased.[4]

8.3 Thin Film Integral Passives

Future direction in the area of integral passives includes optimization in processing and creation of a model database using the high frequency data for circuit design. Various lots have been fabricated to evaluate the design and yield of passive components. These are currently under test. Initial results look promising for reduction of parasitics on the thin film devices by initial creation of a smoother bottom layer on the flex. New ideas are also under investigation to improve the breakdown of the capacitors after top passivation. Optimization of the Ta_2O_5 deposition is currently under way using of a new system recently purchased for GE CRD cleanroom.

ENDNOTES

[1] Model courtesy of Texas Instruments.

[2] D. Costa, W. U. Liu, and J. S. Harris, *IEEE Trans. Electron. Devices*, **38**, (1991).

[3] Y. Gobert, P. J. Tasker, and K. H. Bachem, *IEEE Trans. on Microwave Theory and Tech.*, **45**(1), (1997).

APPENDIX A

PROCESSING STEPS FOR RTD INTEGRATION WITH A SI CIRCUIT

PROCESS 1. MESA ISOLATION

PROCESS STEPS	NOTES	ADDITIONAL NOTES
Step 1. Alpha-step	Record height of existing mesa	compare to device structure
Step 2. Initial Clean	Acetone, IPA, N_2 dry	
Step 3. Bake	125 °C, 10 min.	
Step 5. Photoresist	Hoechst 5214, 4500 RPM, 30 sec.	can also use AZ1400-27 instead of Hoechst for positive process
Step 6. Bake (soft)	100 °C hot plate, 60 sec.	(90 -100 °C)
Step 7. Expose	5 mW/cm^2 on Suss for 10 sec. (10-12 sec usually depends on intensity variations)	
Step 8. Develop	327 MIF approx. 35-40 sec., (or 354 for 30-40 sec.) DI rinse, 2 min. N_2 dry	Time is very temp. dependent and intensity (exposure) dep. i.e. develop by sight (354 for AZ1400-27)
Step 9. Inspect	microscope	
Step 10. Bake	125 °C hot plate, 5 min.	(110-120 °C)
Step 11. Alpha-step	Record resist height	
Step 12. Gold Etch	Cynide Etch	etch time_____
Step 13. Ti/Silicon Nitride Etch	BOE etch DI rinse, 2 min. N_2 dry	etch time_____
Step 14. Mesa etch (InGaAs/InAlAs) *if just etching InGaAs, can use a citric acid etch shown in additional notes	H_2SO_4:H_2O_2:H_2O (1:10:220) @ r. t. (stops on InP substrate) DI rinse, 2 min. N_2 dry note: use teflon tweezers etch time:_____	HF:H_2O_2:H_2O (2:1:100) @ r. t. (etch rate approx. 20-25 Å/sec.) DI rinse, 2 min. N_2 dry or Citric acid:H_2O_2:H_2O:H_3PO_4 (55:5:220:1) etch rate approx. 8 Å/sec. DI rinse, 2 min. N_2 dry
Step 16. Alpha-step	make sure height is equal to resist height + amount you wanted to etch, otherwise, etch for a little longer	compare to device structure
Step 17. Resist Removal	Acetone, IPA, N_2 dry	
Step 18. Alpha-step	meas. and record height etched	

PROCESS 2. SUBSTRATE REMOVAL

PROCESS STEPS	NOTES	ADDITIONAL NOTES
Step 1. Black Wax Application	100 or 120 °C hot plate (put on 150 °C for a few seconds)	using a glass slide helps in keeping the substrate submersed and inverted during etching, therefore, have better etch uniformity
Step 2. Substrate Etch	$HCl:H_3PO_4$ (3:1) or (4:1) for 1-3 hours	varies according to substrate thickness, temp. and etch mixture
Step 3. Transfer Diaphram	contact bond if transfering that day, remove black wax with TCE otherwise, leave black wax on until day of transfer	

PROCESS 3. BOTTOM CONTACT PAD METAL AND PROTECTION OF TOP CONTACT CIRCUIT PAD

PROCESS STEPS	NOTES	ADDITIONAL NOTES
Step 1. Solvent clean	Acetone, IPA, N_2 dry	
Step 2. Bake	125 °C, 10 min.	
Step 3. Photoresist (1st coat)	Hoechst 5214, 4500 RPM, 30 sec.	
Step 4. Bake (soft)	100 °C hot plate, 60 sec.	(90-100 °C)
Step 5. Photoresist (2nd coat)	Hoechst 5214, 4500 RPM, 30 sec.	
Step 6. Bake (soft)	100 °C hot plate, 60 sec.	(90-100 °C)
Step 7. Expose	5 mW/cm^2 on Suss for 10 sec.	
Step 8. Bake	45 sec 110-120 °C hot plate	PR breaks down approx. 130 °C)
Step 9. Flood expose	Suss 5 mW/cm^2, 1.9 min.	
Step 10. Develop	440 MIF approx. 4-6 sec., DI rinse, 2 min. N_2 dry	can also try Shipley's 354 developer for 15 sec. (if not developed by then, redo, else PR will get gooey)
Step 11. Inspect	microscope - check to make sure all gaps for the pad metal are completely developed	
Step 12. Metal	E-beam evaporator 250 Å Ti (5.0 Å/sec.) 400 Å Pt (5.0 Å/sec.) 2500 Å Au (5.0-10.0 Å/sec.)	
Step 13. Lift-off Metal	submerge in acetone, cover and let sit	

PROCESS 4. TRANSFER DEVICE

PROCESS STEPS	NOTES	ADDITIONAL NOTES
Step 1. Wet surface Area	place a drop of water (approx. same size of device area you are transferring) on a clean area of the transfer diaphram, invert and place on circuit pad	
Step 2. Pick Device	find device of interest, invert transfer diaphram and bring device in contact with the water droplet	
Step 3. Align and Bond	align device to the contact pad and apply pressure to bond device to the pad	
Step 4. Inspect Device		

PROCESS 5. POLYIMIDE OVERLAY

PROCESS STEPS	NOTES	ADDITIONAL NOTES
Step 1. Bake	125 °C, 10 min.	
Step 2. Polyimide	2) PI 2611, 4500 RPM, 90 sec.	use a slow ramp up and ramp down and center the thin film device in the center of the chuck
Step 3. Bake (soft)	130 °C oven 10-30 min.	
Step 4. Furnace Anneal	3-5 °C/min. ramp up to 250°C 250°C for 20-30 min. 3-5 °C/min. ramp up to 350°C 350°C for 1 hr.	300 ^{0}C instead of 350 ^{0}C seems to cure fine if ramp is 3 ^{0}C and the bottom pad looks better)
Step 5. Metal Mask	Filament evaporator 1000-1500 Å Al	can also use sputterer (approx. 200 sec evap.)
Step 6. Photoresist (open area for top contact pad)	2) Hoechst 5214, 4500 RPM, 30 sec.	
Step 7. Bake (soft)	100 °C hot plate, 60 sec.	
Step 8. Expose	5 mW/cm^2 on Suss for 10 sec. (usually 10-12 sec depending on intensity)	
Step 9. Bake	45 sec 120 °C hot plate	
Step 10. Flood expose	Suss 5 mW/cm^2, 1.9 min.	
Step 11. Develop	440 MIF approx. 4-6 sec., DI rinse, 2 min. N_2 dry	can also try Shipley's 354 developer (15 sec.)
Step 12. Inspect	microscope - check to make sure gap for the pad is completely developed	
Step 13. Bake (hard)	120 °C hot plate, 5 min.	
Step 14. Etch Al	PAN etch (or gold cynide etch, or 351) (H_3PO_4:Acetic:HNO_3) ratio??? DI rinse, 2 min. N_2 dry	heat etch on 120 °C hot plate rinse really well after etch
Step 15. RIE Etch	O_2 for approx 20 min.	
Step 16. Etch Al	PAN etch (or Gold Cynide or 351) ****use 351 if you have any gold exposed DI rinse, 2 min. N_2 dry	heat etch on 120 °C hot plate rinse really well after etch

PROCESS 6. TOP CONTACT PAD METALIZATION

PROCESS STEPS	NOTES	ADDITIONAL NOTES
Step 1. Solvent clean	Acetone, IPA, N_2 dry	
Step 2. Bake	125 °C, 10 min.	
Step 3. Photoresist (1st coat)	Hoechst 5214, 4500 RPM, 30 sec.	
Step 4. Bake (soft)	100 °C hot plate, 60 sec.	
Step 5. Photoresist (2nd coat)	Hoechst 5214, 4500 RPM, 30 sec.	
Step 6. Bake (soft)	100 °C hot plate, 60 sec.	
Step 7. Expose	5 mW/cm^2 on Suss for 10 sec.	
Step 8. Bake	45 sec 120 °C hot plate	
Step 9. Flood expose	Suss 5 mW/cm^2, 1.9 min.	
Step 10. Develop	Shipley 354 for 15 sec., DI rinse, 2 min. N_2 dry	
Step 11. Inspect	microscope - check to make sure all gaps for the pad metal are completely developed	
Step 12. Metal	E-beam evaporator 400 Å Ti (5.0 Å/sec.) 400 Å Pt (5.0 Å/sec.) 2500 Å Au (5.0-10.0 Å/sec.)	
Step 13. Lift-off Metal	submerge in acetone, cover and let sit	
Step 14. RIE Etch (expose ckt.)	O_2 for approx. 20 min.)	

APPENDIX B

CONVERSION FORMULAS FOR TWO-PORT NETWORKS

Table 1. Conversion between two-port network parameters

S_{11}	S_{11}	$\frac{(Z_{11}-Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}{\Delta Z}$	$\frac{(Y_0-Y_{11})(Y_0+Y_{22})+Y_{12}Y_{21}}{\Delta Y}$
S_{12}	S_{12}	$\frac{2Z_{12}Z_0}{\Delta Z}$	$\frac{-2Y_{12}Y_0}{\Delta Y}$
S_{21}	S_{21}	$\frac{2Z_{21}Z_0}{\Delta Z}$	$\frac{-2Y_{21}Y_0}{\Delta Y}$
S_{22}	S_{22}	$\frac{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}}{\Delta Z}$	$\frac{(Y_0+Y_{11})(Y_0-Y_{22})+Y_{12}Y_{21}}{\Delta Y}$
Z_{11}	$Z_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{11}	$\frac{Y_{22}}{\lvert Y\rvert}$
Z_{12}	$Z_0\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{12}	$-\frac{Y_{12}}{\lvert Y\rvert}$
Z_{21}	$Z_0\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{21}	$-\frac{Y_{21}}{\lvert Y\rvert}$
Z_{22}	$Z_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{22}	$\frac{Y_{11}}{\lvert Y\rvert}$
Y_{11}	$Y_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{Z_{22}}{\lvert Z\rvert}$	Y_{11}
Y_{12}	$Y_0\frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$-\frac{Z_{12}}{\lvert Z\rvert}$	Y_{12}
Y_{21}	$Y_0\frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$-\frac{Z_{21}}{\lvert Z\rvert}$	Y_{21}
Y_{22}	$Y_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{Z_{11}}{\lvert Z\rvert}$	Y_{22}

$|Z| = Z_{11}Z_{22} - Z_{12}Z_{21}$; $|Y| = Y_{11}Y_{22} - Y_{12}Y_{21}$; $\Delta Y = (Y_{11}+Y_0)(Y_{22}+Y_0) - Y_{12}Y_{21}$;

$\Delta Z = (Z_{11}+Z_0)(Z_{22}+Z_0) - Z_{12}Z_{21}$; $Y_0 = 1/Z_0$

VITA

Nicole Andrea Krishnamurthy was born in Huntsville, Alabama on May 16, 1968 to Ernest and Frauke Evers. She graduated from Huntsville High School in 1986. She began her college career at Georgia Institute of Technology in the fall of 1986 where she majored in Electrical Engineering and minored in German. She graduated in 1990 with honors. She went on to complete a Master of Science in Electrical as a graduate co-op in 1992 with a minor in math. She began her studies at Georgia Institute of Technology for her Doctor of Philosophy in Electrical Engineering in 1992 and received a GAANN Fellowship from the United States Department of Education. She received her Doctor of Philosophy in Electrical Engineering in 1998. Her thesis work performed under the direction of Dr. Joy Laskar and Dr. Nan Marie Jokerst was entitled "Mixed Material Integration for High Speed Applications." Dr. Krishnamurthy joined General Electric Corporate Research and Development in September of 1997. Her work includes modeling, testing and characterization of SiC power devices under the DARPA sponsored SiC MegaWatt Power Device Program, SiC microwave power devices, and high frequency integral passives on flex under the DARPA sponsored Integral Passives Program, and high frequency HDI characterization.

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