UNDERSTANDING THE PHYSICS OF HARD AND SOFT FAILURE IN SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

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UNDERSTANDING THE PHYSICS OF HARD AND SOFT FAILURE IN SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

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To my parents,

for always supporting my education.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of this work is to investigate hard and soft failure mechanisms observed when silicon-germanium heterojunction bipolar transistors (SiGe HBTs) are operated outside of traditionally defined electrothermal safe operating areas (SOAs).

In Chapter 1, the need for studying the reliability physics of SiGe HBTs is motivated. Important physical mechanisms in SiGe HBTs such as avalanche multiplication, breakdown mechanisms, and base current reversal are briefly discussed to provide some insight on the physics of failure in later chapters.

Chapter 2 provides an overview of the reliability physics of SiGe HBTs. The damage spectrum of the SiGe HBT is introduced in order to showcase the different soft failure mechanisms when operating a SiGe HBT in typical RF and mixed-signal circuits. All of the relevant damage mechanisms in scaled SiGe HBTs are described in greater detail to understand the impact on overall device performance.

Chapter 3 introduces the concept of hard failures in SiGe HBTs. A new failure metric in SiGe HBTs, known as the hard failure point, is proposed in order to provide additional understanding to the physics of hard failure. This failure metric represents the bias condition at which the device transistor action fails, and the device becomes purely resistive as a result of catastrophic junction failure. An advanced SiGe HBT technology (GlobalFoundries 9HP) was chosen and measured in a variety of ways as a function of geometry, layout configuration, and temperature. Through TCAD simulations and experimental data, two modes of failures in SiGe HBTs were shown. The takeaway is that knowing specific details, such as the exact location of hard failures, the physics that drives them, and what they depend upon, can greatly aid circuit designers to exploit the design space between PDK specified SOAs and hard failures. The analysis presented in Chapter 3 has been published and presented at the 2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting [1].

Chapter 4 presents the use of high-breakdown SiGe HBTs in RF integrated circuits. A medium-breakdown variant in a fourth-generation SiGe BiCMOS technology is described from a processing perspective to understand any subtle differences between its high-performance counterpart. Reliability stress measurement data is shown to provide insight into the differences between high-performance and medium-breakdown SiGe HBTs when biased under high-current and mixed-mode stress conditions. Trade-offs in reliability and performance are described to showcase advantages and disadvantages when using either device variant. Part of the analysis presented in Chapter 4 will be submitted for publication to the 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium.

Lastly, Chapter 5 summarizes the contributions presented in this thesis. A future work section is provided to showcase any additional research work that will result from the analysis done in Chapter 3 and 4.

CHAPTER 1
INTRODUCTION

The invention of the transistor gave rise to a whole new set of applications in the field of science and technology. Today, it is used as the main building block in consumer electronics and electronic warfare systems, among other applications. Due to the rapid development of the semiconductor industry, it is possible to achieve high-performance and low-cost – a win-win scenario from an economic standpoint.

At its core, obtaining high-performance and low-cost requires shrinking the vertical and lateral dimensions of the transistor. Unfortunately, this on-going scaling trend has come with a reliability cost due to a restriction in the safe-operating-areas (SOAs) of these devices (e.g., reduction in operating voltages). As such, designing simultaneously for both high-performance and reliable operation has become a major issue for circuit designers, especially in the radio-frequency (RF) and millimeter-wave (mm-Wave) domain.

To achieve reliable operation, foundries attempt to define the SOA of the transistor to guarantee little to no performance degradation of the device in the long-term operation. However, this foundry-defined SOA tends to be very conservative, limiting the maximum operational range that can be achieved. In many cases, these limits are applied uniformly to all devices regardless of their geometry or configuration. Given the complexity of this problem, it is critical to understand all regions of operation in order to exploit the unavoidable trade-off between high-performance and reliable operation.

Ultimately, the ability to accurately model and understand the entire damage spectrum in a transistor not only provides insight on the onset of reliable operation, but it also allows a circuit designer to make full use of the design space that goes

beyond PDK-defined SOAs established by breakdown voltages alone.

1.1 SiGe BiCMOS Technology

SiGe BiCMOS technology has been proven to be an effective solution to meet the high-performance demand of the RF and mm-Wave spectrum as it combines Silicon-Germanium heterojunction bipolar transistors (SiGe HBTs) along with the best features of CMOS logic and RF passive components. Unlike CMOS, which is primarily driven by scaling, each generation of SiGe BiCMOS technologies is defined by the transistor-level maximum small-signal frequency response rather than miniaturized dimensions [2]. Ultimately, SiGe BiCMOS technology offers outstanding integrability, yield, and cost-performance advantages in comparison to its III-V counterparts.

The current state-of-the-art SiGe HBTs have shown peak transit frequencies (f_T) of 505 GHz and peak maximum oscillation frequencies (f_{max}) of 720 GHz at room temperature [3]. Additional work in the literature has shown the potential of SiGe HBTs to achieve TeraHertz (1 THz = 1,000 GHz) operation, opening doors to new applications such as THz imaging, mm-Wave transceivers, and multi-Gb/s systems [4], [5].

1.2 The SiGe HBT

Fundamentally, the SiGe HBT can be understood by analyzing the basic principles of the silicon bipolar junction transistor (BJT). The main difference between both devices is the introduction of Germanium (Ge) in the base region of the SiGe HBT. Doing this has many implications that result in improved DC and AC performance.

To have a better understanding of the qualitative operation, it is necessary to look at the impact of Ge in the SiGe HBT. Fig. 1.1 shows the energy band diagram for graded-base SiGe HBT (dashed line) and a Si BJT (solid line) biased under forward-mode of operation. It is assumed that both devices are engineered to be more or less

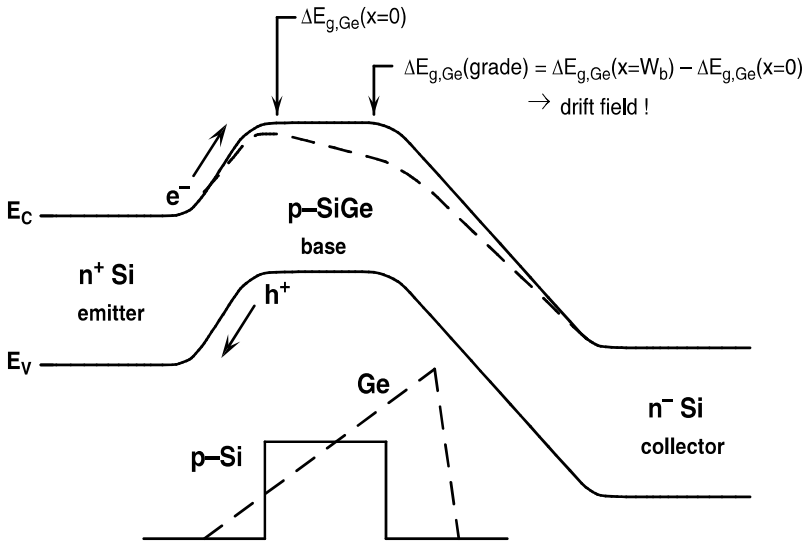

Figure 1.1: Energy band diagram for Si BJT (solid) and SiGe HBT (dashed) under forward active mode (after [2]).

the same and the only difference being the Ge retrograded profile shape in the base region of the HBT.

Introducing Ge into the base of the HBT produces an offset in the valence band. However, Fig. 1 shows that this offset ultimately ends up in the conduction band. To understand this physically, it is important to note that for constant p-type doping in the base region of a BJT, the difference in energy between the Fermi level and the valence band is fixed [2]. When the Ge is introduced, an offset in the valence band occurs. If the system is in equilibrium (i.e., constant Fermi level), then the Fermi level realigns itself and the energy offset is shifted toward the conduction band.

Having an offset in the conduction band in the base of the HBT comes with many benefits from a performance standpoint. Essentially, the potential barrier that carriers have to overcome when traveling from the emitter to the base is reduced. This results in an exponential increase in the number of carriers that are emitted to the base (electron injection) for the same bias condition, providing a higher current gain compared to that of the Si BJT.

The graded Ge across the base also induces a built-in quasi-drift field in the neutral base that has an impact on minority carrier transport. Physically, the Ge-gradient-induced drift-field across the neutral base is aligned in a direction (from collector to emitter) such that it will accelerate the injected minority carriers across the base. Doing this adds a large drift-field component to the minority carrier transport. As a result, the diffusive transport of the minority carriers is sped up and base transit-time (τ_B) decreases, achieving higher f_T and f_{max}.

1.3 Avalanche Multiplication due to Impact Ionization

The fundamental design trade-off in bipolar transistors between maximum operating frequency (f_T/f_{max}) and maximum operating voltage (BV_{CEO}) is known as the Johnson limit [6]. In state-of-the-art bipolar processes, J_C is designed to be sufficiently high so that any charging time associated with parasitic and depletion capacitances is negligible to that of τ_B and τ_E [2].

Achieving peak-f_T in a SiGe HBT implies biasing the device at the onset of the Kirk effect to extract maximum performance (which happens at high current densities). Additionally, to suppress the onset of the Kirk effect, the device is designed to have heavily doped implanted collectors. Raising the collector doping results in a higher electric field through the reverse-biased collector-base (CB) junction, increasing the rate of impact ionization. In practice, the rate of impact ionization is characterized by the avalanche multiplication factor (M-1). For all practical purposes, M-1 is defined in [2] as

$$M - 1 = \frac{I_{n,out}}{I_{n,in}} - 1 = \frac{I_C}{I_E - (I_B)(V_{BE})|_{V_{CB}=0}} - 1, \tag{1.1}$$

where $I_{n,in}$ and $I_{n,out}$ are the electron currents going into and out of the collector-base space-charge region.

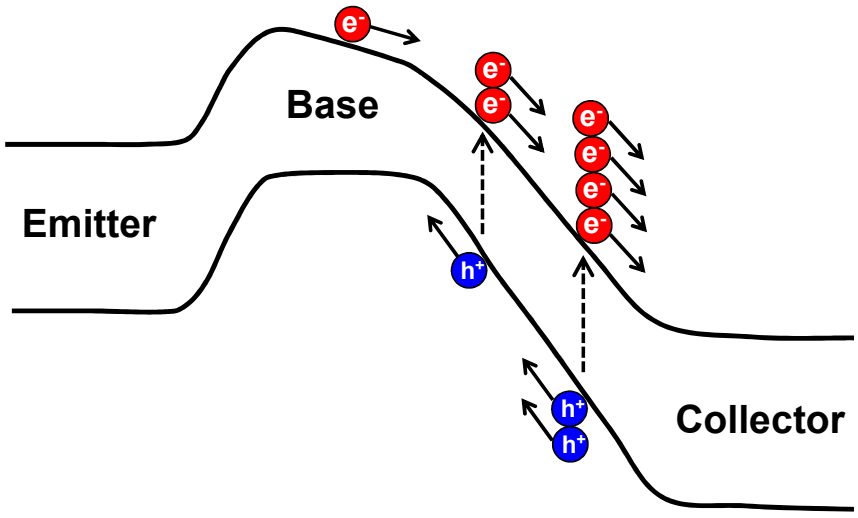

Figure 1.2: Energy band diagram representation of the avalanche multiplication process.

A higher (M-1) will lead to a decreased breakdown voltage, which ultimately explains the reason why there is a trade-off between f_T and BV_{CEO} in bipolar transistors. This is particularly the case as SiGe HBTs are scaled down to operate at higher frequencies.

In advanced SiGe BiCMOS processes, avalanche multiplication has become a critical reliability issue since the electric field in the CB junction is large. When this occurs, carriers injected from the base into the collector enter the high field region of the CB junction and have some probability of undergoing impact ionization. If this event happens, the carriers will impact the lattice with enough energy such that they generate an electron-hole pair. Any secondary carriers generated from this process also have some probability of undergoing impact ionization, creating additional electron-hole pairs. The literature defines this process as avalanche multiplication since the current leaving the CB junction ($I_{n,out}$) is much larger than the current entering the CB junction ($I_{n,in}$). Some implications of avalanche multiplication include device failure due to breakdown. Fig. 1.2 showcases the avalanche multiplication process described above.

1.4 Breakdown Voltages and Base Current Reversal

Classically speaking, there are two breakdown voltage limits in bipolar transistors: the collector-emitter breakdown voltage with an open base (BV_{CEO}) and the collector-base breakdown voltage with an open emitter (BV_{CBO}). Both of these limits depend on the bias configuration being used, either the common-emitter or common-base configurations. Most importantly, the base impedance termination will dictate the range at which either one of the breakdown voltages will occur. As a rule of thumb, the breakdown voltage will decrease with increasing base resistance. The worst case scenario is BV_{CEO}, which occurs when the base resistance is very large ($R_B \rightarrow \infty$). On the other hand, the maximum breakdown voltage limit BV_{CBO} will happen when the base resistance is low ($R_B = 0\,\Omega$). To account for the dependence of base resistance on breakdown voltage, the literature sometimes quantifies such relationship with another FoM known as BV_{CER}, which ranges from BV_{CEO} to BV_{CBO} [7].

BV_{CER} is an outcome of base current reversal. As the name suggests, base current changes polarity beyond BV_{CEO} [8]. The common-base forced-I_E bias configuration (shown in Fig. 1.3(a)), which serves as the setup used for the measurements done in this work, functions in such a way that the base current (I_B) is not fixed by an external high-resistive DC source, unlike for the common-emitter bias configuration. This implies that any excess hole current from impact ionization can freely exit the base terminal [1]. Once the collector-emitter voltage (V_{CE}) surpasses BV_{CEO}, it causes the base current to reverse polarity due to avalanche-generated holes. Mathematically speaking, the product of (M-1) and the current gain (β) becomes greater than unity. Fig. 1.3(b) provides a qualitative representation of what is happening inside the transistor when current reversal is present.

While many assume BV_{CEO} to be a hard limit of operation for many circuit applications, which is the case for foundry-defined SOA boundaries, several works

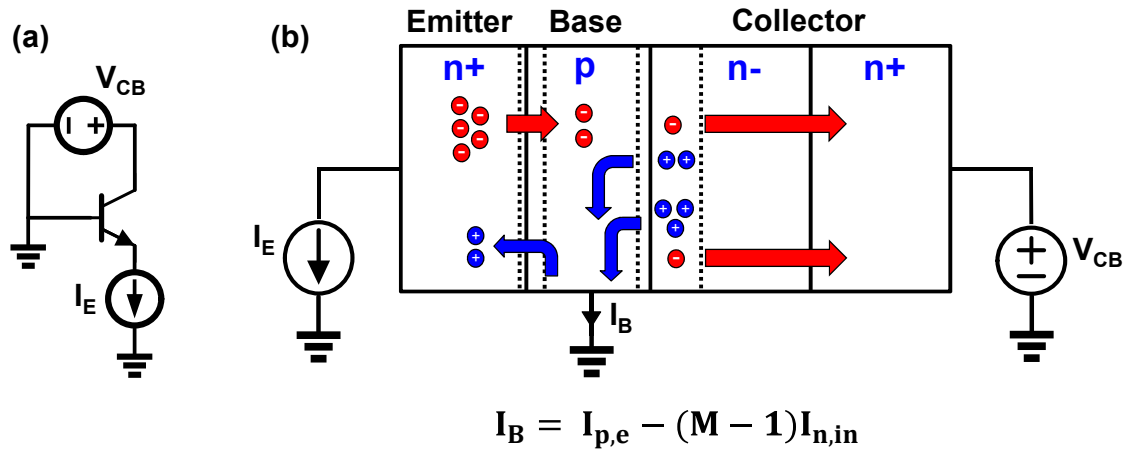

Figure 1.3: (a) Measurement set-up for common-base forced-I_E configuration, and (b) graphical representation of base current reversal.

in the literature have shown circuits operating beyond BV_{CEO} as a commonly-used practice [9], [10]. Furthermore, other works have shown the possibility of operating a SiGe HBT beyond BV_{CBO} [11]. This can be achieved when there is minimal overlap between the voltage-current waveforms as well as optimizing the base impedance used in a SiGe HBT in the common-base configuration. In the power amplifier (PA) world, being able to exploit the operation of an HBT beyond traditionally-defined SOA boundaries (BV_{CEO} and BV_{CBO}) is desirable because it will result in higher output power and power added efficiency (PAE). For these reasons, SiGe HBTs tend to be more suitable for certain PA applications over MOSFETs due to the higher voltage headroom inherently achieved in SiGe HBTs [12].

CHAPTER 2
RELIABILITY PHYSICS OF SIGE HBTS

SiGe BiCMOS technology has been shown to be an excellent choice for analog, digital, RF, and mm-Wave applications that require high levels of integration. Despite showcasing outstanding performance, achieving reliable operation in this technology is of interest in order to meet the stringent requirements imposed by the semiconductor industry.

Practically speaking, it is desired to have an integrated circuit (IC) that not only has high performance but also lasts for several years in a reliable manner. The motivation for studying the reliability physics of ICs is critical, as an unreliable product can be quite costly to a company. In fact, there are entire organizations within a company that devotes all of their work and time to investigate the reliability of their different IC technology offerings [13]. For these reasons, the reliability of ICs has become an important topic of research in both an industry and research setting since achieving robust reliability is essential for any particular IC application.

Ensuring reliable operation in SiGe HBTs (and any other device technology) implies that any circuit or system built from these devices should not degrade under typical operating conditions over an extended period of time (usually determined based on the application) [14]. At the transistor level, the reliability of SiGe HBTs can be quantified in two different ways: hard failures and soft failures. In the context of this thesis, we define the hard failure point of a SiGe HBT as the bias condition at which device transistor action fails, and the device becomes purely resistive as a result of catastrophic junction breakdown ("hard failure"). Based on this definition, a distinction between soft and hard SOA boundaries can be made, which accounts for performance degradation due to soft failure (e.g., degradation of speed, gain, and

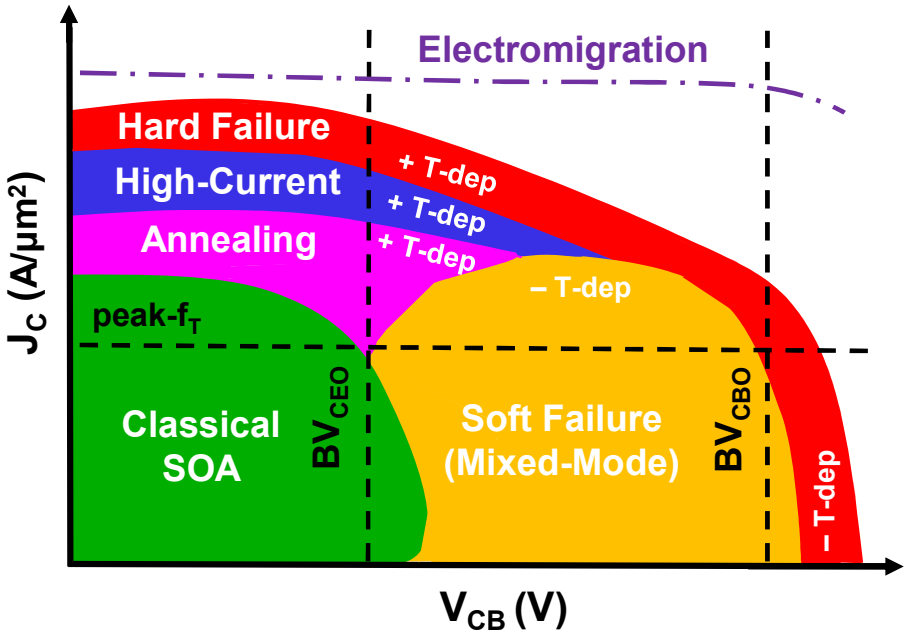

Figure 2.1: Qualitative representation of the damage spectrum of a SiGe HBT

noise) and the limits of hard failure for SiGe HBTs, respectively [8], [1].

2.1 Damage Spectrum of SiGe HBTs

The dynamic load line of a SiGe HBT operating in RF and mixed-signal circuits usually spans several regions of operation on the IV output plane. Fig. 2.1 shows a qualitative representation of the damage spectrum of an HBT for different voltages and currents (plotted J_C vs. V_{CB}).

At first glance, it becomes evident that the damage spectrum is quite "complex," as the distinct regions of operations in a SiGe HBT are driven by multiple damage mechanisms which have different temperature dependencies. The typical foundry-defined SOA is enclosed by the breakdown voltages to ensure little to no degradation over the lifetime of the device as shown by the green contour.

At voltages beyond BV_{CEO} and low-to-medium currents, the degradation of the device is primarily driven by hot-carrier damage due to impact-ionization, which has

a negative temperature dependence. This damage mechanism is referred to as mixed-mode stress damage and is shown by the yellow contour [14], [15].

When operating at medium to high currents and low voltages, the primary physical mechanism (enclosed by the magenta contour) is known as annealing since any traps created by hot-carrier damage are annealed due to self-heating effects of the device. However, at very high-currents (beyond J_C at peak-f_T), there is a high density of carriers at the centroid of the device and it can trigger an Auger generation/recombination process. This physical mechanism is known as high-current stress and is responsible for producing hot-carrier damage at the oxide interfaces. Previous works in the literature have shown experimentally the positive temperature dependence of this physical mechanism [16], [17].

For any currents and voltages beyond traditionally defined SOAs, the device will experience immediate failure due to thermal runaway (low voltage and high current) or "pinch-in effects" (moderate currents and high voltages). This hard failure boundary is denoted by the red contour. The electromigration limit (often referred to as J_{EM} in the literature) is shown by the purple curve [18]. Unlike the hard failure limit, the electromigration limit only considers the degradation of the metal layer and not the resultant intrinsic device degradation.

2.2 Mixed-Mode Stress Degradation

Operating a SiGe HBT beyond classical SOA boundaries (e.g., BV_{CEO}) has many benefits from a performance standpoint. However, when the device undergoes a simultaneous application of high V_{CB} and high J_C, it becomes vulnerable to mixed-mode stress degradation due to impact ionization [15]. This is particularly the case for scaled technologies since the collector doping is increased in order to suppress the Kirk effect, which in return increases the electric field at the CB junction. Doing so results in a much higher impact ionization rate.

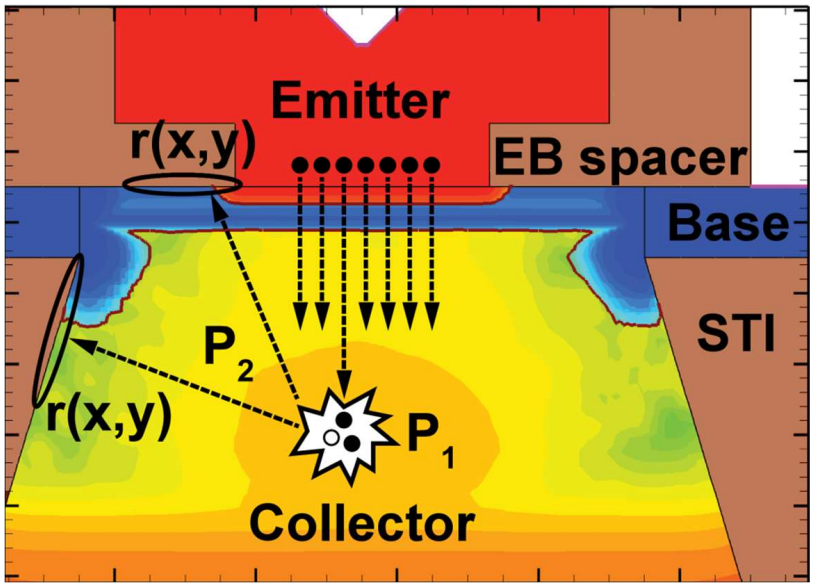

Figure 2.2: 2-D cross-section of a SiGe HBT model showcasing the mixed-mode stress degradation mechanism (after [19]).

Under mixed-mode conditions (high voltage and moderate to high currents), the minority carriers from the base will enter the high field region of the CB junction and they will impact ionize there due to the high field. This impact ionization process produces hot carriers which then with some probability will travel to the oxide interfaces. For a SiGe HBT, the carriers can be redirected to either the EB spacer oxide interface or the shallow-trench isolation (STI) oxide interface as seen in Fig 2.2. If the carriers have enough energy when they reach the oxide interface, they will de-passivate dangling bonds at the oxide/Si interface creating trap states [20]. These trap states are responsible for increasing base leakage current and subsequently collapsing the current gain.

Given the importance of this physical effect, it is desirable to not only characterize it at the transistor level but also model it for circuit applications. A commonly used method to characterize base current degradation due to mixed-mode stress degradation is to measure the Gummel characteristics at specific time intervals under forced-I_E and V_{CB} conditions. Fig. 2.3 shows the forward-mode Gummel characteristics as

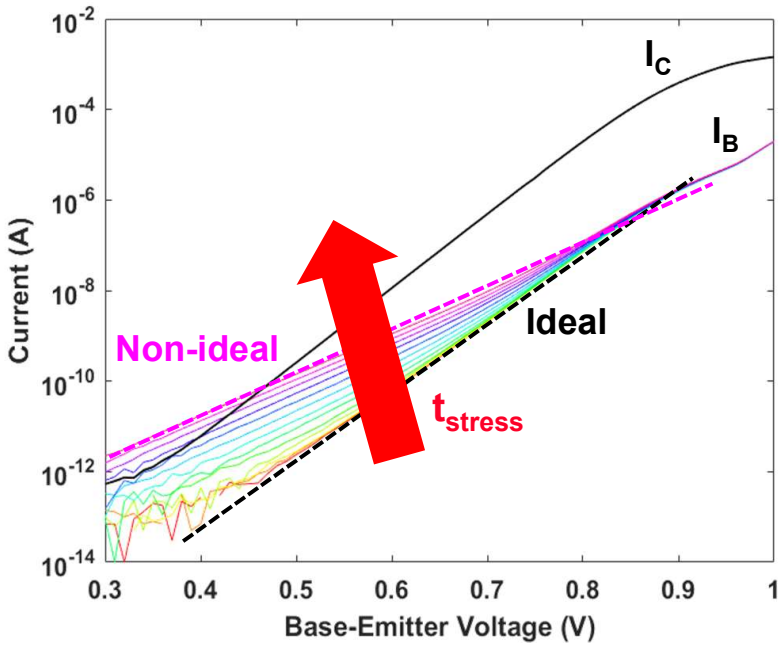

Figure 2.3: Forward-mode Gummel characteristics showing the base current degradation due to mixed-mode stress as a function of cummulative stress time.

a function of cumulative stress time for a typical mixed-mode condition. Based on this measured data, any changes in base current can be monitored over time and then implemented into a simulation environment. In fact, several works in the literature have developed the framework to accomplish this task in both TCAD and compact modeling environments [19, 21, 22, 23, 24].

2.3 High-Current Stress Degradation

A SiGe HBT operating near to or beyond peak-f_T current density and low voltage (high-current stress conditions) will undergo hot-carrier damage due to Auger recombination as suggested by [16, 17]. Unlike mixed-mode stress, where the electric fields are large enough to produce hot-carriers, high-current stress occurs when an electron-hole pair recombines via the Auger process and donates energy to a neighboring carrier. A hot carrier will produce significant damage if it has sufficient energy to break Si-H bonds (approximately 2.3 eV). This will be the case when the current

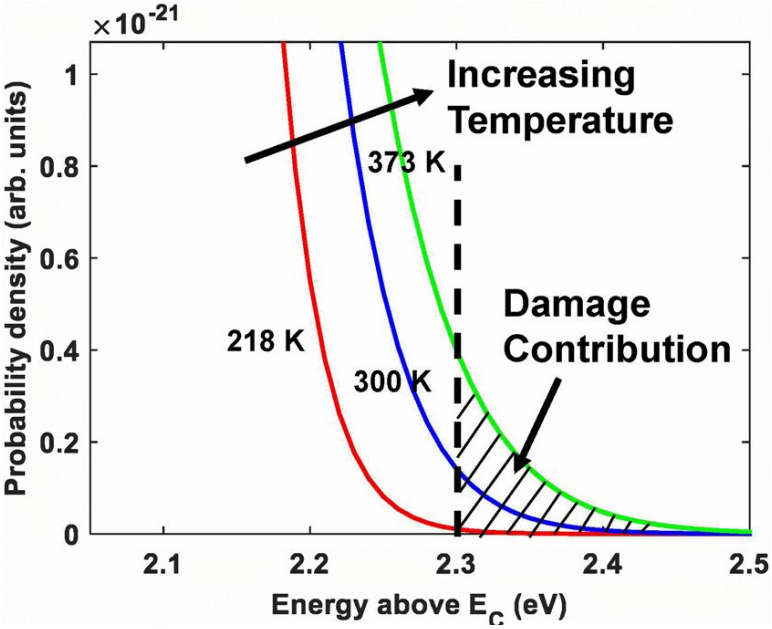

Figure 2.4: Hot-carrier energy distribution for high-current stress (after [16])

density in the device is high enough allowing multiple Auger recombination events to happen and hence providing a hot carrier with enough energy to break the Si-H bonds at the oxide interfaces. In return, this damage will translate into base current degradation over time.

High-current stress damage in SiGe HBTs follows a Maxwell-Boltzmann distribution, which ultimately determines the temperature dependence of this physical mechanism [16]. Fig. 2.4 shows a visual representation of the hot-carrier energy distribution for high-current stress as well as its temperature dependence. Notice that as temperature increases, the energy distribution becomes essentially wider showcasing the positive temperature dependence. More details on this physical mechanism can be found in [17, 16, 25], where they show experimentally the positive temperature dependence of high-current stress in SiGe HBTs as well as the simulation framework to model this effect.

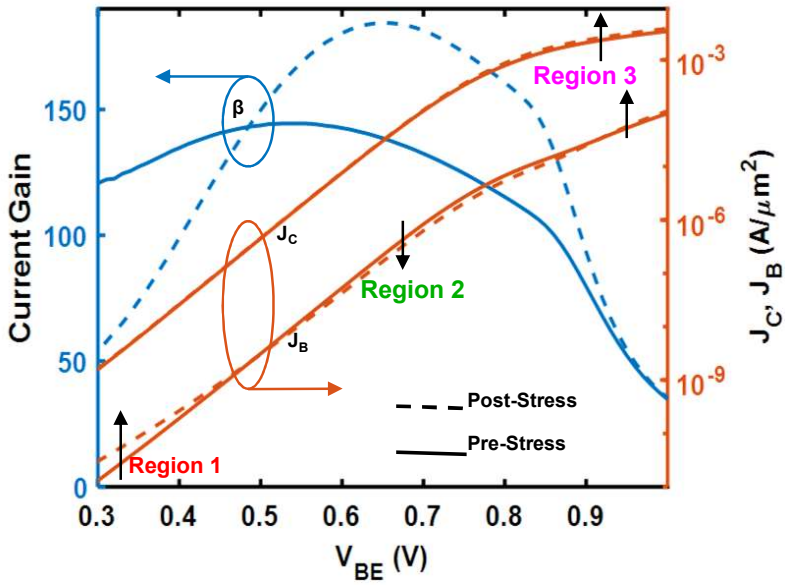

Figure 2.5: Measured degradation of Gummel characteristics and current gain in an NPN SiGe HBT for a high current stress condition of $V_{CB} = 0$ V, $J_E = 21.5$ mA/μm^2 (after [26]).

2.4 Current Gain Enhancement Effects (CGE) in SiGe HBTs

Up to this point, most of the efforts to study hot-carrier damage in SiGe HBTs have been attributed to damage in the oxide interfaces (EB spacer and STI) which translates to an increase in non-ideal base current in the low-injection regime. However, it has been shown recently in [26] that under high-current stress conditions, the degradation of the Gummel characteristics follows a non-classical behavior in the medium-to-high injection regime (base current increases or decreases over time). This behavior can be observed in Fig. 2.5, where Region 1, Region 2, and Region 3 represent the low injection, medium injection, and high injection regimes, respectively. Such non-idealities can be attributed to hot-carrier damage at the polysilicon emitter of a SiGe HBT, which in return enhance the current gain in the medium injection regime (Region 2) hence the name current gain enhancement effect (CGE).

For the most part, SiGe HBTs employ polysilicon emitters in order to block base

current injection and ultimately increase the current gain of the device [27]. In comparison to doped crystalline silicon, the multigrain nature of polysilicon gives rise to much smaller mobilities and minority carrier lifetimes allowing for minority carriers to diffuse shorter lengths in the polysilicon and contribute less to the overall current flow [26]. This implies that the quality growth process and the physical properties of polysilicon will determine how severe the effect of hot-carrier damage can be.

When hot carriers interact with the grain boundaries of the polysilicon, which is the case for both the polysilicon emitter and polysilicon base in a SiGe HBT, any hydrogen atoms that passivate the grain boundaries have a probability of becoming displaced. This particularly occurs under high-current stress conditions, as hot carriers have enough energy to penetrate further into the polysilicon. On the other hand, hot carriers produced due to mixed-mode stress are more likely to stop at the polysilicon-silicon interface since they do not enough energy to continue further and produce damage [26].

Any depassivation due to hot-carrier damage will cause the local mobility of the carriers in the polysilicon to decrease and consequently reduces the diffusion length of minority carriers injected in the polysilicon. When this happens, the base current will decrease and the current gain enhances past its initial value. Fig 2.6 summarizes what happens inside a SiGe HBT when the polysilicon emitter and polysilicon base are subjected to hot-carrier damage due to high current stress. Overall, accurately modeling the current gain enhancement effect is crucial for any RF circuits application since this effect becomes prevalent at medium-to-high injection, where high-speed circuits are typically biased to extract maximum device performance.

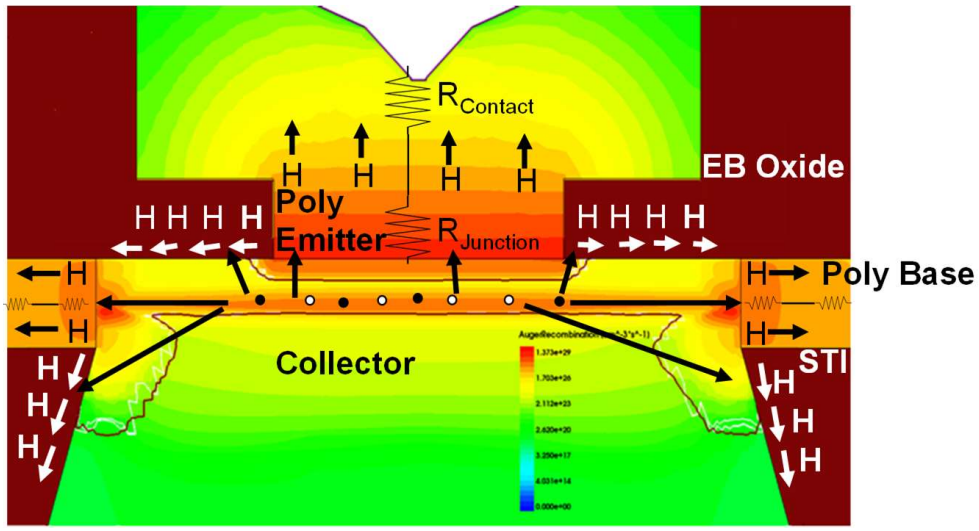

Figure 2.6: Cross-section of a SiGe HBT under high current stress damage done to oxide interfaces and polysilicon emitter and polysilicon base (after [26]).

CHAPTER 3
HARD FAILURES AND MAXIMUM USABLE RANGE OF SIGE HBTS

As the performance of state-of-the-art silicon-germanium heterojunction bipolar transistors (SiGe HBTs) continues to improve, several reliability concerns arise due to the increase in operating current density. A trade-off between breakdown voltage and current carrying capability has become an issue of great importance in scaled SiGe HBT technologies. Thus, a scaled SiGe HBT is forced to operate in a regime where it becomes susceptible to hot-carrier effects driven by the electrical bias conditions (current and voltage) and temperature [21]. Well-known "classical" voltage operating limits, namely collector-emitter breakdown voltage with an open base (BV_{CEO}) and collector-base breakdown voltage with an open emitter (BV_{CBO}), are often used as traditional foundry-defined safe operating area (SOA) boundaries for various bias configurations. However, the maximum limit of the operational range for SiGe HBTs is actually a complex reliability problem that requires additional understanding not provided by breakdown voltages alone. For example, some forbidden boundaries of operation are attainable at high current densities before reaching the limits set by BV_{CEO} and BV_{CBO} [28].

Conventional approaches to quantifying the reliability physics of SiGe HBTs consider exclusively performance degradation over time as the main limiting factor, also known as soft failure. This thesis focuses on exploring the limits of instantaneous failure or hard failure in greater detail. As such, the hard failure point of a SiGe HBT is defined as the bias condition at which the device transistor action fails, and the device becomes purely resistive as a result of catastrophic junction failure. Based on this definition, a distinction between soft and hard SOA boundaries can be made,

which accounts for performance degradation due to soft failure (e.g., degradation of speed, gain, noise) and the limits of hard failure for SiGe HBTs, respectively.

The ability to predict hard failures and maximum usable range of operation in a SiGe HBT provides useful insight to a circuit designer on the current and voltage capabilities of a device biased under conditions that challenge foundry-defined SOA limits. Consequently, it is desirable to define the hard SOA boundaries for SiGe HBTs, given that reliability physics-based models in the literature only predict soft SOA boundaries, while taking electrical-stress-induced aging into consideration [16, 21, 22, 24, 25]. By having access to sophisticated models that predict both soft and hard SOA boundaries, an alternate view to the understanding of SiGe HBT SOA and reliability can be attained. For example, [8] showed that operating the common-base (C-B) device in a cascode amplifier above soft SOA boundaries results in no noticeable degradation to the overall amplifier performance. Knowing the hard SOA boundaries in scenarios such as [8] will greatly aid circuit optimal design.

This thesis investigates the maximum usable range due to collector-base-emitter (C-B-E) and collector-emitter (CE) junction breakdown in scaled SiGe HBT technologies. A new failure metric, J_{Ecrit}, is proposed, which is defined as the maximum allowable emitter current density (J_E) at a given collector-base voltage (V_{CB}) before a SiGe HBT undergoes hard failure. Unlike J_{EM} (the electromigration limit) or snap-back points extracted from flyback methods, J_{Ecrit} is obtained when the device is pushed to high current densities and the point of failure is reached. The boundaries defined using flyback methods estimate the current limits at high V_{CB} (i.e., when impact ionization is present) and low to medium current densities without damaging the device [4]. J_{EM}, on the other hand, is known to be a generous limit that only considers the degradation of the metal layer and not the resultant intrinsic device degradation [18].

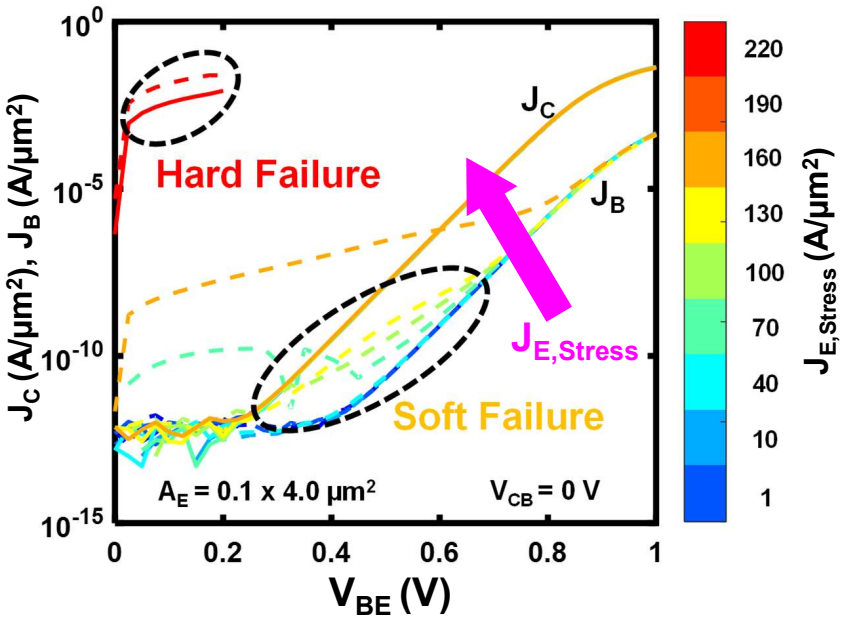

Figure 3.1: Comparison between soft failure (performance degradation) and hard failure for a SiGe HBT with emitter area $A_E = 0.1 \times 4.0\ \mu m^2$. J_C and J_B degradation is shown from Gummel characteristics at $V_{CB} = 0$ V for different $J_{E,Stress}$ until reaching hard failure due to junction breakdown at high current densities.

3.1 Physics of Hard Failure

In recent literature, most of the focus has been devoted to soft failure studies that target the change of performance in SiGe HBTs due to hot-carrier damage [16, 21, 22, 24, 25]. It is important to make a clear distinction between soft failure and hard failure given the nature of this thesis. Fig. 3.1 illustrates the difference between the two damage mechanisms.

Up to high emitter stress current densities ($0\ mA/\mu m^2 \leq J_{E,Stress} \leq 140\ mA/\mu m^2$), there is a shift in base current density (J_B) due to soft breakdown. However, past a certain high J_E limit ($J_E > 200\ mA/\mu m^2$), the bias condition of the device approaches the hard failure limit (J_{Ecrit}), creating a major shift in the base current density (J_B).

Beyond this point, the device no longer operates as a transistor. Once the hard

failure limit is reached, the SiGe HBT undergoes irreversible junction breakdown damage. Nonetheless, knowing precisely the location of the hard SOA boundaries does not provide enough information to ensure complete knowledge of the physics that leads to hard failure.

To have a full understanding of what is happening at the device level, it is necessary to consider the damage mechanisms that come into play as a SiGe HBT reaches its maximum range of operation. Most importantly, the significance of self-heating, impact ionization, and avalanche multiplication induced current-crowding instabilities ("pinch-in" effects) drive the physics of failure within the device.

The C-B forced-I_E bias configuration, which serves as the setup used for the measurements done in this work, functions in such a way that the base current (I_B) is not fixed by an external high-resistive DC source, unlike for the common-emitter bias configuration. This implies that any excess hole current from impact ionization can freely exit the base terminal [29]. Once the collector-emitter voltage (V_{CE}) surpasses BV_{CEO}, it causes I_B to reverse polarity due to avalanche-generated holes.

Ultimately, two competing mechanisms are happening simultaneously within the device when I_B reverses sign. Any voltage drop across the distributed base resistance increases the potential of the emitter-base (E-B) junction at the center of the device forming a positive feedback mechanism. Likewise, the voltage drop across the parasitic emitter resistance due to I_E creates negative feedback, reducing the potential of the E-B junction at the center of the device. The overall effect of the competing mechanisms leads to a nonuniform current distribution that collapses towards the center of the device. This effect has been described in the literature as "pinch-in." Its consequences include electric field collapse and C-E junction breakdown damage if the V_{CB} voltage is high enough, as observed in this thesis [29, 30].

The I_B that sets the limit of operation of the device due to "pinch in," known as critical base current (I_B^*), was modeled in [28] as

$$I_B^* = -\frac{V_T + r_e I_E}{R_{Bx} + r_{bi}} \left[1 + \frac{{w_e}^2}{l_E}\right], \tag{3.1}$$

where V_T is the thermal voltage, r_{bi} is the small-signal internal base resistance, r_e small-signal emitter resistance, R_{BX} is the extrinsic base resistance, l_E is the emitter length and w_E is the emitter width. Note that the magnitude of I_B^* has a positive temperature dependence, mainly due to the V_T and r_{bi} terms.

Although "pinch-in" effects are strongly enhanced by impact ionization at high V_{CB}, high values of J_E at low V_{CB}, in combination with self- heating effects, can cause breakdown due to thermal runaway, in which the device stops functioning permanently as a result of high junction temperatures (T_j) and large J_E quantities. An analogous way of describing this effect is by treating all the device terminals as shorts. This failure mechanism will be further explained qualitatively when analyzing the measured data.

3.2 Measurement Methods

To predict and measure the hard SOA boundaries in the forced-I_E bias configuration given by J_{Ecrit}, on-wafer measurements were performed for the GlobalFoundries 90 nm SiGe HBT platform (9HP) high-performance device variant ($BV_{CEO}/BV_{CBO} = 1.7/5.2\ V, J_C = 20\ mA/\mu m^2$ @ peak $f_T = 300\ GHz$), using various emitter lengths and layout configurations (C-B-E-B-C and C-B-E) [31].

In a C-B bias configuration, V_{CB} was fixed and $J_{E,Stress}$ was applied for one second and swept at intervals of 1 $mA/\mu m^2$. The bias points for all three terminals were recorded accordingly at each $J_{E,Stress}$ interval, in order to monitor for device failure. The stress was interrupted periodically every 10 $mA/\mu m^2$ to measure the degraded Gummel characteristics and track the soft breakdown of the device. Sufficient data were collected until the device reached the instantaneous hard failure limit (Gum-

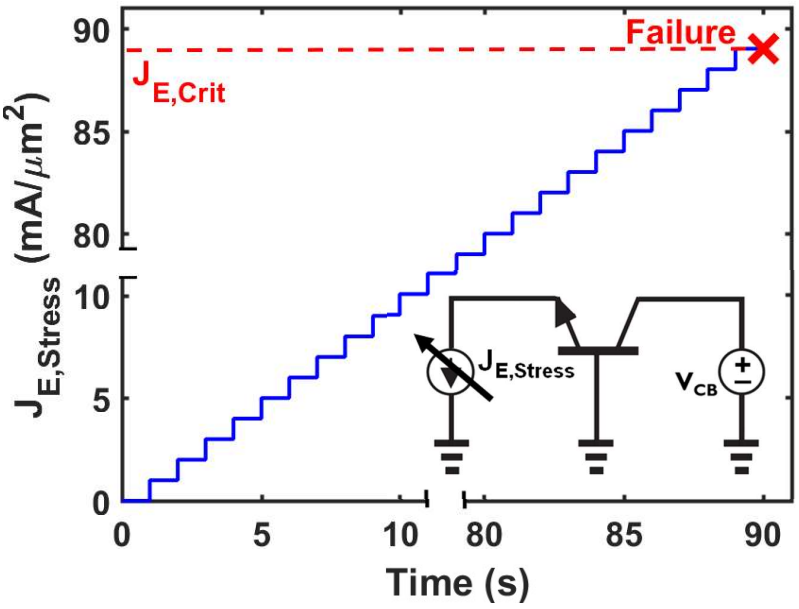

Figure 3.2: Measurement set-up for hard failure measurements using the C-B bias configuration.

mel characteristics strongly deviated from normal operation after reaching the J_{Ecrit} boundary). A visual representation of the set-up can be seen in Fig. 3.2.

3.3 Analysis of Measurement Results

To confirm the theory discussed in the previous sections, both failure mechanisms (C-E/C-B-E junction breakdown) are shown in Fig. 3.3 based on measurements at low and high V_{CB} values of 0 V and 4 V, respectively. As expected, the enhancement of "pinch-in" effects due to high V_{CB} is responsible for producing breakdown at the C-E junction. The C-E junction is shorted and measured values of J_C and J_E are nearly identical, whereas the base terminal presents a high impedance current path, if this condition is met. A similar approach was performed to verify the failure mechanism at low V_{CB} values. The measured J_{Ecrit} for hard failure from thermal runaway was responsible for causing severe self-heating effects. The Gummel characteristics show the expected behavior, as described in the physics of breakdown section (i.e., all three

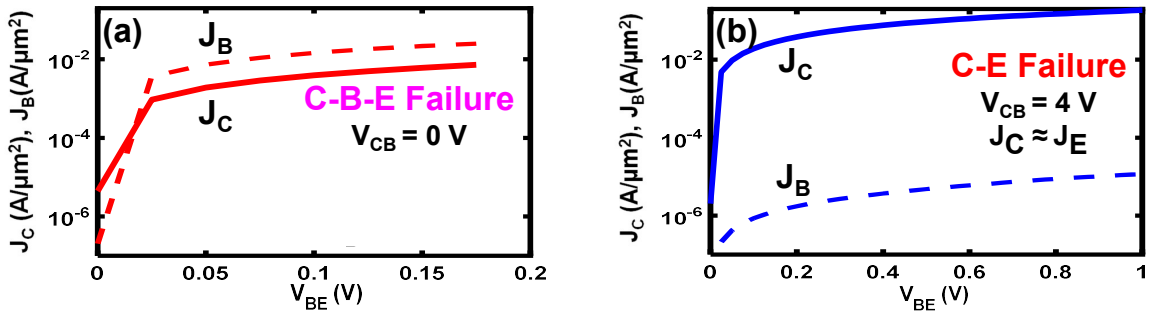

Figure 3.3: Gummel characteristics for failure mechanisms due to C-E junction breakdown (high V_{CB}) and C-B-E junction breakdown (low V_{CB}) plotted vs. a fresh device.

terminals shorted).

3.3.1 Geometry Dependence

Emitter lengths of 2.0 μm, 3.0 μm, and 4.0 μm were chosen for this study based on commonly used sizes as given by the PDK (i.e., the "p-cells"). Fig. 3.4 shows the J_{Ecrit} hard SOA boundaries for the HP C-B-E-B-C configuration with the listed emitter lengths at a fixed w_E = 90 nm. Based on these measurements, geometry clearly plays an important role suggesting that shorter devices have a higher J_{Ecrit} regardless of V_{CB}. An explanation for this is due to the reduced T_j for shorter devices, hence producing weaker self-heating effects in comparison to the larger devices that have a higher thermal resistance (R_{th}) per unit area.

At high V_{CB} (near 4 V), consider the geometry dependence of R_{th} and the proportionality of the ratio of w_E over l_E^2 in (1). This suggests that shorter devices will experience "pinch-in" at a higher current density compared to larger devices. Fig. 3.5 shows the normalized ratio of J_{Ecrit} between the largest device (4.0 μm) and the smaller devices. The inflection points shown near V_{CB} values of 2.0 V − 2.5 V are due to the onset of "pinch-in" effects starting to dominate over breakdown due to thermal runaway. The V_{CB} responsible for triggering "pinch-in" is geometry dependent, as described by (1), resulting in a lower J_{Ecrit} ratio as illustrated in Fig. 3.5.

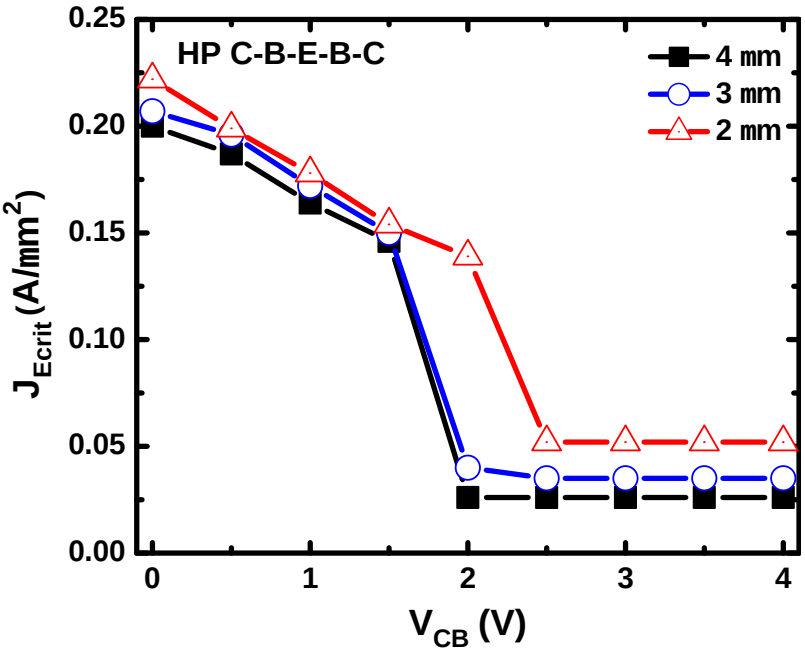

Figure 3.4: Hard SOA boundaries for HP C-B-E devices with different l_E and fixed w_E of 90 nm (single measurement on chosen devices).

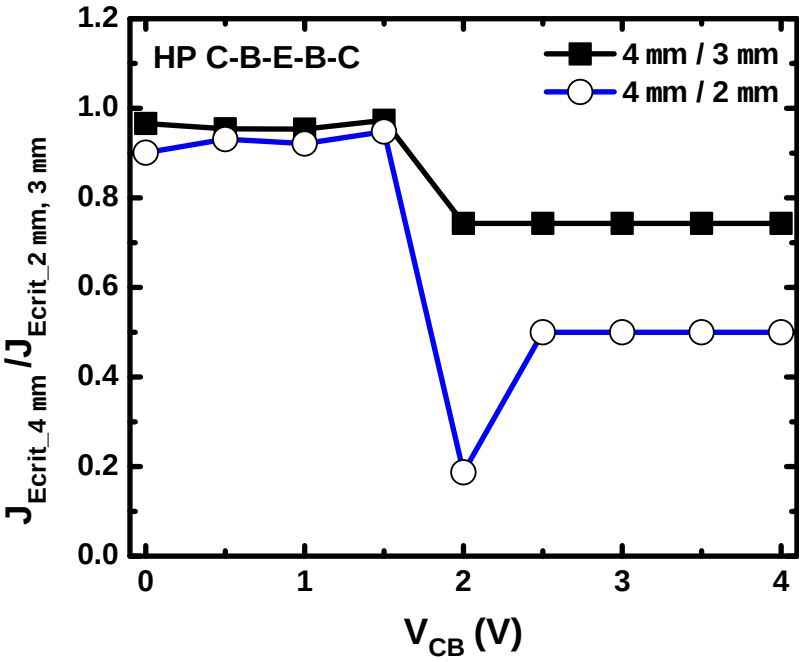

Figure 3.5: Ratio of J_{Ecrit} between C-B-E-B-C and C-B-E devices at a fixed emitter length.

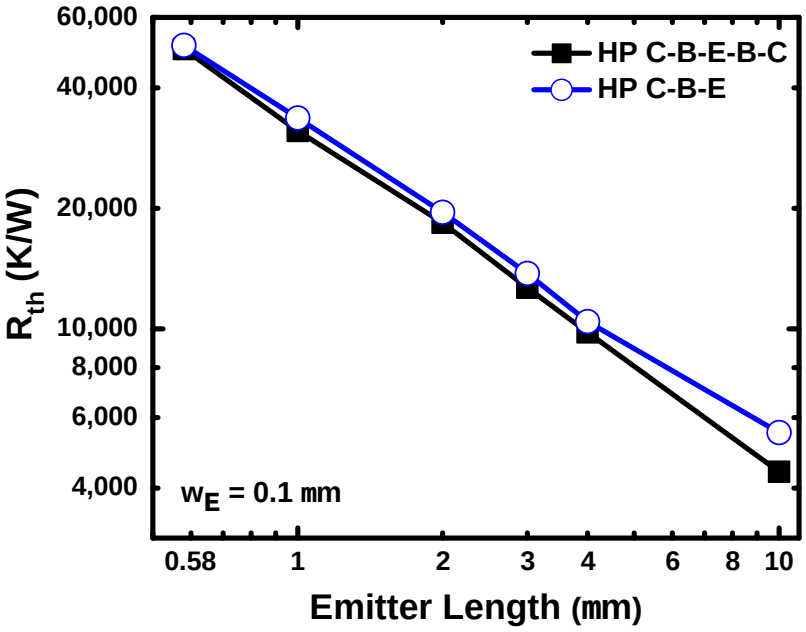

Figure 3.6: R_{th} values for C-B-E-B-C and C-B-E device configurations for different emitter lengths.

3.3.2 Layout Configuration Dependence

Circuit designers enjoy access to multiple geometrical parameters (e.g., emitter length variations) in addition to different layout configurations. There are well-known trade-offs in performance when going from one layout configuration to another. Furthermore, the R_{th} and J_{Ecrit} values also differ to some extent. In [32], the values of R_{th} for the C-B-E configuration are slightly higher than those of the C-B-E-B-C configuration because of smaller device area inside the deep trench footprint, leading to a higher T_j.

To showcase the difference between the R_{th} in the C-B-E-B-C and C-B-E configurations across geometry, measurements were performed for each emitter length available in the PDK using the extraction method from [33]. The measured data is shown in Fig. 3.6, which agrees with the results in [32] and justifies the geometry and layout configuration R_{th} dependence.

In this work, the C-B-E-B-C configuration shows a higher J_{Ecrit} in comparison to

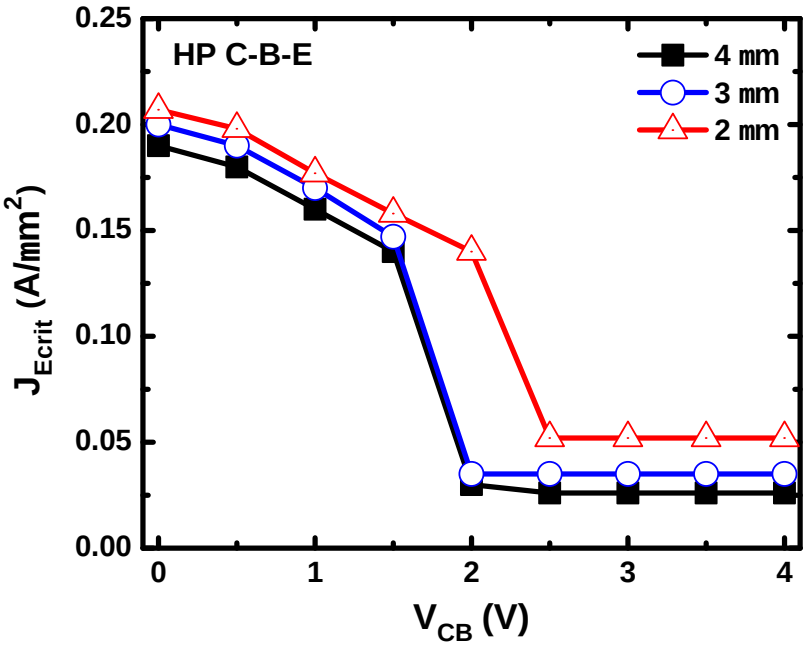

Figure 3.7: Hard SOA boundaries for HP C-B-E devices with different l_E and fixed w_E of 90 nm (single measurement on chosen devices).

the C-B-E configuration at moderately low V_{CB}, which can be seen from the hard SOA boundaries for different geometries in Fig. 3.7 and the normalized ratio of J_E for a fixed V_{CB} between the C-B-E-B-C and C-B-E devices in Fig. 3.8. The difference in J_{Ecrit} can be attributed to the additional base and collector terminals in the C-B-E-B-C configuration. At high J_C, the amount of I_B that is supplied grows non-linearly (i.e., the current gain severely drops). For a C-B-E device, J_B is approximately twice as much as the J_B through a C-B-E-B-C device for the same J_C, posing several reliability constraints: (1) A large J_B allows for additional Auger carrier damage for the same J_C within a C-B-E device, (2) If J_B continues to increase without bounds, the device will experience a catastrophic open base failure at a smaller J_C in a C-B-E device.

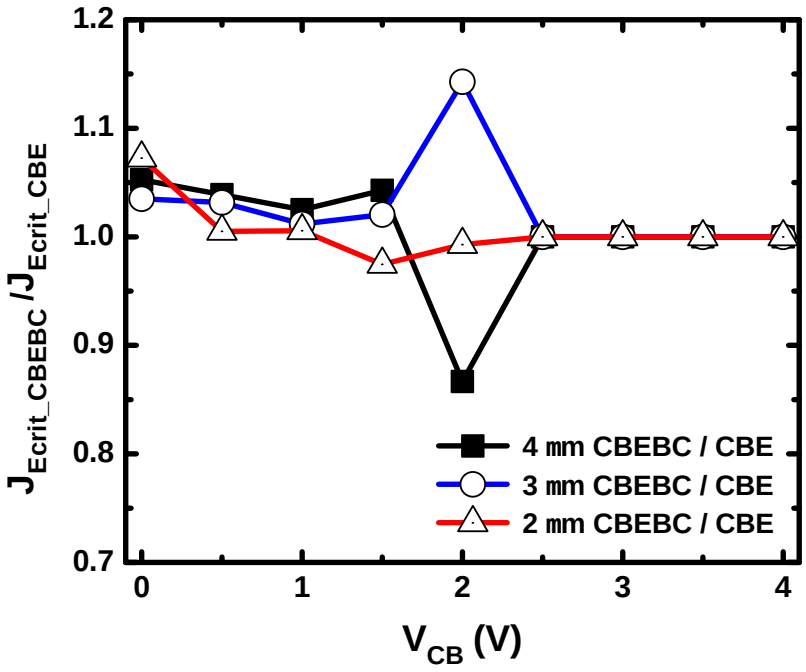

Figure 3.8: Ratio of J_{Ecrit} between C-B-E-B-C and C-B-E devices at a fixed emitter length.

3.3.3 Temperature Dependence

Temperature plays a significant role given that any variation affects the value of J_{Ecrit}. A similar approach was done to measure the hard SOA boundaries for an HP C-B-E-B-C device with emitter length of 10.0 μm at three temperatures (300K, 323K, and 348K) as shown in Fig. 3.9. Based on the assumptions made to describe the temperature dependence in (1), it is expected for J_{Ecrit} to increase at medium V_{CB} as V_T is increased. This is observed for the measured hard SOA boundaries at the onset of "pinch-in" (2.5 V $-$ 3.0 V), which is why the V_{CB} values to trigger "pinch-in" effects happen to be higher as seen in the downward inflection point at $V_{CB} = 3.0$ V in Fig. 3.10. At low V_{CB} bias, J_{Ecrit} is shown to decrease because of enhanced self-heating effects due to the combination of higher ambient temperature and current density operation. A similar study was performed in [28] to investigate the temperature dependence of the V_{CB} needed to trigger "pinch-in" effects. This

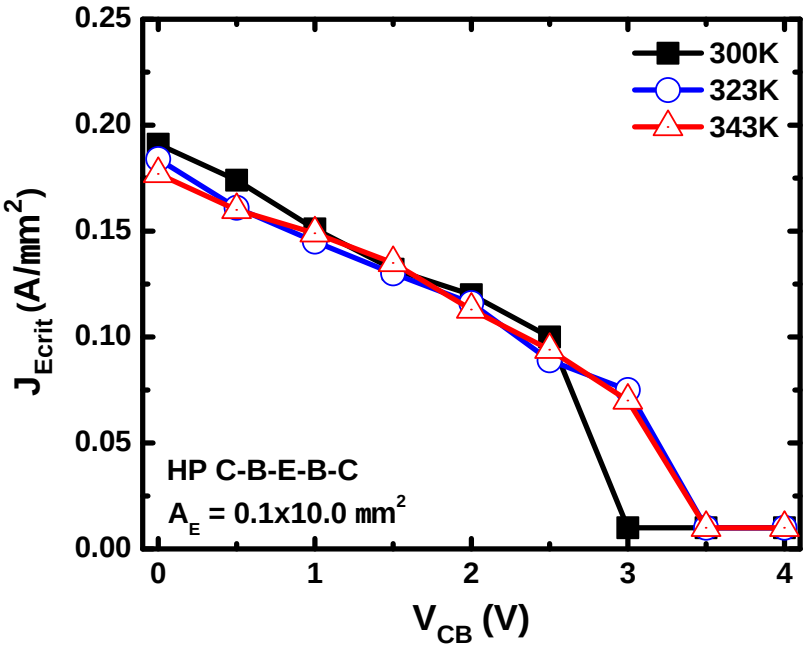

Figure 3.9: Hard SOA boundaries at 300K, 323K, and 348K for a C-B-E-B-C SiGe HBT with $A_E = 0.1 \times 10.0\ \mu m^2$ (single measurement on chosen devices).

V_{CB} value was shown to decrease when exposed to lower temperatures due to the temperature dependence of impact ionization, suggesting additional evidence to what was observed in this work.

3.4 Summary

The hard SOA boundaries of operation for scaled SiGe HBTs, as given by a newly defined hard failure metric, J_{Ecrit}, were investigated in this thesis. Key physical parameters such as geometry, layout configuration, and temperature were demonstrated to impact hard failures. Knowing the mechanisms that lead a SiGe HBT to its maximum range of operation is the first step to implementing a "red flag" warning mechanism that can be used to predict hard SOA boundaries in addition to their respective failure mechanisms. Ultimately, combining both modeling aspects for the prediction of hard and soft SOA boundaries will provide circuit designers with the necessary tools to accurately predict the aging and maximum limits of operation for

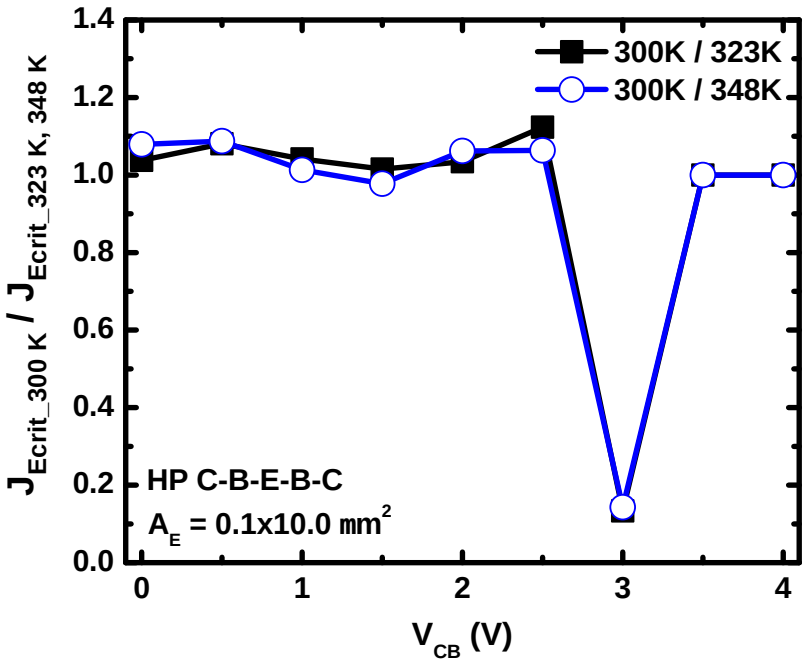

Figure 3.10: Ratio of J_E between temperature at 300 K and higher temperatures (323 K, 348 K).

SiGe HBT circuits.

CHAPTER 4
SOFT FAILURE MECHANISMS IN HIGH-BREAKDOWN SIGE HBTS

Achieving high-frequency performance while maintaining useful operating voltages has been a major challenge in SiGe HBTs due to the unavoidable trade-off in transistor-level maximum small-signal frequency response and breakdown voltage (i.e., the Johnson limit [6]). In order to provide a competitive solution to meet the stringent performance requirements of RF and mm-Wave applications, it is necessary to find clever ways to overcome this trade-off and ultimately enhance the RF power handling capabilities of a SiGe HBT. Therefore, having access to distinct variants of a device with different breakdown voltages (e.g., BV_{CEO} and BV_{CBO}) and peak-transit frequencies (f_T) is desirable in many ways because it provides circuit designers with the flexibility to optimize their design based on any particular application. In fact, this has been the path that many commercial SiGe BiCMOS platforms have followed in order to cover all possible circuit applications ranging from analog to high-speed digital to RF and mm-Wave [34].

For applications that involve the use of RF integrated circuits (RFICs), there are numerous trade-offs that need to be taken into account. Such trade-offs are summarized in the RF design hexagon of Fig 4.1. For example, obtaining a higher gain usually requires using a larger voltage supply. To accomplish this task, the device in play should meet a specific breakdown voltage requirement based on the value of the supply voltage.

Just like how CMOS technologies offer field-effect transistors (FETs) with various threshold voltages and different gate oxide thicknesses to trade-off speed with DC power consumption, the use of high-breakdown (HB) SiGe HBTs is particularly useful

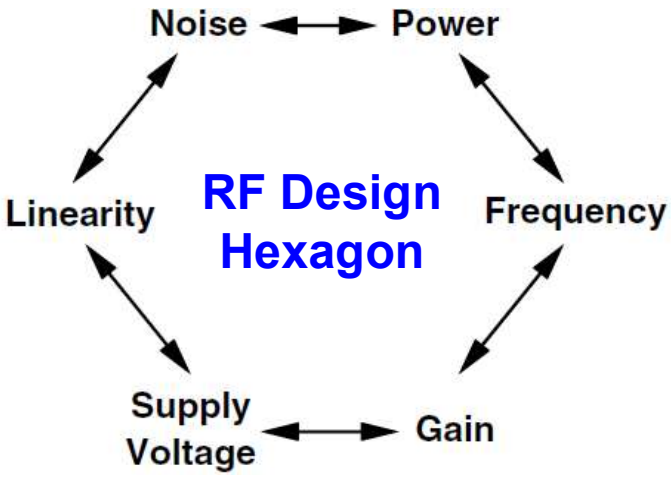

Figure 4.1: RF Design Hexagon (after [35]).

when designing RFICs. Several works in the literature have shown the advantages of using a hybrid approach of both high-performance (HP) and high-breakdown SiGe HBTs to optimize for power, bandwidth, gain, linearity, and output drive voltage in various RF circuit blocks. Two examples are showcased in Fig. 4.2(a) and 4.2(b), which correspond to a high-linearity, X-band low-noise amplifier (LNA) and a high-gain, two-Stage, X-band SiGe power amplifier (PA), respectively [36, 37].

Based on these examples, it is clear that there is a performance advantage when using HB SiGe HBTs. However, the reliability of HB devices is still an unexplored topic that should be taken into consideration. Doing so will allow for more robust designs and ultimately improved performance that cannot be attained by just considering foundry-defined safe-operating areas alone. In the majority of the cases, these SOA rules can be safely violated because there are several physical aspects (e.g., geometry, biasing configuration, and layout configuration) that are ignored to simplify the complexity of the situation. Furthermore, this traditional approach is not practical as it sacrifices the overall performance of a circuit or a system by not fully utilizing the maximum achievable performance of a device [25].

This thesis aims to show a comprehensive study of the various reliability mecha-

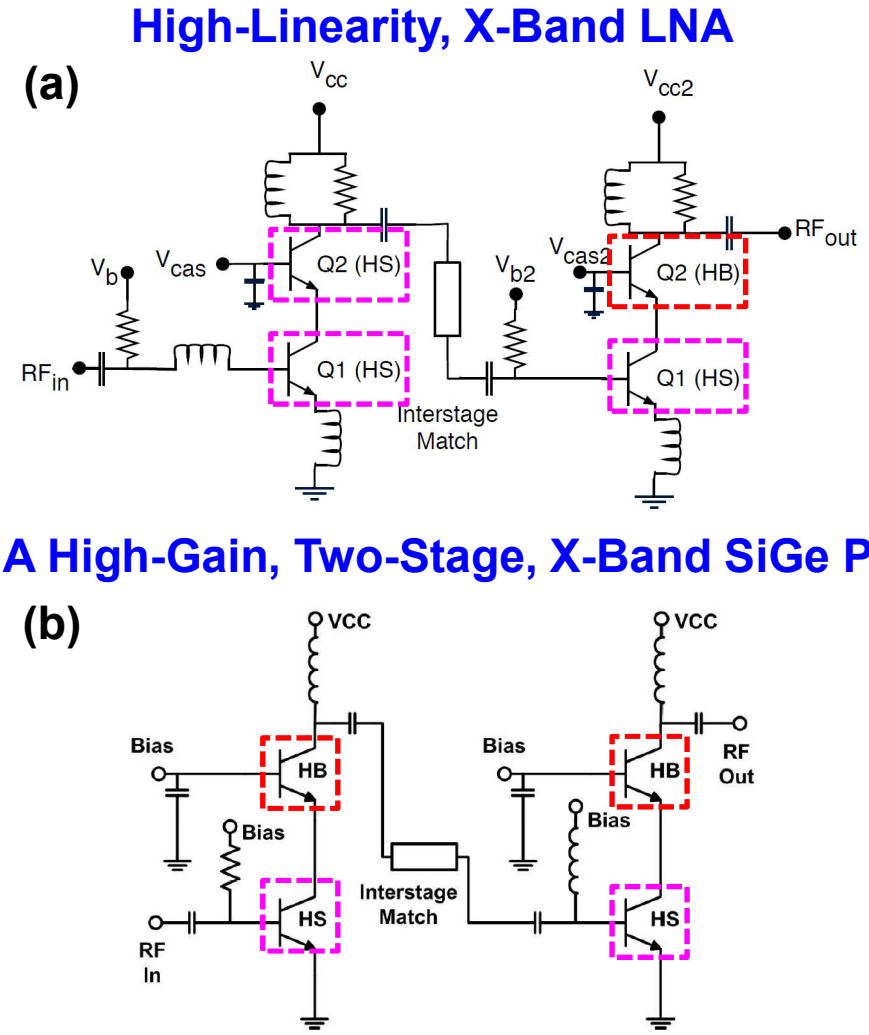

Figure 4.2: (a) A high-linearity, X-band low-noise amplifier (after [37]. (b) A high-gain, two-Stage, X-band SiGe power amplifier (after [36])

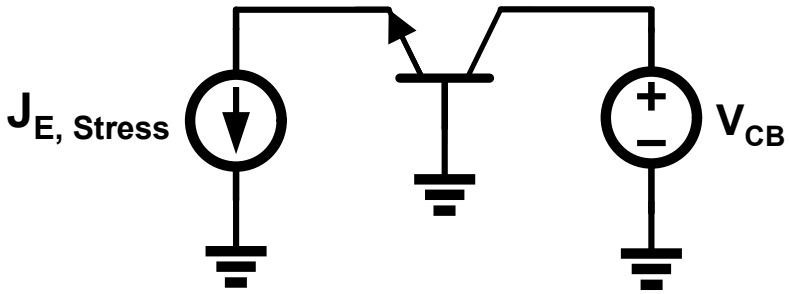

Figure 4.3: Set-up for reliability stress measurements.

nisms in HB SiGe HBTs by comparing it to its HP counterpart. From this comparison, several conclusions can be made with regard to the maximum usable range of these devices as well as any trade-offs in performance and reliability when using either HB or HP variants for circuit design applications that benefit greatly from using a hybrid combination of both variants.

4.1 Testing Set-up

The devices used for this study were high-performance and medium-breakdown SiGe HBTs from GLOBALFOUNDRIES 90 nm 9HP SiGe BiCMOS platform. The npn HP SiGe HBT features a unity current and power gain frequencies f_T/f_{max} of 300/360 GHz, J_C at peak f_T of about 20 $mA/\mu m^2$, open-base breakdown voltage BV_{CEO} of 1.7 V, and open-emitter breakdown voltage BV_{CBO} of 5.2 V. Likewise, the MB npn SiGe HBT offers an f_T/f_{max} = 135/350 GHz, J_C at peak $f_T \approx 5$ $mA/\mu m^2$, BV_{CEO} = 2.4 V, and BV_{CBO} = 7.9 V [31]. Reliability stress measurements were conducted using devices with a single drawn emitter size of 0.1 x 3.0 μm^2 and 0.1 x 4.0 μm^2 unless indicated otherwise. To monitor for soft failure degradation, measurements were performed on-wafer at room temperature (T = 27^{o}C) by applying a constant emitter current density (J_E) and a constant collector-base voltage (V_{CB}) for a stress time t_{stress} = 10,000 sec. The degradation was monitored by interrupting the stress periodically and measuring the Gummel characteristics.

Table 4.1: Key AC and DC figures-of-merit for high-performance and medium-breakdown SiGe HBTs (after [31]).

Device	Parameter	Value
HP NPN CBEBC	peak-f_T	300 GHz
	peak-f_{max}	360 GHz
	BV_{CEO}	1.7 V
	BV_{CEO}	5.2 V
MB NPN CBEBC	peak-f_T	135 GHz
	peak-f_{max}	350 GHz
	BV_{CEO}	2.4 V
	BV_{CEO}	7.9 V

4.2 The Medium-Breakdown SiGe HBT

At its core, the MB device used in this thesis is a modification of the HP device integrated on the same wafer with one-mask deviation. From a processing standpoint, it means that all structural aspects are kept the same with the exception of the collector profile. Doing so reduces cost and process complexity, which is desired in any SiGe BiCMOS platform [34].

In terms of performance, the MB device achieves breakdown voltages (BV_{CEO} and BV_{CBO}) slightly higher than the HP variant at the expense of f_T performance. However, the f_{max} of both variants are comparable, differing by approximately 10 GHz. Table 4.1 summarizes the key AC and DC figures-of-merit for both the HP and MB variants.

To understand any subtle processing differences among the HP and MB devices, a schematic representation of the cross-section for each device is shown in Fig. 4.4(a) and 4.4(b) for the HP and MB variants, respectively (after [34]). The main attribute of the HP device is the use of the selectively implanted collector (SIC), which is used to improve the high collector current density (J_C) performance and tune the breakdown voltage [38].

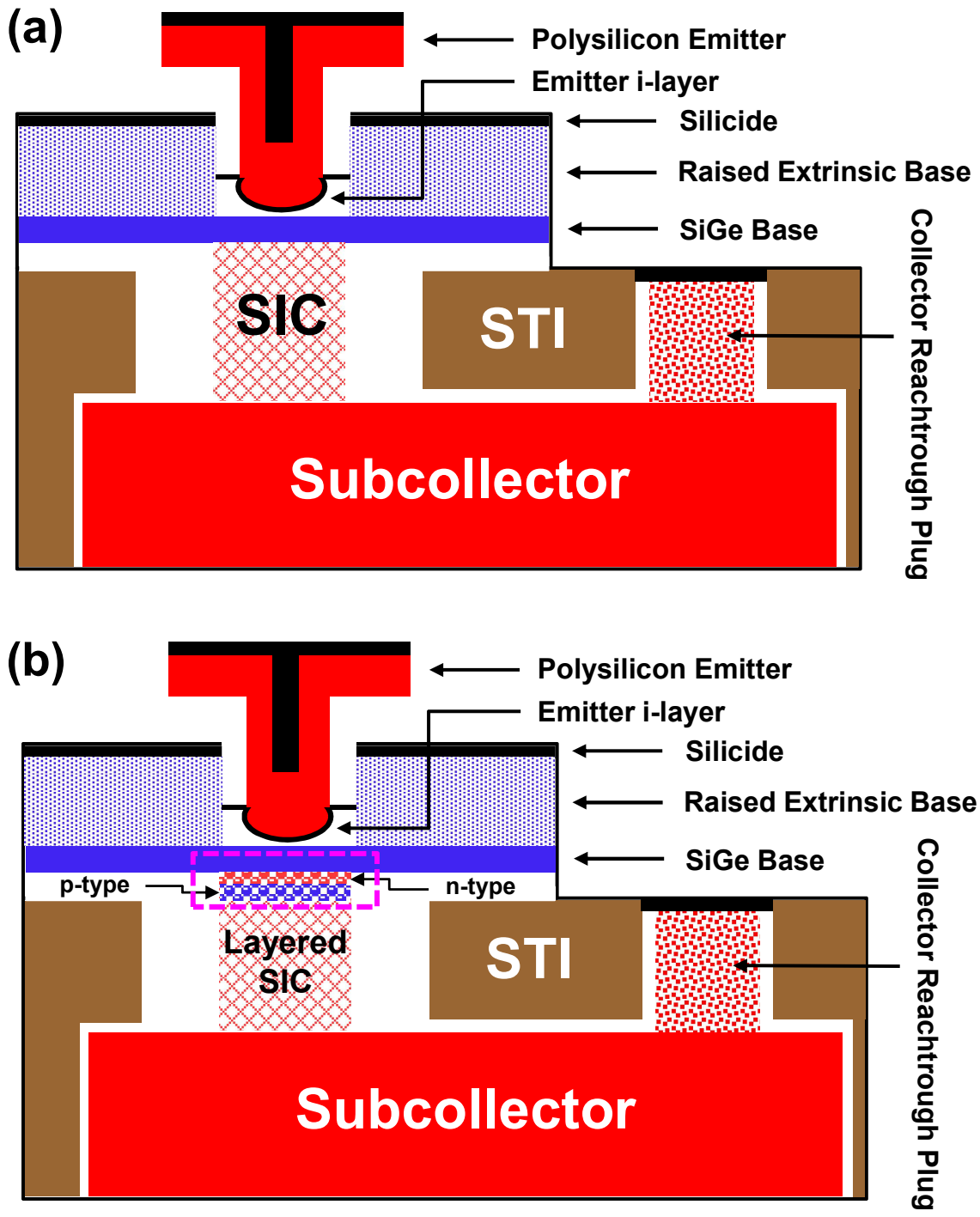

Figure 4.4: Schematic representation of the cross-section for the SiGe HBTs used in this thesis: (a) high-performance SiGe HBT and (b) medium-breakdown SiGe HBT (after [34]).

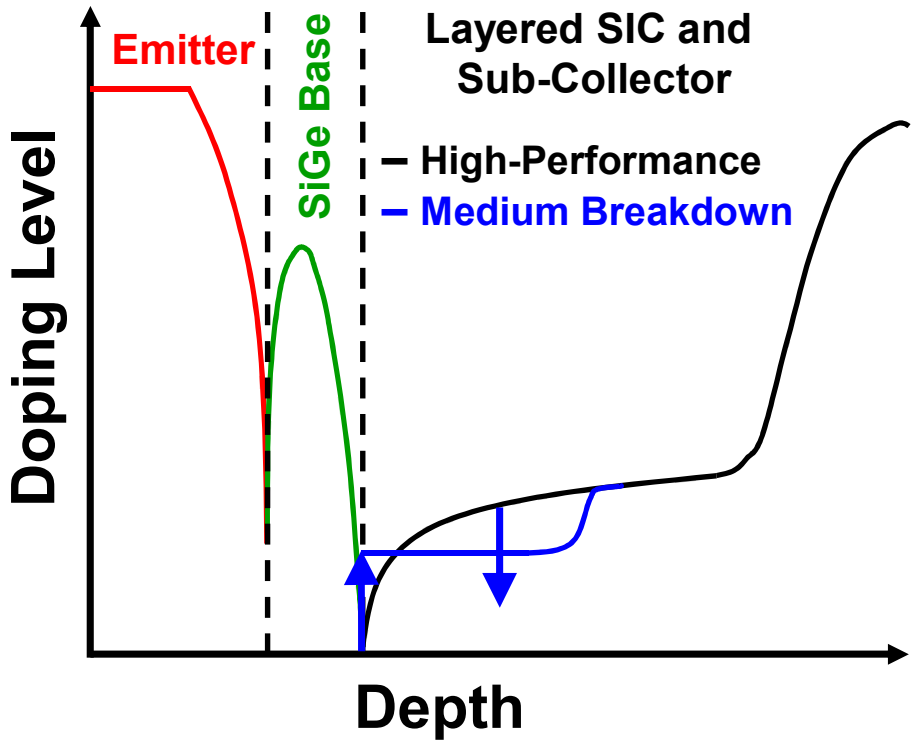

Figure 4.5: Qualitative schematic of the doping profile for a high-performance and medium-breakdown SiGe HBT showcasing the use of a layered SIC.

Although there are several ways to modify the HP device for improved breakdown such as removing the SIC along with increasing the distance from the base of the HBT to the subcollector, a different approach was taken in order to maximize the $f_T \times BV_{CEO}$ product of the MB HBT. This approach involves using a "layered SIC" to push the onset of the Kirk effect while at the same time achieving a high breakdown voltage. In practice, the layered SIC can be constructed by adding a shallow n-type SIC implant in addition to introducing small amounts of p-type doping below this implant as seen in Fig. 4.4(b).

Fundamentally, the internal physics of the layered SIC can be understood by considering the effect of each region separately. The shallow n-type SIC implant is responsible for increasing the electric field near the base region, which in turn pushes the onset of the Kirk effect and increases peak-f_T. Likewise, the addition of the p-

type doping essentially redistributes the electric field from the base to the subcollector. Doing so reduces greatly the impact ionization rate resulting in a greater breakdown voltage. Overall, the effect of the layered SIC on the doping level for each region in the SiGe HBT is shown in Fig. 4.5. For comparison, the doping level of the HP device is also shown in order to highlight the key differences in the collector region (where the layered SIC is located).

It is also important to point out that the concept of the layered SIC follows the same idea of the superjunction, which aims to improve breakdown behavior without having an impact on device speed [39]. More details on the processing of the MB device can be found in [34].

4.3 Mixed-Mode Stress Degradation in Medium-Breakdown SiGe HBTs

The improved breakdown voltage in MB SiGe HBTs implies that for equal voltage conditions, the MB devices will be less susceptible to mixed-mode stress degradation in comparison to the HP device variant. This is due to the fact that the peak electric field in the MB device is not high enough to produce enough hot-carriers and induce damage to the oxide interfaces of the device.

To confirm experimentally this statement, several stress measurements were performed on HP and MB devices for identical stress conditions. The collector-base voltage V_{CB} was set to 2.5 V and the emitter current density $J_{E,Stress}$ was set to 0.1 mA/μm^2, 1 mA/μm^2, and 10 mA/μm^2. The change in base current (ratio of I_B post-stress and I_B pre-stress) was extracted at a collector-current density ($J_{C,extract}$) of 1 $\mu A/\mu m^2$ from the Gummel characteristics and then plotted as a function of stress time in Fig. 4.6. The measured data confirms the statement provided above since the HP device experiences a significant change in I_B, whereas the MB device sees little to no degradation.

In order to observe changes in I_B in the MB device, more stress measurements

were performed at a fixed $J_{E,Stress}$ of 0.5 mA/μm^2 for different values of V_{CB} that are beyond the BV_{CEO} of the device (4 V, 5 V, and 6 V). The measured data is plotted in Fig. 4.7. As expected, increasing V_{CB} produces a higher field in the CB junction, which leads to increased mixed-mode stress degradation. However, past a certain current and voltage condition, the device is likely to experience hard failure as it approaches BV_{CBO}. This is the case for the condition when V_{CB} is set to 6 V and the device is stressed for more than 1,000 seconds.

Based on these results, it can be concluded that the breakdown voltage of the device is a key parameter in determining how severe the effect of mixed-mode stress degradation can be. If the voltage across the device exceeds BV_{CEO}, the device will experience significant damage due to mixed-mode stress degradation because the electric field is high enough to produce hot-carrier damage at the oxide interfaces (EB spacer and shallow-trench isolation).

4.4 High-Current Stress Degradation in Medium-Breakdown SiGe HBTs

Another consequence of using a layered SIC to engineer the collector profile of a SiGe HBT is changing the onset of the Kirk effect to a much lower J_C. This value is often referred to $J_{C,Kirk}$ and it has been shown to be dependent on the collector doping level. It is usually estimated in the literature by the following equation:

$$J_{C,Kirk} \approx q v_s N_{dc} \left[1 + \frac{2\epsilon(V_{CB} + \phi_{bi})}{q N_{dc} W_{epi}^2} \right], \tag{4.1}$$

where v_s is the electron saturation velocity, W_{epi} is the collector epi-layer thickness, ϕ_{bi} is the CB built-in potential, and N_{dc} is the collector doping [2].

Intuitively, this equation is relevant because it implies that in order to provide additional immunity to Kirk effect, it is necessary to increase the collector doping. This also explains why it is necessary to bias the HP device at higher current densities

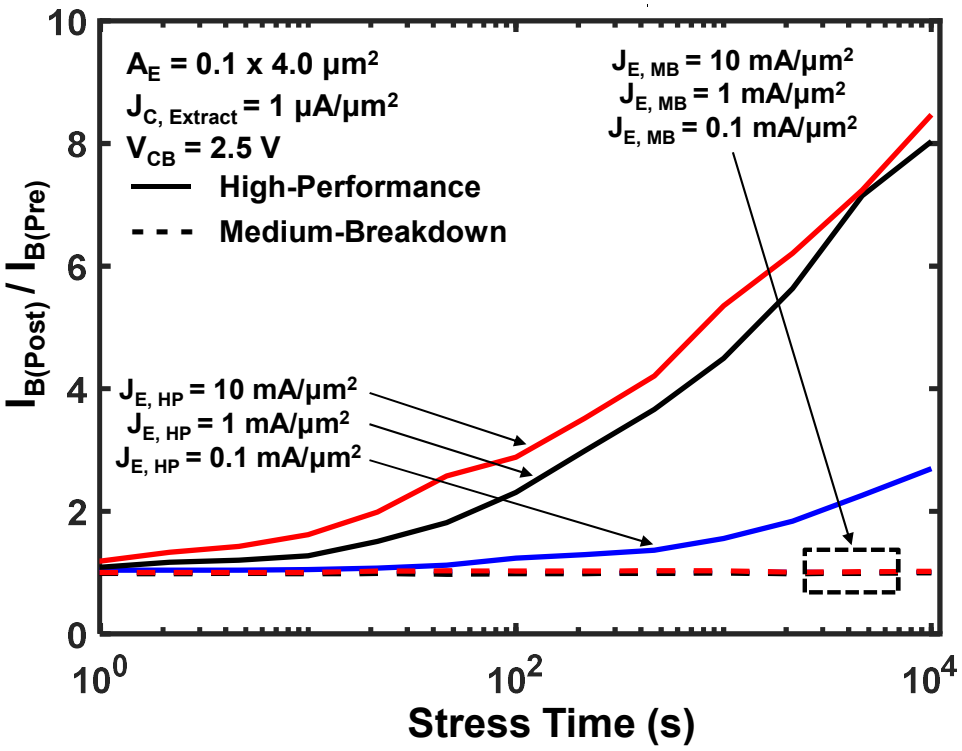

Figure 4.6: Measured forward mode mixed-mode stress degradation in HP and MB SiGe HBTs with Area = $0.1 \times 4.0\ \mu m^2$ following electrical stress with $V_{CB} = 2.5$ V and $J_{E,Stress} = 0.1\ mA/\mu m^2$, $1\ mA/\mu m^2$, and $10\ mA/\mu m^2$. Extracted from Gummel characteristics at $J_C = 1\ \mu A/\mu m^2$.

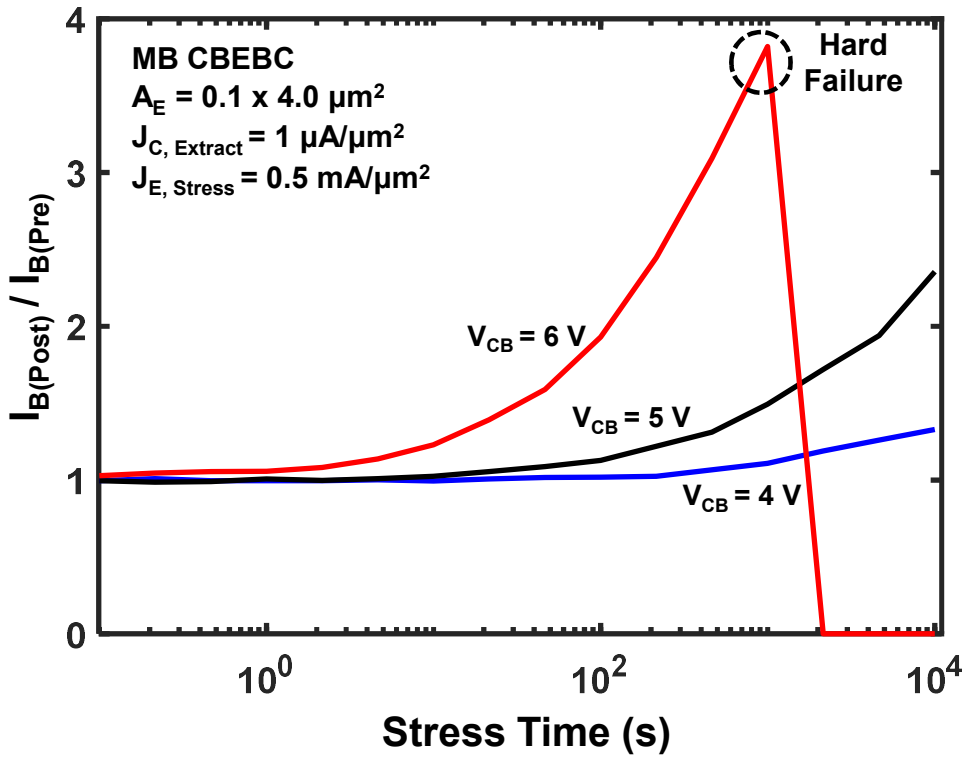

Figure 4.7: Measured forward mode mixed-mode stress degradation in MB SiGe HBTs with Area = 0.1×4.0 μm^2 following electrical stress with $J_{E,Stress} = 0.1$ $mA/\mu m^2$ and V_{CB} = 4 V, 5 V, and 6V. Extracted from Gummel characteristics at $J_C = 1$ $\mu A/\mu m^2$.

to extract maximum device performance. As a reminder, J_C at peak-f_T for the HP device happens at approximately 20 mA/μm^2 and at 5 mA/μm^2 for the MB device. This value will also dictate the current density at which high-current stress degradation will become pronounced. As a rule of thumb, devices with lower J_C at peak-f_T will be more vulnerable to high-current stress degradation at reduced current densities [17].

Just like the previous section, an experimental comparison of high-current stress degradation was done for both HP and MB devices for identical stress conditions. A similar approach was taken to measure changes in base current over time. To isolate the effects of high-current damage, the stress voltages were kept minimal (V_{CE} ¡ BV_{CEO}) and the devices were biased beyond the J_C at peak-f_T point. The change in base current was extracted from the Gummel characteristics at $J_{C,extract}$ of 1 $\mu A/\mu m^2$ and plotted for three different stress conditions in Fig. 4.8. From the measured data, it can be inferred that past the J_C at peak-f_T, hot-carrier damage due to Auger generation/recombination starts to become an issue. Since the MB device has a lower J_C at peak-f_T, Kirk effect will happen at lower current densities in comparison to the HP device and the effective Auger rate for identical stress conditions will be much higher. As a result, the MB device will see more high-current damage, which can be seen from the measurement results in Fig. 4.8.

Even though the MB device is more vulnerable to high-current damage due to having a much lower J_C at peak-f_T, there are several performance benefits that should be taken into account when designing integrated circuits. These benefits include having reduced power consumption, shot noise, and thermal dissipation from operating at lower current densities. Additionally, a larger bandwidth matching will be obtained as a consequence of having reduced parasitics [40].

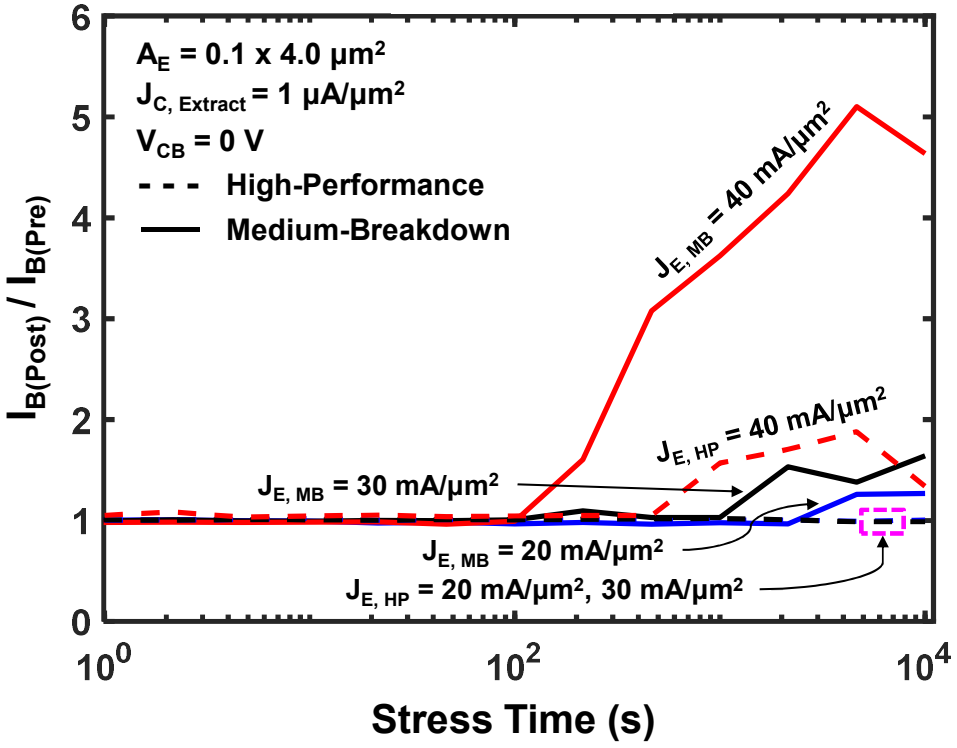

Figure 4.8: Measured forward mode high-current stress degradation in HP and MB SiGe HBTs with Area = $0.1 \times 4.0\ \mu m^2$ following electrical stress with $V_{CB} = 0$ V and $J_{E,Stress} = 20\ mA/\mu m^2$, $30\ mA/\mu m^2$, and $40\ mA/\mu m^2$. Extracted from Gummel characteristics at $J_C = 1\ \mu A/\mu m^2$.

4.5 Summary

An overview of the soft failure mechanisms of MB SiGe HBTs was presented to show potential reliability issues under mixed-mode and high-current stress conditions. The MB device was explored in detail from a processing perspective in order to understand any subtle differences between the HP and MB devices, which ultimately dictate the underlying physics of failure of the device. Under MM stress degradation, the MB SiGe HBT was shown to be more robust for identical bias conditions when compared to the HP SiGe HBT. This is due to the fact that the breakdown voltages for the MB device are much higher and the electric field is not strong enough to produce hot-carrier damage at the oxide interfaces. A similar comparison was done for HC stress degradation and it was shown that HP devices have an advantage over MB devices when operating at identical current densities. This is attributed to the onset of the Kirk effect, which happens at reduced current densities for the MB device. As a result, the Auger recombination rate for identical bias conditions is much higher for the MB devices. Ultimately, this will translate to higher degradation in comparison to the HP device [25].

There are many performance and reliability trade-offs that should be taken into account when using either HP or MB device variants. The circuit application will dictate whether or not there is an advantage of using a hybrid of these two devices. In order to provide a greater understanding of the physics of failure for either variant, TCAD simulations are needed. A further study related to this topic is currently under investigation and will be explored as an extension to this work. In the end, having such knowledge is desired in order to build a comprehensive predictive aging model such as the one shown in [25].

CHAPTER 5
CONCLUSION

5.1 Contributions

The results presented in Chapter 3 on hard failure mechanisms in a fourth-generation SiGe BiCMOS technology show the underlying physics when a SiGe HBT is operated outside of traditionally defined SOAs. A new failure metric was proposed to quantify the maximum usable range of a SiGe HBT before undergoing hard failure. Through extensive measurement results, two modes of hard failure were shown. In addition, hard failures were explored as a function of geometry, layout configuration, and temperature. Knowing the exact location of these hard failure limits is desirable in order to develop a physics-based model to predict the maximum usable range in SiGe HBTs within a circuit design environment. The results in this chapter have been published and presented at the 2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting. An extension of this work is currently in preparation and will be submitted for publication in IEEE Transaction on Electron Devices.

Chapter 4 introduced the use of high-breakdown SiGe HBTs for applications in RF integrated circuits. An MB variant in a fourth-generation SiGe BiCMOS platform was chosen for this study to provide an overview of the soft failure mechanisms between the MB variant and its HP counterpart. To understand the physics of failure in the MB device, important details from a processing standpoint were briefly discussed that affect the device performance. Lastly, reliability and performance trade-offs were discussed from a circuit designers perspective to identify possible advantages of using a hybrid of both HP and MB SiGe HBTs. The analysis presented in Chapter 4 will be submitted for publication to the 2019 IEEE BiCMOS and Compound Semiconductor

Integrated Circuits and Technology Symposium.

5.2 Future Work

5.2.1 Modeling Hard Failures in SiGe HBTs

In order to provide additional understanding to the hard SOA boundaries, it is necessary to measure hard failures by fixing J_E and sweeping V_{CB} until the device reaches the hard failure point and is no longer usable. The measurement method used in Chapter 3 is more relevant to understand the current handling capability of a SiGe HBT. However, the voltage handling capability at different current densities is of particular interest for many circuit applications. TCAD simulations can also be used to comprehend the device behavior before it reaches the hard failure point.

Once all of the failure mechanisms are understood and the exact location of hard failures are found, a physics-based model can be implemented within a circuit design environment which will serve as a red flag warning mechanism to identify the maximum usable range of a SiGe HBT. In addition, a similar study on hard failures can be done in high-breakdown devices to have a better understanding of the current and voltage handling capabilities of either device variants.

5.2.2 TCAD Modeling of Soft Failure Mechanisms in Medium-Breakdown SiGe HBTs

A well-calibrated 2-D device profile of the MB SiGe HBT in the Synopsys Sentaurus TCAD suite is needed to investigate the underlying physics when operating a SiGe HBT under high-current and mixed-mode stress conditions. There are several parameters that can be extracted from simulation results such as the peak-electric field, effective Auger rate, and lattice temperature. Such parameters can be compared side by side for both the HP and MB devices in order to understand in greater detail the differences in damage shown in the measured soft failure data.

Just like the framework provided in [25], a similar approach can be taken to model the aging of MB SiGe HBTs. This will be beneficial for circuit designers since they will be able to predict with accuracy the end-of-life characteristics of RF and mm-Wave circuits that make use of MB devices.

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