

# **A Comprehensive Study of Safe-Operating-Area, Biasing Constraints, and Breakdown in Advanced SiGe HBTs**

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# **A Comprehensive Study of Safe-Operating-Area, Biasing Constraints, and Breakdown in Advanced SiGe HBTs**

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# SUMMARY

This thesis presents a comprehensive assessment of breakdown and operational voltage constraints in state-of-the-art silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS technology. Technology scaling of SiGe HBTs for high frequency performance results on lower breakdown voltages, making operating voltage constraints an increasingly vital consideration in SiGe HBTs. In Chapter I, important technology aspects and the device physics of state-of-the-art SiGe HBT BiCMOS are discussed, and a brief overview of breakdown mechanisms is presented.

In Chapter II, operating voltage constraints are experimentally characterized as a function of technology generation, device geometry, and operating condition, to provide practical guidelines for stable device operation, and show the influence of technology scaling on breakdown voltage constraints and safe-operating-area (SOA).

Chapter III experimentally investigates the practical implications associated with of operating voltage constraints at the device and circuit level, addressing compact modeling issues, small signal instabilities, mixed-mode reliability, self-heating, and thermal coupling issues.

# CHAPTER I

## INTRODUCTION

### ***1.1 Motivation***

Next-generation communications systems will place increasingly stringent demands upon the supporting technologies. Market and industry expectations call for emerging wireless communications infrastructure to support data and multimedia alongside voice, providing high value content to wireless communications, thereby requiring extremely high data rates. Additionally, the transmission of this content should be of high quality, with interruption-free data transfer and mobile voice indistinguishable from wireline voice. Also, these systems will be required to operate at higher frequencies (well into the GHz range) as regulators allocate these higher frequency ranges for wireless communications in order to provide bandwidth for additional subscribers and content [1]. Finally, perhaps representing the most crucial component to the success of emerging wireless communications systems, customers expect mobile handsets to decrease in size, increase in functionality, sustain longer battery life, and remain affordable.

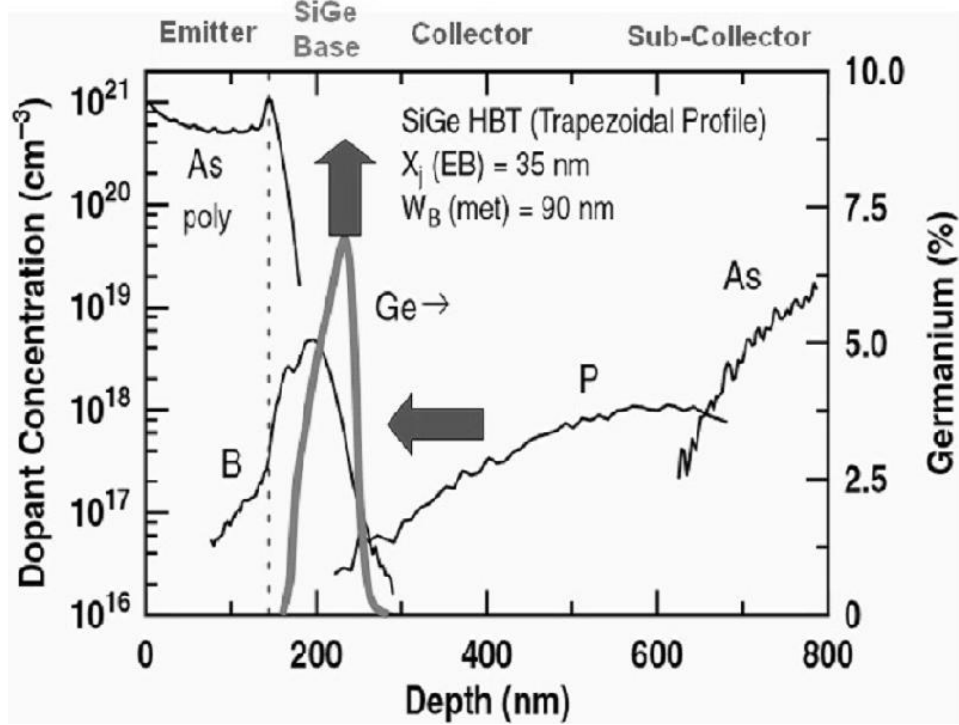
Silicon-Germanium (SiGe) Heterostructure Bipolar Transistor (HBT) BiCMOS technology can address all of these concerns, and has established itself as strong technology contender for a host of circuit applications including analog, mixed signal, RF and millimeter wave. The peak unity gain frequency ( $f_T$ ) of state-of-the-art SiGe HBTs far exceeds that of standard Si BJTs and rivals the best of III-V technologies. The compatibility of SiGe with Si permits higher yield and superior levels of system complexity and integration, leveraging the benefits of best-of-breed Si CMOS to offer powerful "mixed-signal" solutions. With the ability fabricate high performance analog circuits alongside powerful CMOS logic on a single silicon wafer, SiGe HBT BiCMOS technology enables powerful



"system-on-a-chip" (SoC) architectures that facilitate reduced chip count, reduced power consumption, reduced packing complexity, and overall reduced cost [2].

However, achieving higher performance (in terms of peak  $f_T$ ) in SiGe HBTs inherently requires a tradeoff in transistor breakdown voltage, raising important considerations for circuit designers. The ever-decreasing operating voltage limits of scaled SiGe HBTs often pose non-obvious constraints on the biasing and operation of SiGe HBTs used in mixed-signal circuits [3], [4]. The understanding, for instance, of how much "usable" voltage actually exists in the region between the open-base breakdown voltage ( $BV_{CEO}$ ) and the open-emitter breakdown voltage ( $BV_{CBO}$ ) remains to be sufficiently addressed, particularly when considering the complex interactions between impact-ionization, self-heating, and avalanche-induced, current-crowding instabilities (often referred to as "pinch-in" effects), and their corresponding dependence on current density. In addition, important issues concerning the practical, circuit-level implications of operating a device up to and even beyond its conventionally-defined operating voltage constraints (the so-called "safe-operating-area" (SOA)) remain unclear. Moreover, standard industry compact models (e.g., VBIC, HICUM, MEXTRAM) often fail to accurately capture important features such as breakdown instabilities, and robust 2-D simulation of such effects remains particularly difficult [4].

This thesis presents a comprehensive assessment of breakdown and operational voltage constraints in state-of-the-art SiGe HBTs, experimentally examining these characteristics as functions of technology generation, device geometry, bias configuration, and operating point. New definitions for breakdown voltage, adopted from standard measurements, are developed and utilized. Practical design implications and physical origins of breakdown are explored using 2-D simulations and quasi-3D compact models. Device and circuit level reliability implications of breakdown effects operating voltage constraints in SiGe HBTs will be emphasized. Some of these results were presented at the 2005 *IEEE International Reliability Physics Symposium* [5], and others submitted to the 2005 *IEEE Bipolar/BiCMOS*

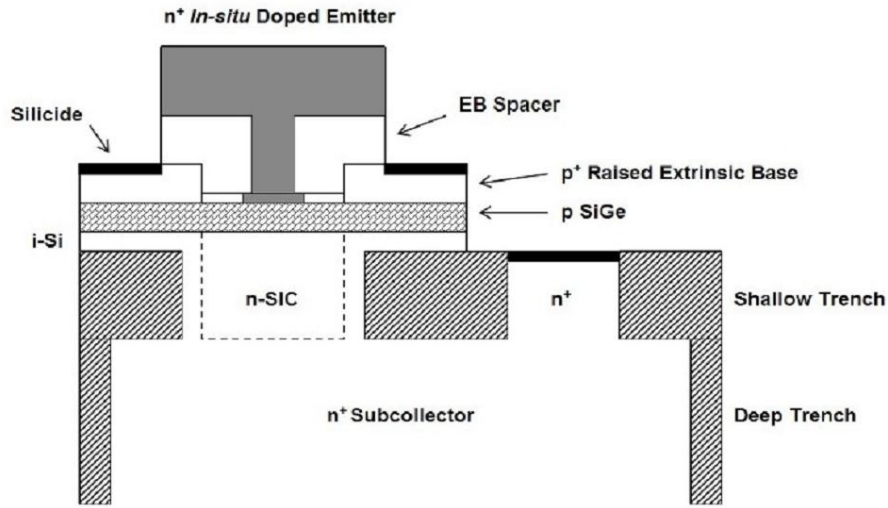


**Figure 1:** Vertical SIMS profile showing doping concentration and Ge profile within a first generation SiGe HBT.

*Circuits and Technology Meeting [6].*

## 1.2 SiGe HBT BiCMOS Technology

Several generations of SiGe HBT BiCMOS technology exist in commercial production worldwide, and are deployed in a wide variety of applications including cellular handsets, wireless LAN, satellite communications, radar systems, and beyond. The key difference between SiGe HBTs and standard Si BJTs is the inclusion of the compositionally graded SiGe alloy within the boron doped epitaxial layer of the active base region of the transistor. This feature, depicted in the SIMS doping and Ge profile of a first generation SiGe HBT shown in Figure 1, facilitates bandgap engineering for optimized device performance while maintaining process compatibility with standard Si CMOS. The Ge layer is typically grown using ultra-high vacuum/chemical vapor deposition (UHV/CVD), allowing for a lower thermal cycle and excellent process control during deposition. This extra process



**Figure 2:** A schematic device cross-section of a third generation BiCMOS SiGe HBT.

step can be added in modular fashion to standard Si CMOS processes with relatively little impact on HBT performance, CMOS characteristics, fabrication yield, and overall throughput [2].

The vertical self-alignment scheme, shown in Figure 2 for a third generation SiGe HBT, is typically employed in SiGe HBT fabrication due to several advantages, including reduced parasitics and thin base region. These factors result in reduced carrier transit time, and thus higher device performance. The low thermal budget of UHV/CVD is necessary to maintain the thinness of the base region due to the diffusive nature of boron in Si. Small amounts of carbon doping may also be included in the active base region to suppress boron out-diffusion and maintain a narrow base profile and enhance device performance [2]. Shallow and deep trench isolation is incorporated, as shown in Figure 2. Selectively implanted collector (SIC) doping allows devices with different breakdown voltages to be fabricated side by side in a given SiGe HBT technology. Typically, devices come in at least two flavors: "high performance" with high collector doping and low breakdown voltage, and "high breakdown" with reduced collector doping and higher breakdown voltage.

**Table 1:** Characteristic device parameters for three SiGe BiCMOS technology generations.

SiGe BiCMOS Technology SiGe HBT Parameters	IBM 5HP	IBM 7HP	IBM 8HP
Drawn Emitter Width ( $\mu\text{m}$ )	0.5	0.2	0.12
peak $\beta$	100	200	400
$V_A$ (V)	65	120	> 150
$BV_{CEO}$ (V)	3.3	2.5	1.7
$BV_{CBO}$ (V)	10.5	7.5	5.5
Peak $f_T$ (GHz)	48	120	207
Peak $f_{max}$ (GHz)	69	100	285
min. $NF_{min}$ (dB)	0.8	0.4	< 0.3

Trans-generational SiGe HBT performance enhancements may be achieved through lateral and vertical scaling and Ge profile optimizations. The SiGe HBT BiCMOS technology generations examined in this thesis are referred to as SiGe 5HP, SiGe 7HP, and SiGe 8HP, and are in commercial production at IBM. Important HBT technology and performance characteristics are summarized in Table 1. At times, these technologies may be referred to by their approximate peak  $f_T$  performance: 50 GHz, 120 GHz, and 200 GHz, respectively.

As mentioned previously, compatibility with state-of-the-art Si CMOS technology is a major feature of the SiGe HBT. For the SiGe 5HP BiCMOS technology, the respective CMOS has an effective length of  $0.35 \mu\text{m}$  with  $3.3\text{V } V_{DD}$  [7]. The SiGe 7HP BiCMOS technology incorporates  $0.18 \mu\text{m}$  ( $1.8\text{V } V_{DD}$ ) and  $0.3 \mu\text{m}$  ( $3.3\text{V } V_{DD}$ ) Si CMOS devices [8]. Two types of  $130 \text{ nm}$  Si CMOS devices are available in the SiGe 8HP BiCMOS technology, with minimum channel lengths of  $0.12 \mu\text{m}$  ( $1.2\text{V } V_{DD}$ ) and  $0.24 \mu\text{m}$  ( $2.5\text{V } V_{DD}$ ).

### 1.3 Device Physics of SiGe HBTs

Simply stated, SiGe HBT technology enables bandgap engineering in a Si system to obtain impressive performance metrics in terms of high speed, high current gain, high linearity, and low noise. A well-engineered Ge profile in the base region of the transistor can effectively decouple key device parameters that otherwise lead to critical performance tradeoffs

in standard Si BJT devices.

From a physical perspective, the crystalline lattice constants differ between Si and Ge, and as a result, a SiGe alloy naturally has a slightly larger lattice constant than does Si. This lattice mismatch results in compressive straining on the SiGe layer grown pseudomorphically on Si. For a given Ge content, therefore, the SiGe film must be thinner than a certain critical value to retain thermodynamic stability and avoid relaxation defects. The compressive strain in the SiGe film also has important features in carrier mobility enhancement, and aids in transport properties of the device. The bandgap of Ge (0.66 eV at 300K) is considerably smaller than that of Si (1.12 eV at 300K). As a result, the bandgap in a SiGe alloy is effectively tunable through respective Si and Ge content (approx. -7.5 meV per 1% Ge), insofar as thermodynamic stability allows.

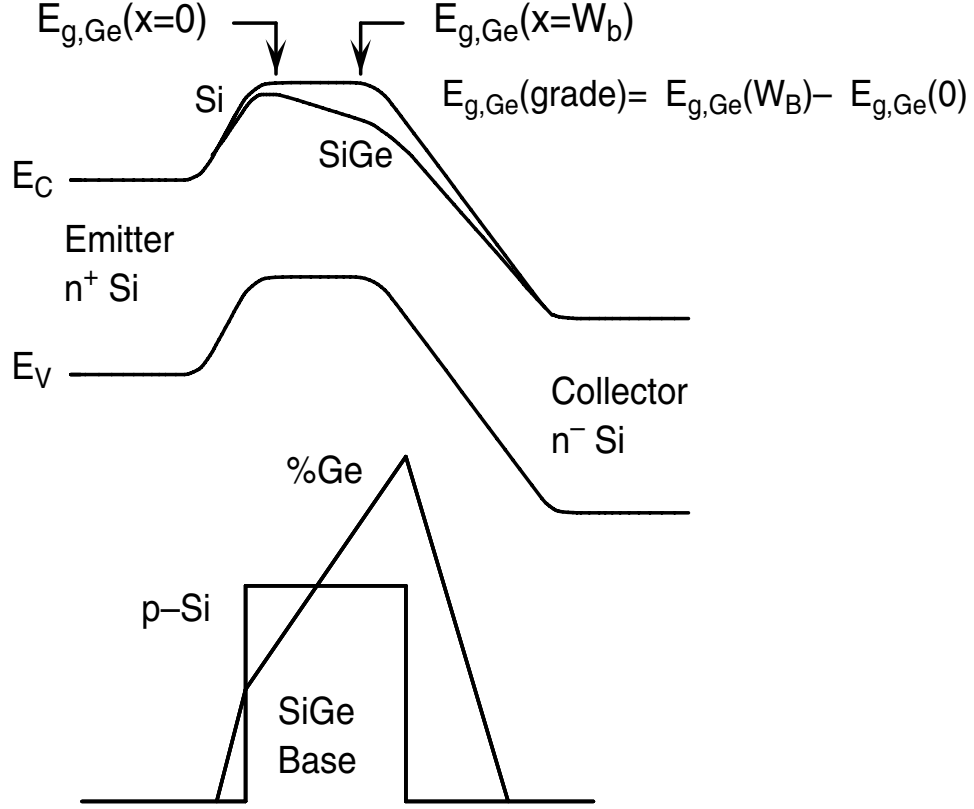
The energy band diagram for a standard Si BJT and a comparable SiGe HBT, biased in forward active mode, is shown in Figure 3. The effect of the graded Ge content in the base region is apparent in the offset between the respective conduction bands. As a result, the potential barrier for minority carrier injection into the base region is reduced for a given  $V_{BE}$ , resulting in increased collector current density ( $J_C$ ) and thus increased gain for the SiGe device. This result can be physically expressed using the generalized Moll-Ross relation for collector current density [9],

$$J_C = \frac{q(e^{qV_{BE}/kT}-1)}{\int_0^{W_b} \frac{p_b(x)dx}{D_{nb}(x)n_{ib}^2(x)}} \quad (1)$$

and an equation relating the Ge-induced offset of the bandgap to the intrinsic carrier concentration as a function of position:

$$n_{ib}^2 = \gamma n_{io}^2 e^{\Delta E_{gb}^{app}/kT} e^{[\Delta E_{g,Ge}(grade)]x/(W_b kT)} e^{\Delta E_{g,Ge}(0)/kT} \quad (2)$$

where  $\Delta E_{gb}^{app}/kT$  is the apparent bandgap narrowing resulting from heavy doping in the base. The low-doping intrinsic carrier density for Si is  $n_{io}^2 = N_C N_V e^{-E_{go}/kT}$  and  $\gamma = (N_C N_V)_{SiGe}/(N_C N_V)_{Si} < 1$  is the effective density-of-states ratio between SiGe and



**Figure 3:** Energy band diagram for a graded base SiGe HBT and a Si BJT.

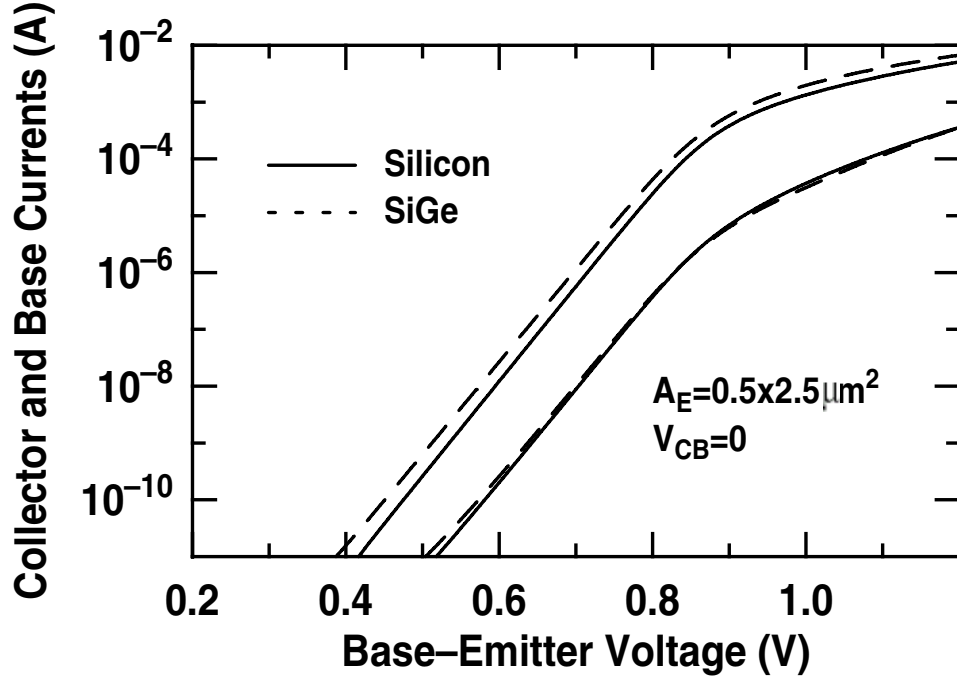
Si [10]. Combining Equations (1) and (2), and assuming a linearly graded Ge profile ( $\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0)$ ) results in an overall expression for collector current density ( $J_C$ ) in a SiGe HBT [11],[12]:

$$J_{C,SiGe} = \frac{qD_{nb}}{N_{ab}^- W_b} (e^{qV_{BE}/kT} - 1) n_{io}^2 e^{\Delta E_{gb}^{app}/kT} \left\{ \frac{\tilde{\gamma}\tilde{\eta} e^{\Delta E_{g,Ge}(0)/kT} \Delta E_{g,Ge}(grade)/kT}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\} \quad (3)$$

where the symbol “ $\sim$ ” denotes a position-averaged quantity,  $N_{ab}^-$  is the ionized doping level in the base, and  $\tilde{\eta} = \left( \overline{D_{nb}} \right)_{SiGe} / (D_{nb})_{Si} > 1$  is the minority electron diffusivity ratio between SiGe and Si. The influence of the Ge-induced energy band offset on collector current density is contained entirely in the second term of this relation, and thus can be described as the SiGe current gain enhancement factor:

$$\frac{\beta_{SiGe}}{\beta_{Si}} \cong \frac{J_{C,SiGe}}{J_{C,Si}} = \frac{\tilde{\gamma}\tilde{\eta} \Delta E_{g,Ge}(grade)/kT e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \quad (4)$$

The SiGe current gain enhancement factor demonstrates that Ge-induced energy band



**Figure 4:** Representative Gummel plot for a SiGe HBT as compared to a Si BJT.

offset at the EB junction ( $\Delta E_{g,Ge}(0)$ ) exerts an exponential influence on the gain increase of the device. This enhancement is depicted in Figure 4, which compares the Gummel characteristics for a typical SiGe HBT and a similarly constructed Si BJT. The SiGe HBT clearly exhibits higher collector current with approximately the same base current as the Si BJT, and hence, increased current gain.

In the case of "strong Ge grading" ( $\Delta E_{g,Ge}(grade) \gg kT$ ), characteristic of a triangular Ge profile, the exponential term on the denominator becomes very small and this factor approximately reduces to  $\approx (\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/kT)e^{\Delta E_{g,Ge}(0)/kT}$ . In the case of "weak Ge grading" ( $\Delta E_{g,Ge}(grade) \ll kT$ ), characteristic of a box Ge profile, the SiGe current gain enhancement factor is shown to be approximately  $\tilde{\gamma}\tilde{\eta}e^{\Delta E_{g,Ge}(0)/kT}$ .

In addition to current gain ( $\beta$ ), the output conductance ( $\partial I_C / \partial V_{CE}$  at fixed  $V_{BE}$ ) of a transistor is a key consideration in analog design. This factor is equivalently described using the output resistance  $r_o$ , with output conductance equal to  $1/r_o$ . The ideal transistor

possesses infinite output resistance, and thus zero output conductance. However, it is well known that actual transistors possess finite values of  $r_o$  due to what is referred to as the "Early Effect". Increasing  $V_{CB}$  causes backside depletion on the neutral base. This reduces the effective width of the active base region, which increases the minority carrier (electron) concentration gradient across the base and thus increases the collector current. This behavior is commonly characterized using an experimental parameter known as the Early voltage ( $V_A$ ):

$$V_A = J_C(0) \left\{ \left. \frac{\partial J_C}{\partial V_{CB}} \right|_{V_{BE}} \right\}^{-1} - V_{BE} \approx \left\{ \left. \frac{\partial J_C}{\partial W_b} \right|_{V_{BE}} \frac{\partial W_b}{\partial V_{CB}} \right\}^{-1} \quad (5)$$

The  $V_A$  enhancement ratio between a comparable SiGe HBT and Si BJT is given by

$$\left. \frac{V_{A,SiGe}}{V_{A,Si}} \right|_{V_{BE}} = e^{\Delta E_{g,Ge}(grade)/kT} \left[ \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right] \quad (6)$$

This relation shows the exponential influence of the Ge-induced bandgap grading on Early voltage. Thus, the Ge profile in a SiGe HBT provides separate "levers" for optimizing  $\beta$  and  $V_A$  ( $\Delta E_{g,Ge}(0)$  and  $\Delta E_{g,Ge}(Grade)$ , respectively). In standard Si BJTs, enhancement of one of these two factors fundamentally requires degradation of the other since they both are related to the base doping. But with the effective decoupling of  $\beta$  and  $V_A$  from base doping (and, thus, each other) in a well constructed Ge profile, this tradeoff is sidestepped and the overall  $\beta \cdot V_A$  product, an important device parameter in analog circuits, of a SiGe HBT is substantially higher than that of a similar Si BJT.

SiGe HBTs also show substantial improvement in *ac* performance over conventional Si BJTs, allowing SiGe HBTs to achieve frequency response characteristics suitable for even high frequency RF and microwave applications. The base transit time comprises a significant portion of the total transport delay time for carriers in bipolar devices, and thus can be a limiting factor in overall *ac* performance. Ge grading induces a drift field in neutral base that accelerates minority carriers and reduces the base transit time ( $\tau_b$ ), given by

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} [1 - e^{-\Delta E_{g,Ge}(grade)/kT}] \right\} \quad (7)$$



Additionally, since the emitter charge storage delay time ( $\tau_e$ ) is proportional to  $1/\beta$ , the higher  $\beta$  of a SiGe HBT will reduce this factor according to

$$\frac{\tau_{e,SiGe}}{\tau_{e,Si}} \simeq \frac{J_{C,Si}}{J_{C,SiGe}} = \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\tilde{\gamma}\tilde{\eta}^{\frac{\Delta E_{g,Ge}(grade)}{kT}} e^{\Delta E_{g,Ge}(0)/kT}} \quad (8)$$

and thus improve the total transit time.

A standard figure-of-merit for dynamic transistor performance is the unity-gain cutoff frequency ( $f_T$ ). For low-injection, this parameter can be written as

$$f_T = \frac{1}{2\pi} \left[ \frac{1}{g_m} (C_{eb} + C_{cb}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{cb} \right]^{-1} \quad (9)$$

As stated above and shown explicitly here in Equation (9), reduction of  $\tau_b$  and  $\tau_e$  will result in reduced overall transit time ( $\tau_{ec}$ ) and thus increase  $f_T$ . Likewise, the unity power-gain frequency (or, maximum oscillation frequency,  $f_{max}$ ) will also improve since it is a function of  $f_T$ , given by

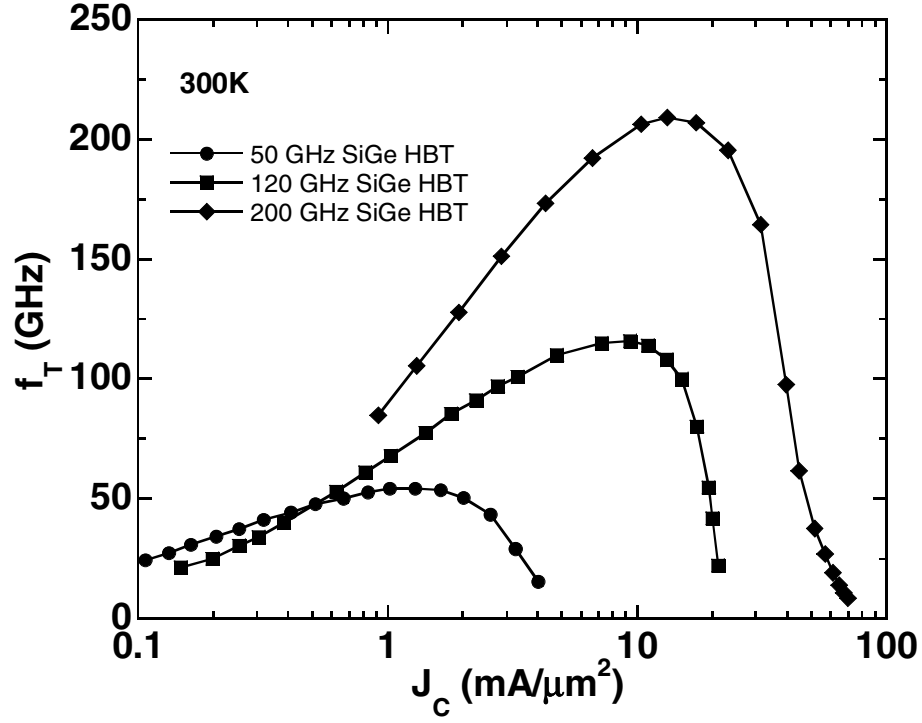
$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} r_b}} \quad (10)$$

Thus, the Ge grading in the base region of the SiGe significantly improves both  $f_T$  and  $f_{max}$ , and thus overall *ac* performance.

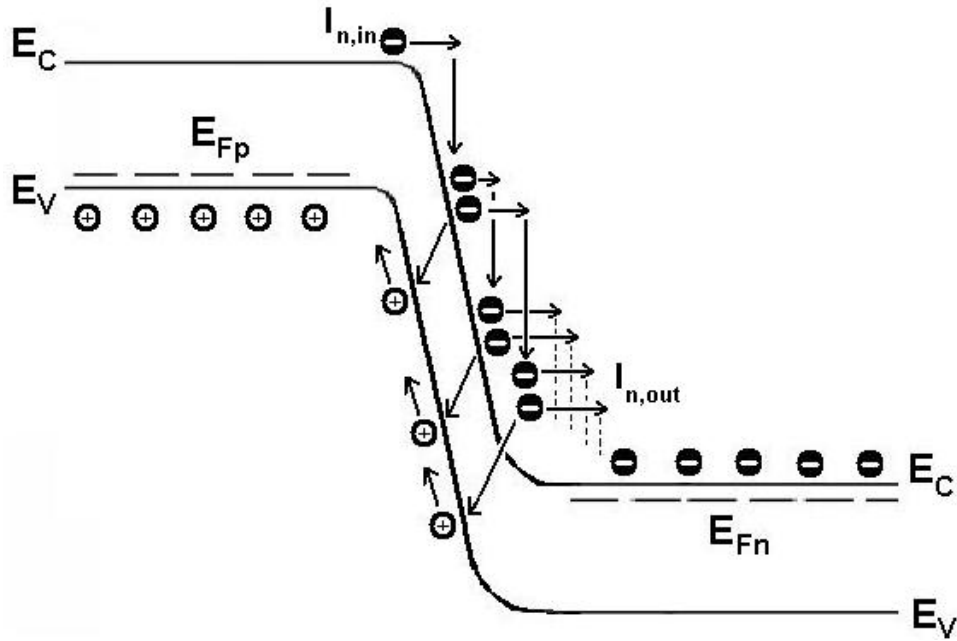
## 1.4 Breakdown Fundamentals

As demonstrated in Equation (9), with reduction in  $\tau_b$  and  $\tau_e$ , the time delay imposed by the parasitic capacitances within the device becomes more significant. To counter this limiting factor to performance enhancement, an increase in collector current density ( $J_C$ ) is required to decrease the charging times of the parasitic capacitances ( $C_{eb}$  and  $C_{cb}$ ). Therefore, increased  $J_C$  is a common characteristic associated with technology scaling and  $f_T$  optimization in SiGe HBTs, as shown in Figure 5.

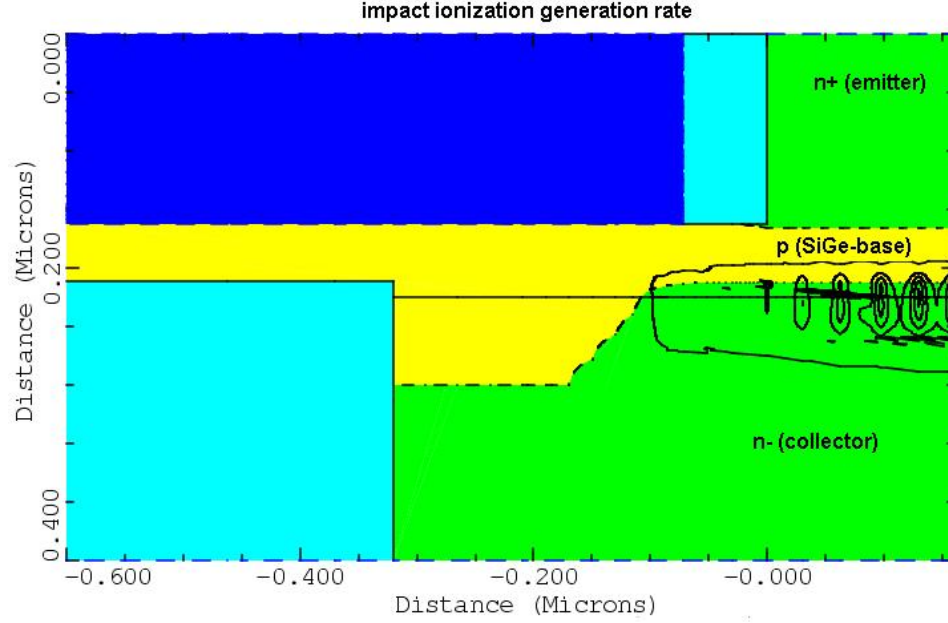
At high  $J_C$ , carriers in the collector-base space charge region (CB-SCR) will compensate the local ionized charge, leading to a collapse of the electric field in this region. As a result, the base region will "push-out" into the CB-SCR (the Kirk effect), decreasing the



**Figure 5:** Cutoff frequency as a function of collector current density for three generations of SiGe HBT BiCMOS technology.



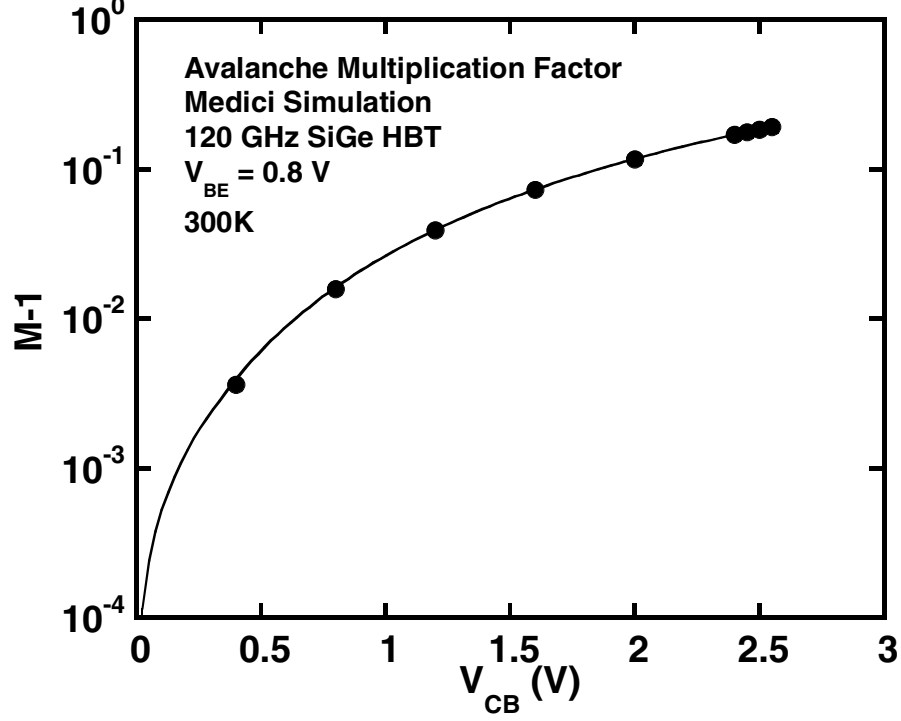
**Figure 6:** Schematic illustration of the avalanche multiplication process in a reversed bias p-n junction.



**Figure 7:** MEDICI device simulation of a 120 GHz SiGe HBT showing contours of impact ionization generation rate with respect to the device profile.

current gain and degrading the performance of the transistor. Therefore, in order to operate at high  $J_C$ , higher collector doping is required to suppress the Kirk effect. Increasing the collector doping will increase the magnitude of the drift field within the CB-SCR, causing conduction electrons in this region to obtain high kinetic energy. In the event that an electron of sufficient velocity collides with the lattice, excess energy may be transferred to an electron in the valence band, promoting this carrier to the conduction band and creating an electron-hole pair (EHP). This generation process is the inverse of the Auger effect, and is known as impact ionization [13]. As an electron generated during an impact ionization event is accelerated due to the drift field, it too may undergo a lattice collision and generate an additional EHP, and so on, as illustrated in Figure 6. This "snowballing" phenomenon of impact-ionized carriers is referred to as avalanche multiplication. Figure 7 shows the location of impact ionization centers as determined by a two dimensional device simulation in MEDICI for a 120 GHz SiGe HBT at  $I_E = 500 \mu\text{A}$  and  $V_{CB} = 4 \text{ V}$ .

As the reverse bias potential across the junction ( $V_{CB}$  in a bipolar transistor) increases, the probability that each carrier in the depletion region will undergo an impact ionization



**Figure 8:** MEDICI device simulation of a 120 GHz SiGe HBT showing  $M - 1$  as a function of collector voltage.

event increases, eventually leading to junction breakdown. This probability is typically represented as the avalanche multiplication factor ( $M$ ), which is the ratio of reverse-biased junction current without impact ionization to the junction current with impact ionization, or

$$M = I_{n,out} / I_{n,in} \quad (11)$$

for  $I_{n,in}$  being the electron current entering the CB-SCR and  $I_{n,out}$  being the electron current exiting the CB-SCR. The avalanche multiplication factor can be extracted from standard measurements ([14]) and is commonly plotted as  $(\log) M - 1$  verses (linear) collector-base voltage ( $V_{CB}$ ), as shown in Figure 8 taken from a MEDICI simulation of a 120 GHz SiGe device. The holes generated during the avalanche multiplication process flow into the neutral base region and out of the base terminal, causing the total current at the terminal  $I_B$  to be reduced according to

$$I_B = I_{p,e} - (M - 1)I_{n,in} \quad (12)$$

for which neutral base recombination (NBR) is neglected and  $I_{p,e}$  defined as the base current due to holes injected into the emitter. As  $M - 1$  increases with  $V_{CB}$ , the second term, which represents the avalanche current, eventually becomes equal to  $I_{p,e}$ , at which point  $I_B = 0$ . This condition results when the product  $\beta(M - 1) = 1$ , which is equivalent to the condition of open-base breakdown  $BV_{CEO}$  [15] [16], a standard breakdown Figure of merit given in Table 1 for the 50, 120, and 200 GHz SiGe HBT technologies. If  $V_{CB}$  is allowed to increase further, the sign of  $I_B$  becomes negative and holes generated by avalanche multiplication flow out of the base terminal. This situation is known as base current reversal, and is an important factor in breakdown related transistor instabilities at high  $V_{CB}$ , as shall be discussed further in Chapter II [17] [18] [19]. If  $V_{CB}$  continues to increase, the CB junction will eventually undergo full reverse biased junction breakdown at the open-emitter breakdown voltage  $BV_{CBO}$ . Thus,  $BV_{CBO}$ , as given in Table 1 for the 50, 120, and 200 GHz SiGe HBT technologies, represents the absolute maximum collector voltage of a transistor.

For simplicity, in many cases  $M - 1$  for a given  $V_{CB}$  is treated as a constant with respect to current density,  $J_C$ , and for low injection this approximation is usually acceptable. However, it is well known that at high injection  $M - 1$  shows a stronger dependence on  $J_C$ , due to high carrier charge concentration reducing the effective doping, and thus the effective electric field, within the CB-SCR [2]. Also,  $M - 1$  possess a negative temperature coefficient due to changes in carrier mean free path and phonon scattering, which absorbs energy during carrier-lattice collisions and reduces the probability of EHP creation [20]. As a result, we expect and observe breakdown effects to be aggravated for low temperature (cryogenic) operating conditions.

Overall, increasing the collector doping, as required to achieve higher device performance in SiGe HBTs, increases the rate of avalanche multiplication within the device and thus reduces its breakdown voltage. This is reflected in Table 1, which shows the open-emitter reverse bias collector junction breakdown voltage ( $BV_{CBO}$ ) to decrease from 10.5 V to 5.5 V over the three technology generations as peak  $f_T$  increases from 50 GHz to 200

GHz. Thus, an inherent (and well known) tradeoff exists between peak  $f_T$  and breakdown voltage in SiGe HBT device design. This fundamental limit is more accurately described by the (larger)  $BV_{CES} \cdot f_T$  product ( $BV_{CES} \approx BV_{CBO}$ ) than the traditional  $BV_{CEO} \cdot f_T$  product [21], but clearly the ever-decreasing operating voltage limits of scaled SiGe HBTs reveal the growing importance breakdown related issues, particularly in the realm of mixed-signal circuit design.

## 1.5 Summary

In this chapter, we highlighted the emerging needs of next-generation communications systems, and introduced the silicon-germanium heterostructure bipolar transistor, describing the strengths that make SiGe HBT BiCMOS technology a suitable candidate for a variety of high frequency applications. However, with performance gains in SiGe HBTs come reductions in breakdown voltage, making operating voltage constraints an increasingly vital consideration in SiGe HBTs. Important technology aspects of state-of-the-art SiGe HBT BiCMOS were reviewed, and the relevant physics of the SiGe HBT device was discussed. Also, a brief overview of breakdown voltage and avalanche multiplication in bipolar devices was given.

In Chapter II, additional discussion will be paid to breakdown for different transistor biasing configurations, and operating voltage constraints will be experimentally characterized as a function of technology generation, device geometry, and operating condition. Chapter III will experimentally address the practical implications of operating voltage constraints at the device and circuit level, discussing compact modeling issues, small signal instabilities, mixed-mode reliability, self-heating, and thermal coupling between devices. Finally, Chapter IV will provide overall conclusions and discuss future directions for further study.

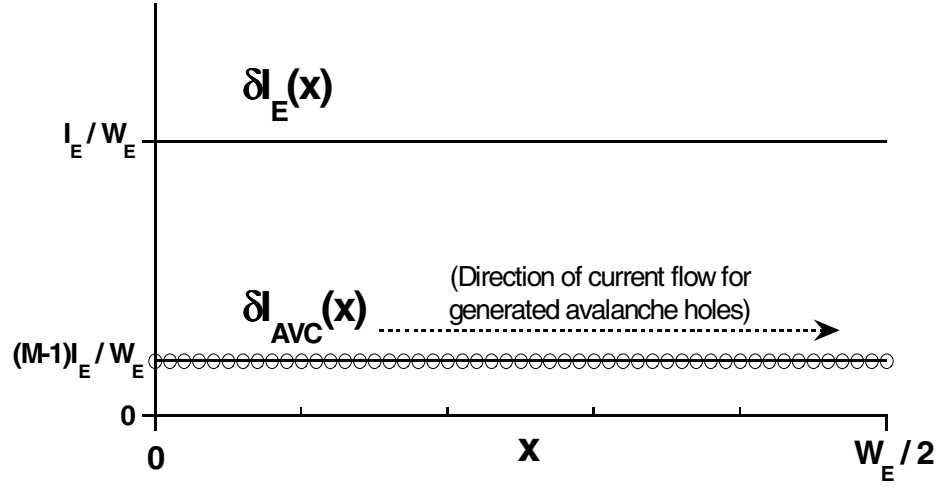
## CHAPTER II

### BREAKDOWN CHARACTERISTICS IN SIGE HBTS

#### 2.1 *Introduction*

As shown in Chapter I, breakdown voltages ( $BV_{CEO}$ ,  $BV_{CBO}$ ) in SiGe HBTs can be expected to become lower as high frequency device performance improves. As a result, circuit designers are faced with increasingly stringent device operating restrictions as maximum limits of usable collector voltage are compressed. However,  $BV_{CEO}$  and  $BV_{CBO}$  do not tell the full story of breakdown voltage constraints, and transistors are often required to operate in the region between the two breakdown voltages for many practical circuits. We find, in fact, that SOA limits vary considerably between different bias configurations and have a strong dependence on current injection level.

In this chapter, we will experimentally examine breakdown and practical operational voltage constraints in state-of-the-art SiGe HBTs as they relate to technology generation, device geometry, bias configuration, and operating point. First, a more detail background of breakdown related instabilities in SiGe HBTs will be presented and supported by qualitative, simulated, and experimental analysis. The key breakdown-related differences between different bias configurations will be addressed. New definitions for breakdown voltage, adopted from standard measurements, will be presented and examined. Next, the breakdown characteristics for three generations of SiGe HBT technology (50 GHz, 120 GHz, and 200 GHz peak  $f_T$ ) will be examined experimentally for different bias configurations and device geometries in order to generate practical design guidelines to ensure stable device operation under high voltage conditions.



**Figure 9:** Simplified depiction of injected current ( $A/\mu m$ ) and avalanche generation as a function of position within the device.

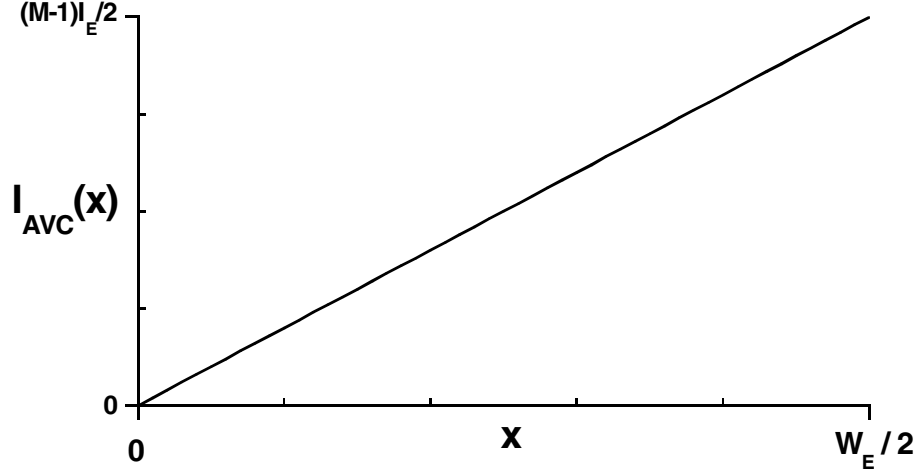
## 2.2 Background

### 2.2.1 Pinch-in Effects

Avalanche-induced base current reversal, as described in Chapter I, may cause constriction of current flow within the device which result in unstable device behavior. These current flow non-uniformities are referred to as "pinch-in" effects. Starting with a few basic assumptions, this section will provide a simplified and qualitative examination of pinch-in related phenomena.

To illustrate the origin on the pinch-in effect, consider a simplified 1-dimensional horizontal cross section through the neutral base of a transistor profile with two extrinsic base contacts on either side of the emitter window (as shown in Figure 2). We will assume the active device is horizontally symmetrical about the center of the neutral base region, which we will denote as position  $x = 0$ . Therefore, for drawn emitter width  $W_E$ , the boundaries of the active base occur at  $x = +W_E/2$  and  $x = -W_E/2$ . For a moment we will make the assumption that current distribution  $I_E$  is uniform within the device. Therefore, the current passing within the small segment between  $x$  and  $x + \delta x$  is simply a constant with respect





**Figure 10:** Simplified depiction of avalanche current (A) as a function of position within the active device.

to position, or

$$\delta I_E(x) = \delta I_E = \frac{I_E}{W_E} \quad (13)$$

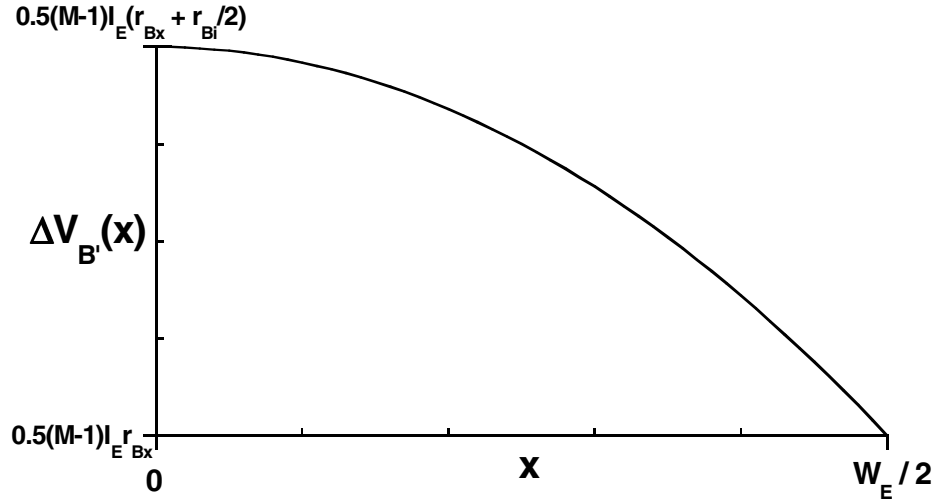
This scenario is depicted in Figure 9. The excess current generated by impact ionization in the CB-SCR is

$$I_{AVC} = \frac{I_E}{(\beta + 1)} [(M - 1)\beta - 1] \approx (M - 1)I_E \quad (14)$$

for current gain  $\beta \gg 1$ . We will likewise assume that the product  $(M - 1)\beta \gg 1$ , and thus the forward injected hole current ( $I_{p,e}$ , in Equation (12)) is very small compared to  $I_{AVC}$  and can be neglected. The avalanche current consists of both an electron current component, which is swept into the collector, and as hole current component, which is swept into the base. Therefore, the avalanche hole current generated within the small segment between  $x$  and  $x + \delta x$  within the base region is

$$\delta I_{AVC}(x) \approx \frac{(M - 1)I_E}{W_E} \quad (15)$$

Assuming the base current ( $I_B$ ) is not fixed externally, the excess holes generated by avalanche multiplication will flow from their point of origin ( $0 < x < W_E/2$ ) to the extrinsic base boundary ( $x = W_E/2$ ) and exit through the base terminal. The total avalanche



**Figure 11:** Simplified depiction of intrinsic base potential (V) as a function of position within the active device.

current at a particular point  $x$  within the base is the summation of the generated avalanche current for each small segment  $\delta x$  between the center of the device ( $x = 0$ ) and the position  $x$ , and therefore can be represented as

$$I_{AVC}(x) = \int_0^x \delta I_{AVC}(y) dy \approx \frac{(M-1)I_E}{W_E} x \quad (16)$$

This is plotted in Figure 10. Clearly, the hole current is vanishingly small at the center of the symmetric device, and equals half of the total avalanche current at  $x = +W_E/2$ . (The other half of the avalanche current exits the device through the other extrinsic base contact at  $x = -W_E/2$ .) We define the intrinsic base potential  $V_{B'} = V_B + \Delta V_{B'}$ . Treating the intrinsic base resistance  $r_{Bi}$  as a uniformly distributed factor yields  $\delta r_{Bi}(x) = \delta r_{Bi} = \frac{r_{Bi}}{W_E/2}$ .

Therefore

$$\Delta V_{B'}(x) = \int_x^{W_E/2} \delta r_{Bi} I_{AVC}(y) dy \quad (17)$$

Substituting the result from Equation (16) into (17), and assuming a potential drop across the extrinsic base resistance is equal to  $r_{Bx} I_{AVC}(0)$ , we obtain

$$\Delta V_{B'}(x) = \frac{r_{Bi}(M-1)I_E}{4} - r_{Bi}(M-1)I_E(x/W_E)^2 + r_{Bx}(M-1)I_E/2 \quad (18)$$

as plotted in Figure 11. At this point we are forced to reevaluate our initial assumption of uniform current distribution, given that  $I_E(x)$  is a function of intrinsic base potential  $V_{B'E'}(x)$ , according to

$$I_C = I_S e^{V_{BE}/(kT/q)} \quad (19)$$

Therefore, for saturation current  $I_S$ , and  $I_E = \frac{\beta}{\beta+1} I_C \approx I_C$ ,

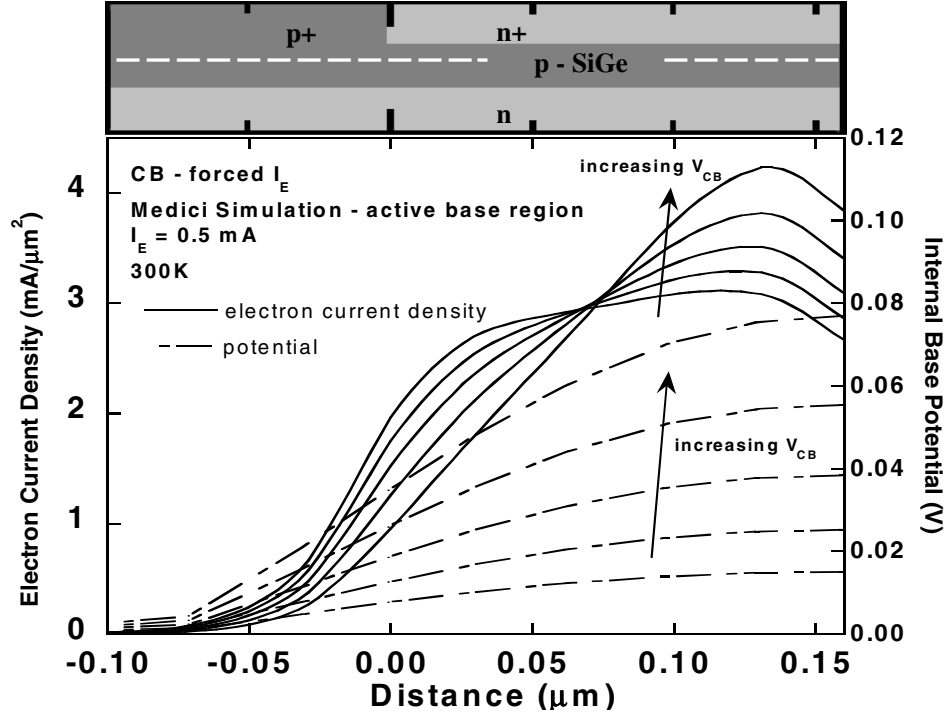
$$\delta I_E(x) = I_E(x)/W_E \approx \frac{I_S}{W_E} e^{V_{B'E'}(x)/(kT/q)} \quad (20)$$

Ignoring the potential drop across the parasitic emitter resistance ( $r_E$ ) we define  $V_{B'E'}(x) = V_{BE} + \Delta V_{B'}(x)$ . We also define the thermal voltage  $V_T = kT/q$ . Thus,

$$\Delta V_{B'}(x) = \int_x^{W_E/2} \left[ \frac{2r_{Bi}}{W_E^2} (M-1) I_S e^{V_{BE}/V_T} \right] e^{\Delta V_{B'}(y)/V_T} y dy \quad (21)$$

The terms enclosed within the brackets may be treated as a constant factor. It is clear, however, that the change in intrinsic base potential ( $\Delta V_{B'}(x)$ ) is an exponential function of itself, and that this integral must be solved iteratively. Forgoing that, we can use this expression to note the positive-feedback mechanism associated with pinch-in, concluding that the intrinsic base potential distribution is stable for  $\Delta V_{B'} \ll V_T$ , and unstable for  $\Delta V_{B'} \approx V_T$ , at which point pinch-in occurs. If we consider the voltage drop across the emitter resistance ( $r_E$ ), then  $V_{B'E'}(x) = V_{BE} + \Delta V_{B'}(x) - \Delta V_{E'}(x)$ . Clearly this additional term produces a stabilizing effect, particularly as the emitter current increases. This will be discussed further from an experimental side in the sections to follow.

A 2-D device simulation of was performed using MEDICI (including hydrodynamic energy balance and impact ionization) for various values of  $V_{CB}$ . Figure 12, taken from these simulations, shows the onset of distributed current and voltage non-uniformities within a cross-section of the active base region. The relevant device profile is aligned with the spatial dimensions of the plot in the inset above Figure 12, and the examined cross-section is highlighted. The severe current localization associated with pinch-in is then subject to a myriad of instabilities associated with self-heating and electric field collapse [22]. Attempting to simulate within this unstable region at higher  $V_{CB}$  results only in

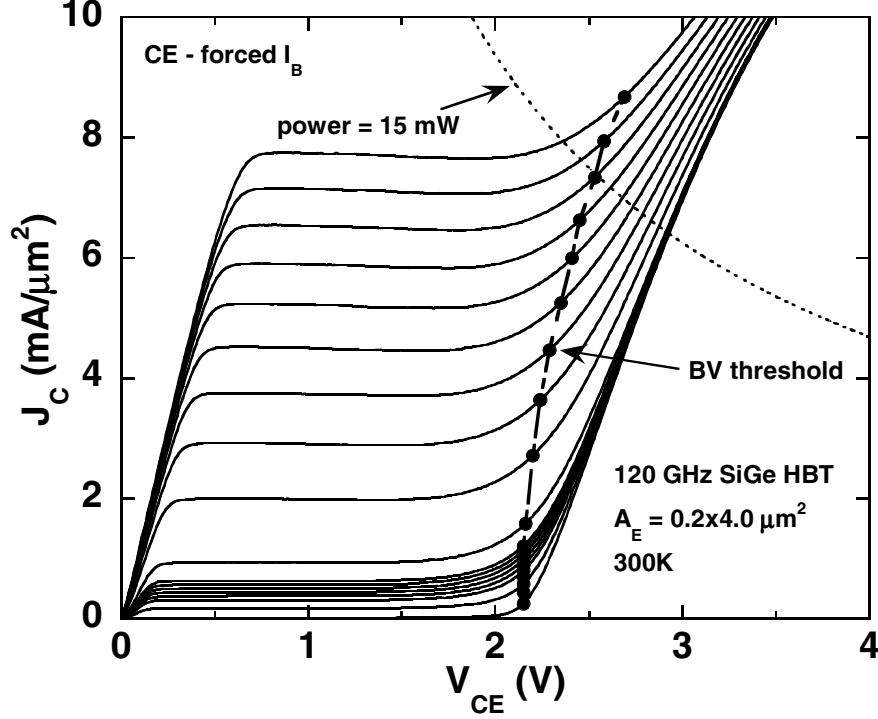


**Figure 12:** MEDICI simulation of a 120 GHz SiGe HBT showing the intrinsic potential distribution and onset of current constriction within the neutral base.

non-convergent numerical solutions.

### 2.2.2 Common-emitter bias with forced base current

For the common-emitter bias configuration driven by a constant base current ( $CE-I_B$ ),  $I_B$  is held constant by an external current source (similar to the constant zero current "driven" during open-base operation), so excess holes, generated in the CB-SCR by impact ionization and swept into the base region, must then be injected into the emitter [15]. Thus, the avalanche current is amplified by the forward current gain  $\beta$  across the E-B junction, which in turn increases the collector current and thus the avalanche current via positive feedback, leading to premature breakdown. As a net result, the open-base breakdown voltage ( $BV_{CEO}$ , for  $I_B = 0$ ) and corresponding fixed  $I_B$  breakdown voltages (constant  $I_B > 0$ ) are much lower than the collector-base reverse junction breakdown voltage ( $BV_{CBO}$ ). In many SiGe technologies, the ratio between the two breakdown voltages has been observed to be approximately one-third [4].



**Figure 13:** CE - forced  $I_B$  output characteristic with BV thresholds indicated.

For this study, the  $CE-I_B$  BV threshold is defined as the point at which the slope of  $J_C$  on  $V_{CE}$  exceeds the ratio of  $J_C$  at peak  $f_T$  over  $BV_{CEO}$  for that technology. For demonstration, this constant-slope BV threshold is plotted together with an output characteristic family in Figure 13 for a typical 120 GHz SiGe HBT in this bias configuration. It should be noted, however, that in typical mixed-signal circuit design devices are usually subjected to finite external impedance between the base and emitter terminals. In light of this, one might consider  $BV_{CEO}$ , or the similar (non-zero) fixed base current breakdown voltages, to be irrelevant from a practical standpoint. In any case, open-base and  $CE-I_B$  breakdown presents a worst-case (lowest) BV threshold [4], and in this sense is useful for technology performance comparisons.

### 2.2.3 Common-emitter bias with forced base voltage

A second biasing condition we will examine is the common-emitter bias driven by a constant base-emitter voltage ( $CE-V_{BE}$ ). As noted above, practical circuits are not typically

driven by a constant current source as occurs in the  $CE-I_B$  case, and the  $CE-V_{BE}$  configuration is more commonly encountered in practical circuits. The  $CE-V_{BE}$  driving condition differs fundamentally from the forced- $I_B$  case because excess hole current resulting from impact ionization is allowed to freely exit the base terminal due to the low series impedance ( $R_s = 0 \Omega$  in the ideal case) of the applied voltage source. At sufficiently high collector voltage (approximately  $BV_{CEO}$ ) the product of current gain and avalanche multiplication factor exceeds unity and the base current reverses sign. As discussed in a previous section, this reversal of base current, with increased  $V_{CB}$ , can eventually lead to central current crowding and bias instabilities. However, depending on the circuit application, stable bias can still be achieved (and may in fact be required) in regions of considerable base current reversal, thus  $CE-V_{BE}$  bias allows operation at higher voltages (between  $BV_{CEO}$  and  $BV_{CBO}$ ) than does  $CE-I_B$  bias [3], [22].

A complex set of interactions determine the  $CE-V_{BE}$  breakdown voltage constraints [15], [16], [17] [18], [19], [22], [23], [24], [25]. The primary driving mechanism is impact ionization, which, at sufficiently high levels, causes base current reversal, as described above. As qualitatively illustrated in a previous section, the current flowing over the parasitic intrinsic base resistance creates a potential distribution within the neutral base favoring current flow at the center of the device (highest internal  $V_{BE}$ ). As  $|I_{B_{rvs}}|$  increases further, this potential distribution eventually becomes unstable and a significant portion of the current collapses to the center of the device in a phenomenon described as "pinch-in" [3], [22].

The stable voltage limits for  $CE-V_{BE}$  operation were explored in [22] in terms of a critical reverse base current  $I_{B_{rvs\_crit}} (< 0)$ :

$$I_{B_{rvs\_crit}} = -\frac{V_T + r_E I_E}{(r_B G)} \quad (22)$$

for ( $I_E > 0$ ) with

$$G = 1.5 + \frac{2.6}{(3 + l_E/w_E)} \quad (23)$$

The parameters  $l_E$  and  $w_E$  correspond to the device emitter length and width, respectively. As shown in Equations (22) and (23), this factor is dependent on device geometry and the parasitic emitter and base resistances. Reverse base current can then be related to the avalanche multiplication factor:

$$I_{B\_rvs} = \frac{-I_E}{(\beta + 1)}[(M - 1)\beta - 1] \approx -(M - 1)I_E. \quad (24)$$

Therefore, for  $\beta \gg 1$ ,

$$(M - 1)_{critical} \approx -\frac{I_{B\_rvs\_crit}}{I_E}. \quad (25)$$

For low injection (neglecting the  $M - 1$  dependence on operating current), the avalanche multiplication factor can be related to  $V_{CB}$  via the following empirical fit [22]:

$$(M - 1) = c \left( \frac{V_{CB}}{1\text{volt}} \right)^a. \quad (26)$$

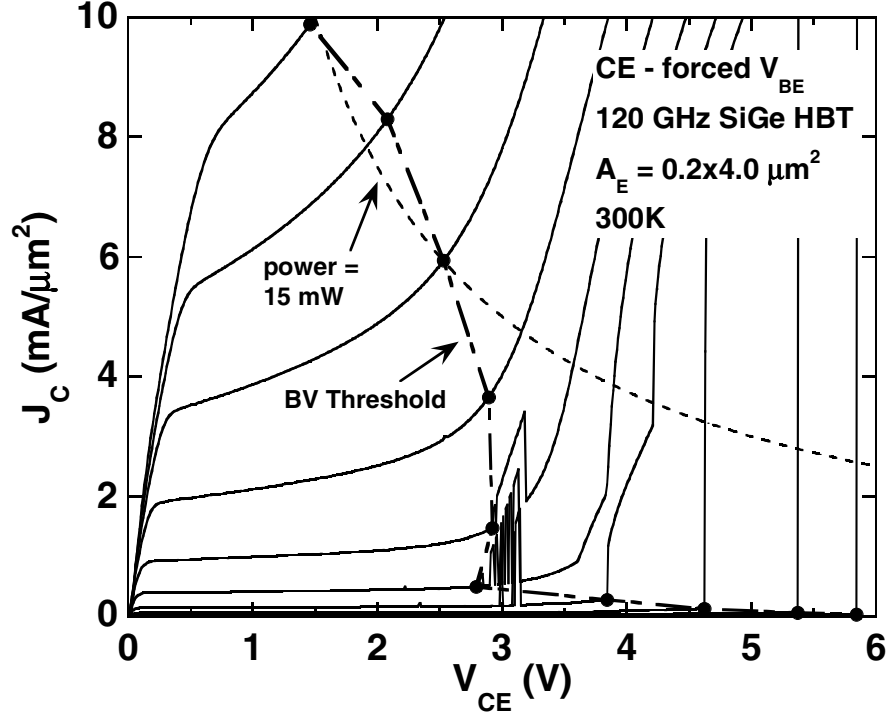
For accurate extension of avalanche current to high bias, a more complicated current dependant  $M - 1$  relation, as discussed in [26] and [27], may also be used.

Combining Equations (25) and (26) and rearranging the terms yields a functional relation between forced emitter current and maximum stable  $V_{CB}$ , based either on critical base current  $I_{B\_rvs\_crit}$ , or more generally, on the parasitic emitter and base resistances:

$$V_{CB\_crit} = \left( \frac{|I_{B\_rvs\_crit}|}{cI_E} \right)^{1/a} \cdot (1\text{volt}) \quad (27)$$

$$= \left[ \frac{(V_T + r_E I_E)}{cI_E r_B G} \right]^{1/a} \cdot (1\text{volt}). \quad (28)$$

Overall, these relations illustrate that pinch-in will occur when the magnitude of the internal base potential distribution becomes non-negligible with respect to the thermal voltage  $V_T = kT/q$ , taking into account the proportionality factor  $G$  and the series potential drop across the parasitic emitter resistance,  $r_E I_E$ . Limiting the discussion to low injection operation allows a degree of simplification of the relevant parameters comprising the critical reverse base current. For instance, the avalanche factor  $M - 1$  possesses a much stronger dependence on  $V_{CB}$  than  $I_E$ , particularly at lower injection. To extend the discussion to higher injection, the current dependence of the  $M - 1$  should likewise be accounted

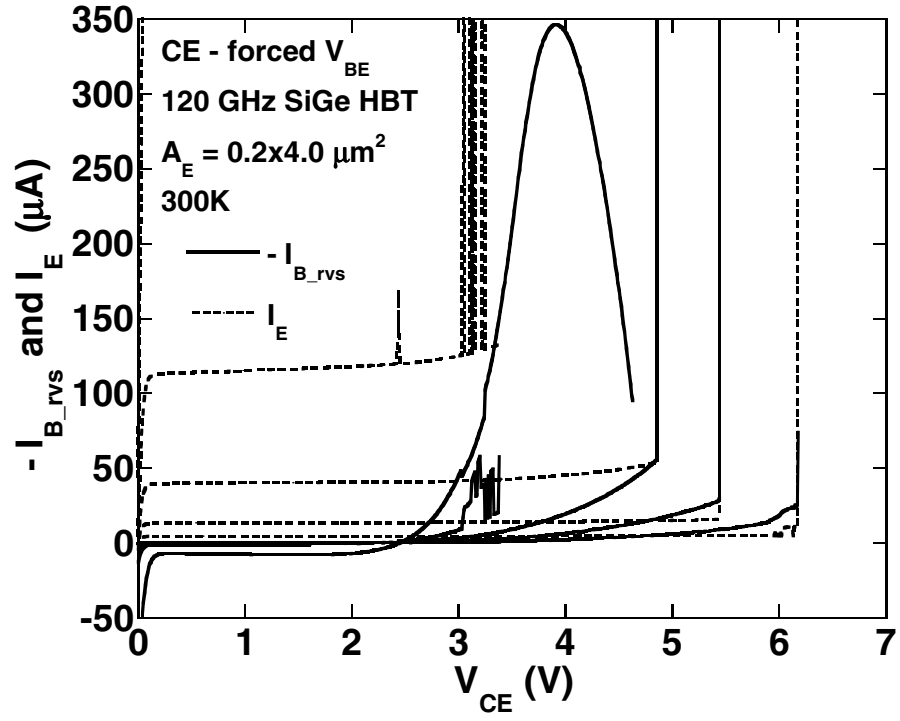


**Figure 14:** CE - forced  $V_{BE}$  output characteristic with associated BV thresholds.

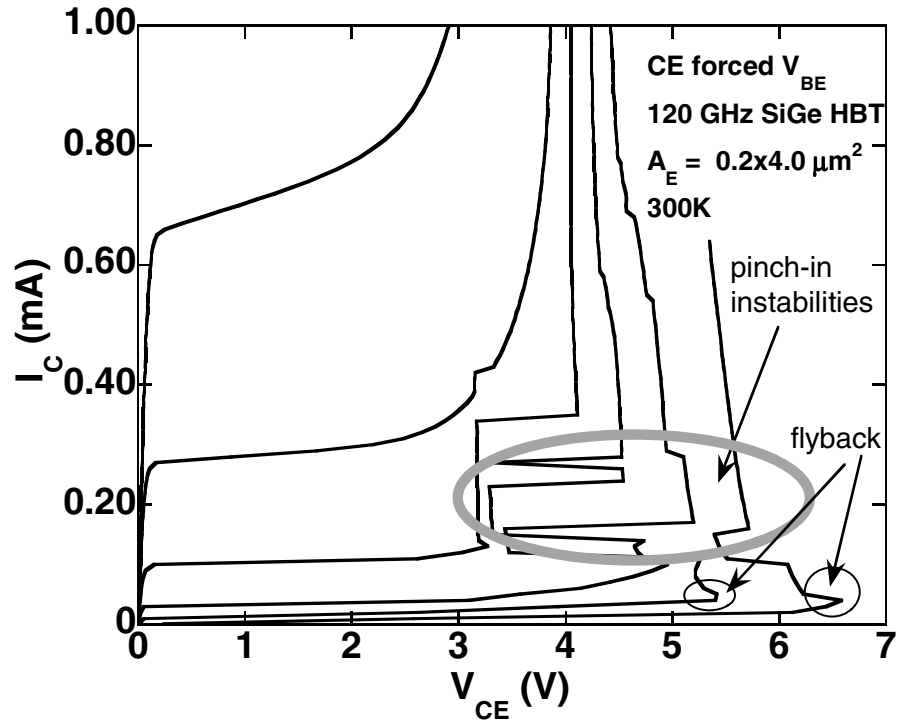
for [26], [27]. In addition, it is appropriate to consider the dependence of base sheet resistance on  $V_{CB}$  and collector current [22], [25], [28]. At increased injection levels, the role of the parasitic emitter resistance becomes non-negligible since, with increased  $I_E$ , the potential drop across  $r_E$  (also dependent on current level and current crowding) significantly (with respect to the thermal voltage  $V_T$ ) debiases the center of E-B junction and thus increases the magnitude of the maximum sustainable reverse base current, allowing the device to remain in stable operation at higher  $M - 1$ , and thus higher  $V_{CB}$  [22]. Self-heating also becomes an important consideration at high-injection. These considerations shall be explored further in Chapter III.

Similar to the  $CE-I_B$  case, for this study the  $CE-V_{BE}$  BV threshold is defined as the point at which the slope of  $J_C$  on  $V_{CE}$  exceeds the ratio of  $J_C$  at peak  $f_T$  over  $BV_{CEO}$  for that technology. A typical family of  $CE-V_{BE}$  output characteristics is provided in Figure 14. The breakdown voltage threshold and a contour of constant power are also provided for comparison. The output characteristic shows considerable differences in behavior as  $V_{BE}$





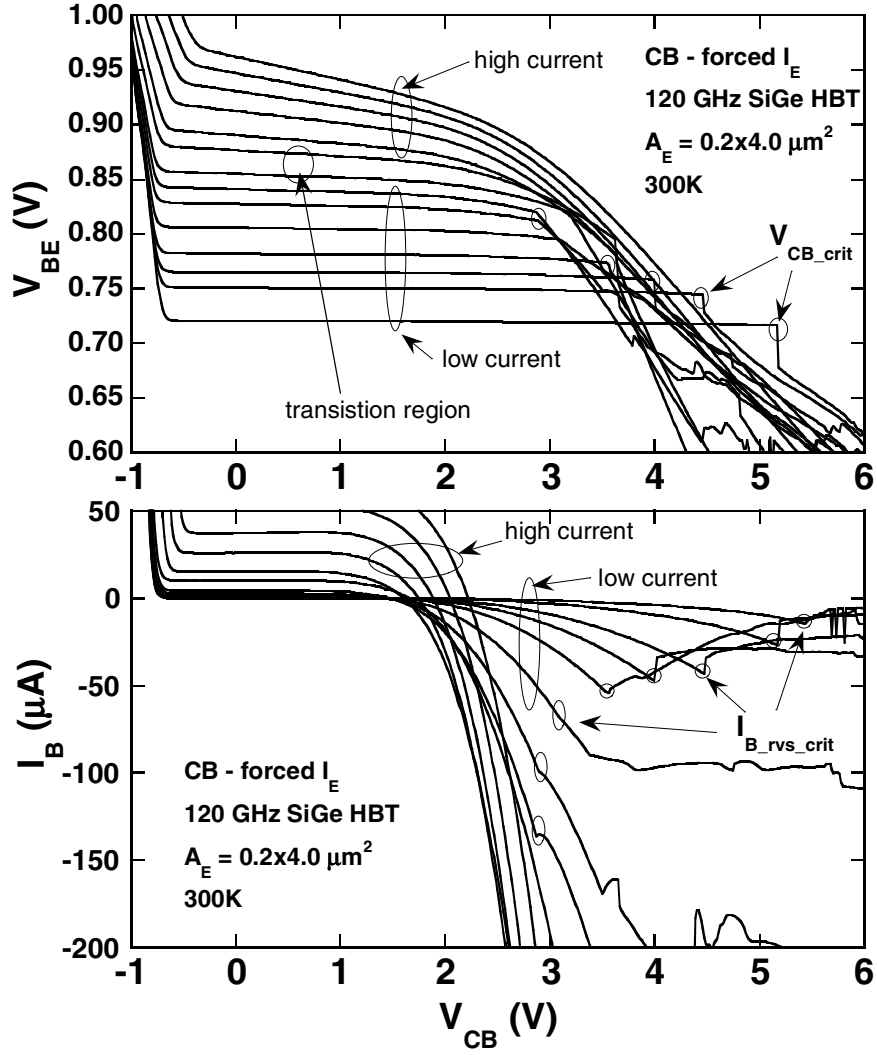
**Figure 15:** Reverse base current and emitter current characteristics resulting from CE - forced  $V_{BE}$  measurement.



**Figure 16:** CE - forced  $V_{BE}$  output characteristic with  $I_C$  swept and  $V_{CE}$  measured.

increases. For the cases at low  $V_{BE}$  (and thus low  $J_C$ ), at high  $V_{CE}$  the device undergoes electro-thermal runaway, abruptly entering breakdown as the collector current rapidly increases (with a slope approaching infinity) until reaching the external limit (or destroying the device). However, for the curves at high  $V_{BE}$  (and thus high  $J_C$ ), the collector current increases smoothly with  $V_{CE}$ . This difference is also reflected in base and emitter currents, as shown in Figure 15. At low  $V_{BE}$ , both  $I_E$  and  $|I_{B_{rvs}}|$  increase rapidly at  $V_{CB_{crit}}$ . However, for higher  $V_{BE}$ ,  $|I_{B_{rvs}}|$  reaches a peak, then begins to decrease as  $I_E$  increases due to self-heating and forward injected base current component ( $I_{p,e}$  from Equation (12) discussed in Chapter I) becomes more dominant. At sufficiently high current, base current reversal is suppressed entirely.

For additional insight, Figure 16 shows a similar  $CE-V_{BE}$  characteristic, except with the  $I_C$  swept and  $V_{CE}$  measured. For low  $V_{BE}$ , device breakdown occurs at the collector current "fly back" point, at which  $V_{CE}$  decreases for increased  $I_C$  due to a combination of self heating and the increased intrinsic base potential due to the flow of  $I_{B_{rvs}}$  over the parasitic base resistance. Note that while this "fly back" characteristic is aggravated by the pinch-in effect, as observed in the severe instabilities measured in this region, this characteristic of decreasing  $V_{CE}$  with increasing  $I_C$  is observable in  $CE-V_{BE}$  simulations that do not take into account current flow non-uniformities or pinch-in related effects. Clearly, the fly back of the collector current during  $CE-V_{BE}$  operation introduces a bistability to the output characteristic [29]. This, when considered in relation to unpredictable nature of pinch-in instabilities, may explain the unstable region in the output characteristic (as shown in Figure 14) observed in the transition between the low injection snapback behavior and high injection self-heating behavior. However, we note with caution that the precise structure of the resulting instabilities, as shown, may well be an artifact of the particular measurement setup, and thus should be investigated further.



**Figure 17:**  $V_{BE}$  and  $I_B$  characteristics from CB - forced  $I_E$  measurements at low and high injection.

#### 2.2.4 Common-base bias with forced emitter current

A common-base bias configuration driven by a constant emitter current ( $CB-I_E$ ) will be an important focal point for this study, since it lends itself to many practical circuit applications (e.g., amplifier output stages). Like  $CE-V_{BE}$ , the  $CB-I_E$  driving condition allows excess hole current resulting from impact ionization is allowed to freely exit the base terminal, which, at high  $V_{CB}$ , can lead to central current crowding and pinch-in instabilities. However, since stable bias is possible under conditions of considerable base current reversal, thus  $CB-I_E$  bias allows operation at higher voltages (between  $BV_{CEO}$  and  $BV_{CBO}$ ) than does  $CE-I_B$  bias [3]. Moreover, since the  $I_E$  is held constant, electro-thermal runaway, as

may occur in the case where  $V_{BE}$  is held constant, is prevented during  $CB-I_E$  operation as long as  $V_{CB} < BV_{CBO}$ .

From [22], the critical reverse base current under  $CB-I_E$  operating conditions is

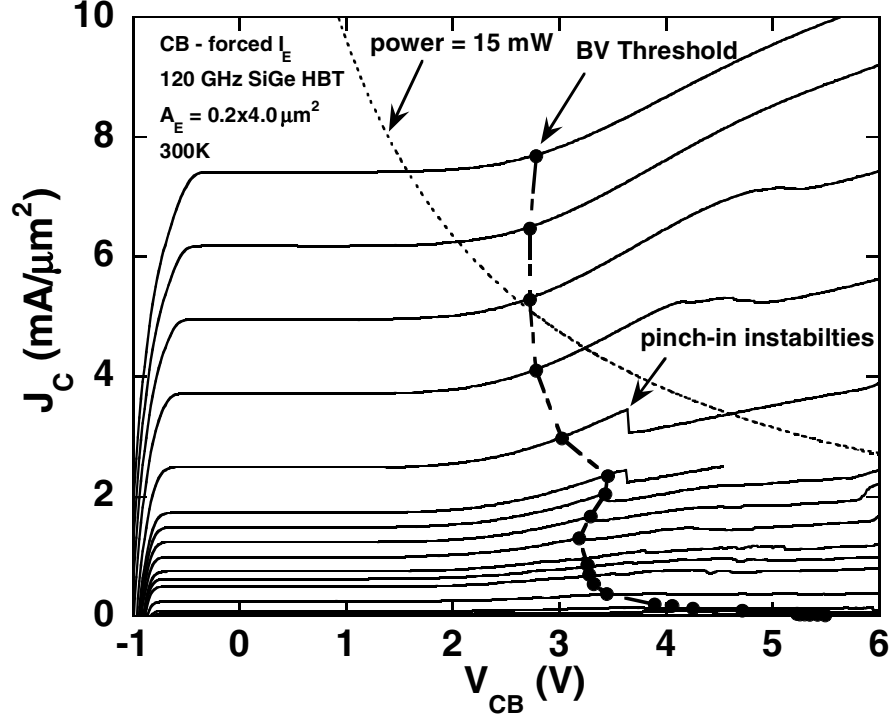
$$I_{B_{rvs\_crit}} = I'_{B_{rvs\_crit}} \left[ 1 + \left( \frac{w_E}{l_E} \right)^2 \right] \quad (29)$$

where  $I'_{B_{rvs\_crit}}$  represents the critical reverse base current for constant base voltage drive ( $CE-V_{BE}$ ). For  $l_E \gg w_E$  (as is assumed for the device geometries examined in the present paper)  $I_{B_{rvs\_crit}} \approx I'_{B_{rvs\_crit}}$ . Given this assumption, the final result for  $V_{CB\_crit}$  is identical to that shown in Equations (27) and (28).

During  $CB-I_E$  operation a considerable roll-off of  $V_{BE}$  with increased  $V_{CB}$  is commonly observed [3], [22]. One cause is the voltage drop of  $I_{B_{rvs}}$  across  $r_B$ . For example, momentarily neglecting self-heating, for emitter potential  $V_E$  ( $< 0$  and equal to  $-V_{BE}$ ),  $|V_E|$  must decrease to maintain a constant  $V_{B'E'}$  as the internal base potential  $V_{B'}$  increases above the zero volt potential of the common-base terminal. Self-heating becomes an important factor in the  $V_{BE}$  on  $V_{CB}$  characteristic at higher current densities and during pinched-current operation, resulting in a decrease of the internal  $V_{B'E'}$  to maintain constant  $I_E$  at elevated operating temperature.

The contrast between low-injection (minimal self-heating) and high-injection (considerable self-heating)  $V_{BE}$  on  $V_{CB}$  behavior is depicted in Figure 17. Points at which pinch-in occurs are indicated. Figure 17 also shows the reverse-base-current characteristics across bias, with the threshold  $I_{B_{rvs\_crit}}$  indicated on each curve. Similar to findings presented in [22], these results show a considerable bias dependence on the magnitude of  $I_{B_{rvs\_crit}}$ . This dependence, and its relation to device geometry, is discussed further in Section 2.3.

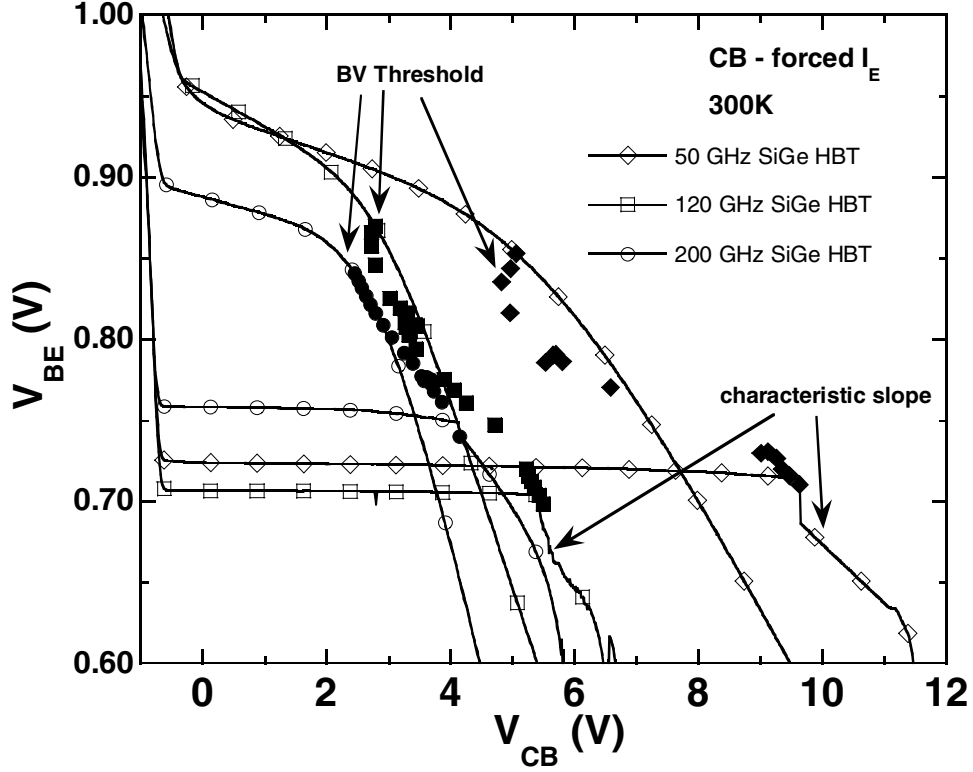
For the  $CB-I_E$  bias configuration, the BV threshold, as depicted in Figure 18, is conveniently defined with respect to a constant  $V_{BE}$  on  $V_{CB}$  slope. The critical  $V_{BE}$  on  $V_{CB}$  slope ( $< 0$ ) for a given technology is determined from the characteristic  $V_{BE}$  roll-off under pinched-current operation (observable at  $V_{CB} > V_{CB\_crit}$  at low  $J_C$ ), as shown in Figure 19 for three generations of SiGe HBT technology. This BV definition for  $CB-I_E$  operation



**Figure 18:** CB - forced  $I_E$  output characteristic with associated BV thresholds.

is similar to, and provides consistent results with, the approach detailed in [30], but is better suited to BV extraction at very high operating current densities found in advanced SiGe HBTs, and takes into account the role of self-heating and parasitic base resistance under both pinched (low current and high voltage) and non-pinched (high current and low voltage) conditions.

A dramatic change in the nature of the BV threshold is observed at higher currents (for  $V_{BE} > 0.85$  V in Figure 17, and  $J_C > 2 \text{ mA}/\mu\text{m}^2$  in Figure 18), as self-heating becomes an important factor in the roll-off of  $V_{BE}$  with increasing  $V_{CB}$ . In this high-injection region, the defined BV threshold no longer corresponds with pinch-in instabilities, and at sufficiently high current levels, pinch-in is effectively suppressed [22]. Defining the  $CB-I_E$  BV with respect to  $V_{BE}$  acknowledges these important considerations at high injection, providing clear indication of the prudent bias limits, even in regions where pinch-in no longer plays a significant role in device behavior. Reliability aspects of this voltage limit associated with hot-carrier degradation at high current will be explored further in Chapter III.



**Figure 19:**  $V_{BE}$  characteristics from CB - forced  $I_E$  measurements at low and high injection for three generations of SiGe HBTs.

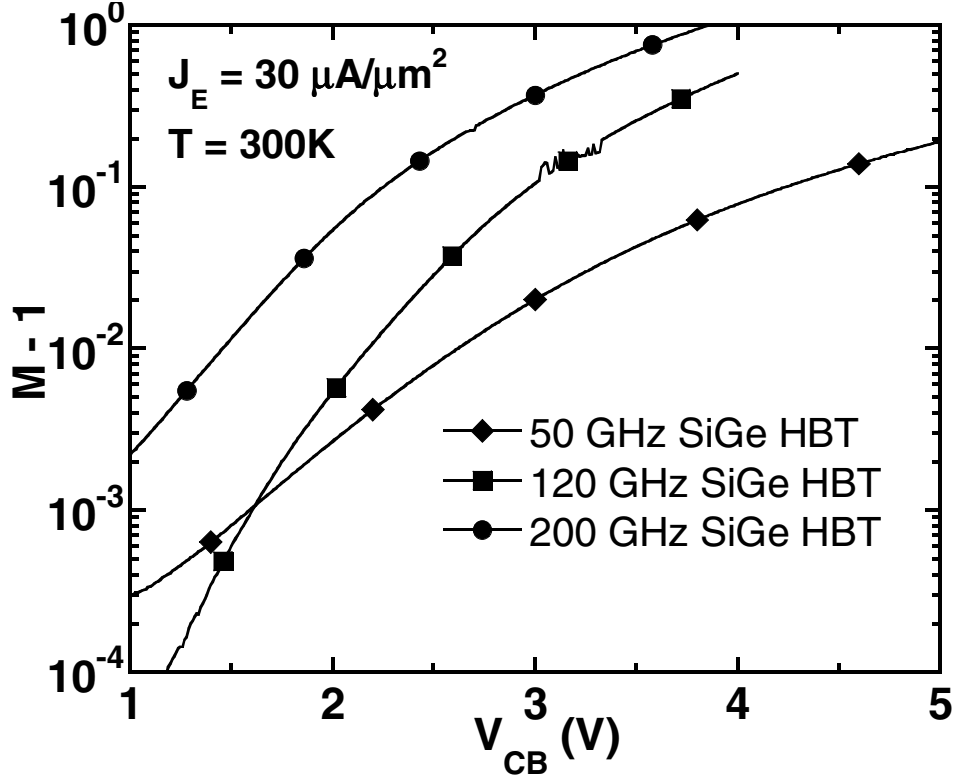
## 2.3 Experimental Characterization

### 2.3.1 Experiment

Samples from three generations of commercially available SiGe HBT technology (50 GHz, 120 GHz, and 200 GHz peak  $f_T$ ) were measured at *dc* under various bias conditions ( $CE-I_B$ ,  $CE-V_{BE}$ ,  $CB-I_E$ ) to characterize and compare breakdown effects and operating voltage constraints across technology generation. These measurements were performed on-wafer using the Agilent 4155C Semiconductor Parameter Analyzer. For this study, both high  $f_T$  (HP, or low BV) and high breakdown (HB) devices were characterized.

### 2.3.2 High Performance Results

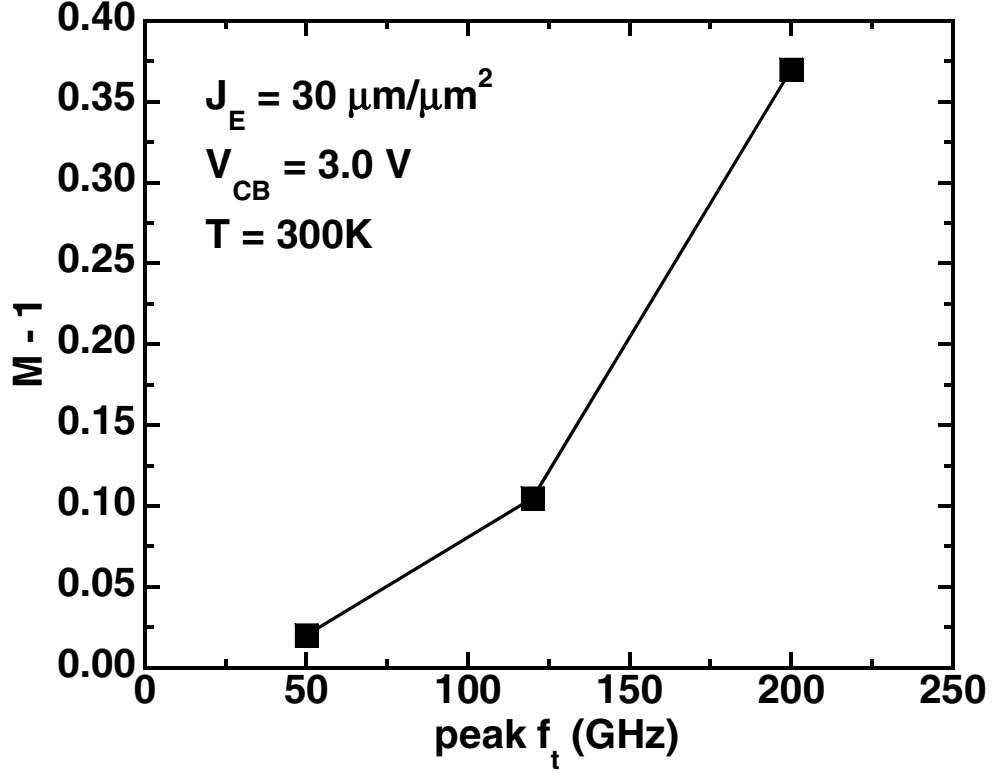
The  $M - 1$  characteristics for the three SiGe HBT technology generations of interest are plotted as a function of  $V_{CB}$  in Figure 20. Figure 21 shows, for a specified  $V_{CB}$ , the significant increase in the avalanche multiplication factor as peak  $f_T$  rises, as was described



**Figure 20:**  $M - 1$  characteristics for three generations of high performance SiGe HBT technology.

in Chapter I. Measured  $CE-I_B$ ,  $CE-V_{BE}$ , and  $CB-I_E$  BV thresholds, as defined in the previous section and normalized to  $J_C$  at peak  $f_T$ , are shown as a function of technology generation in Figures 22, 23, and 24. The transition from CE operation driven by constant  $V_{BE}$  (zero  $\Omega$  external impedance between base and emitter terminals) to constant  $I_B$  drive (infinite external impedance on the base terminal) is depicted in the set of curves of increased external base resistance in Figure 22. As demonstrated in these results, trans-generational device scaling for increased peak  $f_T$  is accompanied with strong decreases in BV for all bias configurations, although  $r_B$  optimization between the 120 GHz and 200 GHz generations dramatically offsets this trend, allowing the 200 GHz SiGe device to sustain approximately the same pinch-in  $V_{CE}$  as the 120 GHz SiGe device [3].

Overall, these results also show that the  $CB-I_E$  bias configuration allows a substantially higher maximum collector voltage than does the  $CE-I_B$  for all three SiGe HBT generations. The corresponding dependency of BV on injection level is also apparent.

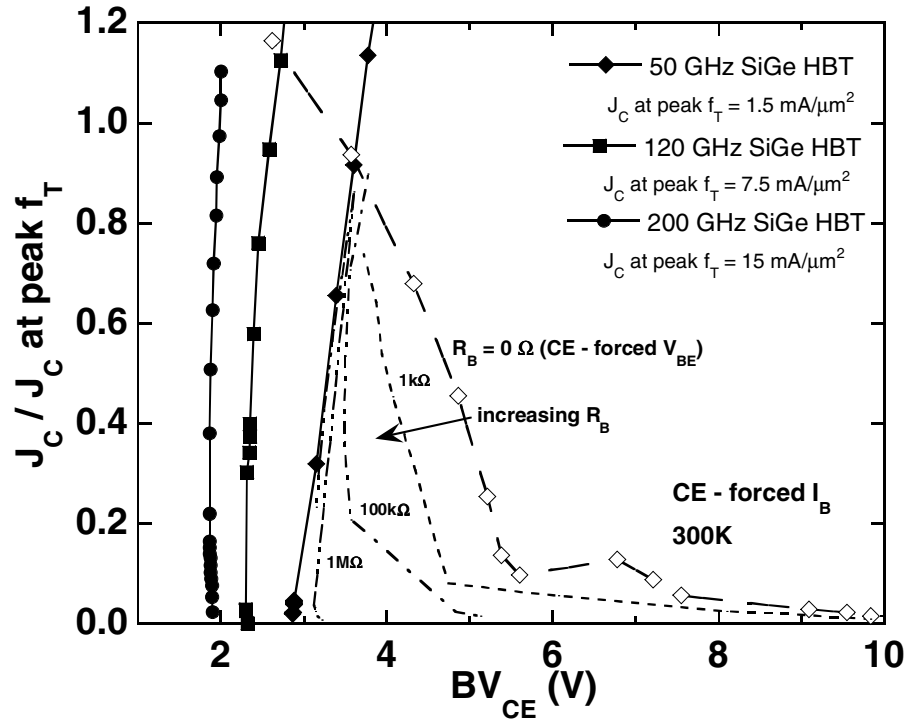


**Figure 21:**  $M - 1$  at constant  $V_{CB} = 3$  V as a function of SiGe HBT technology generation.

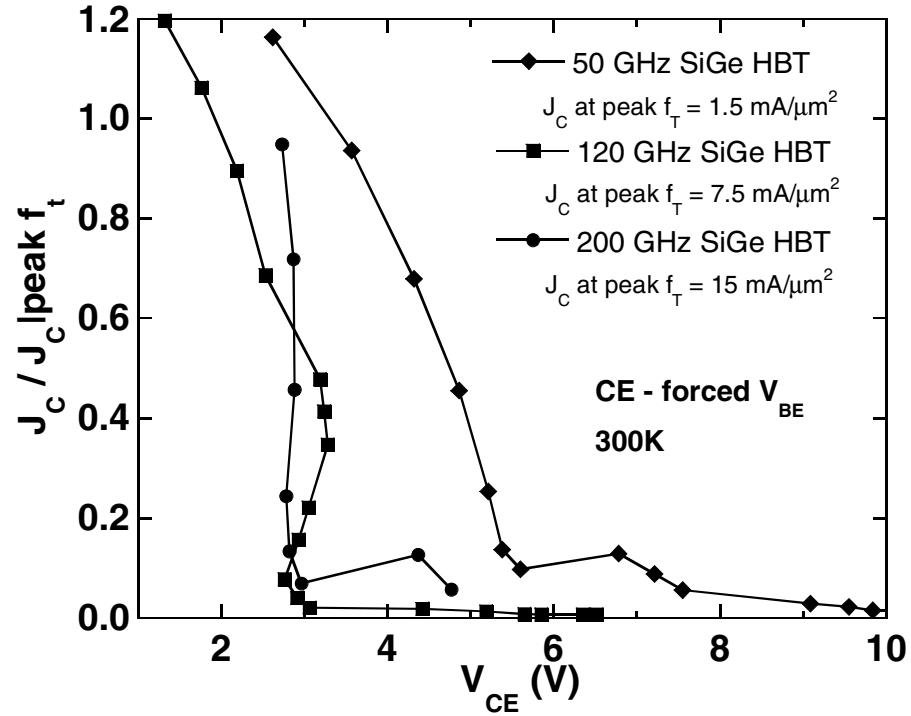
At low injection, the  $CE-V_{BE}$  and  $CB-I_E$  results are strikingly similar, as predicted by Equations (22) through (29), which describe the critical reverse base current and critical collector-base voltage thresholds. However, at high injection these characteristics diverge as self-heating effects begin to strongly influence the  $dc$  behavior of the device operating in the  $CE-V_{BE}$  configuration and degrade its SOA. Self-heating will be discussed in further detail in Chapter III.

Figure 25 shows a comparison between measured  $V_{CB}$  at pinch-in (solid circles) and the maximum  $V_{CB\_crit}$  calculated using Equation (27) (broken and solid lines) for low injection values of  $I_E$  in a 120 GHz SiGe HBT.  $M - 1$  was measured using the forced emitter-current method [14]. The resulting avalanche factor fitting parameters  $c$  and  $a$  (see Equations (26), (27), and (28)) for this device were found to be 0.0015414 and 4.8164, respectively. For the device geometry examined, ( $0.2 \times 4.0 \mu\text{m}^2$ ) the factor  $G$  (see Equations (22), (23), and (28)) was determined to be approximately 1.6. The broken line in Figure 25 shows

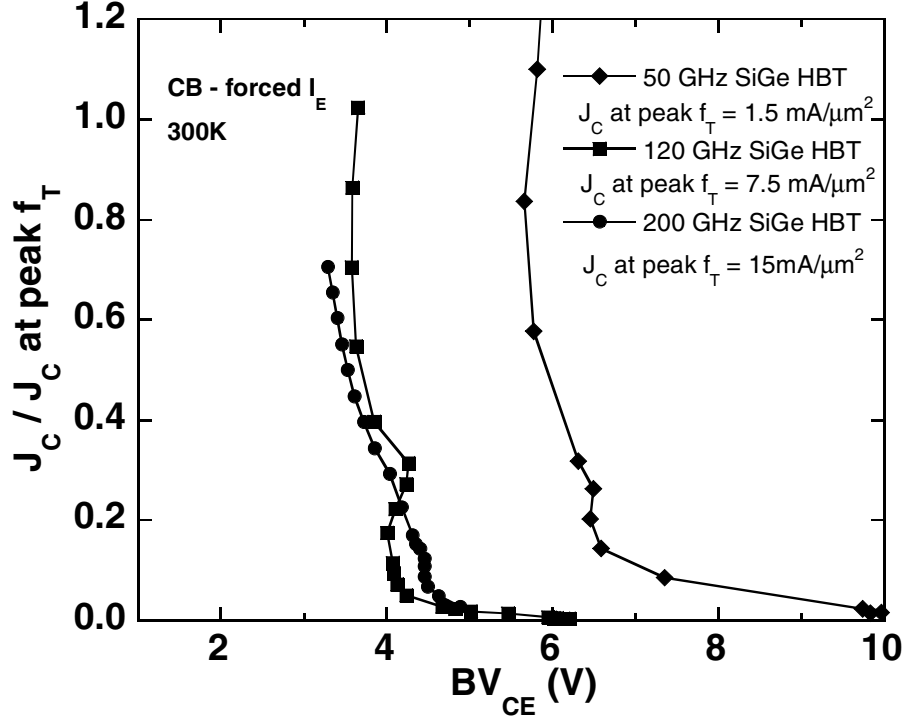




**Figure 22:** CE - forced  $I_B$  BV thresholds for three generations of SiGe HBT technology. An external resistance on the base terminal is varied between  $0\ \Omega$  (CE operation with fixed  $V_{BE}$  drive) and  $1\ \text{M}\Omega$  for the 50 GHz peak  $f_T$  device.

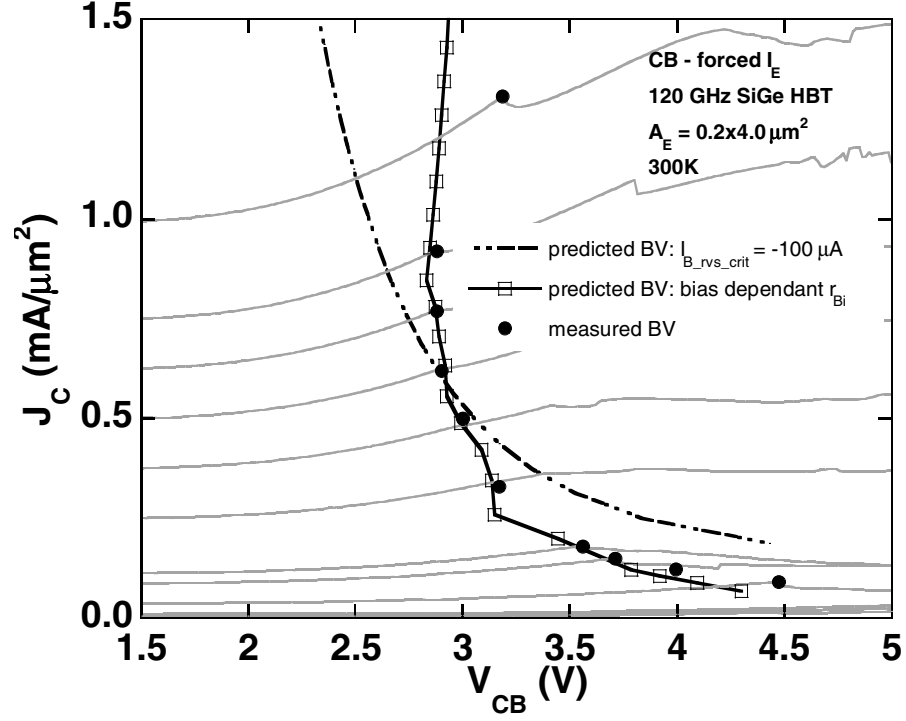


**Figure 23:** CE - forced  $V_{BE}$  BV thresholds for three generations of SiGe HBT technology.



**Figure 24:** CB - forced  $I_E$  BV threshold for three generations of SiGe HBT technology.

the approximation that can be achieved by simply assuming a constant  $I_{B\_rvs\_crit}$  of  $-100 \mu\text{A}$  for all biases. This simplification can serve as a quick-and-dirty guide for predicting low-injection breakdown instabilities by simply using the voltage dependent  $M - 1$  characteristic. However, typical  $CB-I_E$  measurements show a significant bias dependence for  $I_{B\_rvs\_crit}$  (increases strongly as  $I_E$  increases), primarily due to changes in  $r_B$  and  $I_E$ . Therefore, a much better fit can be achieved if the bias dependence of  $r_B$  (even assuming constant  $r_E$  across bias, as in this case) is accounted for, as demonstrated by the close fit between these calculated values (open squares) and the measured pinch-in  $V_{CB}$  values in Figure 25. Extending this close fit to even higher injection levels (above approximately 1.0 mA in this case) requires careful characterization of the bias dependence of both  $M - 1$  and  $r_E$ .



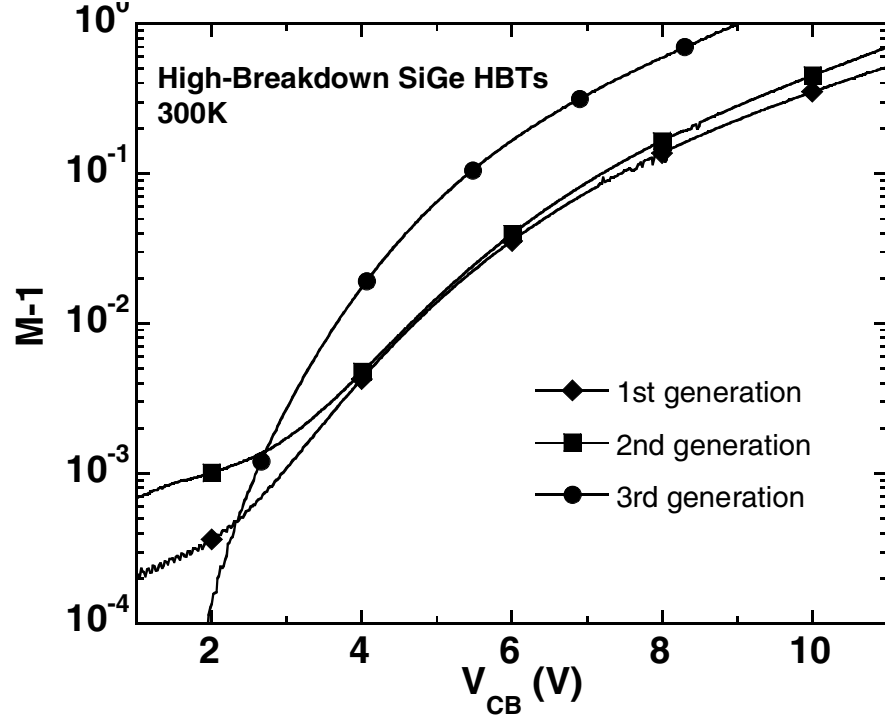
**Figure 25:** Comparison between measured and calculated  $CB$ - $I_E$  pinch-in instabilities.

**Table 2:** Relevant breakdown parameters for HB devices for three SiGe BiCMOS technology generations.

SiGe BiCMOS Technology SiGe HBT BV Parameters	1st generation (IBM 5HP)	2nd generation (IBM 7HP)	3rd generation (IBM 8HP)
$BV_{CEO}$ (V)	5.4	5	4
$BV_{CBO}$ (V)	14.5	12.5	11
$J_C$ at $\beta$ roll-off ( $\text{mA}/\mu\text{m}^2$ )	0.30	0.20	1.60

### 2.3.3 High Breakdown Results

An overview of the relevant BV parameters for the high breakdown (HB) devices from the three SiGe HBT BiCMOS technology generations of interest is provided in Table 2. The  $M - 1$  characteristics were experimentally measured and plotted as a function of  $V_{CB}$  for these HB devices in Figure 26. It is worth noting that  $M - 1$  for the first and second generation HB devices is quite similar, although the third generation HB device shows significantly higher  $M - 1$ . Figure 27 shows the  $CE$ - $I_B$  BV characteristics for the HB devices experimentally extracted across the three technology generations. The characteristics are

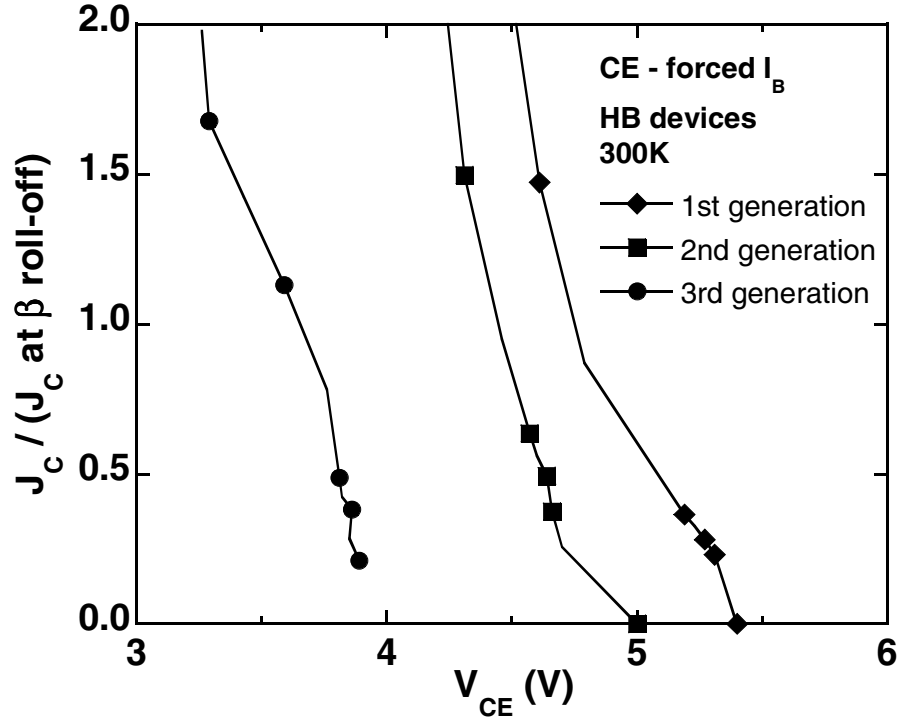


**Figure 26:**  $M - 1$  characteristics for HB devices from three generations of SiGe HBT technology.

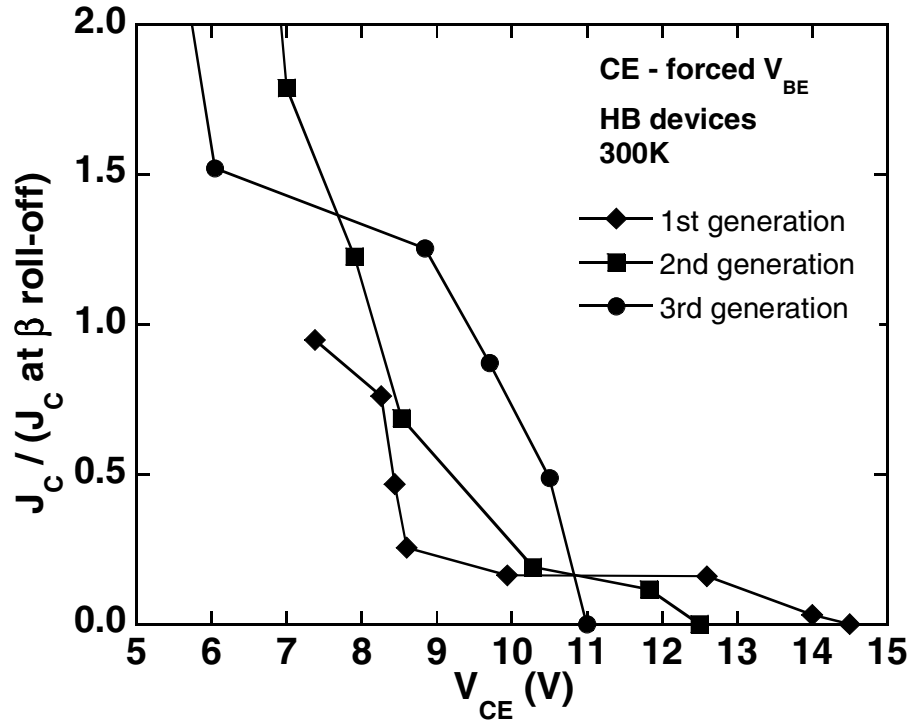
normalized to the  $J_C$  at which strong  $\beta$  degradation is observed (as given in Table 2) to allow comparison between technology generations. Similar to the HP results shown in Figure 22, degradation in the BV threshold is observed between technology generations due to increases in  $M - 1$  and  $\beta$  with technology scaling. However, in the HB case, the  $CE-I_B$  BV thresholds show a decrease with increasing injection.

The HB  $CE-V_{BE}$  BV thresholds are shown in Figure 28. As was shown in Figure 23 for the HP devices, the stable thresholds for the HB devices in this case span a much wider range of  $V_{CE}$  across bias than was observed during  $CE-I_B$  operation. While the first generation HB device certainly shows higher stable  $V_{CE}$  at lowest bias (due to higher  $BV_{CBO}$ ), the third generation HB device shows the highest stable voltage threshold across a wide range of  $J_C$ .

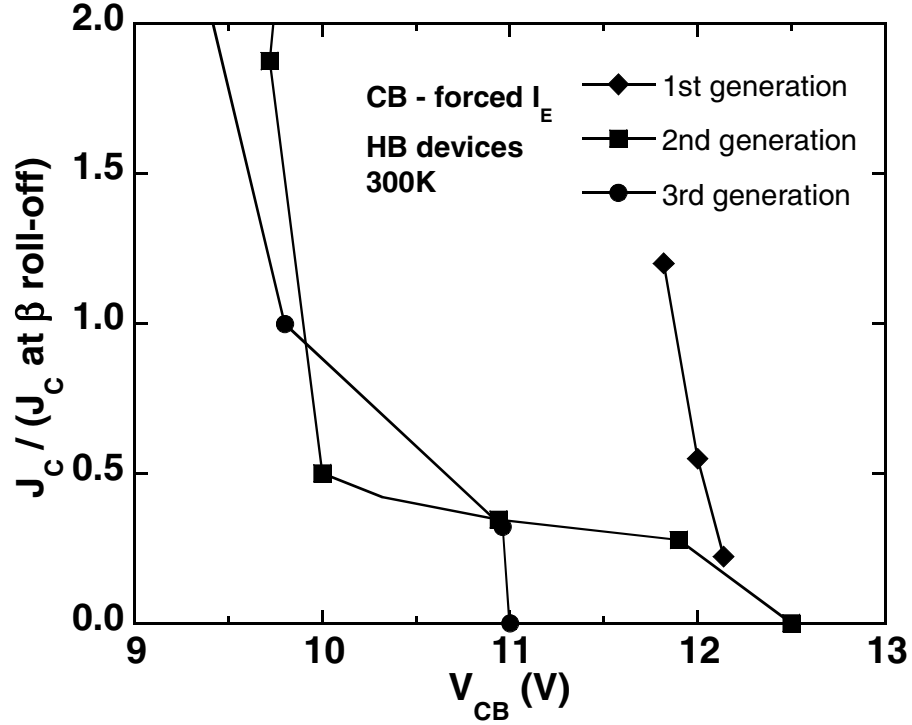
In the  $CB-I_E$  case, shown in Figure 29, the BV characteristics for all three SiGe HBT technology generations were confined to higher voltage ( $V_{CE} > 9V$ ) across bias. The



**Figure 27:** CE - forced  $I_B$  BV threshold for HB devices from three generations of SiGe HBT technology.

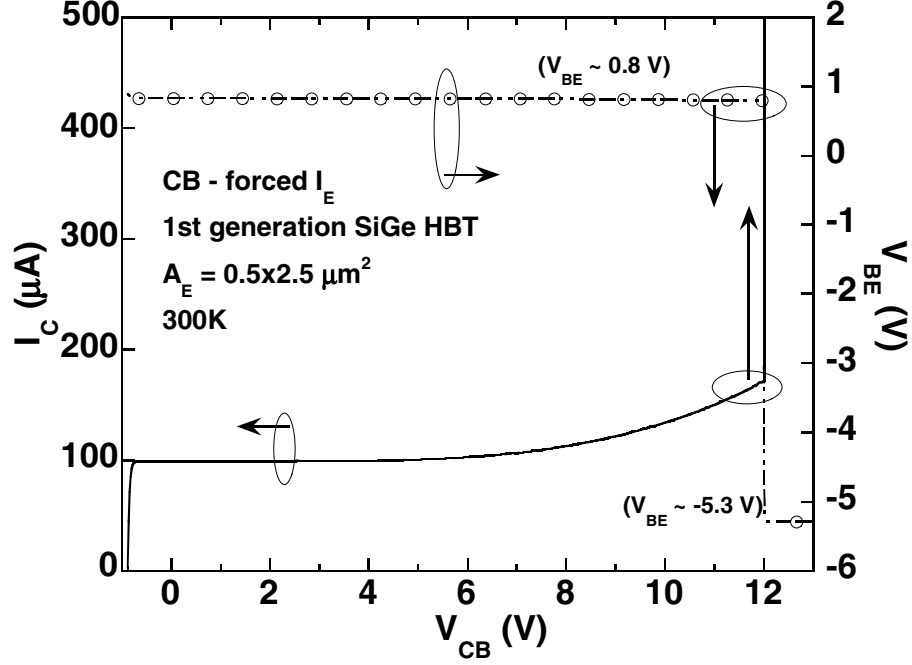


**Figure 28:** CE - forced  $V_{BE}$  BV threshold for HB devices from three generations of SiGe HBT technology.



**Figure 29:** CB - forced  $I_E$  BV threshold for HB devices from three generations of SiGe HBT technology.

first generation device showed the least  $J_C$  dependence in the bias configuration, with the stability threshold occurring at approximately 12 V across the examined injection range. However, for the first generation HB devices, operation at this stability threshold proved destructive for the device-under-test, a result not as commonly observed in the second and third generation HB devices, or in the HP devices operating in the  $CB-I_E$  configuration whatsoever. The breakdown mechanism associated with the destruction on the first generation HB devices operated in the  $CB-I_E$  mode is depicted in Figure 30. As shown, the device, biased at  $I_E = 100\mu\text{A}$ , shows normal stable operation until approximately 12 V  $V_{CB}$ , at which point the polarity of the E-B junction abruptly reverses, suddenly shifting from the normal forward bias  $V_{BE}$  ( $\approx 0.8\text{V}$ ) to a reverse bias (in excess of  $-5\text{ V}$ )  $V_{BE}$ . The reverse-biased E-B junction thus feeds the constant emitter current source with avalanche current generated in the EB-SCR. At this point the collector current is observed to increase rapidly and the device ceases to operate.



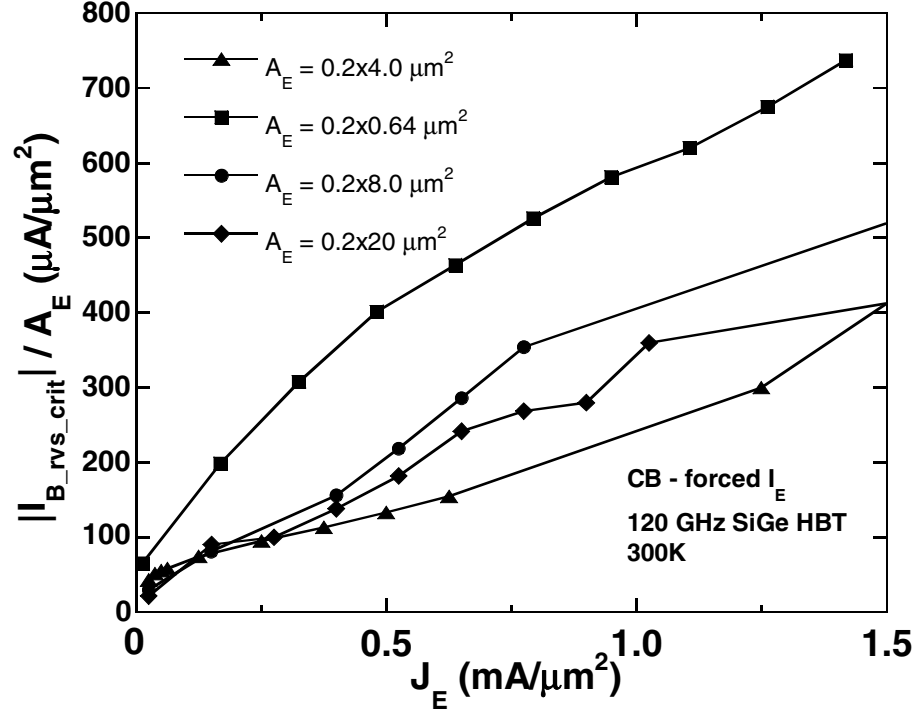
**Figure 30:**  $I_C$  and  $V_{BE}$  characteristics from a 1st generation HB SiGe HBT operating in the  $CB-I_E$  configuration.

As in the HP case discussed in the previous section, the  $CE-V_{BE}$  and  $CB-I_E$  configurations allow higher the operating voltage constraints in the HB devices than does the  $CE-I_B$  configuration, particularly at low injection. Clearly, these initial results show the SiGe HBT HB devices show interesting characteristics, both in terms of technology scaling and in device behavior within unstable operating regions at high  $V_{CB}$ , and thus warrant further study.

### 2.3.4 Geometry Dependence

Figure 31 shows the dependence of  $I_{B\_rvs\_crit}$  on  $I_E$  for different geometries of 120 GHz SiGe HBTs. The respective currents are scaled to  $A_E$  for comparison. As one might expect considering Equation (22), this plot suggests a quasi-linear relationship between  $I_{B\_rvs\_crit}$  and  $I_E$ . It is also apparent that device with the smallest  $A_E$  ( $0.2 \times 0.64 \mu\text{m}^2$ ) sustained the highest normalized  $I_{B\_rvs\_crit}$  of all the samples examined.

This dependence of the threshold  $I_{B\_rvs\_crit}$  on device geometry is reflected in a similar

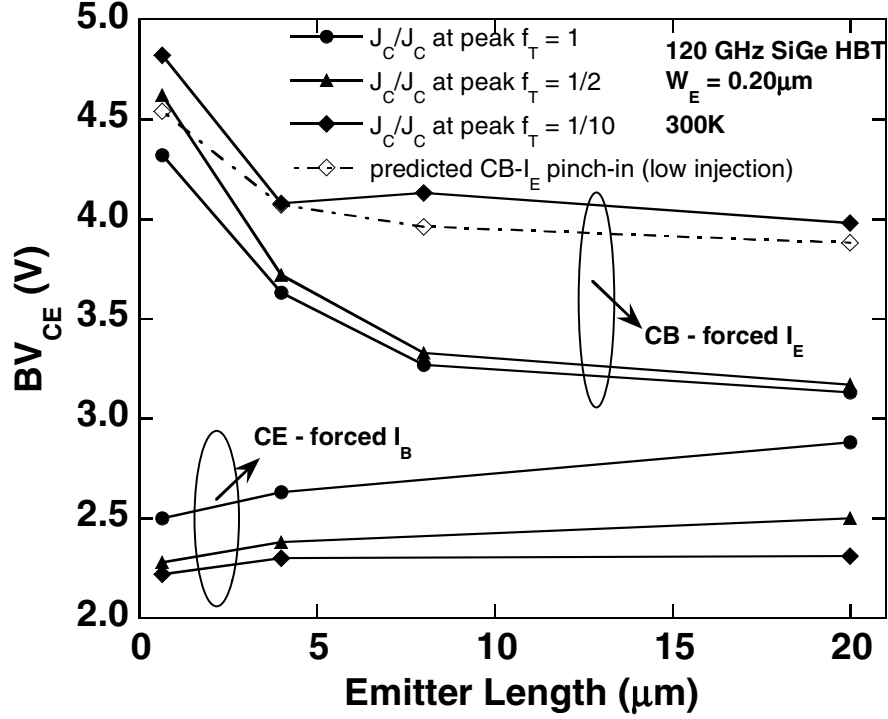


**Figure 31:** Critical reverse base current (scaled by  $A_E$ ) as a function of  $J_E$  for several geometries of 120 GHz SiGe HBTs.

geometry dependence of  $V_{CB\_crit}$ , as shown in Figure 32, which depicts BV as a function of emitter length for 120 GHz SiGe HBTs at fixed emitter width. For comparison, both  $CB-I_E$  and  $CE-I_B$  results are shown for various levels of injection. This result illustrates the potential benefit, in terms of higher stable  $V_{CE}$ , of using multiple short devices (or emitter stripes) in parallel versus using a long single emitter-stripe device for operation at a given current. BV thresholds calculated from Equations (22) and (27) for different emitter lengths (dashed line in Figure 32), assuming the same  $M - 1$  fitting parameters across geometry, show a very similar trend for low injection.

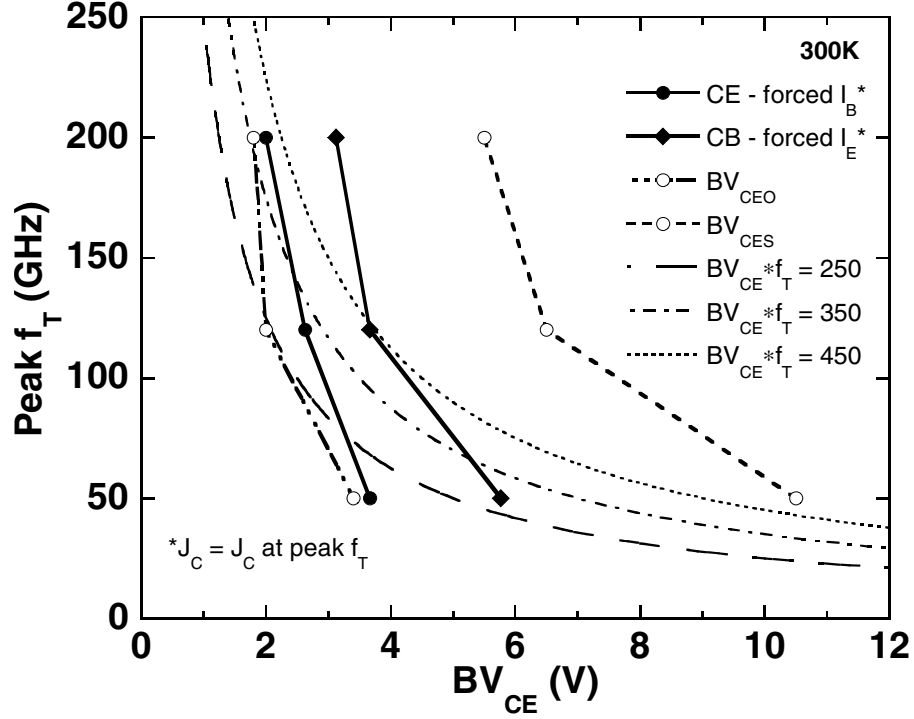
Theoretically, it stands to reason that larger devices will suffer lower values of stable maximum  $V_{CB}$  for two reasons: 1) increasing  $A_E$  tends to decrease  $r_E$ , thus reducing the debiasing effect of  $r_E I_E$  on the E-B junction, and 2) the critical voltage distribution within the neutral base is determined by the unscaled critical reverse base current ( $I_{B\_rvs\_crit}$ , as opposed to a current density value scaled to emitter area). For fixed  $J_C$ , one should then





**Figure 32:**  $BV$  vs. emitter length for  $CE-I_B$  and  $CB-I_E$  modes at low, medium, and high bias. For low injection  $CB-I_E$ , the critical  $V_{CB}$  predicted by Equation (27) is also shown.

expect a device with longer emitter length, despite the improvement (lower value) for intrinsic  $r_B$ , will exceed the critical the base current threshold at lower  $M - 1$  and thus lower  $V_{CB}$ . At the same time, increasing the emitter width not only scales the total avalanche current as before, but also degrades (raises) the intrinsic base resistance. Thus, not only is the magnitude of reverse base current at given  $J_C$  and  $V_{CB}$  increased, but the magnitude of the critical reverse base current for pinch-in is also lowered! The dependence on  $w_E$  was demonstrated experimentally on multiple devices of fixed emitter length ( $l_E = 4\mu m$ ). Increasing  $w_E$  from  $0.2\mu m$  to  $0.8\mu m$  resulted in a 1.3 V (approx. 37%) decrease in the critical  $V_{CB}$  for pinch-in at medium bias. It is important to also note that standard industry models (e.g., VBIC) will not capture this dependence of device geometry on maximum  $V_{CB}$  related to  $CB-I_E$  pinch-in instabilities, since the models do not account for lateral non-uniformities in current distribution and thus are unable to capture the pinch-in effect in its entirety.



**Figure 33:** Peak  $f_T$  vs.  $BV$  for three generations of SiGe HBT technology. Contours of constant  $BV$ - $f_T$  products are also shown.

## 2.4 Summary

In this chapter, we discussed in detail the origins of key breakdown characteristics including the "pinch-in" effect, and the role of bias configuration ( $CE$ - $I_B$ ,  $CE$ - $V_{BE}$ ,  $CB$ - $I_E$ ) on the voltage thresholds for stable operation. Practical definitions of breakdown voltage, taken from standard measurements, were adopted for each configuration to aid in determining the threshold of stable device operation between  $BV_{CEO}$  and  $BV_{CBO}$ . Three generations of SiGe HBT technology (50 GHz, 120 GHz, and 200 GHz peak  $f_T$ ) were experimentally examined for differing driving configurations and device geometries in order to extract the bias dependant breakdown voltage constraints. These characteristics may serve as practical design guidelines to ensure stable device operation for collector voltages exceeding  $BV_{CEO}$ . Also, an analytical relation between  $M - 1$ ,  $r_B$ ,  $r_E$ ,  $I_E$ , and  $V_{CB\_crit}$  was compared to experimental results.

To summarize these results, peak  $f_T$  for the three studied SiGe HBT technology generations is plotted as a function of various breakdown voltages in Figure 33. Breakdown voltage constraints were extracted at  $J_C$  which corresponds to peak  $f_T$  performance. A clear progression from lower to higher  $BV_{CE} \cdot f_T$  products is observable with each successive SiGe HBT generation, which, despite the continued compression of operating voltage limits with technology scaling, is good news in terms of the overall tradeoff between breakdown and performance.

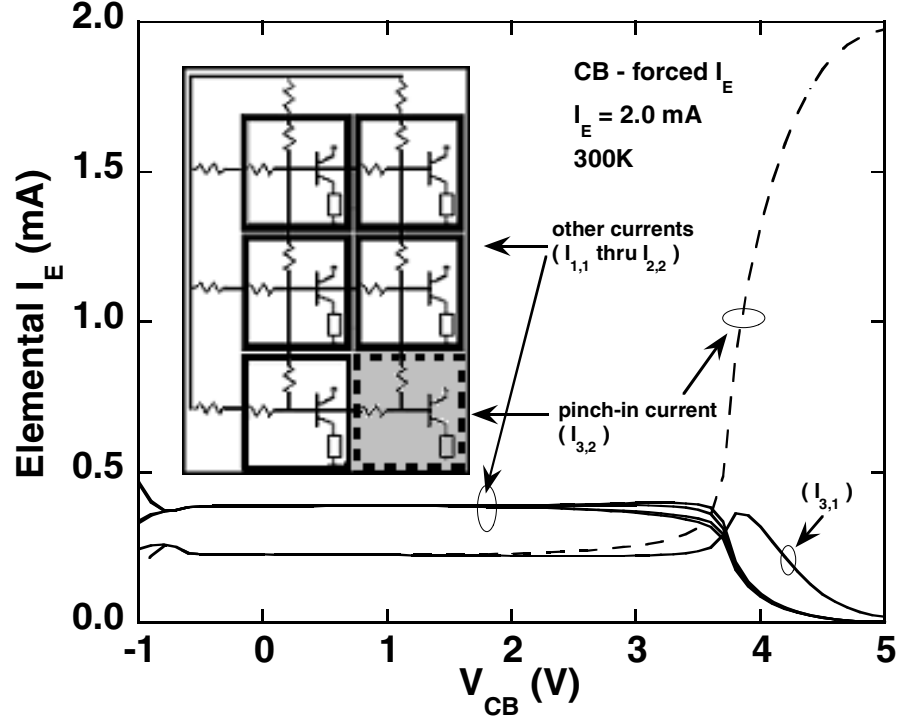
# CHAPTER III

## IMPLICATIONS OF OPERATING VOLTAGE CONSTRAINTS

### ***3.1 Introduction***

Considering the extensive complexities of breakdown voltage constraints, as evidenced in the discussions in Chapter II, it is appropriate to discuss some of the practical implications related to breakdown and safe-operating-area issues. First, modeling issues will be addressed, since standard industry models, such as VBIC, HICUM, and MEXTRAM do not capture pinch-in related instabilities. A calibrated multi-transistor quasi-3D VBIC model for the SiGe HBT will be explored, and key parameters that influence breakdown will be examined. Next, practical circuit issues related to breakdown voltage constraints will be investigated, both experimentally and using calibrated models. Emphasis will be placed on the implications related to power amplifier (PA) design, since this circuit serves as an important component for RF applications that is strongly affected by breakdown voltage constraints.

Also shown in Chapter II, pinch-in related instabilities are often suppressed at high injection levels. However, other device and circuit reliability issues such as mixed-mode stress induced hot-carrier degradation, self-heating, and thermal coupling become more important at high current. Therefore, the prior discussion of low-injection pinch-in related stable voltage constraints will be complemented by an examination of high current reliability issues in order to experimentally determine the prudent bias constraints of SOA for SiGe HBTs at all levels of injection. Finally, implications related to the dependence of thermal coupling on layout will be experimentally examined using wafer thermal imaging



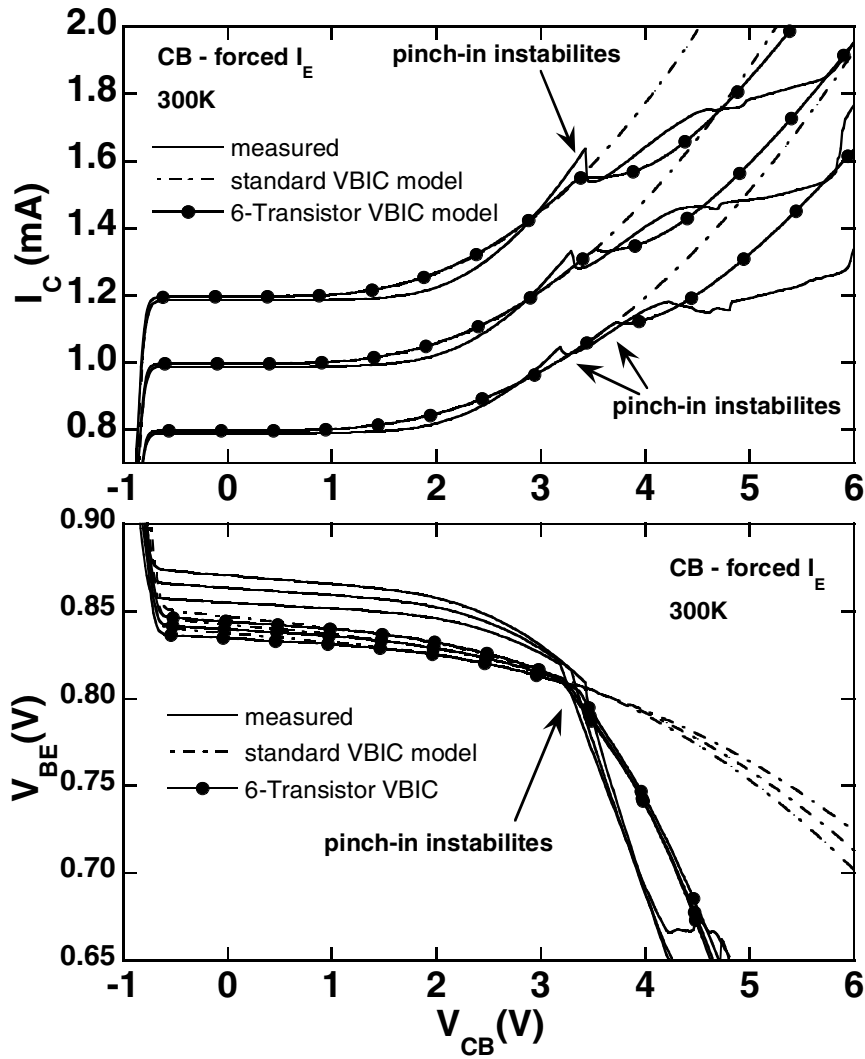
**Figure 34:** Current constriction in six-transistor VBIC model during CB - forced  $I_E$  operation.

and thermal correlation techniques.

## 3.2 Modeling of Breakdown Effects

### 3.2.1 Six-Transistor Model

As noted in the introduction, standard one-dimensional compact models will not capture all aspects of breakdown related instabilities, namely those associated with the current injection non-uniformities associated with pinch-in. Following the approach used in [31], a quasi-3-D multi-transistor compact model (see inset of Figure 34) comprised of six VBIC elements was constructed, and a resistive network interconnecting the base terminals was implemented to approximate current-crowding effects in modern SiGe HBTs. However, in contrast to the multi-transistor model demonstrated in [31], this model includes thermal coupling between elements to account for instabilities related to self-heating. The individual transistor elements are labeled by their row and column. The VBIC element in the upper left ("1,1") represents the outside corners of the device. Similarly, the VBIC element



**Figure 35:** Comparison between measurement, standard VBIC, and six-transistor VBIC models.

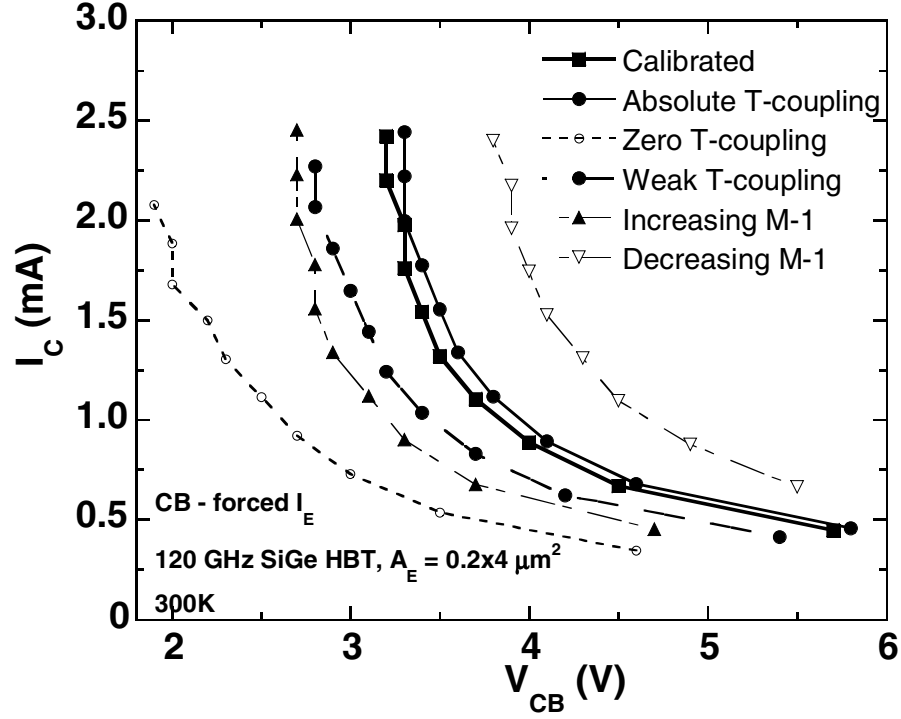
in lower right ("3,2") represents the center of the transistor. This 3-D compact model was calibrated to measured *dc* and *ac* data. Figure 34 shows the individual emitter currents of each transistor element. At the onset of pinch-in induced bias instabilities, at high  $V_{CB}$ , the transistor element at the center of the device "hogs" the entirety of the emitter current, while effectively shutting off the surrounding elements. This six-transistor VBIC model is compared to the standard VBIC model and measured *dc* data in Figure 35. Most notably, the six-transistor model captures the pinch-in instabilities (signified by a collapse in  $I_C$  at higher  $V_{CB}$ ) observed in typical *CB*- $I_E$  measurements, while the standard VBIC model does not. Although the  $I_C$  collapse in the six-transistor model is subtle compared to the

measured characteristics, a more complex distributed multi-transistor model (e.g., including a greater number of transistor elements) would demonstrate a more drastic  $I_C$  collapse during pinch-in. However, in our experience, the simpler six-transistor model serves as an adequate compromise, and remains useful for circuit design.

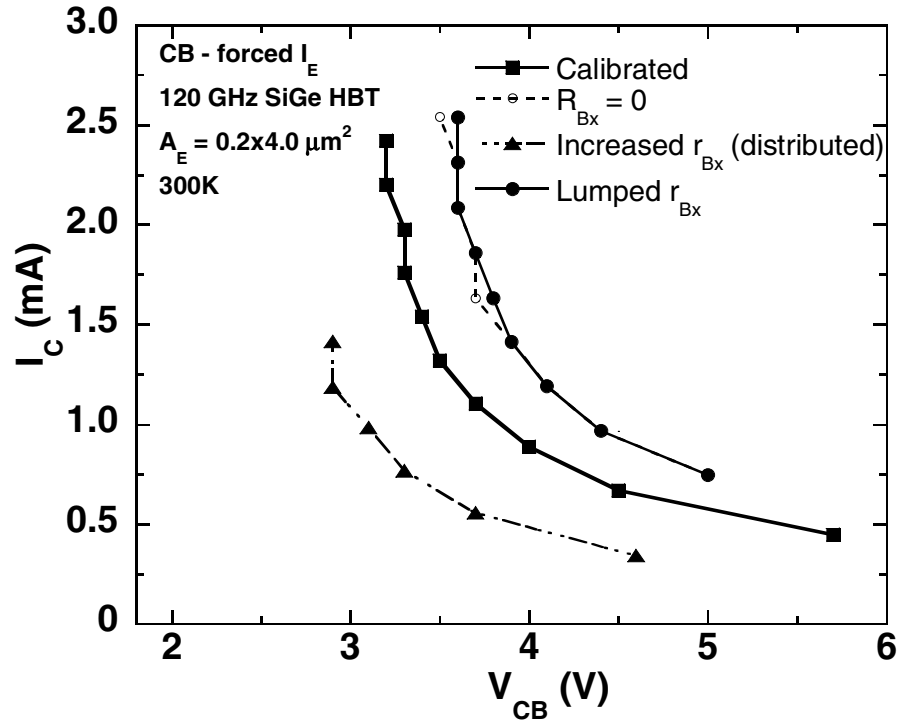
The thermal-coupled six-transistor VBIC model was calibrated according to the following assumptions: the intrinsic and extrinsic base resistances are distributed [31]; the parasitic emitter resistance consists of both a larger lumped component and a smaller distributed component; the intrinsic collector resistance is distributed; and the extrinsic collector resistance is lumped. Additionally, the temperature gradient within the active region is assumed to be small, based on lattice temperature simulations in MEDICI. Therefore, the temperature differential along  $w_E$  ( $= 0.2 \mu\text{m}$ ) is assumed to be insignificant, and the temperature differential along  $l_E$  ( $= 4.0 \mu\text{m}$ ) is small, requiring strong thermal coupling between individual elements. The temperature dependence of  $M - 1$  is not considered. Due to this strong thermal coupling among the individual transistor elements, the difference between the BV characteristic, with and without self-heating, is very small. However, even with self-heating turned off, a sharp decrease in  $V_{BE}$  is observed at  $V_{CB\_crit}$  due to the abrupt increase in the base parasitic resistance and thus the intrinsic base potential for the pinched-in active region. As expected, examining the intrinsic E-B junction potential (approximated by the potential difference between the base and emitter terminals of the "center" VBIC element) with self-heating turned off in the model shows nearly constant  $V_{B'E'}$  across  $V_{CB}$ .

### 3.2.2 Model Perturbation

Keeping in mind the simplifications and limitations of the six-transistor model, it may serve as a useful tool to gain additional insight into the nature of various internal device interactions and three dimensional effects related to pinch-in. Starting with the calibrated, thermal coupled six-transistor VBIC model, certain model parameters were systematically



**Figure 36:** Modeled BV thresholds, with modifications to thermal coupling and avalanche multiplication factors in six-transistor model.



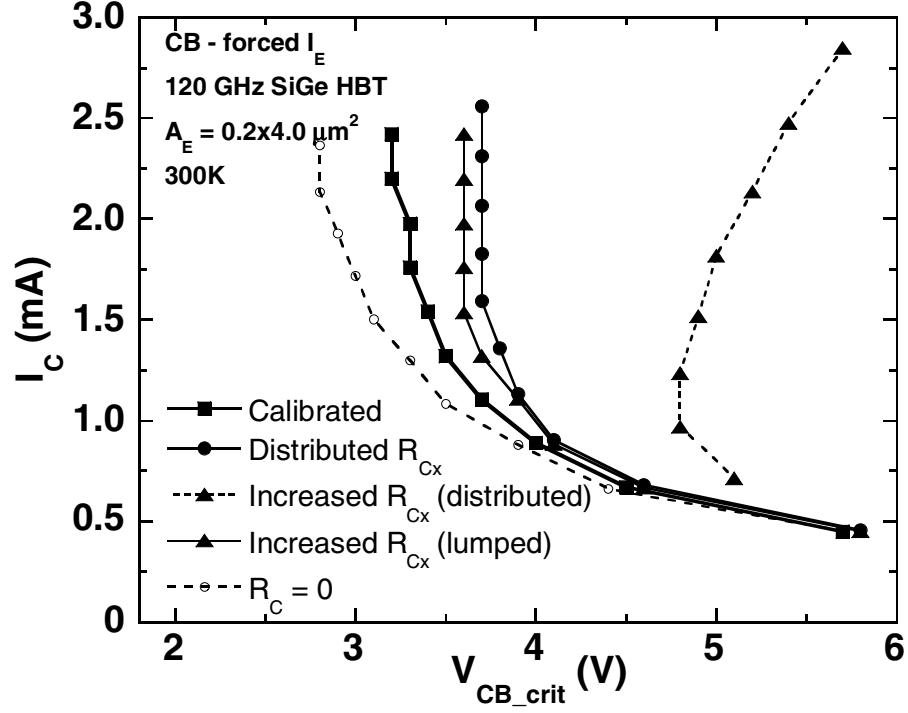
**Figure 37:** Modeled BV thresholds, with modifications to extrinsic base resistance in six-transistor model.



modified and exaggerated to demonstrate and compare their respective influence on current non-uniformities and pinch-in instabilities within the model.

The effects of inter-device thermal coupling on the stability threshold  $V_{CB\_crit}$  are shown in Figure 36. For the calibrated model, strong thermal coupling within the device was assumed based on MEDICI simulation results and observations (see Section 3.6) showing relatively small thermal gradients within the active region of a device. In the cases of weak or no thermal coupling, the resulting strong temperature gradient across the individual model elements creates a strong non-equilibrium that favors current flow in the center elements. With this additional positive feedback for central current crowding, the stable threshold for  $V_{CB}$  is significantly reduced. For absolute thermal coupling, thermal equilibrium is maintained over all elements and this positive feedback mechanism is removed entirely, and (neglecting the temperature dependence of  $M - 1$ ) the stable voltage limits are no longer a function of self-heating or temperature in general. The influence of the avalanche multiplication factor ( $M - 1$ ) is also shown in Figure 36. Clearly, modifications to  $M - 1$  (for constant  $I_{B\_rvs\_crit}$ ) show the same inverse relationship to  $V_{CB\_crit}$  that one would expect in examining Equations (26) and (27) from Chapter II. Changes to either thermal coupling or  $M - 1$  demonstrate considerable influence at both low and high current.

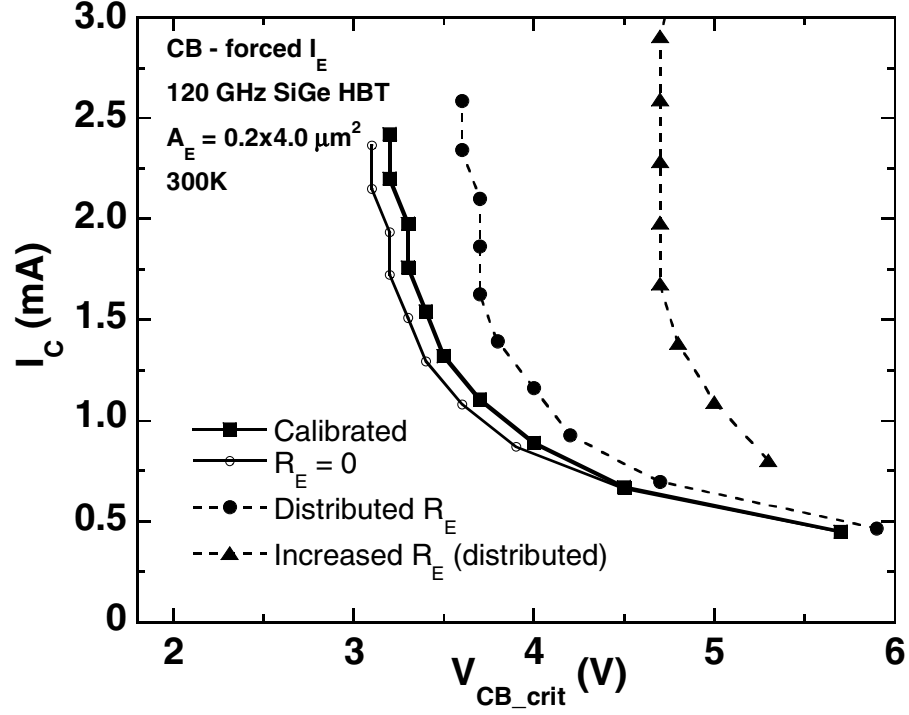
The extrinsic base resistance ( $r_{Bx}$ ), examined in Figure 37, plays a strong role in the onset of current non-uniformities and the threshold of device stability. When  $r_{Bx}$  is treated as a distributed parameter (as does the calibrated six-transistor model), it promotes non-uniformities in junction potential within the active device. Figure 37 shows the change in the breakdown characteristics when this distributed resistance is increased by 4x (strong degradation of the stability threshold at both low and high injection), and the effect of removing this resistance entirely (the opposite effect). Treating  $r_{Bx}$  as a lumped resistance is shown to be very similar in effect to setting its value to zero, since overall equilibrium is maintained within the device. Likewise, increasing the value of the lumped  $r_{Bx}$  shows no effect on  $V_{CB\_crit}$  since this modification affects all elements equally.



**Figure 38:** Modeled BV thresholds, with modifications to thermal coupling and avalanche multiplication factors in six-transistor model.

Figure 38 shows the effects of the parasitic collector resistance on the breakdown performance of the six-transistor model. Clearly, increasing  $r_{Cx}$  allows higher sustainable  $V_{CB\_crit}$ , because the voltage drop across  $r_C$  decreases the field across the CB junction, thus decreasing the avalanche and reverse base current. While this effect is strongest when  $r_{Cx}$  is treated as a distributed resistance, similar behavior is still observed when  $r_{Cx}$  is lumped due to an overall decrease of avalanche current across all elements. Neglecting the collector resistance (e.g., setting  $r_{Cx}$  and  $r_{Ci}$  to zero) has the opposite effect, resulting in a reduction of  $V_{CB\_crit}$ . For the calibrated model, the parasitic collector resistance is treated as a larger lumped component in series with a smaller distributed component. From these simulation results, it is clear that the influence of  $r_{Cx}$  on  $V_{CB\_crit}$  is much stronger at high current than at low current.

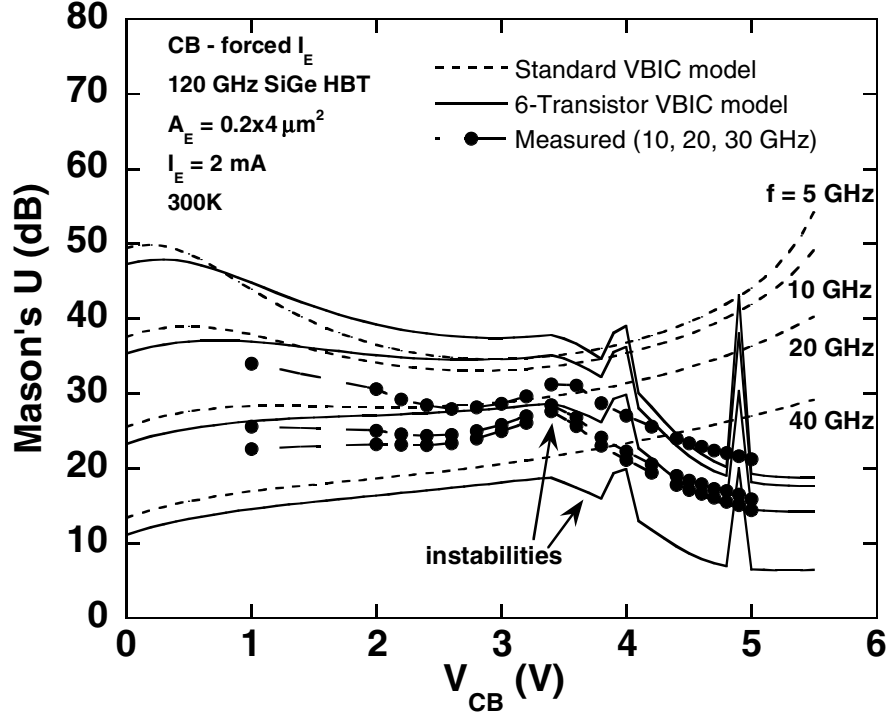
As shown in Figure 39, the emitter resistance also provides negative feedback with respect to pinch-in, but only to the degree that  $r_E$  is distributed among elements. Treating  $r_E$



**Figure 39:** Modeled BV thresholds, with modifications to emitter resistance in six-transistor model.

as a fully lumped element is, in terms of  $V_{CB\_crit}$ , equivalent to setting its value to zero, and increasing the lumped value of  $r_E$  has no influence whatsoever on  $V_{CB\_crit}$ . The calibrated six-transistor model  $r_E$  is composed of a larger lumped component in series with a smaller distributed component.

Overall, these results illustrate that the stabilizing influence of the parasitic emitter and collector resistances is far more significant at high current than at low current, while the destabilizing effects of  $M - 1$  and the parasitic base resistance remain a strong influence even at low injection. These modeled results are consistent with the qualitative and experimental observations from Chapter II, and provide additional insight into the role of various physical device parameters on operating voltage constraints in SiGe HBTs.



**Figure 40:** Mason's  $U$  vs.  $V_{CB}$  extracted at various frequencies for the standard VBIC and six-transistor VBIC models.

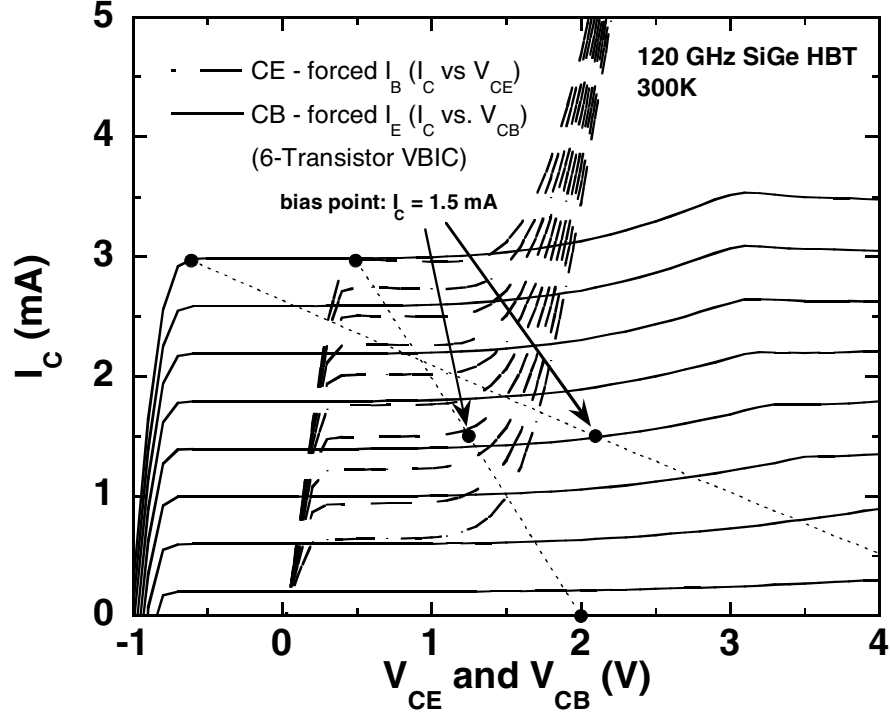
### 3.3 Circuit Implications

#### 3.3.1 Experiment

To investigate the implications of pinch-in related instabilities on small-signal performance, a common-base *ac* test structure was fabricated in a 120 GHz SiGe technology, and its 2-port S-parameters were measured on an HP 8510C 50 GHz Network Analyzer at 50  $\Omega$  system impedance over a range of 1 to 30GHz, at fixed emitter current and various  $V_{CB}$ . Mason's Unilateral Gain was then extracted from these measurements. In addition, Mason's  $U$  was extracted in a similar fashion for both the standard VBIC model and the quasi-3-D six-transistor model biased in the  $CB$ - $I_E$  configuration.

#### 3.3.2 Results and Discussion

As shown in Figure 40, which depicts Mason's  $U$  plotted with respect to  $V_{CB}$  for the measured and modeled cases, the behavior of the two models is similar until a  $V_{CB}$  of approximately 3.5 V, at which point the six-transistor model encounters *ac* instabilities and gain

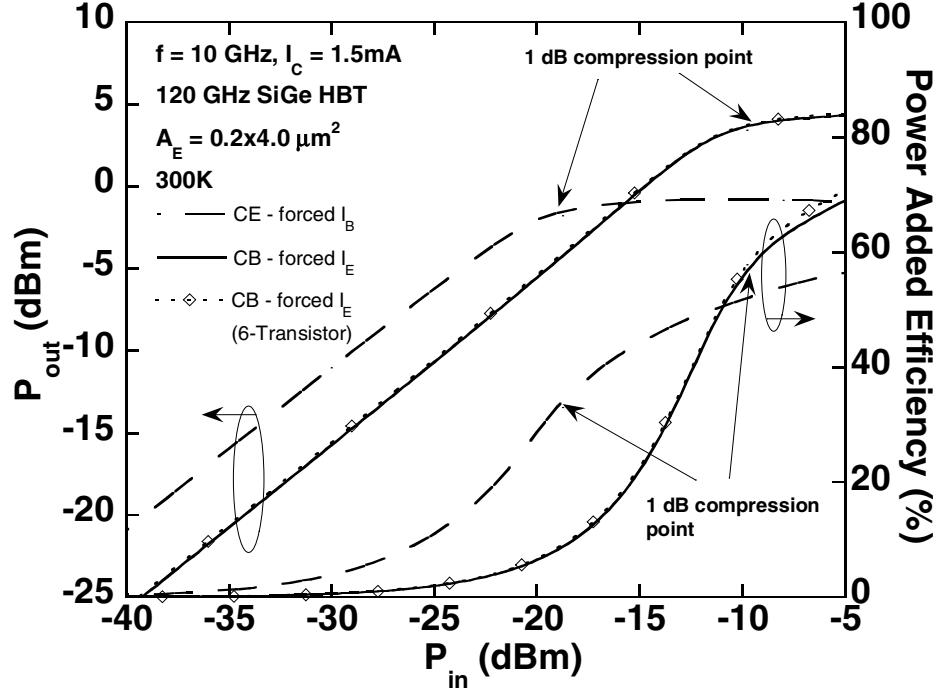


**Figure 41:** Modeled *dc* characteristics and *dc* bias points associated with class A large signal CE and CB operation.

degradation, similar to the measured behavior. It is important to note that these *ac* instabilities coincide with the *dc* pinch-in instabilities at the same current level. This result illustrates important small signal implications (not captured by standard models), in terms of frequency response, *ac* gain, linearity, and RF impedance matching, of attempting to bias a transistor in a region of *dc* breakdown instabilities. Keeping in mind the limitations of the six-transistor model in reliably predicting device behavior in the region of pinch-in instabilities, the similarities between the six-transistor model and the measured results are quite remarkable.

### 3.3.3 Further Circuit Simulations

SiGe HBTs have demonstrated promising results in the realm of power amplifier (PA) applications [30], [32], [33], [34], and a wide range of performance optimization approaches are available to the circuit designer, including device geometry and layout, collector doping, bias current, and, as shall be considered here, transistor bias configuration. Using the



**Figure 42:** Modeled output power and PAE vs. input power for CE and CB class A operation.

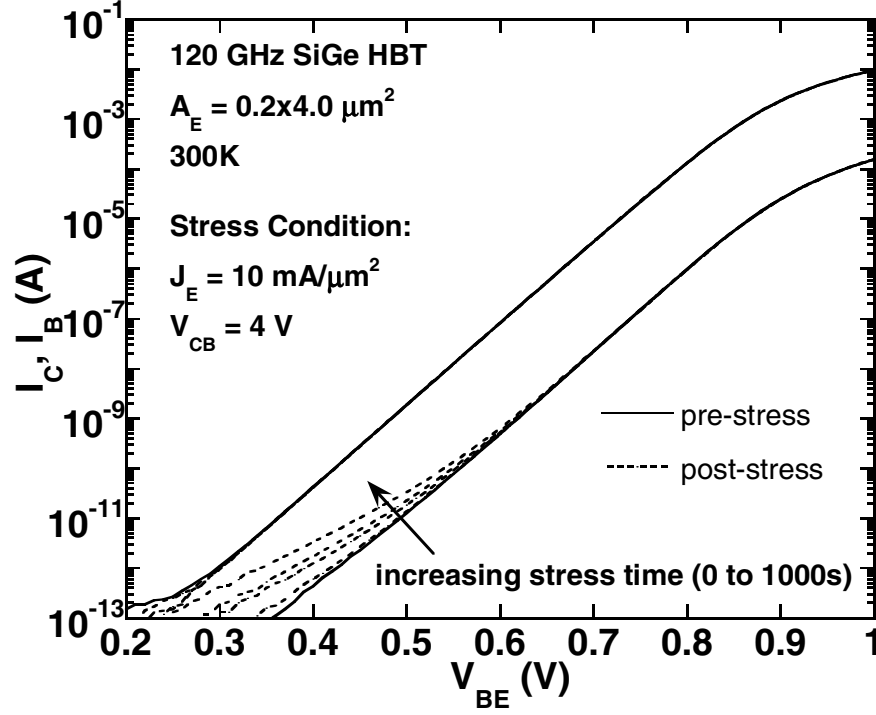
calibrated six-transistor VBIC model, class A output power at 10 GHz was compared for two bias modes:  $CE-I_B$  and  $CB-I_E$ . The  $dc$  characteristics for the two bias modes, and the corresponding operating points (both at 1.5 mA to ensure a fair comparison) are displayed in Figure 41. Since the  $CB-I_E$  configuration facilitates higher maximum collector voltage, one should expect higher output power and efficiency for an amplifier stage in this bias mode.

Both amplifier stages were conjugate-matched independently and operated at 1.5 mA  $I_C$ . For the  $CE-I_B$  bias mode, the  $dc$  collector voltage bias point ( $V_{CE} = 1.25$  V) was examined because it provided the maximum output power and PAE at the 1 dB compression point for this drive configuration and current. Operating in  $CE-I_B$  mode at higher values of  $V_{CE}$  (each independently matched) showed rapid degradation of the simulated power gain, output power, and PAE (examined at the 1 dB compression point) as  $V_{CE}$  approached  $BV_{CEO}$  (approximately 2 V).

The resulting simulated output power and PAE curves for both configurations are plotted versus input power in Figure 42. For low input power, the output power and PAE for the  $CE-I_B$  configuration is noticeably higher than that of the  $CB-I_E$  configuration. However, the  $CE-I_B$  PA reaches the 1 dB compression point at considerably lower input power than the  $CB-I_E$  PA. As a result, at the 1 dB compression point PAE increased from approximately 33% to 58% and a 5.5 dBm improvement in output power was observed for the common-base amplifier stage, with a moderate increase in  $dc$  collector voltage ( $V_{CB} = 2.1$  V). Clearly, utilizing the larger voltage headroom of alternative bias configurations offers considerable appeal for improvement in circuit performance, and if well-modeled, can be exploited by circuit designers.

### 3.4 *Device Reliability*

As indicated in Chapter II, the instabilities associated with pinch-in effects are often suppressed at high current. However, other reliability concerns, such as avalanche-induced hot carrier degradation, must be addressed for high current operation [4], [35]. Of particular interest are "mixed-mode" reliability issues, which occur under conditions of simultaneous application of high  $J_C$  and high  $V_{CB}$ . Mixed-mode stress degradation is exhibited in a decrease in  $\beta$  due to a strong increase in the base current, or " $I_B$  leakage."  $I_B$  increases following mixed-mode stress due to the creation of carrier trap states within the energy bandgap which increase the likelihood of carrier recombination, and thus annihilation of an EHP, which results in an increase in the total base current. Results in [35] and [36] suggest that the trap states are spatially located along the edge of shallow trench oxide and at the emitter-base spacer, and result from an increase in high energy carrier density in these regions at high  $V_{CB}$ .



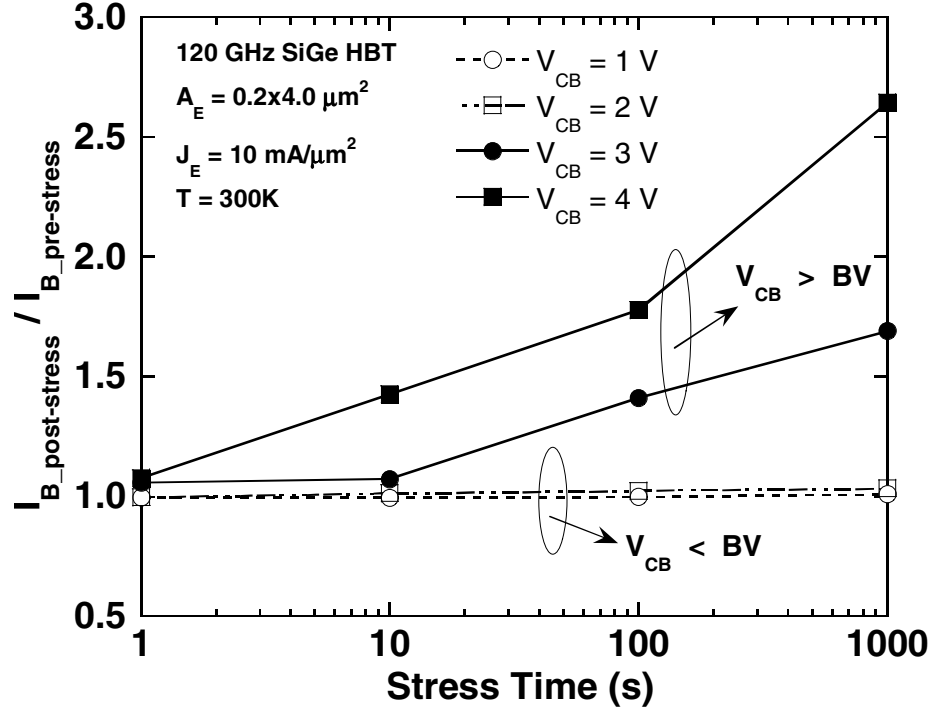
**Figure 43:** Forward Gummel characteristic pre- and post- stressing at  $J_E = 10 \text{ mA}/\mu\text{m}^2$  and  $V_{CB} = 4 \text{ V}$  for various stress times.

### 3.4.1 Experiment

To characterize the link between low injection SOA and high injection device stressing and reliability, 120 GHz SiGe HBTs were stressed at constant emitter current for various times (up to 1000 sec cumulative stress) at various collector voltages, below and above the  $CB$ - $I_E$  BV threshold (as defined and characterized in Chapter II). At various time intervals (1s, 10s, 100s, and 1000s) measurements of the forward and inverse Gummel characteristics were taken, and stressing was immediately resumed. Both the stressing and measurements were performed at  $T = 300\text{K}$  on a Agilent 4155 Semiconductor Parameter Analyzer.

With respect to conventional "mixed-mode" stressing, the stress current chosen in this study ( $J_C = 10 \text{ mA}/\mu\text{m}^2$ ) is relatively low compared to other published values ([4], [35], [36]), in order to investigate stress-induced degradation in a practical operating space easily comparable to the I-V characteristics and BV thresholds depicted in Figures 18 and 24.



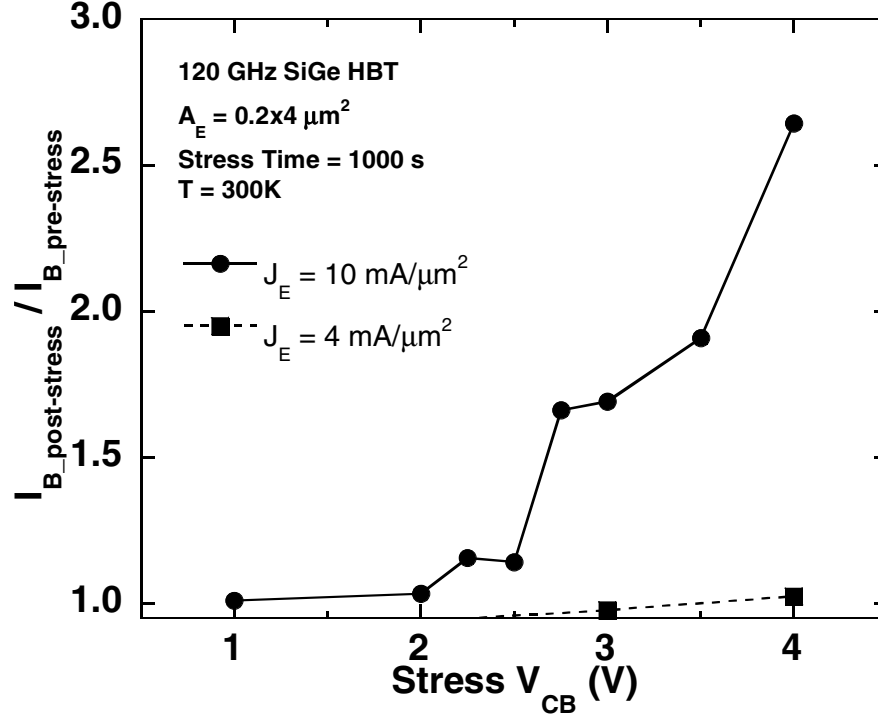


**Figure 44:** Base current degradation vs. time for various levels of stress  $V_{CB}$ .

### 3.4.2 Results and Discussion

Figure 43 shows the pre and post stress Gummel characteristics for the device stressed at  $V_{CB} = 4 \text{ V}$ . As expected, the magnitude of  $I_B$  leakage was observed to increase with increasing stress time. As a result of the relatively low stressing current, the magnitude of base current degradation ( $I_{B\_post}/I_{B\_pre}$ ) was found to be relatively small (2x to 3x as opposed to 10x and above), although consistent and non-negligible. Conversely, the inverse mode Gummel did not show significant  $I_B$  degradation for any  $V_{CB}$ , suggesting that the stress current was too low to induce considerable damage at the shallow trench oxide interface.

Figure 44 shows  $I_{B\_post}/I_{B\_pre}$  as a function of stress time and  $V_{CB}$ . The magnitude of base current degradation was determined from the forward Gummel characteristic at  $V_{BE} = 0.5 \text{ V}$  ( $V_{CB} = 0 \text{ V}$ ). As indicated in Figure 44, biasing at  $V_{CB}$  above the specified BV threshold (approx.  $V_{CB} = 3 \text{ V}$  for this device, as indicated in Figures 18 and 24) results in considerably greater amount of hot-carrier degradation for a given stress current and

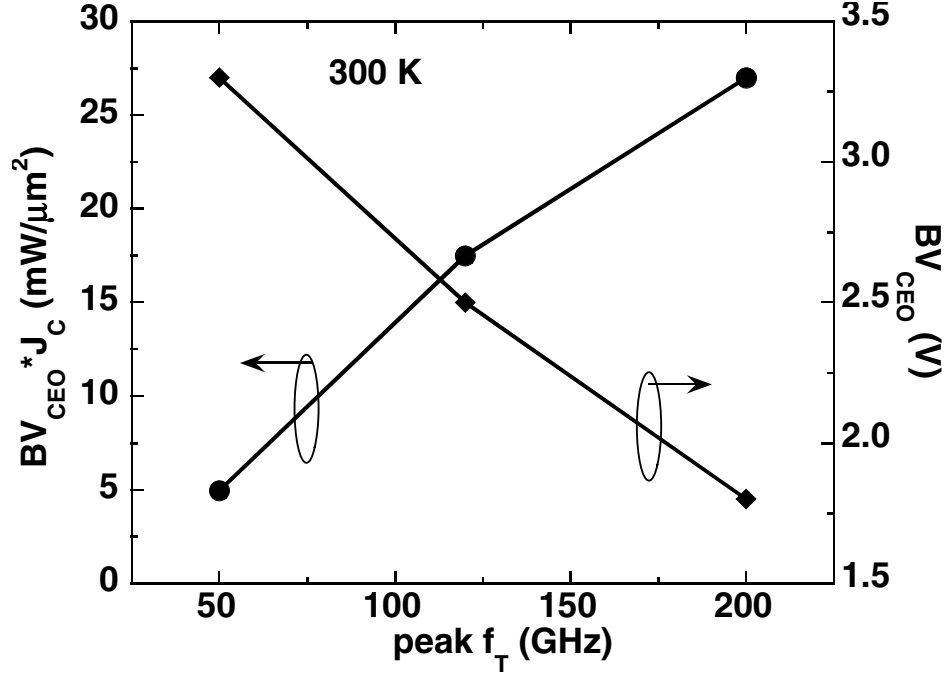


**Figure 45:** Base current degradation as a function of stress  $V_{CB}$ .

stress time. This trend is reflected in Figure 45, which shows the significant increase in  $I_{B\_post}/I_{B\_pre}$  with  $V_{CB}$  at 1000s stressing. Figure 45 also shows that for lower stressing current ( $J_C = 4 \text{ mA}/\mu\text{m}^2$ ), the magnitude of apparent base current degradation is not significant, even at  $V_{CB} = 4 \text{ V}$ , consistent with previously published results [4], [35], [36]).

### 3.5 Self-Heating

Despite the advantageous thermal properties of bulk silicon compared to other technologies (SOI, III-V), thermal issues represent an emerging concern in SiGe HBT BiCMOS technology, particularly with technology scaling as the frequency response of SiGe HBTs surpasses the 350 GHz peak  $f_T$  mark [37]. Even as the breakdown voltage decreases with increases in transistor performance, the higher current density required to achieve peak performance results in an overall increase in the  $BV_{CEO} \cdot J_C$  product, as shown in Figure 46. Operating at higher power density results in an increase in device temperature due to the thermal resistance ( $R_{th}$ ) and self-heating ( $\Delta T = P/R_{th}$ ), which can have a significant

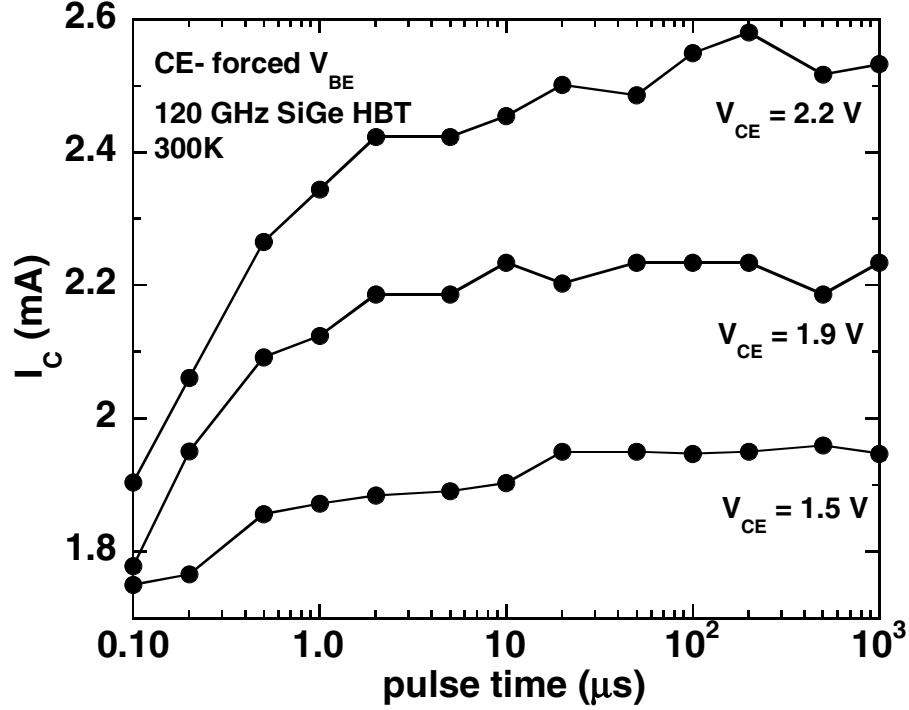


**Figure 46:** Breakdown voltage, current density product vs. peak  $f_T$  in various SiGe device technologies.

impact critical transistor parameters. In this section we will examine the influence of self-heating on output conductance for devices operating in the  $CE-V_{BE}$  configuration using  $dc$  and pulsed measurement techniques.

### 3.5.1 Experiment

To study the effects of self-heating on SiGe HBTs, test structures were fabricated in 120 GHz and 200 GHz SiGe HBT technologies. Precision pulsed-mode and  $dc$  measurements were performed on wafer using the Dynamic I-V Analyzer (DIVA) measurement system. In addition to performing  $dc$  characterization, the DIVA system allows short signal pulses (down to 100 ns) to be performed at specified intervals from a specified  $dc$  operating point (or pulse origin). Thus, self-heating effects can be minimized during I-V measurements, assuming sufficiently short signal pulse length, sufficiently wide pulse interval, and sufficiently low  $dc$  pulse origin.

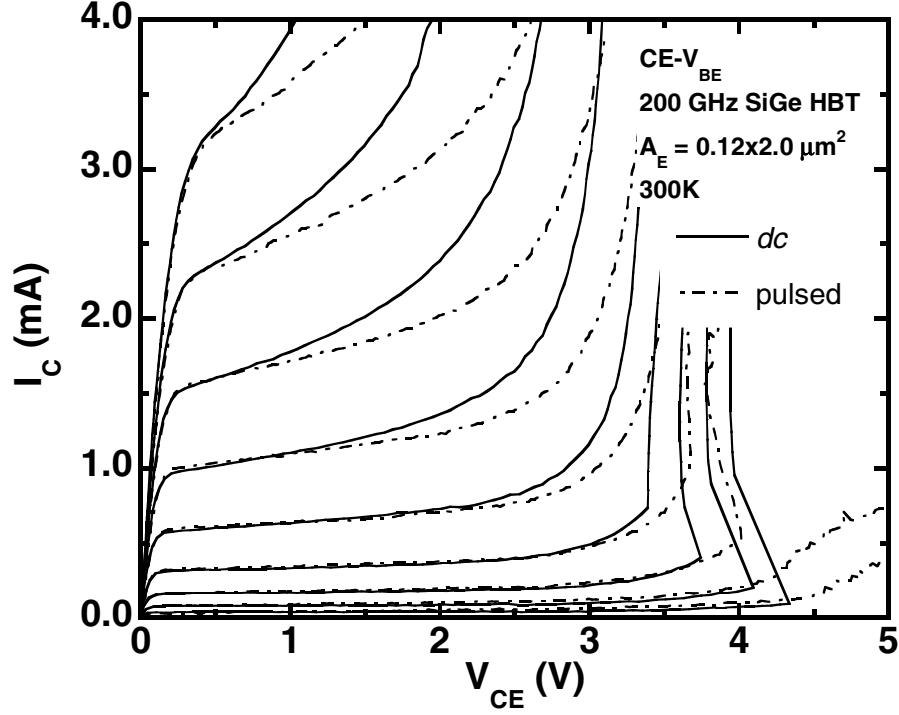


**Figure 47:**  $I_C$  at fixed  $V_{BE}$  (0.84 V) and  $V_{CE}$  as a function of time.

The DIVA system uses a two-port test network, thus CE *ac* test structures were examined.  $CE$ - $V_{BE}$  output characteristics were measured using *dc* and pulsed-mode stimulation, and the results were compared to determine the influence of self-heating. The pulse length chosen was 100 ns with 1 ms spacing between subsequent pulses. The *dc* pulse origin was chosen to be  $V_{BE} = 0.84$  V,  $V_{CB} = 1$  V. In addition,  $CE$ - $V_{BE}$  output characteristics were measured on *dc* test structures using an Agilent 4155 Semiconductor Parameter Analyzer. All measurements were performed at room temperature (300 K).

### 3.5.2 Results and Discussion

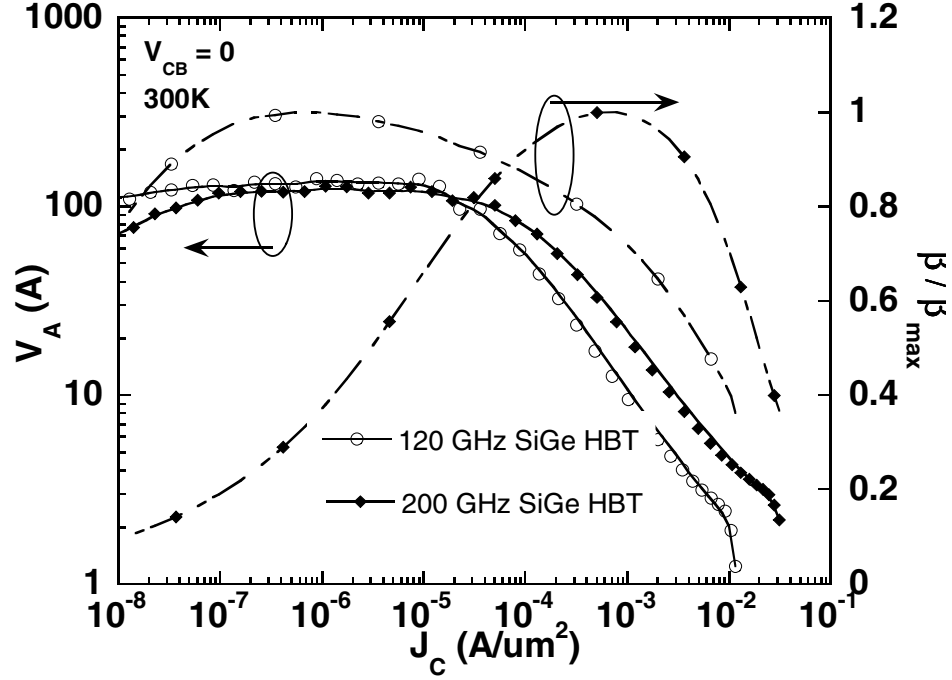
To demonstrate the transient behavior of self-heating effects, the collector current of a 120 GHz SiGe HBT biased at constant  $V_{CB}$  and  $V_{BE}$  is plotted against time in Figure 47. Results are shown from 0.1  $\mu$ s, which represents the shortest pulse time attainable on the DIVA system, to 1 s, assumed to represent *dc* operation. Even with the bias point fixed at constant  $V_{CB}$  and  $V_{BE}$ , a clear increase in  $I_C$  is observed as a function of time due to



**Figure 48:** Comparison between *dc* and pulsed measurements during CE - forced  $V_{BE}$  operation for a 200 GHz SiGe HBT.

self-heating. As one should expect, the bias point with the highest power ( $V_{CE} = 2.2$  V) induces the greatest change in  $I_C$  (approximately 32 %). This result implies a considerable difference between the self-heating effects of *dc*-bias power and high frequency power.

The  $CE-V_{BE}$  output characteristics from the DIVA *dc* and pulsed-mode measurements are presented in Figure 48. At high injection, where self-heating effects are most evident, comparing the *dc* and pulsed results for this 200 GHz SiGe HBT underscores the strong degradation (increase) of output conductance (and thus reduction in  $V_A$ ) in the *dc* case due to self-heating within the device. These results are typical for all devices examined. The effects self-heating become apparent in Figure 48 at  $J_C$  of approximately  $5 \text{ mA}/\mu\text{m}^2$ , well below  $J_C$  at peak  $f_T$  (around  $15 \text{ mA}/\mu\text{m}^2$ ) for this technology. While not emphasized in Chapter II, the significant reduction of the  $CE-V_{BE}$  BV characteristics at high  $J_C$  (recorded in Figure 23 in Chapter II) are in fact largely due to the self-heating-induced increase in the  $J_C$  on  $V_{CB}$  slope. These results should catch the attention of any circuit designer seeking



**Figure 49:** Current gain and Early voltage characteristics versus  $J_C$  during CE - forced  $V_{BE}$  operation for 120 and 200 GHz SiGe HBTs.

peak  $f_T$  device performance.

The differences between *dc* and pulsed  $CE$ - $V_{BE}$  measurements were not exclusively confined to high injection. For low injection, Figure 48 shows a substantial suppression of the collector current fly-back characteristics under pulsed mode operation at high  $V_{CB}$ . Clearly, the reduction of self-heating plays a significant role in the electro-thermal stability for devices that operate at high  $V_{CB}$  and low  $J_C$ . This result is good news in terms of stability for high frequency transistor stages with large load swings that may approach  $V_{CB\_crit}$  at low current.

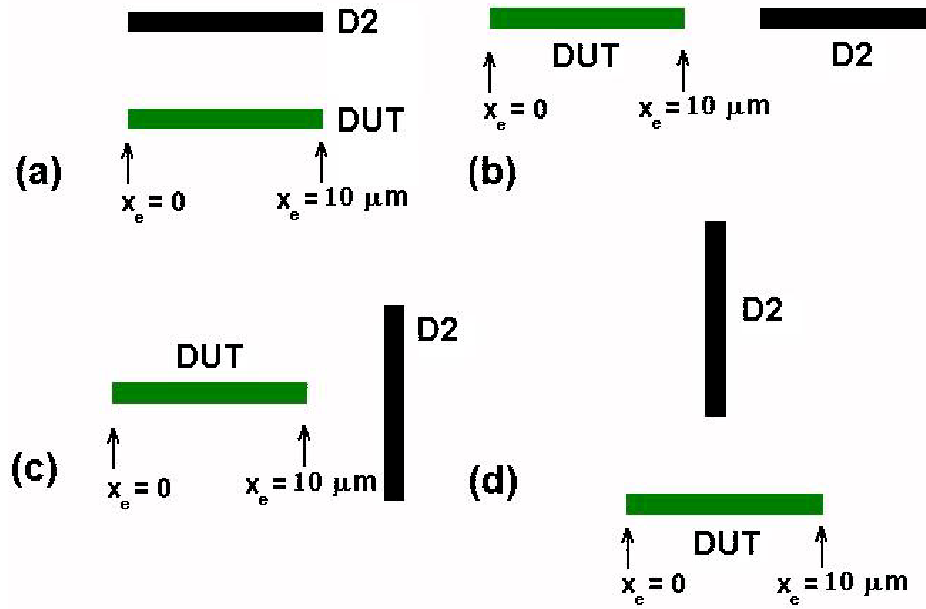
In Figure 49,  $V_A$  and  $\beta$  (normalized to peak  $\beta$ ) were extracted across bias for the 120 and 200 GHz SiGe HBTs from *dc* measurements using the Agilent 4155. These results are similar to those published in [38], in which the authors additionally used a novel forward-biased collector-substrate junction thermometer technique to verify the extent of self-heating within the device. The reduction of  $V_A$  with increasing current is apparent, and

very similar in nature between the 120 and 200 GHz SiGe HBT generations. However, the respective current gain characteristics reveal an important distinction: the  $V_A$  characteristic of the 200 GHz SiGe HBT shows strong degradation at  $J_C$  well below the onset of strong  $\beta$  degradation. Clearly, self-heating effects will become increasingly serious with technology scaling.

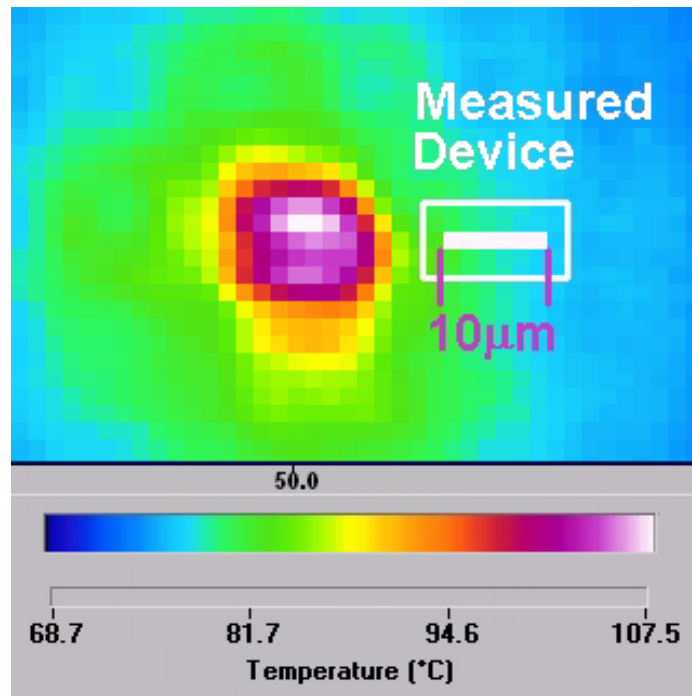
### ***3.6 Thermal Coupling***

The increasing operational temperatures resulting from self-heating in SiGe HBTs, as discussed in Section 3.5, can produce similar inter-device thermal degradation effects as those seen in III-V and Silicon-on-Insulator (SOI) technologies, for which both intra- and inter-device electro-thermal feedback has been extensively studied [39], [40], [41], [42]. Due to the relatively high thermal conductivity of silicon (compared to III-V and SOI), most thermal interaction studies in SiGe HBTs have been limited to multi-finger single transistors [43]. However, minimum spacing rules used in current IC designs allow for spacings between devices which can be smaller than the effective length of the device itself, which may compromise the assumption that the mutual thermal coupling factor ( $R_{21}$ ) acts as a lumped element, potentially introducing inherent modeling "issues." Specifically, the higher thermal conductivity of Si can produce large thermal gradients across the active regions of transistors placed within close proximity of one another.

One-dimensional thermal layout techniques related to power amplifier design in SiGe, were explored in [44]. However, for the current study, the thermal effects of minimum-spaced transistors are analyzed for various two-dimensional layout orientations. Through the use of infrared photography, we are able to measure the thermal distribution across one device that results from the high power operation of another adjacent device. From these results, we demonstrate varying temperature gradients across active fingers as a function of layout orientation, correlate this to an effective operating temperature, and discuss the effects that this causes on performance of measured SiGe HBT parameters [6].



**Figure 50:** Four measured transistor orientations, with the measured device shown in green and heat source device shown in black. In subsequent plots, these orientations will be referred to as a) | |, b) — —, c) — |, d) | —, where the left device is the measured one.



**Figure 51:** Infrared picture of the heat source transistor and the resultant thermal distribution that is seen across the measured device.



### 3.6.1 Theory

The base-emitter voltage temperature coefficient is defined as

$$\varphi = \left. \frac{\partial V_{BE}}{\partial T} \right|_{I_C} \quad (30)$$

and is furthermore shown to be a temperature independent constant for a given value of  $I_C$ , as is shown in [45]. A change in the base-emitter voltage with respect to ambient voltage  $V_{BE0}$  (which corresponds to the ambient temperature  $T_0$ ) at fixed  $I_C$ , can be used to calculate a corresponding change in temperature and, ultimately, the operating temperature of a given device, according to

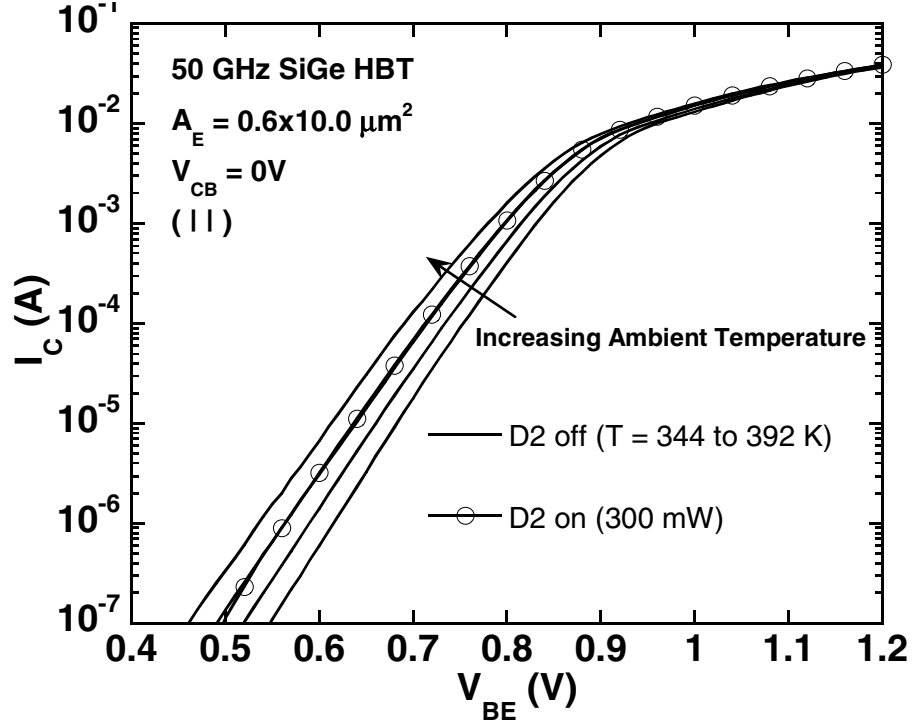
$$T_1 = -\frac{V_{EB1} - V_{EB0}}{\varphi} + T_0 \quad (31)$$

### 3.6.2 Experiment

Using a commercially-available 50 GHz SiGe technology,  $0.6 \times 10 \mu\text{m}^2$  single emitter stripe devices were fabricated in a common-base configuration in the four orientations shown in Figure 50. In the cases a) and b), device pairs were spaced with both  $4 \mu\text{m}$  and  $10 \mu\text{m}$  separation. For the cases of c) and d), only the  $10 \mu\text{m}$  separation was used.

Thermal images were obtained of the devices under operation through use of a Quantum Instruments Infrascopes II thermal imaging camera. An example image is shown in Figure 51. This camera has a spatial resolution of  $2 \mu\text{m}$ . To obtain high quality images of the devices, an ambient system temperature of at least 343 K was required. Therefore, all temperature rises are referenced to 343 K throughout this work. An Agilent 4155 Semiconductor Parameter Analyzer was used to measure the *dc* characteristics of the devices.

Gummel characteristics were taken on the measured device in each orientation, while the adjacent heat source device was driven at a known power level. Infrared images were taken with the heat source operating at different power levels while the measured device was off to determine the temperature gradient resulting from thermal coupling across the

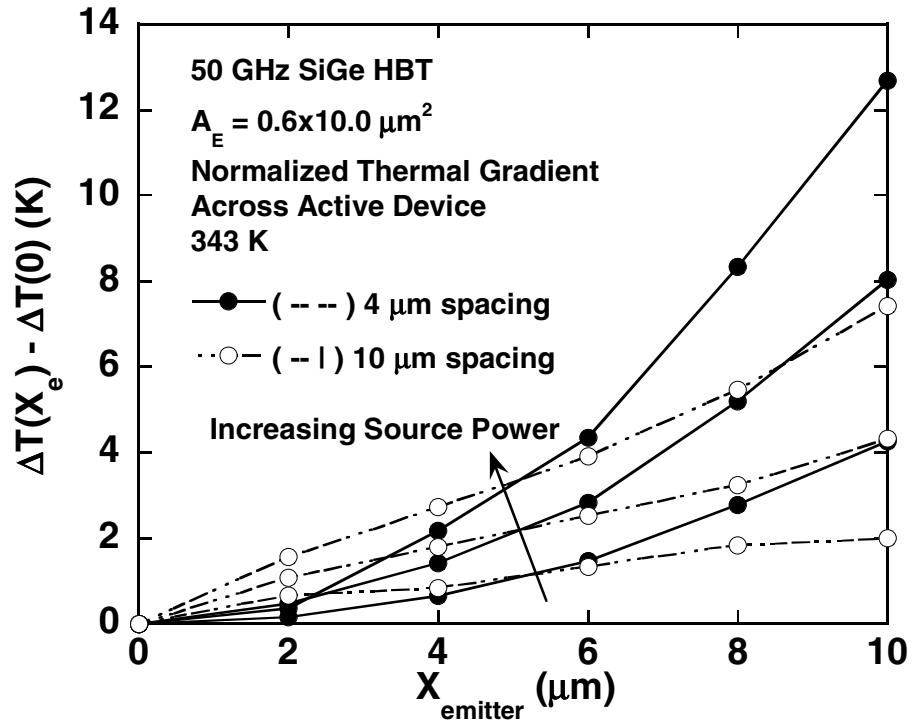


**Figure 52:** Gummel characteristics on measured device at different ambient temperatures. The characteristic for the measured device operating with the heat source on is superimposed.

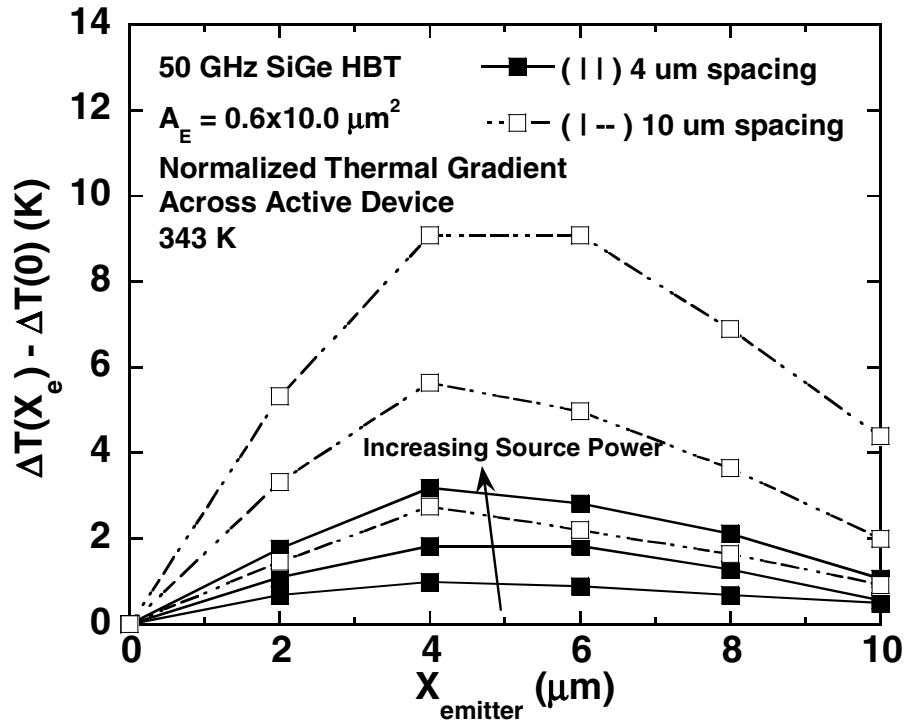
measured device as a function of adjacent device power. Next, with the heat source device off, Gummel characteristics were systematically taken on the measured device for different ambient temperatures, in 4 K increments from 343 K to the maximum temperature observed across the device from the infrared image. Using Equation (31) it was then possible to determine the effective operating temperature of the device at a given  $I_C$ , or for the entire Gummel characteristic, as is seen in Figure 52.

### 3.6.3 Results and Discussion

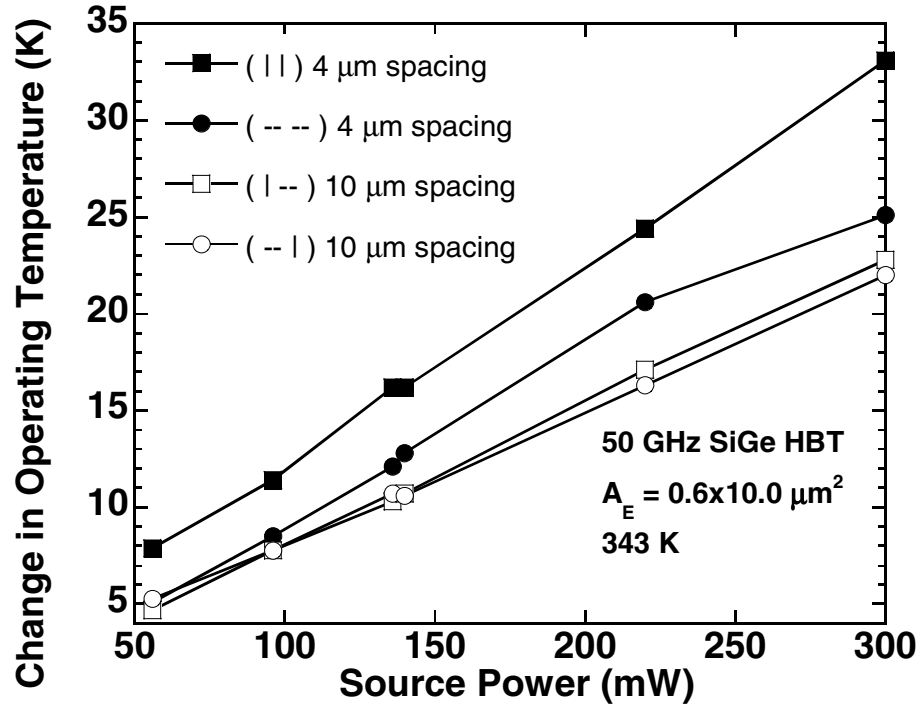
As expected, the temperature distribution across the measured devices was found to differ significantly between the different layout orientations of the device pairs. With measured devices layed-out in a horizontal fashion, as shown in cases b) and c) in Figure 50, the device is heated asymmetrically along the length of the emitter ( $L_e$ ), as shown in Figure 53. The temperature variation across the measured device in the -- case, with maximum



**Figure 53:** Temperature variations across horizontal measured devices normalized to the minimum temperature rise per configuration.



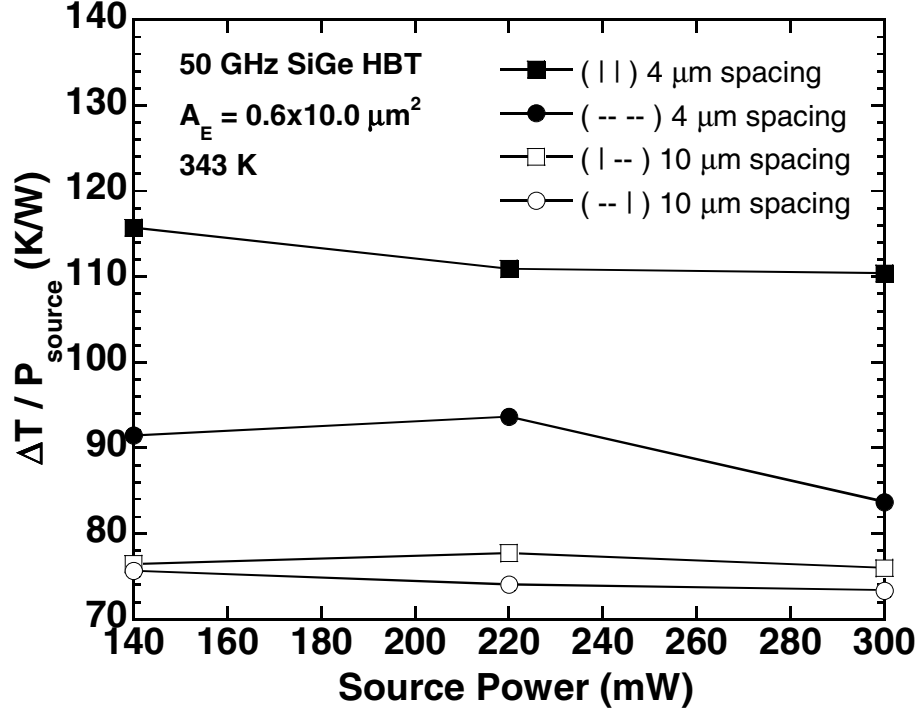
**Figure 54:** Temperature variations across vertical measured devices normalized to the minimum temperature rise per configuration.



**Figure 55:** Average infrared measured temperature change vs. heat source power.

source power in the adjacent device, is in excess of 12 K and exhibits a quasi-exponential type decay. For the  $-|$  case, the temperature gradient is not as severe, due to the fact that the devices are separated by an additional  $6 \mu\text{m}$ . Also, the temperature profile across the device exhibits a higher degree of linearity than the other case. This is again due in part to the greater distance from the heat source. It should also be noted that the full emitter length of the adjacent heat source is exposed to the measured device at a linear distance on the order of the device length. Thus, from a modeling perspective, it is clear that the adjacent device should not be treated simply as a point source of heat, as it could have been in the prior case. If the measured device in this orientation were moved closer to the heat source, its linear thermal behavior would become more exponential, but to a lesser degree than was observed in the  $---$  case.

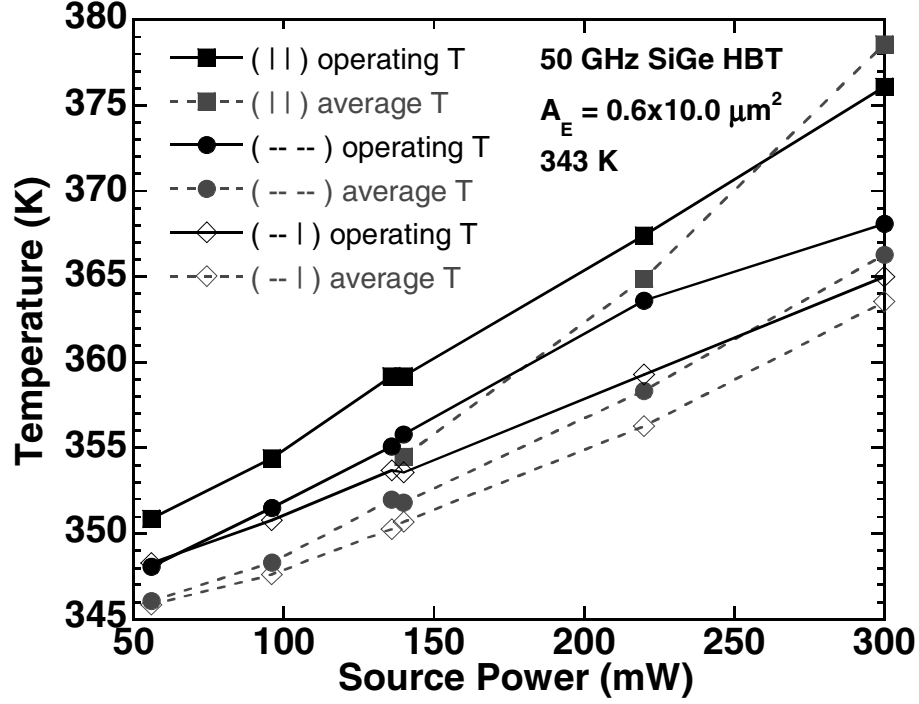
The temperature variation across the vertically-oriented transistors, cases a) and d) in Figure 50, are shown in Figure 54. In both cases the thermal distribution is similar to what one would see due to conventional self-heating, with the peak temperature centered along



**Figure 56:** Infrared temperature measured variation independence across heat source power.

$L_E$ . Interestingly, the 4  $\mu\text{m}$  spaced || case exhibits less deviation across the device, even though it undergoes the most heating among all the cases. This is due to parallel orientation of the adjacent heat source, which acts quite evenly along the measured transistor. Conversely, the 10  $\mu\text{m}$  | – case exhibits a stronger thermal gradient (although lower overall temperature rise) due to the perpendicular orientation of the adjacent heat source which act strongest on the center ( $X_e = L_e/2 = 5\mu\text{m}$ ) of the measured device.

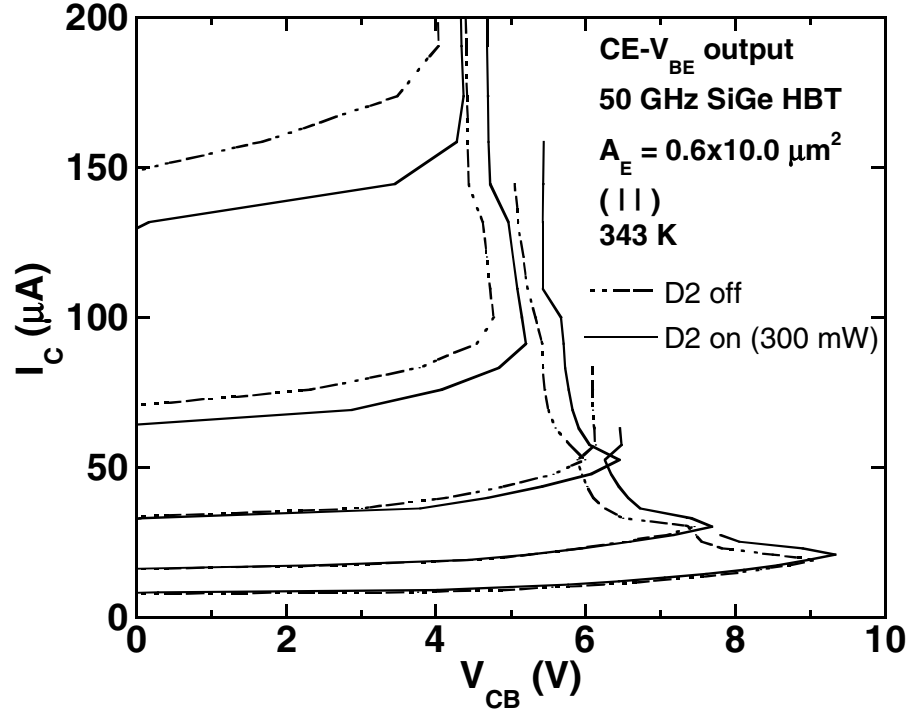
The Gummel characteristics taken for different adjacent heat source power levels were then compared to the Gummel characteristics taken across ambient temperature. Using Equation (31), the change in effective operating temperature was calculated as a function of layout orientation and heat source power, as shown in Figure 55. The results show that the highest temperature rise is attributed to the || case, which is expected since the greatest device area is "visible" to the heat source in this configuration. The --- shows the next most temperature rise, which is dominated by device proximity. The other two cases are barely



**Figure 57:** Average infrared measured temperature and electrically extracted temperature of the measured devices.

distinguishable, due primarily to the fact that the temperature at the  $10 \mu\text{m}$  distance has been substantially dissipated due to the silicon substrate. The data of Figure 55 is reformatted in Figure 56 to demonstrate that the coupling between the two devices is virtually constant across heat source power, demonstrating a nearly uniform  $R_{21}$  across power that varies considerably between the different layout configurations.

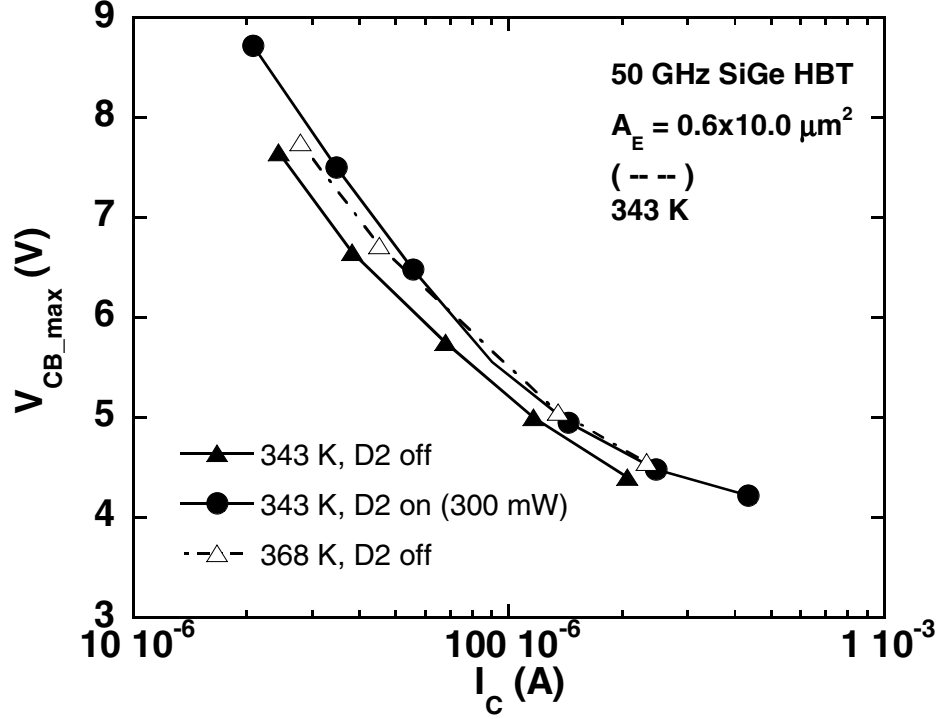
Finally, infrared temperature averages are compared to electrically extracted temperatures using Equation (31), with results shown in Figure 57. The trend of the average infrared temperature and the extracted temperature are consistent across orientation and power. This trend demonstrates that even though wide temperature variations can be seen across the measured device, as was shown in Figures 53 and 54, that the effective device temperature as related to its *dc* Gummel characteristic is in essence the average temperature across the device. This finding allows for lumped  $R_{21}$  electro-thermal modeling for device networks in SiGe, independent of device orientation, and is clearly good news from a thermal modeling perspective.



**Figure 58:** Common-emitter output characteristics under forced  $V_{BE}$ , with and without thermal coupling from adjacent heat source ("D2").

### 3.6.4 Breakdown Implications

The decrease in breakdown voltage with technology scaling in SiGe HBTs (see Figure 46) imposes important design constraints on device biasing and operation [4]. Additional measurements were taken to detect any influence of emitter thermal gradients from the various layout configurations on device ruggedness and breakdown voltage instability thresholds. Figure 58 shows a common-emitter (CE) output characteristic under forced  $V_{BE}$ .  $I_C$  is swept and  $V_{CB}$  monitored to detect the fly-back point, where the device enters electro-thermal runaway. No degradation in the maximum  $V_{CB}$  was observed when the heat-source was powered on. In fact, the maximum  $V_{CB}$  was observed to be slightly higher in this case, due to the weak decrease in  $M - 1$  with increasing temperature. Similarly, safe-operating-area (SOA) characteristics across bias presented in Figure 59 show a slight increase in SOA with the thermal source on, and little difference from the case of increased ambient temperature. Results were similar for all layout cases examined. This is clearly good news in



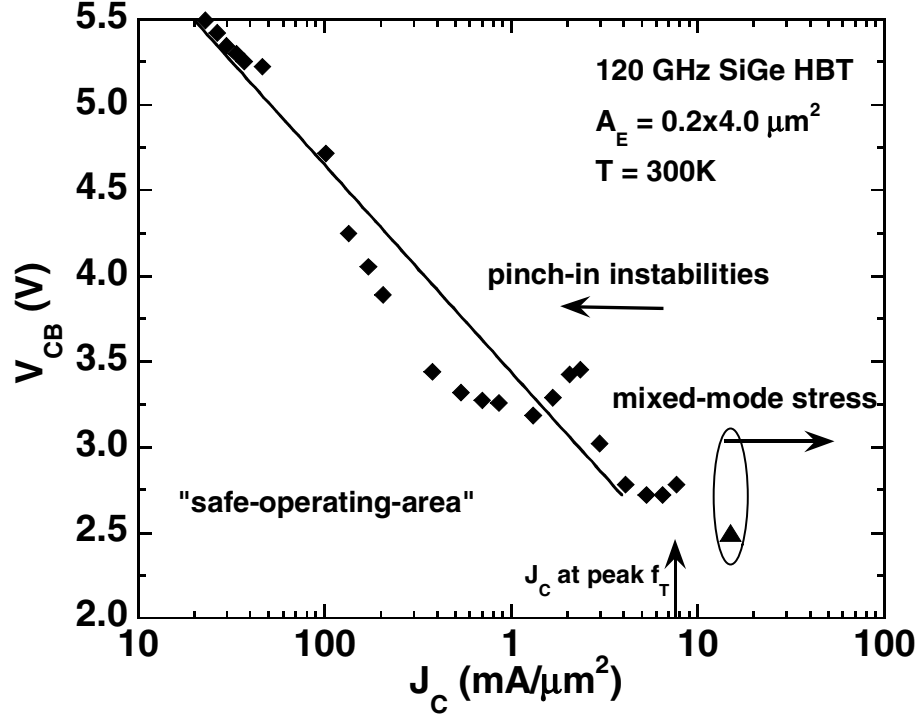
**Figure 59:** Safe-operating-region characteristics of the SiGe HBTs in the (---) configuration, comparing operation with and without thermal coupling, and operation at raised ambient temperature.

terms of device ruggedness for SiGe HBTs subjected to strong thermal coupling.

### 3.7 Summary

This chapter explored practical device and circuit level implications of breakdown voltage constraints. We noted the failure of standard industry models (VBIC, HICUM, MEX-TRAM) to capture the "pinch-in" effect, and resulting collector voltage instability threshold ( $V_{CB\_crit}$  in the  $CB-I_E$  bias configuration. A calibrated quasi-3d six-transistor model was explored and compared to measured data, and key model parameters were systematically adjusted to explore the influence of various transistor characteristics on device ruggedness and stability. Transistor frequency response was examined as a function of collector voltage, and *ac* instabilities were observed at  $V_{CB}$  greater than  $V_{CB\_crit}$  in both measurement and quasi-3D simulation. RF Power amplifier (PA) performance was compared for different bias configurations.





**Figure 60:** Practical safe-operating-area considering both low-bias instabilities and high-bias mixed-mode stressing for the 120 GHz SiGe HBT.

The practical SOA limits were extended into high current with a discussion of mixed-mode stressing and device reliability. A practical SOA for the 120 GHz SiGe HBT BiCMOS technology generation, including both low-current pinch-in related effects and high-current mixed-mode stress degradation, is presented in Figure 60. Clearly, the voltage swing at  $J_C$  at peak  $f_T$  is severely limited, an important practical concern for high frequency applications. Finally, thermal coupling effects between transistor pairs were experimentally characterized as a function of layout, demonstrating that large thermal gradients need not be treated in a distributed manner, and that these gradients do not adversely affect such *dc* characteristics as breakdown voltage and operating point instabilities at high  $V_{CB}$ .

# CHAPTER IV

## CONCLUSION

### ***4.1 Conclusion***

As we demonstrate in this thesis, operating voltage constraints are an important consideration in SiGe HBTs BiCMOS design, with implications ranging from *dc* bias stability, small signal gain, linearity, device reliability, and beyond. As SiGe devices attain higher performance through technology scaling, breakdown effects become more serious and voltage limits more severe. With heavy reliance on both experimental characterization and device and circuit simulation, we present a comprehensive assessment of breakdown and other operational voltage constraints in SiGe HBTs, discussing physical origins, effects of technology scaling, modeling issues, and impacts on device and circuit reliability.

In Chapter I, we introduced the SiGe HBT, highlighting its compelling and unique combination of traits: a device with extremely high frequency performance that is compatible with standard Si processes. Thus, high performance analog or RF components using SiGe HBTs can be fabricated alongside state-of-the-art CMOS digital logic for system-on-a-chip level integration. Important aspects of SiGe HBT BiCMOS technology were discussed, followed by a review of physics of the SiGe HBT. Finally, a general overview of avalanche multiplication and breakdown in SiGe HBTs was given.

Chapter II was devoted to the study of breakdown characteristics in SiGe HBTs. Specific breakdown issues relating to transistor bias configuration ( $CE-I_B$ ,  $CE-V_{BE}$ ,  $CB-I_E$ ) were discussed, including an overview of avalanche-induced current constriction (pinch-in). Breakdown voltage constraints in SiGe HBTs were experimentally examined as a function of numerous factors including technology generation, bias configuration, injection level, and device geometry. Finally, Chapter III examined the broader implications of

operating voltage constraints in SiGe HBTs, including issues related to modeling, circuit reliability, device reliability, self-heating, and thermal coupling.

Overall, the analysis presented in this thesis offers designers 1) prudent guidelines for device operation, clarifying the range of usable voltage for stable operation beyond  $BV_{CEO}$  for various operational bias conditions, and 2) a description of some of the issues that may be encountered for aggressive bias at excessive  $V_{CB}$ . For instance, degradation due to mixed-mode stressing, typically studied under accelerated conditions at very high  $J_C$  and  $V_{CB}$ , was shown to emerge for  $J_C$  and  $V_{CB}$  comparable to  $J_C$  at peak  $f_T$  and its respective (extrapolated) breakdown voltage limit. In addition, self-heating effects, which can emerge at injection levels considerably lower than  $J_C$  at peak  $f_T$ , require careful consideration, particularly since these effects are expected to become more serious with technology scaling.

## 4.2 *Future Directions*

The general overview presented in this thesis regarding the practical implications of operating voltage constraints, particularly with respect to circuits, is far from complete. Opportunities for further study include a more specific analysis of the influence of high voltage operation to circuit-level reliability, particularly in the realm of RF components, and specifically power amplifier designs. Also, the thermal coupling studies performed here in a first generation SiGe HBT technology should be extended to the second and third generation technologies, with additional emphasis on the modeling aspects of thermal issues as they relate to circuit layout. Circuit reliability issues related to thermal coupling should be experimentally examined. Again, the PA serves as an attractive component to study.

The area of extreme environments (e.g. applications in outer space) is a growing focus of study for SiGe HBTs, and provides numerous opportunities for further study. For instance,  $M - 1$  increases significantly as temperature decreases, suggesting that breakdown

effects should be aggravated at cryogenic temperatures. As a result, breakdown related issues should be characterized for various SiGe HBT technology generations as a function of temperature. Also, the effects of radiation exposure on breakdown voltage constraints and device stability should be examined. Moreover, open issues and questions regarding radiation tolerance of devices exposed under bias (e.g. for various levels of  $V_{CB}$  and  $J_C$ ) make this area an important focus for future studies.

In addition, the results of our characterization of the high breakdown (HB) devices across technology generation show that further study of these devices, in both normal and extreme operating environments, will be very fruitful from both the device level and the circuit level perspectives. Such a study will be very relevant for applications (such as PAs) that require high output power, and thus high voltage swing, and thus a comprehensive understanding of the behavior of HB devices at high voltage has importance in terms of circuit performance and reliability.

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