LOW-POWER, HIGH-EFFICIENCY, AND HIGH-LINEARITY CMOS MILLIMETER-WAVE CIRCUITS AND TRANSCEIVERS FOR WIRELESS COMMUNICATIONS

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Eric A. Juntunen

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LOW-POWER, HIGH-EFFICIENCY, AND HIGH-LINEARITY CMOS MILLIMETER-WAVE CIRCUITS AND TRANSCEIVERS FOR WIRELESS COMMUNICATIONS

Approved by:

Professor Ioannis Papapolymerou,
Advisor
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor Gee-Kung Chang
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Debasis Dawn, Adjunct Faculty and
Co-Advisor
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor Emmanouil M. Tentzeris
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor John D. Cressler
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor Christos Alexopoulos
School of Industrial and Systems
Engineering
Georgia Institute of Technology

Date Approved: April 16, 2012

To Clyde,

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Advancements in standard CMOS technology over the past decade have provided dramatic increases in speed and reductions in both chip area and power consumption of digital circuits. Consequently, the usable operating frequencies for analog circuits have risen as well. This has created the opportunity for consumer-volume applications in the millimeter-wave regime (30-300 GHz), an area that has historically been used almost exclusively for government and non-consumer products due to the high cost of applicable semiconductor technologies.

This dissertation presents the design and implementation of circuits and transceivers in CMOS technology to enable many new millimeter-wave applications. Chapter I first gives a brief introduction to the development of CMOS technology to support millimeter-wave design, then provides several examples of emerging millimeter-wave applications. Chapter II discusses a simple approach utilized for accurately modeling the millimeter-wave characteristics of transistors not fully captured by contemporary parasitic extraction techniques. Chapter III presents the integration of a low-power 60-GHz CMOS on-off keying (OOK) receiver in 90-nm CMOS for use in multi-gigabit per second wireless communications. The use of non-coherent OOK demodulation by a novel demodulator enabled a data throughput of 3.5 Gbps and resulted in the lowest power budget (31pJ/bit) for integrated 60-GHz CMOS OOK receivers at the time of publication. Chapter IV presents the design of a high-power, high-efficiency 45-GHz VCO in 45-nm SOI CMOS. The design is a class-E power amplifier placed in a positive feedback configuration. This circuit achieves the highest reported output power (8.2 dBm) and efficiency (15.64%) to date for monolithic silicon-based millimeter-wave

VCOs. Results are provided for the standalone VCO as well as after packaging in a liquid crystal polymer (LCP) substrate. In addition, a high-power high-efficiency (5.2 dBm/6.1%) injection locked oscillator is presented. In chapter IV, the design of a 2-channel 45-GHz vector modulator in 45-nm SOI CMOS for LINC transmitters is presented. A zero-power passive IQ generation network and a low-power Gilbert cell modulator are used to enable continuous 360° vector generation. The IC is packaged with a Wilkinson power combiner on LCP and driven by external DACs to demonstrate the first ever 16-QAM generated by outphasing modulation in CMOS at in the Q-band. Finally, chapter V summarizes the techical contributions of this dissertation and provides suggestions for future research.

CHAPTER I

INTRODUCTION

1.1 Motivation

The millimeter-wave spectrum is defined as 30-300 GHz. Historically, millimeter-wave bands have been used almost exclusively for government and non-consumer products due to the cost barrier of semiconductor technologies like Gallium Arsenide (GaAs) and Indium Pohosphide (InP) that could operate at such high frequencies [1],[2]. However, the maturation of silicon technologies like CMOS and SiGe BiCMOS has created the possibility for consumer-volume products and low-cost non-consumer-volume products uniquely suited for millimeter-wave operation [3],[4]. The following sections will introduce some of these applications.

1.2 Background

1.2.1 The evolution of CMOS-based radio

During the late 1980s, when the cellular telephone market was emerging, silicon bipolar technologies were developed with transit frequencies near 10 GHz. This provided enough margin to support devices with carrier frequencies below 1 GHz [5]. Earlier in the decade, RF design had been dominated by GaAs, but the prospect of expanding the role of less expensive silicon bipolar technologies compatible with common CMOS fabrication equipment motivated the industry to develop high performance RF silicon technology.

By the mid 1990s, industry leaders were in a race for market share in the rapidly expanding cellular handset market. At that time CMOS processes were far inferior to silicon bipolar technologies and III-V devices such as Gallium Arsenide (GaAs) with respect to high-frequency analog design. Therefore, due to time-to-market constraints

and the limited availability of designers familiar with differing radio architectures, silicon bipolar and GaAs development dominated the private sector.

The systems developed in industry during that time were characterized by low levels of integration, with many discrete elements assembled on PC boards. Academia, however, was not bound by market constraints and began to explore the possibility of developing highly integrated CMOS chips for the RF domain in the hopes that its success in the baseband wireline market could soon be applied to the wireless arena [6]. RF CMOS research drove the development of on-chip inductors with practical usage for high-volume production. This enabled CMOS front-end circuits previously unavailable to the system engineer. The first inductors to appear were suspended spiral inductors that eliminated the prohibitive problems of substrate capacitance and eddy current loss [7]. The availability of these new on-chip inductors allowed for the design of fully integrated, tuned low-noise amplifiers [8].

Later, improved layout approaches suitable for mass-production replaced the suspended inductor and were offered in RF CMOS processes [9]. The major roadblock for on-chip spiral inductors had been their lossy nature compared to discrete components [10]. Resistive losses were mitigated by implementing processes with a thick top metal layer available to the designer. More problematic, however, were substrate losses due to eddy currents. This led to the development of new generations of CMOS substrates with low doping levels. In addition, shielding metal layers were placed below the spirals whose geometry prevented the flow of eddy currents [11]. The availability of these new higher-Q inductors led to fully on-chip CMOS oscillators whose phase noise performance could complete with that of discrete transistor oscillators. The ability of the MOSFET to function as a switch enabled frequency tuning using switched reactive elements [12]. This led to band switching techniques that could extend the useful range of frequency selection and/or correct for frequency shift due to process variation.

The emergence of markets for IEEE 802.11 and Bluetooth® products came with a different set of rules for engineering firms. In contrast to cellular handsets, the success of WLAN chipsets would be determined more by production costs because service providers would no longer subsidize the technology. This would require higher levels of integration to eliminate the need for costly off-chip discrete components. The solution was the development of complete systems on single chips in the least expensive semiconductor process available, CMOS. Emerging standards were written with specifications relaxed in such a way that CMOS radios became viable solutions. This brought CMOS development to the forefront of industrial development.

1.2.2 Millimeter-Wave CMOS

The continued maturation of CMOS technology to operate at millimeter-wave frequencies is in some ways a byproduct of the research and development driven by digital concerns. Over the past decade, CMOS geometry scaling motivated primarily by the need for smaller area, faster speeds, and lower power consumption in digital circuits has pushed the transit frequency, f_T, and maximum frequency of oscillation, f_{max}, of standard, production-level CMOS into the many hundreds of GHz [13],[14]. This has enabled robust millimeter-wave front-end design in standard CMOS technology [3]. Seen in Figure 1 is a plot from [13] illustrating the scaling of f_T with CMOS process node. The opportunity now exists for highly integrated CMOS transceivers with reliable millimeter-wave front-ends, mixed-signal content, and full digital back ends on a single die.

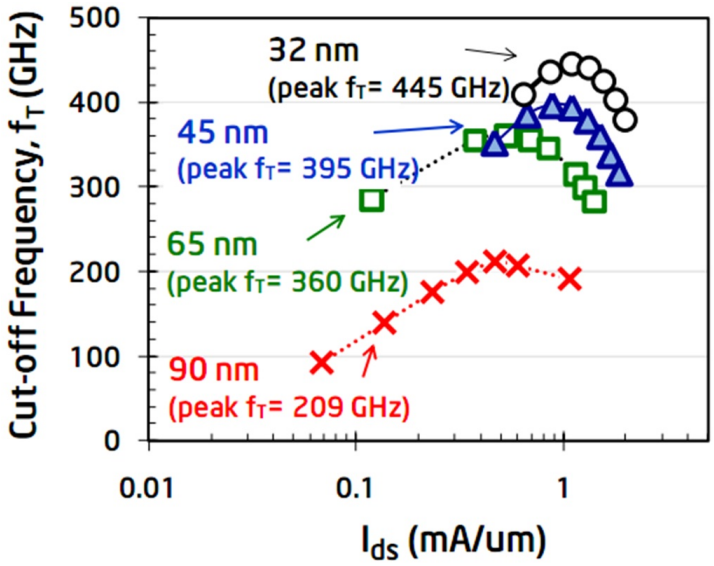


Figure 1: Maturation of CMOS technology f_T.

1.2.3 SOI versus Bulk CMOS

This work advocates the use of CMOS technology for millimeter-wave System on Chips (SoCs) that will combine millimeter-wave front end radios with digital back end signal processing and calibration. Therefore, a brief discussion of the implications that modern CMOS technology advances driven by digital concerns will have on analog front ends is included.

Seen in Figure 2 are cross-sections of an nMOS transistor in conventional bulk CMOS, partially-depleted (PD) silicon-on-insulator (SOI) CMOS, and fully-depleted (FD) SOI CMOS. In bulk CMOS, the body of the transistor is formed by the p-substrate. In SOI CMOS, there exists an electrically insulating layer, usually silicon dioxide, below the transistor structure, separating it from the wafer substrate. This geometry has a number of well-understood benefits to digital circuitry. The decreased junction capacitances result in higher speed and a 30-40% reduction in power consumption [15]. Decoupling the transistor body from the substrate eliminates the possibility of latchup and increases the isolation between devices, which allows for

tighter transistor packing. Furthermore, substrate coupled noise is dramatically reduced, benefiting both digital and analog circuits. Specific benefits for analog and RF circuits include an increase in f_T due to the reduction of parasitic junction capacitance, and an increase in transconductance from a decreased bulk effect [16].

SOI CMOS does, however, present a number of challenges when it is used for analog and RF circuit design. Temperature rise due to thermal insulation from the buried oxide can cause a degradation in charge carrier mobility and saturation velocity [17]. This effect is not an issue for digital circuits because it is seen only during switching periods, but it can be very detrimental for analog circuits biased well into saturation. In PD SOI, the body is in a floating, or quasi-static, state. This causes memory effects whereby the residual charge contained in the body resulting from past operation affects the present device characteristics [16]. The floating body also leads to a parasitic BJT structure formed by the drain, body, and source regions. For high enough drain to source voltages, this BJT will turn on, creating an additional current path parallel to the CMOS channel. This results in a "kink" effect in the I_D versus V_{DS} curves [16]. The use of body contacts eliminates these effects, but comes at the cost of larger transistor area.

In FD SOI, the distance between the gate oxide and the buried oxide is made much smaller. Therefore, the depletion region extends all the way down to the buried oxide layer. This eliminates the floating body effects seen in PD SOI, but the tradeoff is a threshold voltage sensitivity to the thickness of the silicon layer [16]. This yields an increased risk of process variation induced mismatch between devices.

The continued attraction of CMOS for RF and millimeter-wave designs will be driven largely by its ability to incorporate dense, low-power digital subsystems on the same die as analog circuitry. Therefore, because of the many benefits SOI technology provides for digital circuits, RF and analog designers must understand the implications of SOI CMOS technology.

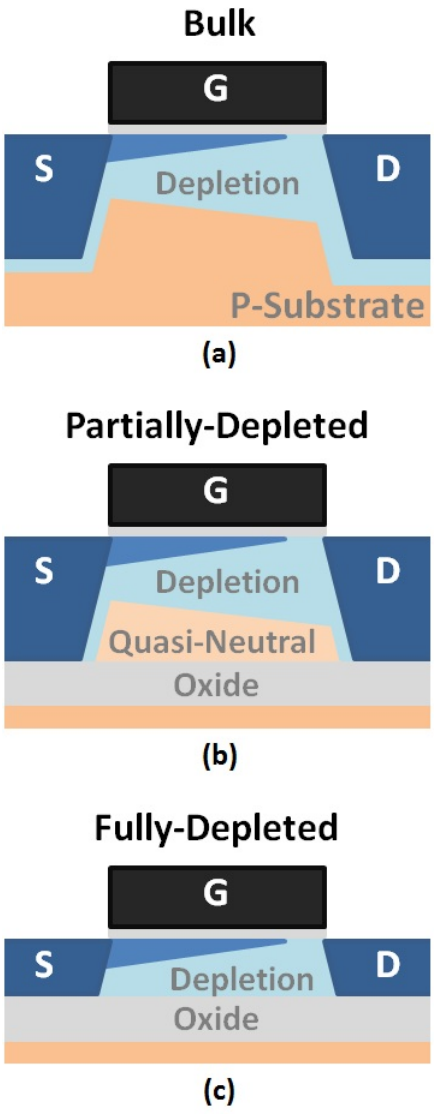


Figure 2: Cross-sectional view of (a) bulk, (b) partially depleted SOI, and (c) fully depleted SOI CMOS.

1.2.4 Liquid Crystal Polymer Substrate for Millimeter-Wave Packaging

CMOS technology is an attractive solution for bringing millimeter-wave systems to a large consumer market because of its low cost and high digital integration for back-end functionality. However, a low-cost package with good performance at millimeter-wave frequencies must be utilized to enable the complete solution.

Liquid Crystal Polymer (LCP) has gained considerable attention recently as a low-cost millimeter-wave substrate and packaging material since it became commercially available in 2003 [18]-[20]. Its stable dielectric constant (2.95-3.16), low loss tangent (0.002-0.004) over a wide frequency range (30-110 GHz), inherent near-hermetic property and low processing temperature make LCP a very attractive packaging solution for microwave applications [21]. LCP was demonstrated to be a suitable substrate for creating high-quality resonant microwave structures in [22] and an appropriate packaging material for MMICs in [23]. Recently, a millimeter-wave SiGe VCO packaged in LCP was demonstrated in [24].

1.3 Millimeter-Wave Applications

The following sections describe a number of emerging opportunities in the lower portion (< 110GHz) of the millimeter-wave spectrum. Figure 3 summarizes these applications.

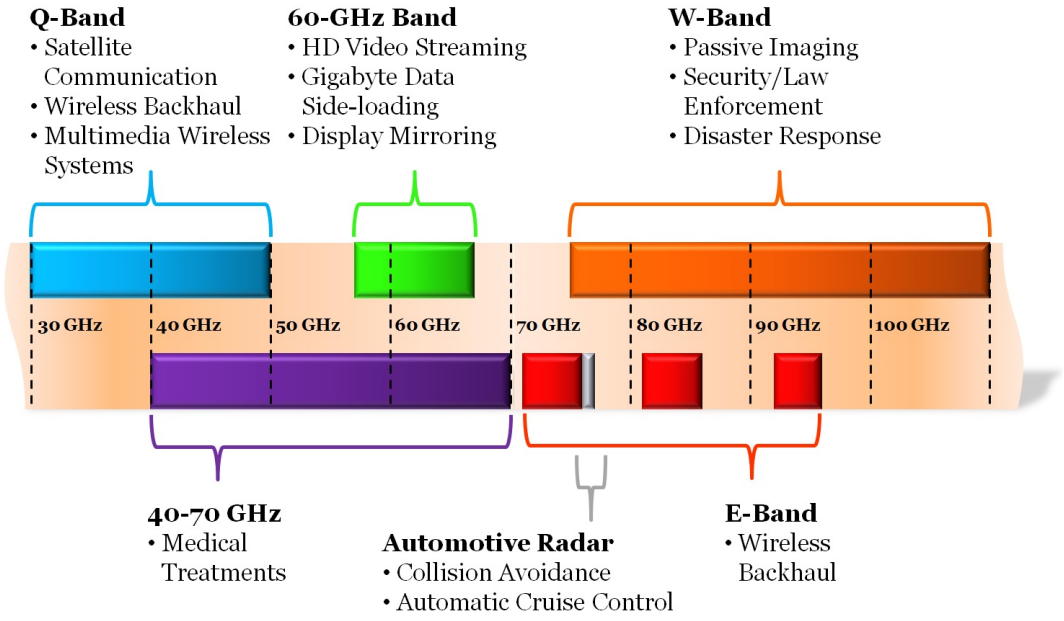


Figure 3: Millimeter-wave spectrum opportunities.

1.3.1 60-GHz Band for Multi-Gigabit Wireless Communications

The proliferation of high-definition digital multimedia content and increasing data storage capabilities on fixed and mobile devices alike will drive the need for higher data-rate wireless connectivity than can be provided with existing commercial standards such as 802.11n [25]. For this reason, governments worldwide have made large spectral allocations to support unlicensed multi-gigabit wireless communications as seen in Figure 4.

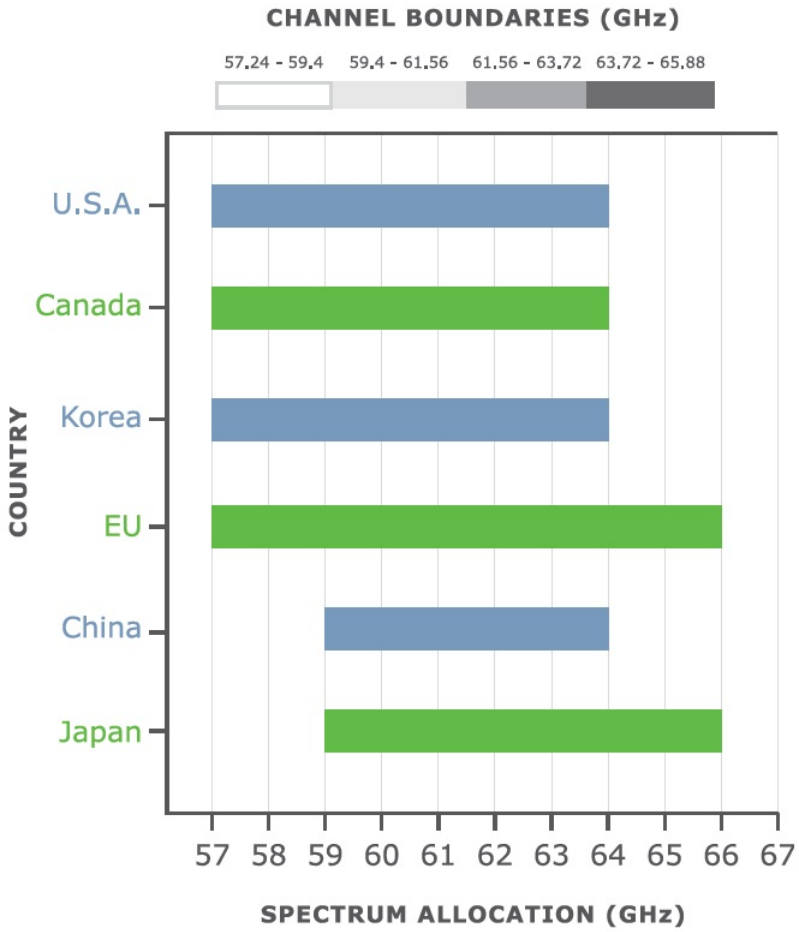


Figure 4: Worldwide spectrum allocation in the 60-GHz band.

The 60-GHz band has a number of characteristics that make it particularly attractive for short-range wireless communications. The free space path loss is given

by (1), where the distance d is in meters and the frequency f is in GHz.

$$FSPL(dB) = 20log(d) + 20log(f) + 32.45 \quad (1)$$

Based on this phenomenon alone, the link budget at 60 GHz is approximately 21 dB less than for an equidistant 5-GHz 802.11 WLAN link. However, there exists an atmospheric oxygen absorption peak at 60 GHz that contributes additional loss [26]. Furthermore, since antenna directivity increases with frequency, millimeter-wave links will be strongly line-of-sight [27]. Although a drawback for long-distance terrestrial communications, both of these characteristics can be leveraged to enable frequency reuse such that many multi-gigabit links between various devices may coexist within close proximity. The types of connectivity that can be enabled using the 60-GHz band include wireless high-definition multimedia streaming and Gbps data side-loading as depicted in Figure 5.

Figure 5: Examples of Gbps connectivity in the 60-GHz band.

In pursuit of these types of connectivity, many organizations have been in competition to drive the standardization of 60-GHz interoperability. In 2005, the IEEE 802.15.3c technical committee was formed to develop a millimeter-wave based physical layer (PHY) specific to the 60-GHz band as an extension of the existing 802.15.3 wireless personal area network (WPAN). Later, in 2007, the IEEE 802.11 working group

for wireless local area network (WLAN) standards formed the very high throughput study group (VHT-SG) that would work to define a new task group organized under 802.11. In early 2009 the VHT-SG completed its work with the formation of the 802.11ad task group, which would also focus on 60-GHz standardization. In late 2009 the 802.15.3c entered hibernation after ratifying the *802.15.3c Multi-gigabit speed Wireless PAN Standard.* During the same period, ECMA International was developing yet another 60-GHz standard. The ECMA-387 standard was released in late 2008. In 2009 ISO/IEC JTC 1 amended and approved the first version of ECMA-387.

In addition, a number of industry consortia have formed to leverage influence on the development of 60-GHz standardization including Wireless HD, The Wireless Gigabit Alliance (WiGiG), The WiMedia Alliance, and the Wireless Home Digital Interface (WHDI) Consortium. Currently, WiGig appears to have the most traction and is currently drafting PHY and medium access control (MAC) specifications that will serve as the basis for the IEEE 802.11ad draft standard [28]. The WiGig specification will define a common MAC shared between existing Wi-Fi devices operating at 2.4 and 5 GHz with the new 60-GHz devices, the goal being to provide seamless switching between these three bands to support connectivity modes with different requirements.

1.3.2 Q-band for Terrestrial and Space Communications

A large spectral space that heretofore has received less attention from academia and industry is the Q-band, defined from 30 GHz to 50 GHz. This band is used primarily for high data-rate satellite communications as well as high-resolution radar [29]. However, there exists growing interest in exploiting this spectrum for high-bandwidth terrestrial links such as fixed point to point cellular backhaul applications or multimedia distribution systems [30].

1.3.3 77-GHz Band for Automotive RADAR

Another millimeter-wave application with large-scale commercial viability is automotive radar [31]. The 77-GHz band has been reserved for the implementation of features such as automatic cruise control, blind-spot monitoring, and front and rear object detection for collision avoidance as illustrated in Figure 6 [32]. Both Freescale and Infineon have developed integrated SiGe transceivers for Automotive RADAR in the 77-GHz band. Until the present, Automotive RADAR systems have mainly found adoption in the high-end car market. However, as the cost of these systems is brought down through further development in inexpensive silicon technologies, they will soon be feasible for the mid-rage automobile market. This will allow these increased safety benefits to reach a larger number of drivers.

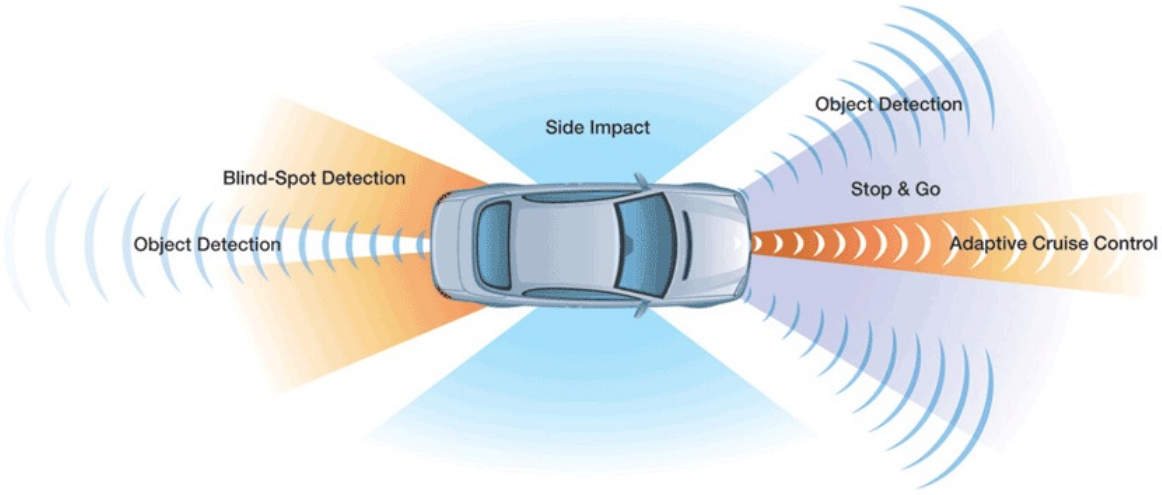


Figure 6: Automotive RADAR location and function on commercial vehicles.

1.3.4 W-band for Passive Imaging

It has been demonstrated that the W-band (75-110 GHz) is well suited for passive radar imaging [33],[34]. At these frequencies, there is a unique intersection of high spatial resolution, material penetration, and low atmospheric absorption. Potential

applications include security, law enforcement, and body detection in low or zero-visibility conditions such as fires or natural disasters. Seen in Figure 7 is a passive radar image showing the discovery of a concealed weapon that would have gone unnoticed using a metal detector [35].

Figure 7: Passive millimeter-wave imaging in the W-band.

1.3.5 E-band for Wireless Backhaul

In 2003, the FCC designated 13 GHz of previously unused spectrum from 71-76 GHz, 81-86 GHz, and 92-95 GHz for licensed, fixed wireless communications [36]. These three bands, collectively termed the E-band, can enable multi-gigabit links with distances on the order of one mile. The high transmission-power of these systems prohibits the use of full CMOS transceivers. However, moving all but perhaps the PA and LNA to a silicon-based design can yield tremendous cost savings in the deployment of backhaul networks.

1.3.6 Millimeter-Wave Medical Therapy

It has been shown that exposure to low-levels of millimeter-wave energy may have a number of medical benefits [37],[38]. Potential areas of application include treatment

of cardiovascular disease, mitigation of chronic pain such as arthritis, and tissue regeneration stimulus. Treatments are typically administered at hospitals using large, expensive machines. However, the ability to generate low-power millimeter-wave energy in low-cost silicon technologies can enable inexpensive in-home treatment options for such conditions.

1.4 Organization of the Dissertation

Chapter II discusses the simple approach utilized for accurately modeling the millimeter-wave characteristics of transistors that are not fully captured by contemporary parasitic extraction techniques. Next, Chapter III presents the integration of a low-power 60-GHz CMOS OOK receiver in 90-nm CMOS for use in multi-gigabit per second wireless communications. Chapter IV presents the design of a high-power, high-efficiency 45-GHz voltage controlled oscillator (VCO) and an injection-locked oscillator (ILO) in 45-nm SOI CMOS. One version of the VCO is packed in LCP to demonstrate the suitability of LCP for millimeter-wave packaging. In chapter V, the design of a 2-channel 45-GHz vector modulator in 45-nm SOI CMOS for LINC transmitters is presented. The IC is packaged with a Wilkinson power combiner on LCP and driven by external DACs to demonstrate the first ever 16-QAM generated by outphasing modulation in CMOS in the Q-band. Finally, chapter VI summarizes the technical contributions of this dissertation and provides suggestions for future research.

CHAPTER II

MILLIMETER-WAVE MODELING

To perform reliable millimeter-wave CMOS design, additional modeling effort is needed beyond what would likely be required at lower frequencies. Typically, scalable compact models with accuracy beyond 30 GHz are not readily available to the designer. Furthermore, conventional post-layout parasitic extraction software cannot capture the small inductances introduced by metal interconnects that have a large impact on the frequency response and port impedances of active and passive circuit elements at millimeter-wave frequencies. This requires that models for transistors, capacitors, transmission lines, and inductors be verified and fine-tuned using in-house empirical data.

A simple and effective modeling approach, which may be used directly in the native design environment of the circuit, is to take the PDK element provided by the foundry and add parasitic components surrounding it to match its simulated performance with its measured performance [39], as seen in Figure 8. Shown in Figures 9 - 13 are the measured versus modeled versus post-layout RC parasitic extracted (PEX) S-parameters for a 120-μm common-source NMOS device. Note in particular that the phase of S_{21} seen in Figure 12, which is of critical importance in determining the oscillation frequency of the VCO in Chapter 4, has the largest discrepancy between PEX and measurement.

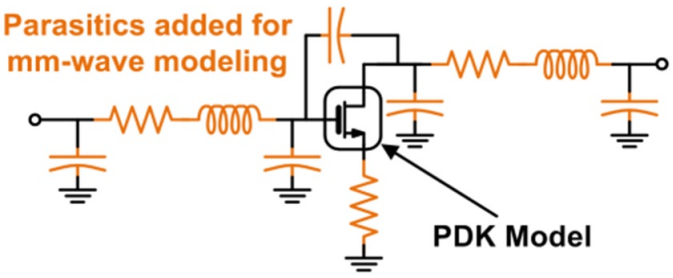


Figure 8: Millimeter-wave modeling using added parasitic elements.

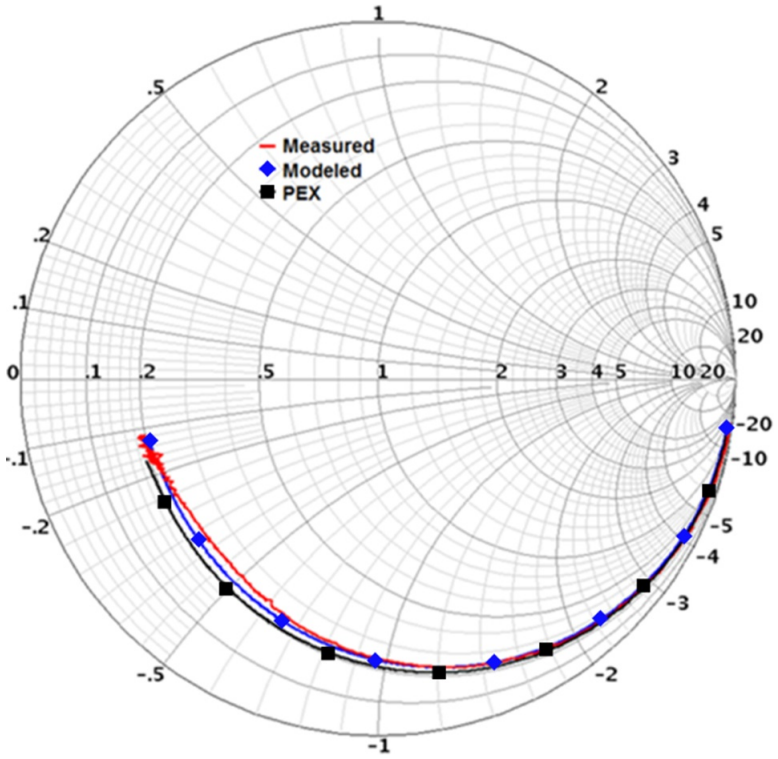


Figure 9: Measured versus modeled versus PEX S_{11} for a 120-μm NMOS, 1-90 GHz.

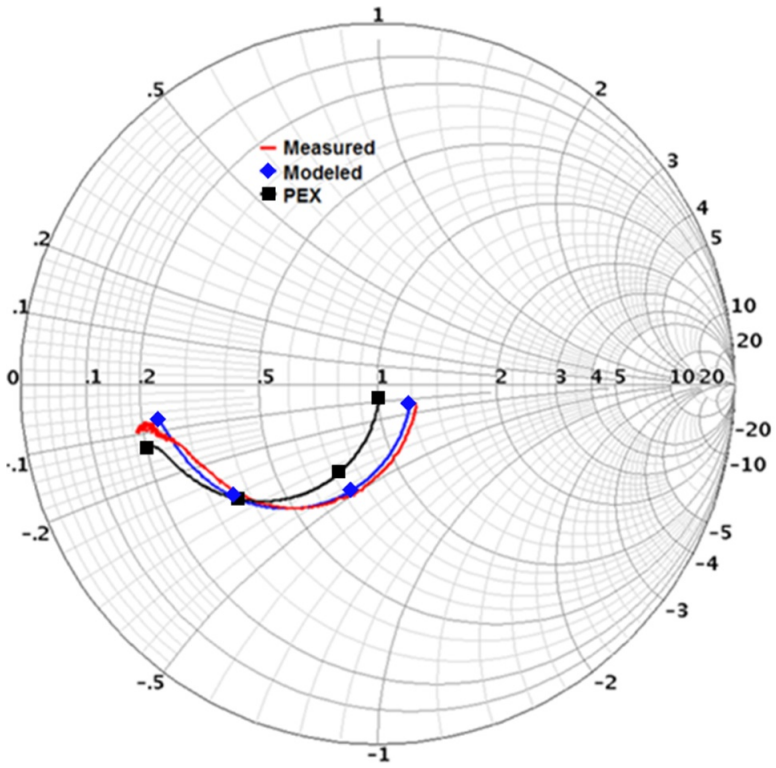


Figure 10: Measured versus modeled versus PEX S_{22} for a 120-μm NMOS, 1-90 GHz.

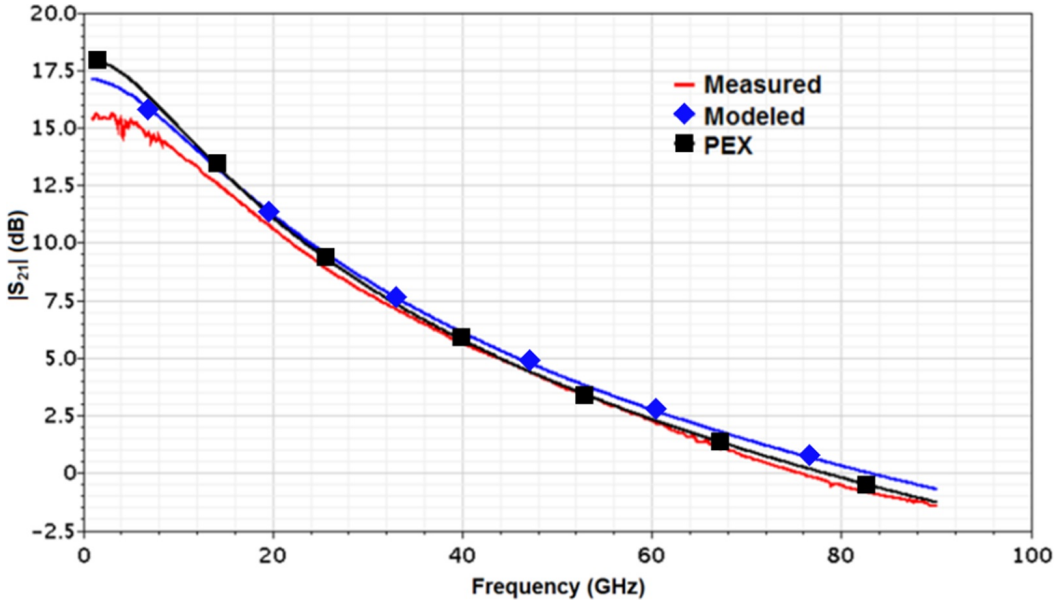


Figure 11: Measured versus modeled versus PEX $|S_{21}|$ for a 120-μm NMOS, 1-90 GHz.

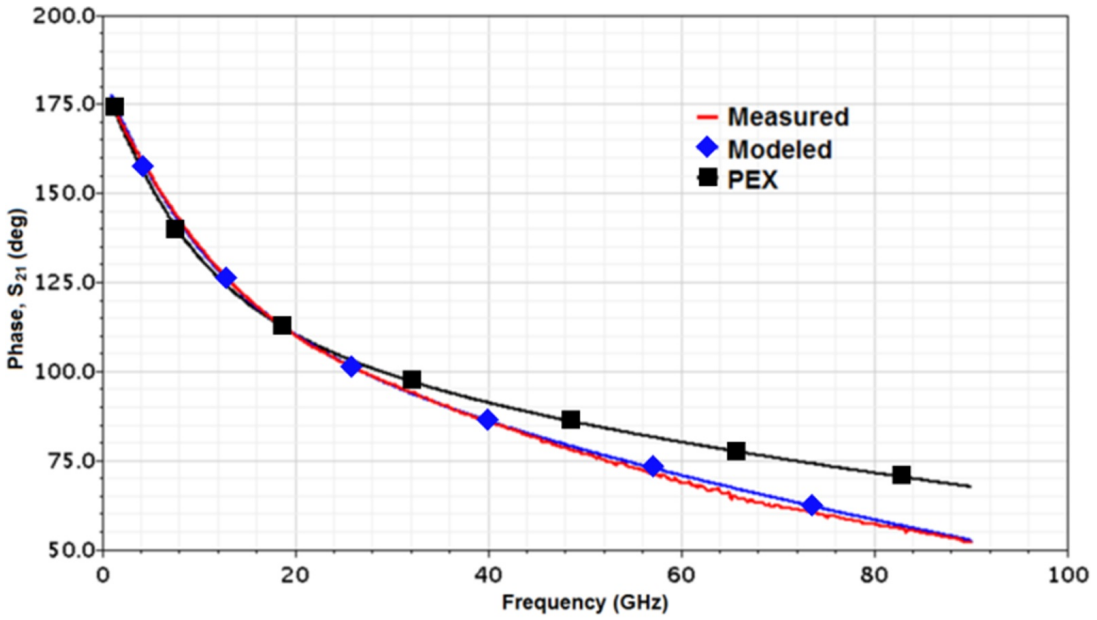


Figure 12: Measured versus modeled versus PEX phase(S_{21}) for a 120-μm NMOS, 1-90 GHz.

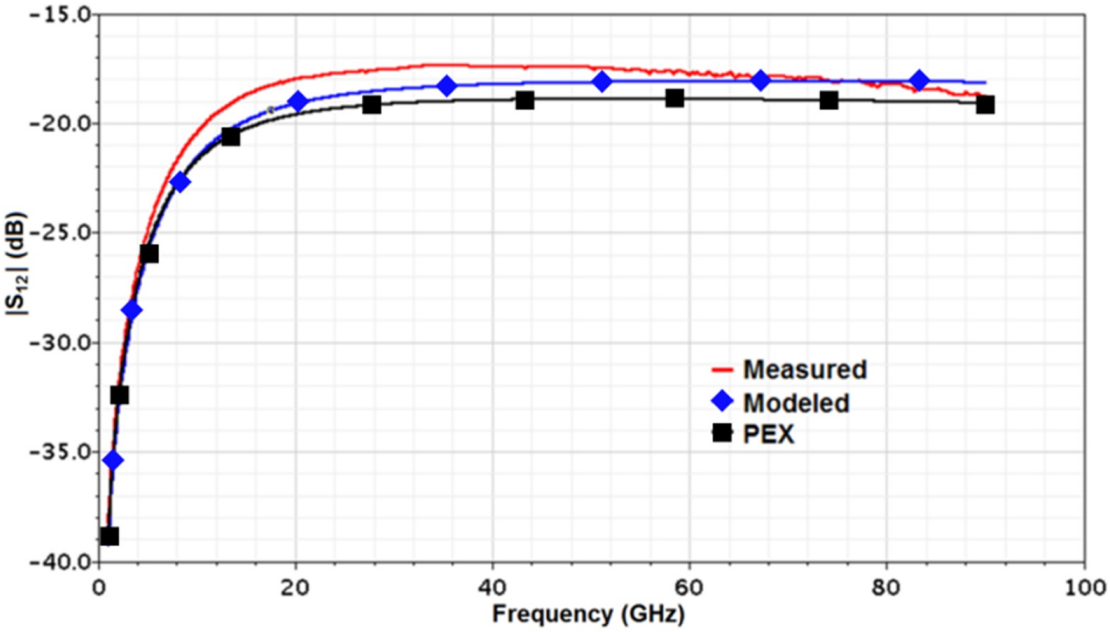


Figure 13: Measured versus modeled versus PEX $|S_{12}|$ for a 120-μm NMOS, 1-90 GHz.

CHAPTER III

60-GHZ OOK RECEIVER INTEGRATION

3.1 60-GHz OOK Receiver

Component design for a proposed 60-GHz on-off keying (OOK) Receiver was performed in [40]. These components were subsequently integrated into a receiver that was part of a fully-integrated single-chip 60-GHz transceiver [41]. The receiver architecture is shown in Figure 14. The lineup includes a four-stage 60-GHz low noise amplifier (LNA), a 60-GHz power detector for OOK demodulation, and a high-gain baseband amplifier. In addition, a 1-bit comparator and a linear Hodge clock and data recovery (CDR) circuit are integrated to provide a clocked serial output of digital data.

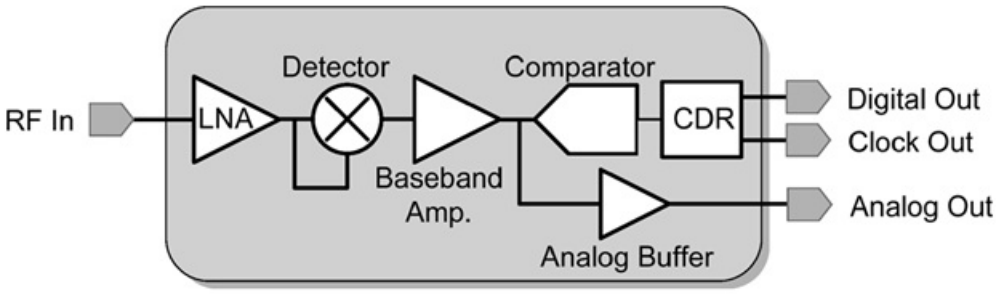


Figure 14: 60-GHz OOK receiver architecture.

3.2 60-GHz LNA Measured Results

Seen in Figure 15 is the schematic diagram of the 4-stage LNA [41]. A die photograph of a four-stage LNA test structure along with its measured s-parameter performance is seen in Figure 16. The LNA occupies a die area of 0.6 mm x 0.75 mm while delivering a peak gain of 24 dB and a 7.5-dB noise figure at a DC power consumption

of 64 mW.

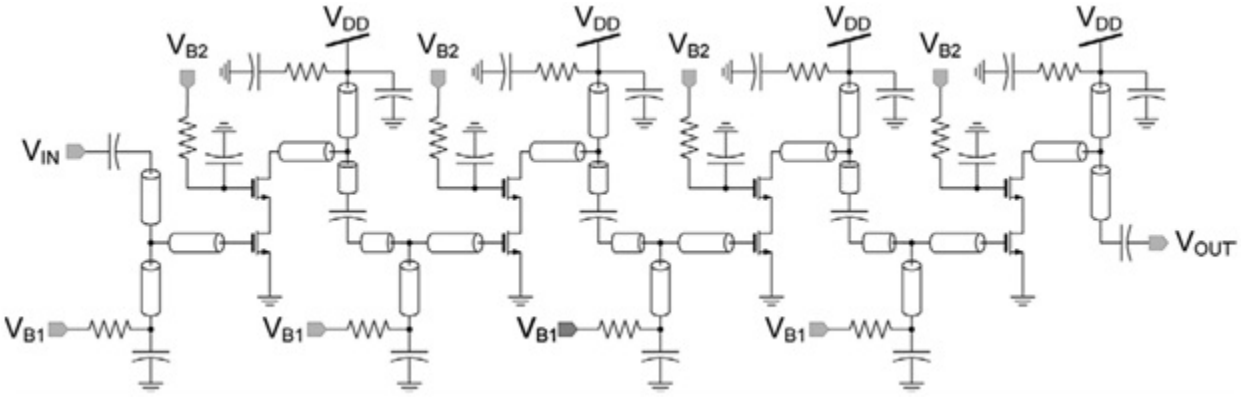


Figure 15: Four-stage 60-GHz LNA schematic.

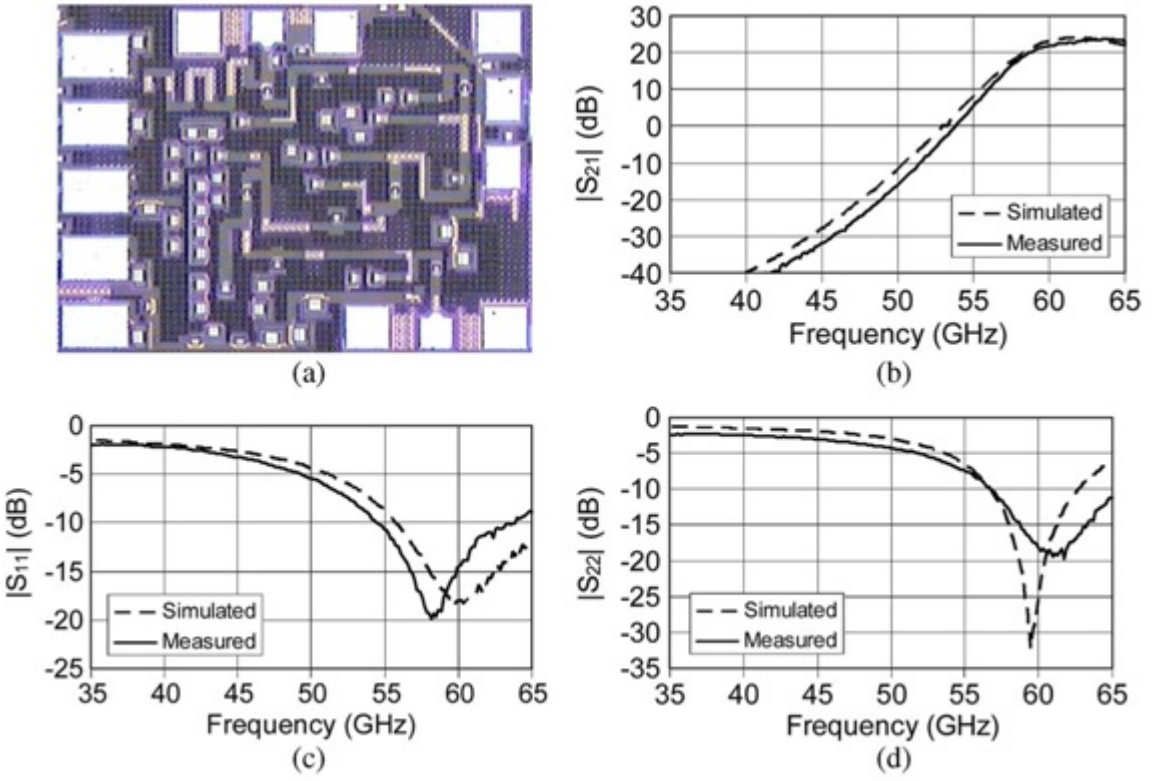


Figure 16: 60-GHz LNA: (a) die photograph, simulated versus measured (b) $|S_{21}|$, (c) $|S_{11}|$, (d) $|S_{22}|$.

3.3 60-GHz Direct-Conversion Demodulator

An innovative demodulator circuit, seen in Figure 17, was designed to extract baseband data from a 60-GHz OOK-modulated signal. The circuit is an autocorrelator based upon dual-gate mixer architecture. The input is matched to 50 Ω using a series-stub micro-strip matching network. Power detection is performed by multiplying the 60-GHz input signal by a 180° delayed version of itself. The series transmission line at the v_2 port creates a phase delay $\phi = 180°$ between the waveforms at the v_1 and v_2 ports. Additionally, this line functions as a resonant structure that provides a voltage gain due to the high-impedance loading at the v_2 port. This voltage boost, denoted by β, was simulated to be a factor of approximately 1.5. The $\lambda/4$ open-circuit stub is a short at 60 GHz to suppress the RF signal at the output.

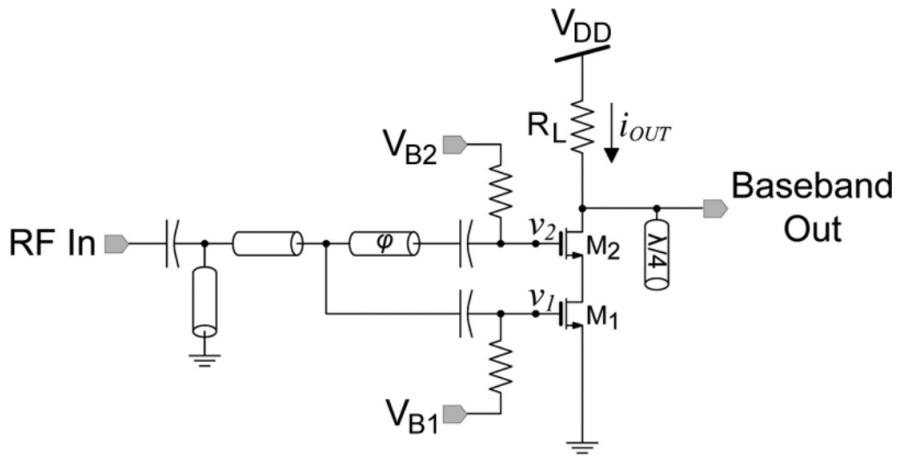


Figure 17: Demodulator schematic.

Extraction of the baseband data is described as follows: The small-signal output current given by (2) is the input voltage to M_1 multiplied by its small-signal transconductance, g_{m1}. Shown in (3) is the small-signal transconductance, g_m, for an above-threshold MOSFET, where $K = \mu_n C_{ox} W/L$ is the large-signal transconductance.

$$i_{OUT} = g_{m1} v_1 \tag{2}$$

$$g_m = \begin{cases} K(V_{GS} - V_T) & (V_{DS} > V_{GS} - V_T) \quad (saturation) \\ K(V_{DS}) & (V_{DS} < V_{GS} - V_T) \quad (linear) \end{cases} \tag{3}$$

The g_m in the saturation region is dependent on the overdrive voltage, $V_{DS-Sat} = V_{GS} - V_T$, whereas in the linear region it is dependent upon the drain to source voltage, V_{DS}. Mixing action can be enabled in (2) if the drain voltage, and therefore the g_m, of M_1 can be modulated via the source follower stage of M_2.

The AC waveforms at the gates of M_1 and M_2 are expressed by (4) and (5), respectively, where v_2 is a 180° shifted version of v_1 boosted by the series resonator and V_M is the magnitude of the OOK modulated signal that contains the baseband data.

$$v_1 = V_M sin(\omega t) \tag{4}$$

$$v_2 = -\beta V_M sin(\omega t) \tag{5}$$

The use of direct-conversion multiplication is taken advantage of by applying 180° out of phase signals at the v_1 and v_2 ports. This allows for a larger swing at the drain of M_1 from the constructively-interfering voltage outputs of the common-source M_1 stage and the source-follower M_2 stage. This effect is accounted for by the parameter α and has been simulated to provide a signal swing at the drain of M_1 nearly twice as large as the case where v_1 and v_2 are in phase. This effect has a direct increase on the conversion gain as will be shown in the following discussion. If the drain of M_1 is biased at the edge of the linear/saturation region, i.e. $V_{DS1} = V_{DS-Sat}$,

the periodically-varying $g_{m1}(t)$ can be described as in (6) where $f(t)$ is a half-wave-rectified sine wave described by the Fourier series in (7). This action is illustrated in Figure 18, where $g_{m1-Sat} = KV_{DS-Sat}$.

$$g_{m1} = K(V_{DS-Sat} - \alpha\beta V_M f(t)) \tag{6}$$

$$f(t) = \frac{1}{\pi} + \frac{sin(\omega t)}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{cos(2n\omega t)}{1-4n^2} \tag{7}$$

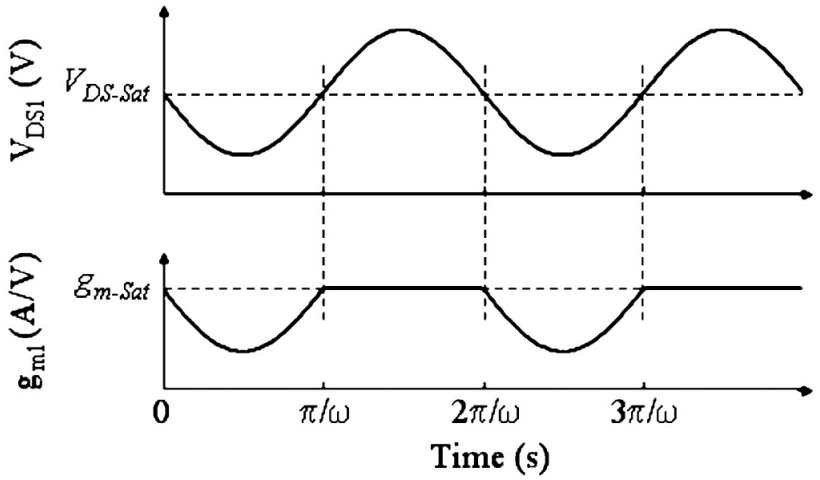


Figure 18: Small-signal transconductance, g_m, of M_1 modulated by M_2.

To evaluate the baseband mixing product, only the $sin(\omega t)/2$ term in $f(t)$ needs to be considered since the high-frequency terms will be filtered by the low-pass nature of the circuit. Therefore, the small-signal output current is given by (8). Expanding and again removing the high-frequency terms yields the small-signal output current given by (9).

$$i_{OUT} = v_1 g_{m1}(t) \approx V_M sin(\omega t)\left(g_{m1-Sat} - \frac{K\alpha\beta V_M sin(\omega t)}{2}\right) \tag{8}$$

$$i_{OUT} \approx -\frac{K\alpha\beta V_M^2}{4} \tag{9}$$

The voltage conversion gain is defined as the baseband output voltage divided by the magnitude of the input voltage. Assuming the output resistance is approximately equal to R_L, this is given by (10).

$$A_V = -\frac{i_{OUT} R_L}{V_M} \tag{10}$$

Plugging (9) into (10) shows the voltage conversion gain is proportional to input voltage magnitude, as in (11).

$$A_V = V_M \left(\frac{K\alpha\beta R_L}{4} \right) \tag{11}$$

Therefore doubling the LNA gain will quadruple the conversion gain of the entire receiver. Shown in Figure 19 is the simulated detector conversion gain versus input power where the conversion gain at the receiver minimum sensitivity (plus the LNA gain) has been indicated.

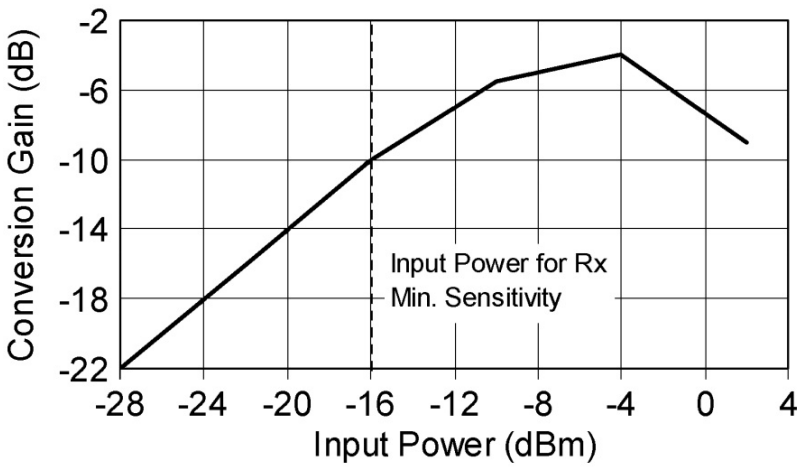


Figure 19: Detector conversion gain versus input power for a 61-GHz carrier.

Figs. 20 and 21 show a fabricated detector test structure and its measured $|S_{11}|$ performance, respectively. The measured results show a very good input matching around 60 GHz with greater than 10 GHz 10-dB input-matching bandwidth. The demodulator consumes 16 mW of DC power. The simulated 3-dB RF bandwidth is greater than 4 GHz.

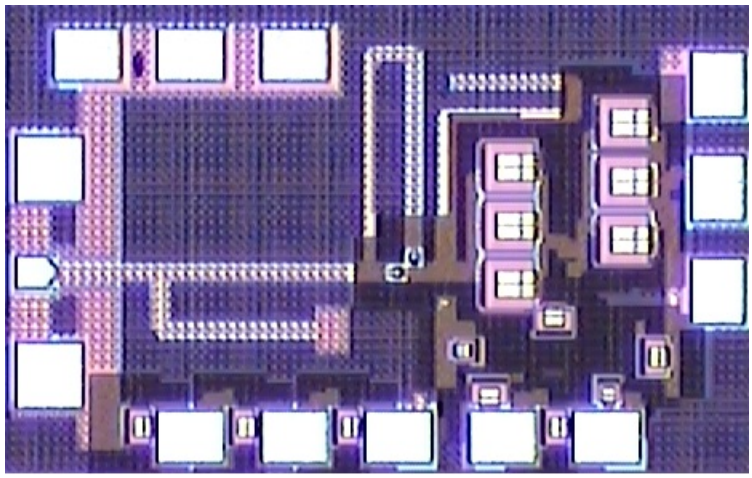


Figure 20: Detector test structure die photograph.

[32]

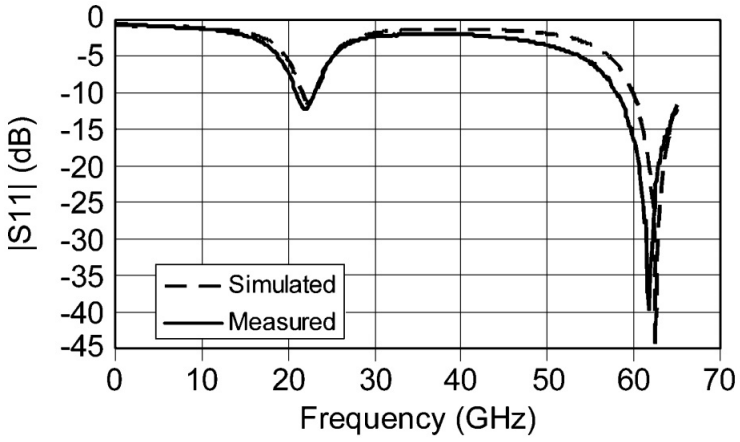


Figure 21: Detector test structure measured versus simulated $|S_{11}|$.

3.4 Integrated OOK Receiver Measured Results

Figure 22 shows the 60-GHz OOK receiver die photograph. The receiver occupies a die area of 1.8 mm x 1 mm. An external 60-GHz OOK modulator with pseudo-random binary sequence (PRBS) input was used to perform bit error rate (BER) measurements on the receiver for swept-power inputs at multiple data rates. Figure 23 shows the BER versus received input power. Figure 24 shows measured eye-diagrams of the digital baseband output for 1.728-Gbps and 3.456-Gbps data. The receiver consumes 108 mW of DC power and exhibits a noise figure of 8.5 dB at -40 dBm input. The minimum sensitivity of the receiver for 1.728-Gbps data at a BER of less than 10^{-6} is -40 dBm at the probing pad. Table 1 summarizes the measured performance alongside other reported 60-GHz OOK receivers.

Figure 22: 60-GHz OOK receiver die photograph.

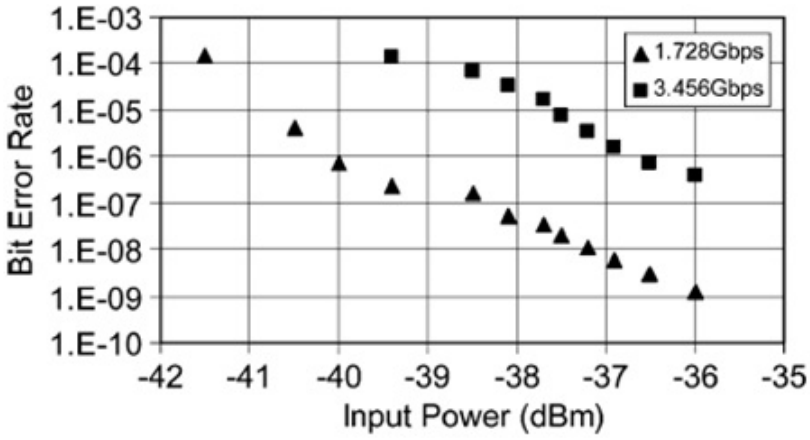


Figure 23: Receiver bit error rate versus input power.

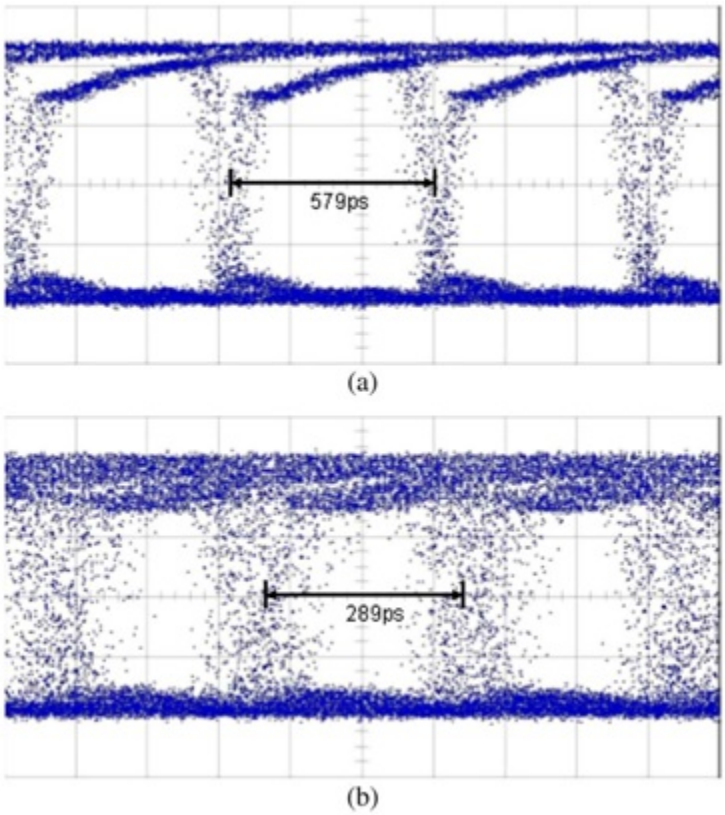


Figure 24: Measured eye diagrams for (a) 1.728-Gbps and (b) 3.456-Gbps data.

Table 1: 60-GHz OOK receiver comparison.

Reference	This Work, [41]	[42]	[43]
DC Power (mW)	108	800	103
Data Rate (Gbps)	3.5	>1	2.5
pJ/Bit	31	800	41
Modulation	OOK	ASK	OOK
NF (dB)	8.5	-	7
Process	90-nm CMOS	GaAs	90-nm CMOS

CHAPTER IV

HIGH-POWER, HIGH-EFFICIENCY 45-GHZ OSCILLATORS FOR LOW-OVERHEAD LO DISTRIBUTION

Mobile devices such as smartphones or tablets have very stringent power consumption requirements. Therefore as additional functions are added it is critical that they place as little burden as possible on the existing power budget of a given device or system platform. Due to the high degree of loss and directionality of wireless propagation at millimeter-wave frequencies, multi-element beam-forming transceivers will be an attractive solution for point to point communications [27]. Phase-shifting in the local oscillator (LO) path as opposed to the signal path is advantageous from a linearity perspective. However, a compelling argument against phase-shifting in the LO path is the increased power consumption resulting from parallel signal conversion paths and LO distribution [44]-[46]. However, this problem can be mitigated with the integration of a high-power, high-efficiency voltage controlled oscillator (VCO) that can reduce or eliminate the need for buffer stages or redundant oscillator structures, which must be phase-locked to a central signal.

This work presents the design of a single-ended output VCO based on a class-E power amplifier (PA) core and a single-ended input/differential output injection-locked oscillator (ILO) using a cross-coupled design in 45-nm SOI CMOS. These oscillators in conjunction with a passive distribution network can enable highly-efficient LO distribution for multi-element CMOS millimeter-wave transceivers such as MIMO or phased-array architectures. An example transmitter architecture utilizing the elements presented in this work is shown in Figure 25. For a specified central VCO

output power, P_{VCO}, required input power to lock the injection-locked oscillator, P_{INJ}, and the insertion loss of each power division in the LO distribution path, IL, the number of transceiver elements this type of architecture could support is given by (12).

$$No.of elements = 2^{\frac{P_{VCO}-P_{INJ}}{3+IL}} \tag{12}$$

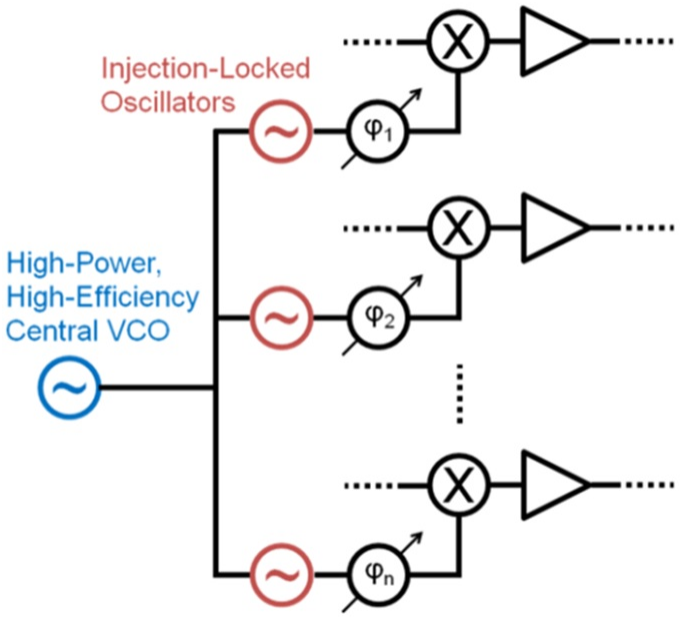


Figure 25: Example system using high-efficiency LO distribution.

4.1 Power amplifier classes of operation

Power amplifiers can be broadly classified into two categories: linear and switch-mode. In the linear case, the active device produces an amplified version of the input signal with varying degrees of non-linear distortion depending on its conduction angle. The conduction angle is defined as the period of the input waveform during which the active device is conducting current, in degrees. In the switch-mode case, the active device is utilized as a switch that is driven open and closed by the input waveform in a manner that results in all DC power being transfered to RF power, achieving

a theoretical efficiency of 100%. The penalty is completely non-linear behavior. Table 2 compares the basic classes of PA operation in terms of their conduction angle, linearity, and theoretical efficiency. Classes A through C are of the linear variety whereas classes D and above are switch-mode PAs. Although there are many more types of switch-mode amplifiers only the basic D, E, and F classes will be discussed in this work to explain the unique suitability of the class-E PA for millimeter-wave applications.

Table 2: Power amplifier classes of operation.

Class	Conduction Angle	Linearity	Theoretical Efficiency
A	360°	Best	50%
AB	180°-360°	Good	50-78.5%
B	180°	Moderate	78.5%
C	$< 180°$	Poor	78.5-100%
D, E, F...	0°	Non-Linear	100%

4.1.1 Linear Power Amplifiers

An example schematic of a linear power amplifier can be seen in Figure 26. It consists of an active device for amplification, an RF choke to the supply, V_{DD}, a DC blocking capacitor, and a resistive load.

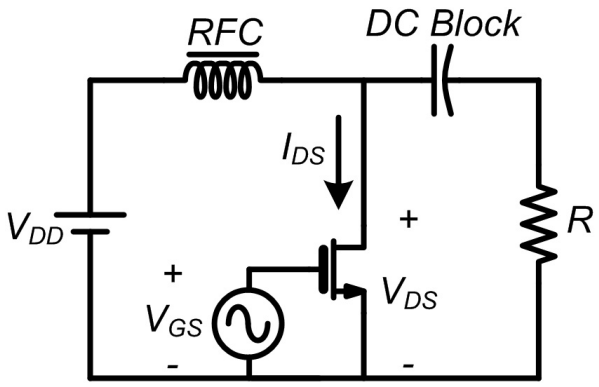


Figure 26: Example linear PA schematic.

The class-A power amplifier has a 360° conduction angle and therefore exhibits the highest linearity and poorest efficiency of all the PA classes. As shown in Figure 27, the active device conducts the output current I_{DS} during 100%, or 360°, of the input votage waveform, V_{GS}, resulting in a perfectly amplified copy of the sinusoidal input at the output. The theoretical efficiency, η, can be calculated by (13). Assuming a sinusoidal signal and for the ideal case where the knee voltage $V_K = 0$ and $V_{DD} = V_{DSmax}/2$, this reduces to 50%.

$$\begin{aligned} \eta &= \frac{P_{RF}}{P_{DC}} \\ &= \frac{V_{rms} I_{rms}}{V_{DC} I_{DC}} \\ &= \frac{\frac{V_{DSmax} - V_K}{2\sqrt{2}} \frac{I_M}{2\sqrt{2}}}{V_{DD} \frac{I_M}{2}} \end{aligned} \tag{13}$$

Similar waveform plots for the class-B, class-AB, and class-C PAs can be seen in Figs. 28- 30. Class-B PAs exhibit a 180° conduction angle and a theoretical efficiency of 78.5%. Class-AB PAs do not have as strict a definition and represent a popular tradeoff between linearity and efficiency whose operation lies somwhere between class A and class B, the exact value of which can be optimized for a specific application. Class C PAs have a conduction angle $< 180°$ resulting in a highly-distorted output but high efficiency. Although the class-C PA allows for a 0° conduction angle in its

extreme case, it is classified among the linear PAs due to its use of a linear active device for amplification. A more detailed and comprehensive discussion of linear power amplifiers can be found in [47].

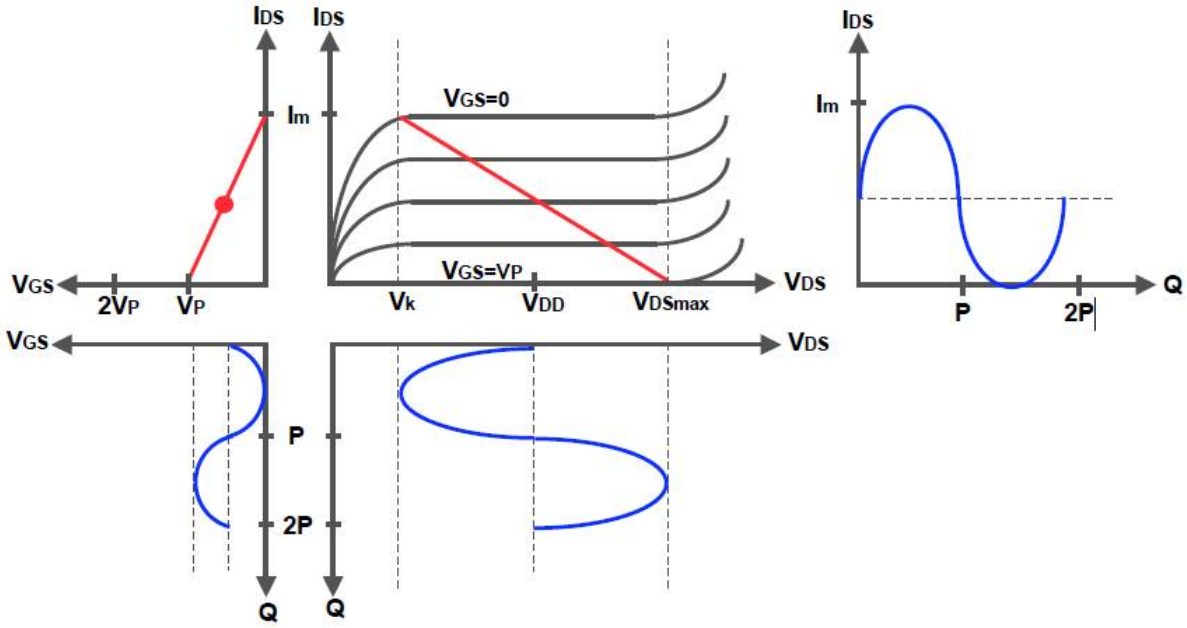


Figure 27: Class-A power amplifier waveforms.

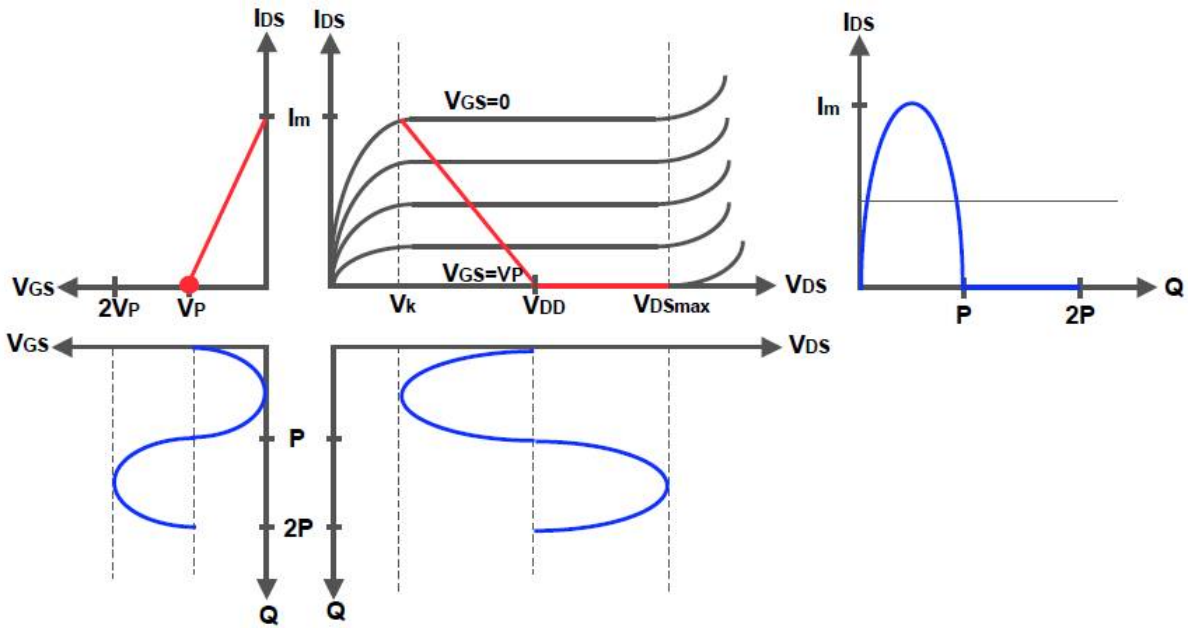


Figure 28: Class-B power amplifier waveforms.

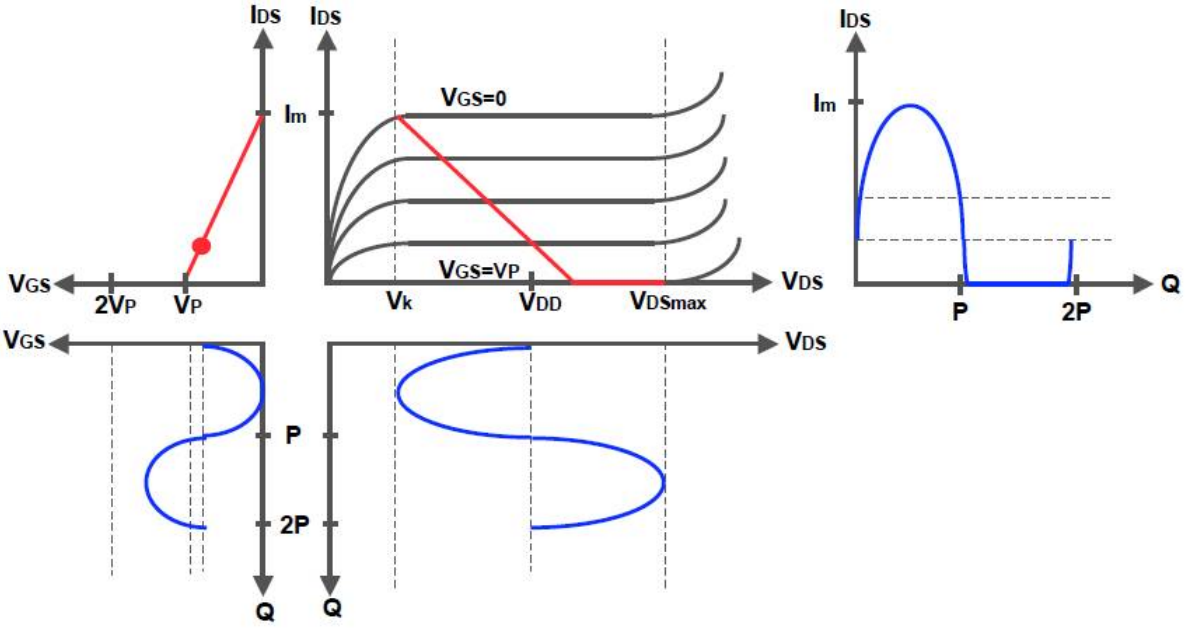


Figure 29: Class-AB power amplifier waveforms.

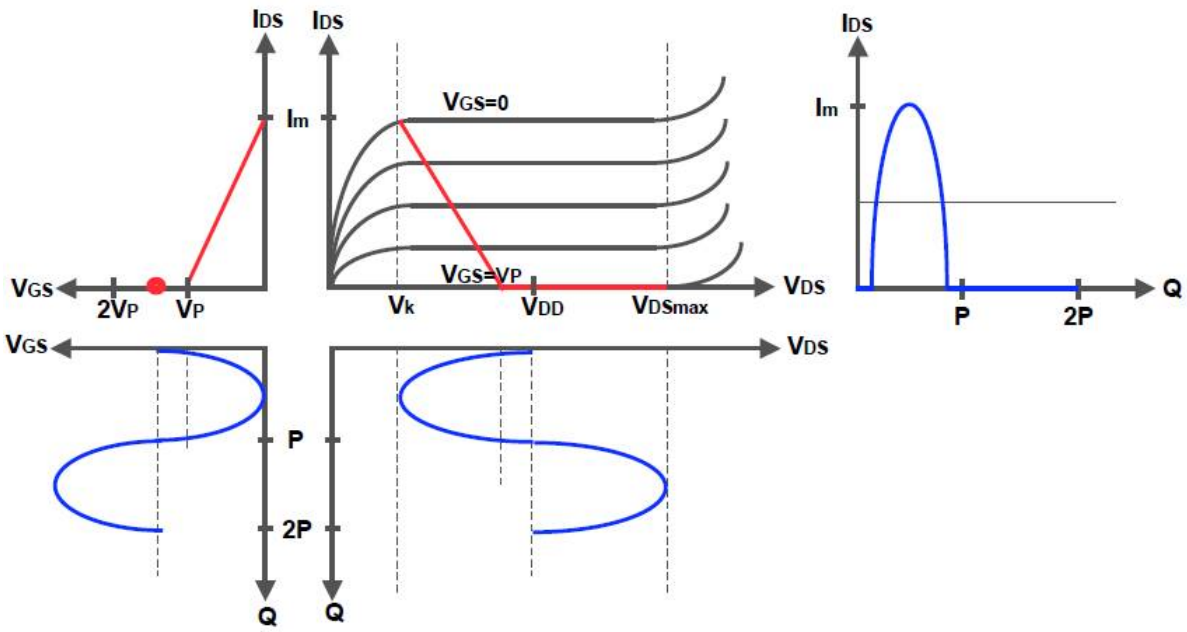


Figure 30: Class-C Power Amplifier Waveforms.

4.1.2 Switch-mode Power Amplifiers

4.1.2.1 Class-D Power Amplifier

The circuit schematic of the ideal class-D PA can be seen in Figure 31. It consists of a series resonant circuit formed by L_0 and C_0 connected to a single-pole double-throw switch. The series resonator is designed to force a sinusoidal current to flow through it and to the load R at the desired frequency. Figure 32 shows the voltage and current waveforms that constitute class-D operation.

The ideal switch is driven by a square wave at the desired frequency. While the switch is connected to the capacitor C, it is discharged by the current $i_1(t)$ that flows to the load resistor R contributing the positive-half sine wave at the output. When the switch is connected to ground, the capacitor C is charged from the V_{DD} through an RF choke. At the same time, the current $i_2(t)$ flows through the resonator in the opposite direction of $i_1(t)$ thus contributing the negative-half sine wave at the output. The summation of these two currents forms $i_0(t)$ at the output. Since there is no V-I

overlap in the switch waveforms, no DC power is consumed. Therefore all DC power is delivered to the output resulting in 100% efficiency.

This analysis is that of an ideal amplifier and therefore makes a number of assumptions about the circuit elements and their behavior. First, all elements are assumed to have infinite Q, such that no power is dissipated in the reactive components. Second, the existence of a perfect switch is assumed. In the practical case, a series/shunt configuration of transistors can be used to implement the switch. These transistors will have parasitic resistances and capacitances that will dissipate power and result in finite opening and closing times for the switch. At low frequencies, these parasitic elements will be easier to model or may even be negligible from an initial design standpoint. However, at millimeter-wave these non-idealities may play a dominant role in determining the waveforms of the circuit. In CMOS technology, two transistors will be needed to implement the single-pole double-throw switch, one in a common-source configuration and the other in a common-gate configuration. The common-gate transistor, which conducts the $i_1(t)$ path current, will be particularly difficult to model using empirical data. Because of the design and modeling complexity resulting from the need for two transistors the class-D PA is not chosen for millimeter-wave applications.

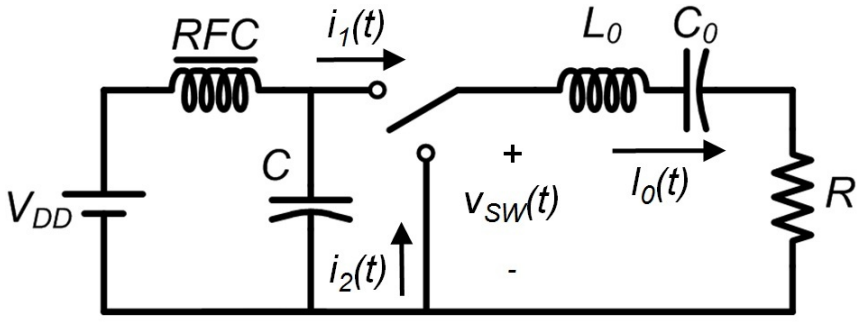


Figure 31: Class-D power amplifier schematic.

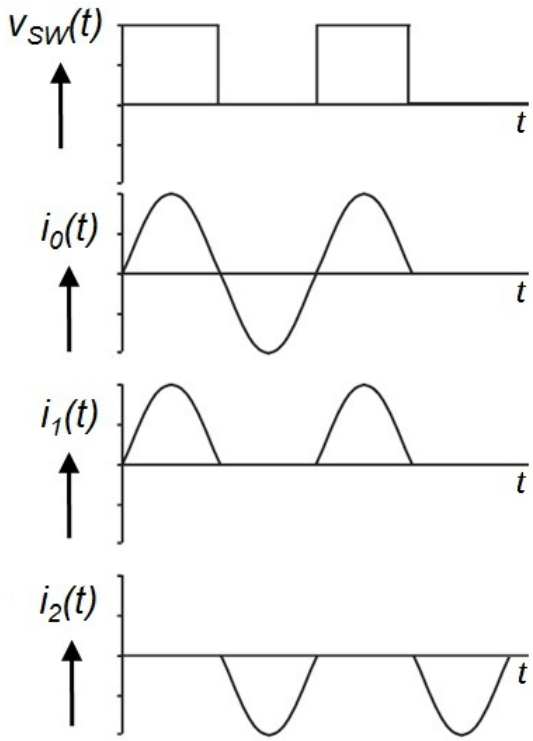


Figure 32: Class-D power amplifier waveforms.

4.1.2.2 Class-F Power Amplifier

If a rigorous definition is applied, the class-F PA might not truly be considered a switch-mode amplifier as its "switching device" is more likely biased like a class-B PA. However, harmonic control at the device output using parallel resonant circuits, as seen in Figure 33, causes the voltage waveform at the device drain to behave as if it were switched completely on and off. The voltage and current waveforms, $V_{Drain}(t)$ and $I_{Drain}(t)$, respectively, are shown in Figure 34. Looking out of the device drain, the odd harmonics of the fundamental signal see an open-circuit as a result of the parallel resonators in the signal path. The ideal case includes an infinite number of odd-harmonic resonators. This forces a square wave in $V_{Drain}(t)$ and a half-rectified sinusoid in $I_{Drain}(t)$. Therefore, no V-I overlap occurs at the device drain resulting in 100% efficiency.

Clearly, the fundamental practical limitation of the class-F amplifier is that an infinite number of parallel harmonic circuits cannot be included. The design choice then becomes how many harmonic circuits to include at the expense of circuit area and cost. Because of the large number of resonators required for harmonic control in the class-F and the unavailability of measurement equipment to verify suppression of harmonics of a millimeter-wave amplifier, the class-F structure is not chosen.

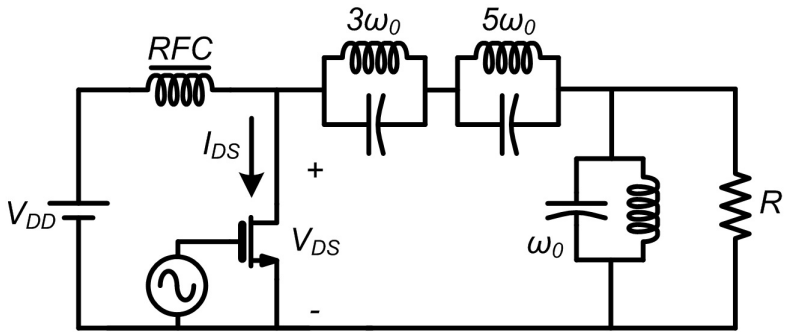


Figure 33: Class-F power amplifier schematic.

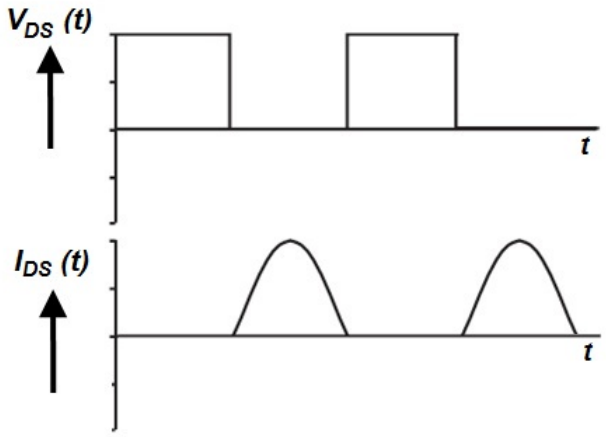


Figure 34: Class-F power amplifier waveforms.

4.1.2.3 Class-E Power Amplifier

Class-E PA operation was first described by Sokal and Sokal in [48] and optimal design equations were first presented by Raab in [49]. Raab also analyzed sub-optimum operation in [50]. The parallel-circuit class-E PA was introduced by Grebennikov and Jaeger in [51]. An examination of the loss mechanisms in parallel-circuit class-E PAs was later given by Lee et al. in [52]. The ideal Class-E power amplifier, as seen in Figure 35, consists of an ideal switch shunted by a capacitor C, a series resonant circuit formed by L_0 and C_0, the load resistance R, and an RF choke to V_{DD}. The effects of series inductor L can be separated mathematically from the series resonant circuit when designing, but L and L_0 are typically lumped together in one device. When a MOSFET is used as the switching device, its drain capacitance can be included in the shunt capacitor C and is no longer considered strictly "parasitic" to the circuit performance. At RF and millimeter-wave frequencies the drain capacitance will likely form the majority if not all of the shunt capacitance. It is for this reason that the class-E PA is chosen as a suitable structure for millimeter-wave operation, as will be discussed further in section 4.2.1.

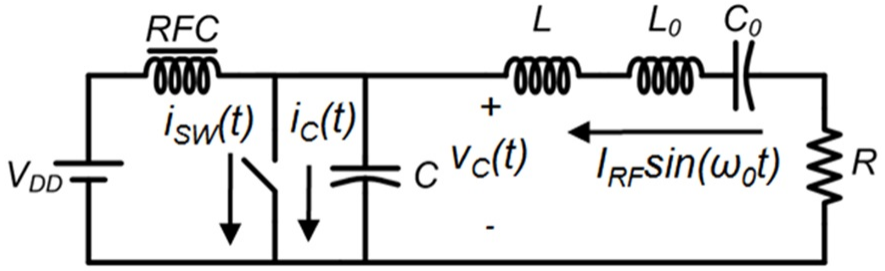


Figure 35: Class-E power amplifier schematic.

100% theoretical efficiency is achieved by implementing non-overlapping current and voltage waveforms in the switch. The series resonator $L_0 - C_0$ forces a sinusoidal current at the design frequency, ω_0. Given a specified load resistance R, the reacive components L and C can be chosen to produce waveforms like those shown

in Figure 36 such that the currents flowing into the switch and the capacitor during the switch closed and switch open periods, respectively, sum to form the sinusoidal current delivered to the load.

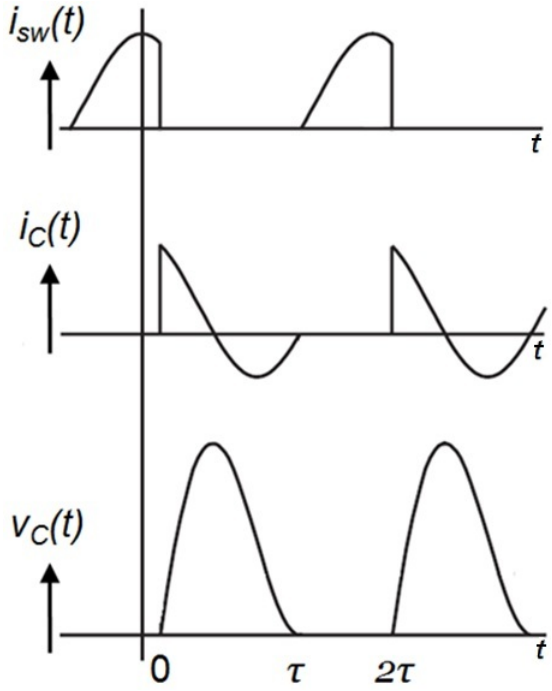


Figure 36: Class-E power amplifier waveforms.

The boundary conditions for the ideal switching condition are given by (14) and (15). At the time, t=τ, when the switch closes, the capacitor voltage and the first time derivative of the capacitor voltage must equal zero. Otherwise the resultant discharging of the capacitor through the closed switch would violate ideal class-E behavior and degrade efficiency. The parallel-class class-E amplifier has essentially the same functionality as the basic class-E amplifier. However, the RF choke at the VDD connection is replaced by a finite-valued inductor and explicitly accounted for in the design equations [11].

$$v_c(t)|_{t=\tau} = 0 \tag{14}$$

$$v_c(t)|_{t=\tau} = 0 \tag{15}$$

The ideal class-E (or parallel class-E) power amplifier can achieve an efficiency of 100%. This, of course, can never be realized in practice. However, the practical efficiency can be maximized through careful examination of major departures from ideal behavior that must happen in any real implementation, as will be discussed in section 4.2.1. Recent examples of class-E operation applied to oscillating structures in CMOS at RF frequencies can be seen in [53]-[55].

4.2 High-Efficiency, High-Power Millimeter-wave Class-E VCO

An essential piece of implementing a power efficient millimeter-wave phased array or LINC transmitter is low-overhead LO distribution. Integration of a high-power, high-efficiency oscillator can reduce or eliminate the need for buffer stages or redundant oscillator structures which must be injection locked to a central signal. This work utilizes the class-E PA topology to enable high-efficiency millimeter-wave oscillators for integration in such systems.

4.2.1 Millimeter-wave Class-E PA Core

In any real design, the class-E power amplifier can never achieve its theoretical 100% efficiency. However, the practical efficiency can be maximized through careful examination of major departures from ideal behavior that must happen in any real implementation.

The fundamental assumption for ideal class-E operation is the existence of a switch that can be opened or closed with zero rise/fall time and that dissipates no power. When using a transistor as a switch there will be an associated ON-resistance, r_{ds} for a MOSFET, which will dissipate power during the switch closed state thus degrading

efficiency. A simple approximation for the associated power loss is given by (16), where $P_{r_{ds}}$ and P_{DC} are the power dissipated by the switching transistor ON-resistance and the DC power, respectively [52].

$$\frac{P_{r_{ds}}}{P_{DC}} \approx 3.138\frac{r_{ds}}{R} \tag{16}$$

When designing at high frequencies, the parasitic drain capacitance C_{drain} of the switching transistor itself will often be used as the shunt capacitor. Based upon C_{drain}, the maximum operating frequency f_{max} (not to be confused with the f_{max} figure of merit for a transistor) can be defined for a parallel-circuit class-E PA by (17) [51].

$$f_{max} = 0.0798\frac{P_{out}}{C_{drain}V_{dd}^2} \tag{17}$$

If C_{drain} for the chosen transistor size is larger than the ideal class-E parallel capacitance, f_{max} will be pushed below the operating frequency f_0. This will result in an efficiency degradation caused by the inability of C_{drain} to be discharged completely before the device is switched on, causing an undesired current flow that violates ideal class-E behavior.

The efficiency degradations due to non-zero r_{ds} and f_0/f_{max} >1.1 present a tradeoff when selecting the size of the switching transistor. Using a larger device, for example, will have lower ON-resistance loss, but its increased drain capacitance may push the f_{max} below the operation frequency resulting in a diminishing return on efficiency improvement. Based upon the f_0/f_{max} efficiency degradation detailed in [50] and the r_{ds} degradation described by (16) an optimum f_0/f_{max} ratio of 1.4 was chosen resulting in a device size of 120 μm. This tradeoff is depicted graphically in Figure 37. Other sources of loss include the matching network, typically required to transform the 50-Ω system impedance to a lower impedance for the PA to drive, and the low-Q

DC feed inductance at the device drain.

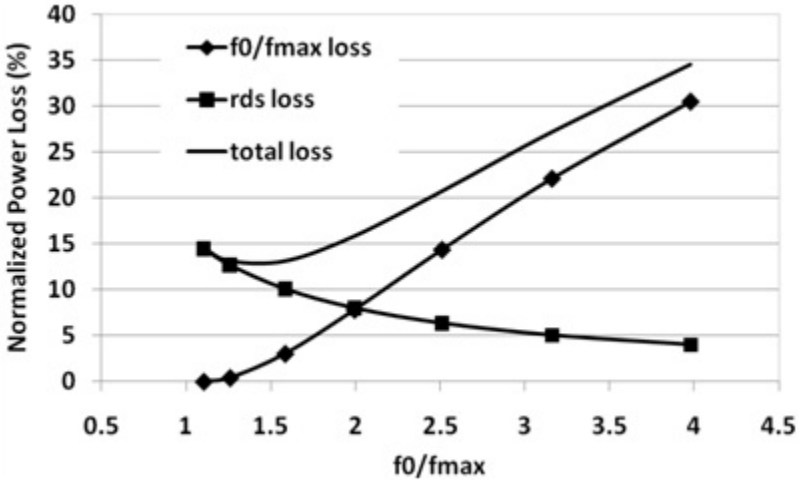


Figure 37: Optimizing the f_0/f_{max} ratio.

The millimeter-wave parallel-circuit class-E PA core can be seen in Figure 38 [56]-[58]. The input of the switching device is matched to 50-Ω using coplanar waveguide (CPW) transmission line. The parallel inductance at the MOSFET drain is realized by a CPW line to V_{DD}. The output matching network is designed to transform the 50-Ω output impedance, which can directly drive a passive 50-Ω LO distribution network, to a low driving impedance for the class-E structure while providing 2nd harmonic suppression via a $\lambda/4$ open stub at $2f_0$.

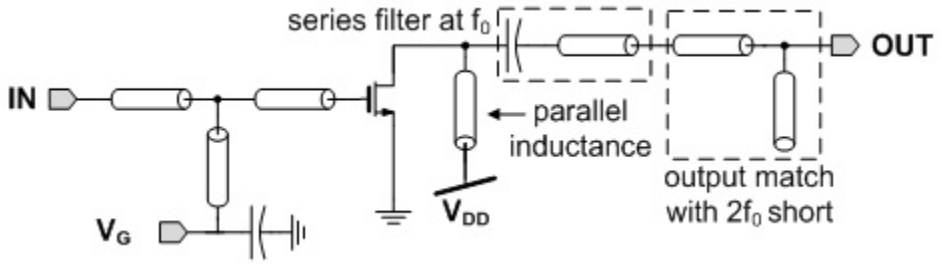


Figure 38: Millimeter-wave parallel-circuit class-E PA core.

As mentioned in section 4.1.2.3, a series resonator is needed to force a sinusoidal

current at the design frequency to flow to the load. This is realized with a series capacitor and transmission line so that the impedance presented to the device drain is low at the design frequency as shown in Figure 39. Shown in Figure 40 are the simulated drain voltage and current waveforms of the transistor exhibiting an out of phase relationship that minimizes the power dissipated.

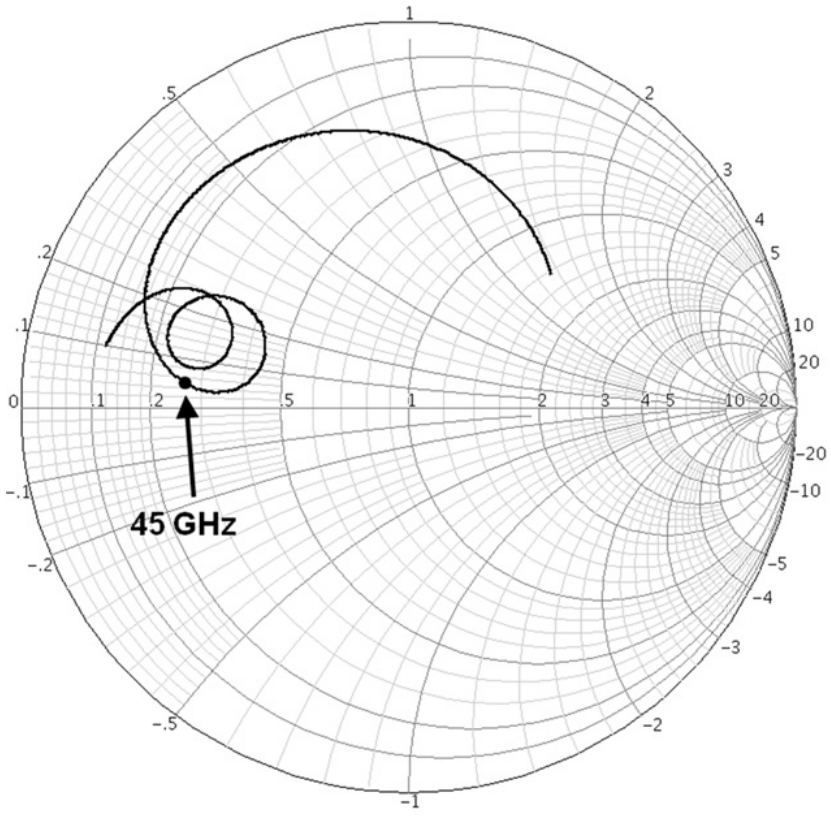


Figure 39: Class-E PA core simulated impedance looking out of the device drain.

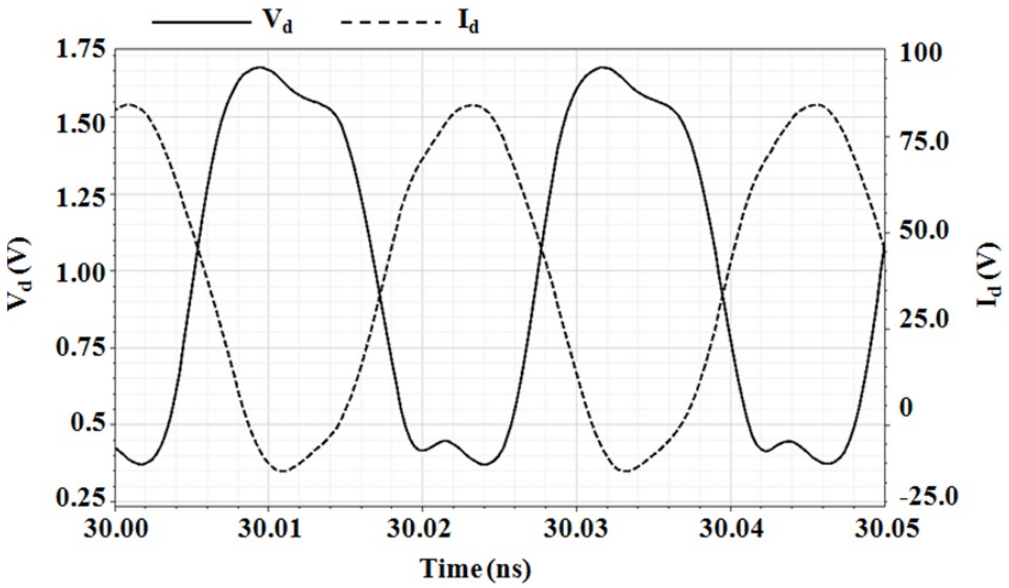


Figure 40: Simulated device drain voltage and current waveforms.

4.2.2 Millimeter-wave Class-E VCO

The millimeter-wave oscillator with class-E parallel-circuit PA core can be seen in Figure 41. Positive feedback is implemented by connecting the output and input with a series transmission line and a DC blocking capacitor. The line length is tuned so that the delay imposed by it plus the input matching network results in a 180° phase shift from the device drain to gate to satisfy Barkhausen oscillation conditions at the desired frequency.

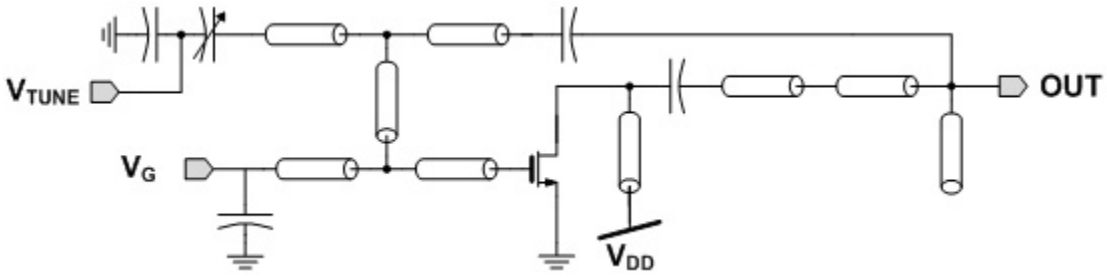


Figure 41: Millimeter-wave class-E VCO schematic.

Frequency tuning is implemented using a $\lambda/4$ stub terminated by a varactor to AC ground. The phase shift contributed by this structure can be approximated by (18), where C_{var} is the tuned capacitance of the varactor. The magnitude response of the phase shifter is approximated by (19), which indicates a greater than 3 dB loss for a phase shift larger than 45°. Eventually for higher phase-shifts, the PA core will not be able to recover the loss introduced by the feedback network in order to sustain oscillation. Therefore, the frequency tuning will be limited by the loop gain of the circuit.

$$\phi = \tan^{-1}\left(\frac{1}{2Z_0\omega C_{var}}\right) \tag{18}$$

$$mag = \frac{1}{\sqrt{1+\frac{1}{(2Z_0\omega C_{var})^2}}} \tag{19}$$

The oscillation frequency can be derived using the simplified circuit model seen in Figure 42. The amplifier gain A need not be stated explicitly and simply indicates a regenerative element in the loop which compensates for the power delivered to the load in Figure 41 and includes the input and output matching networks of the class-E core. The DC blocking capacitor in the feedback path is also excluded for simplicity.

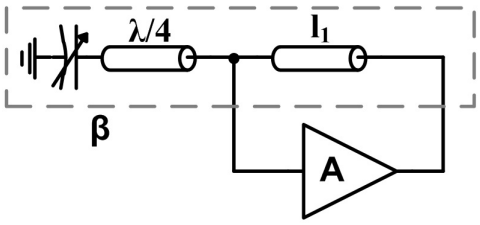


Figure 42: VCO simplified model.

To create a positive feedback condition the phase shifts of the amplifier, ϕ_A and the feedback network, ϕ_B, must sum to 2π as in (20), where ϕ_B is composed of ϕ_{l_1}

and ϕ_{stub}, the phase shifts of the series delay line l_1 and the $\lambda/4$ shunt stub network, respectively (20).

$$\phi_A + \phi_B = 2\pi \tag{20}$$

$$\phi_B = \phi_{l_1} + \phi stub \tag{21}$$

Letting $\theta = 2\pi$ - ϕ_A and approximating the phase shift of the $\lambda/4$ shunt stub network using (18), we find:

$$\beta_{l_1} + tan^{-1}\left(\frac{1}{2Z_0\omega C_{var}}\right) = \theta \tag{22}$$

In order to create a simple design equation we can use the approximation:

$$tan^{-1}(x) \approx \frac{\pi}{4}x, \quad -1 < x < 1 \tag{23}$$

This yields:

$$\omega\frac{l_1}{v_p} + \frac{\pi}{8Z_0\omega C_{var}} = \theta \tag{24}$$

Where we have substituted (25) and v_p is the phase velocity of the guided wave in the transmission line:

$$\beta = \frac{\omega}{v_p} \tag{25}$$

Rearranging (24) gives the quadratic equation:

$$\omega^2 \frac{l_1}{v_p} - \omega\theta + \frac{\pi}{8Z_0C_{var}} = 0 \tag{26}$$

The solution to which is (27) where the usable result is determined by what frequency the series resonant circuit in the class-E core will pass. This describes the oscillation frequency ω in terms of the design parameters l_1 and C_{var}.

$$\omega = \frac{v_p}{2l_1}\left\{\theta \pm \sqrt{\theta^2 - \frac{\pi l_1}{2v_p Z_0 C_{var}}}\right\} \tag{27}$$

Two versions of the class-E VCO were fabricated. Version 1 was included with the first fabrication in IBM 45-nm SOI CMOS, therefore no empirically-derived millimeter-wave models of the type described in chapter III were available while designing [56],[57]. Subsequent to characterization in measurement of both the VCO version 1 and device test structures, version 2 was designed using the custom millimeter-wave models and fabricated. The result was a 3.6 dB increase in output power as well as an increase in efficiency from 11.54% to 15.64%. Also, in order to demonstrate the usefulness of LCP as a millimeter-wave substrate, Version 1 was packaged in LCP and its performance unpackaged versus packaged is compared [58]. Seen in Figures 43 and 44 are the dimensioned circuit schematics of versions 1 and 2, respectively.

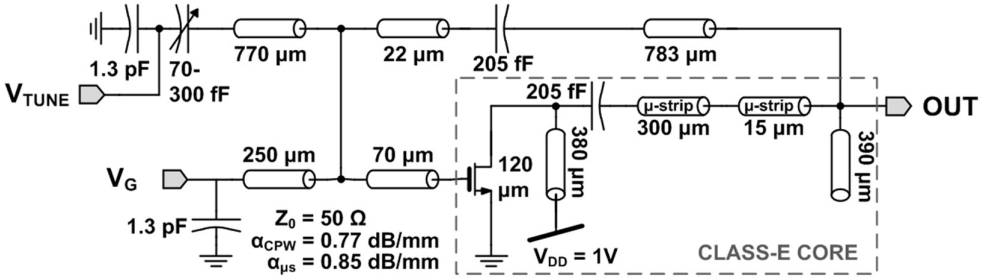


Figure 43: Class-E VCO version 1 schematic.

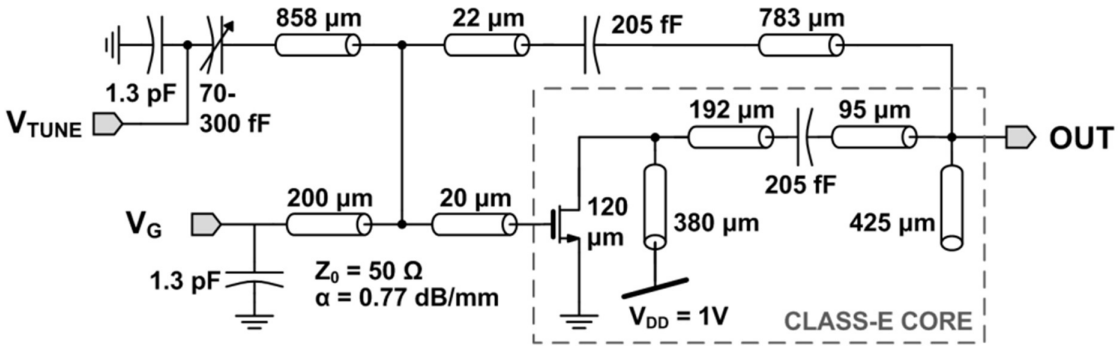


Figure 44: Class-E VCO version 2 schematic.

4.2.3 Millimeter-wave Class-E Oscillator Packaging on LCP

Version 1 of the oscillator was packaged on LCP substrate to verify its suitability for packaging CMOS at millimeter-wave frequencies. A double copper clad 20-mil 3850 LCP sheet from Rogers Corporation is used to package the oscillator. Precise alignment holes were drilled using a KrF 248-nm excimer laser. Attempting to bond gold wires directly to copper can be problematic. Therefore, the copper signal lines were electroplated with a 7-μm gold layer to ensure proper adhesion. Before gold plating, a seed layer of 150-$\mathring{A}$ Ti / 0.25-μm Au was created by evaporating titanium and gold to ensure proper gold deposition on LCP. Next, the feeding transmission lines were patterned on the top of the board using standard photolithography. Afterwards, gold and titanium etchants were used to etch the gold and titanium. After the patterning was completed, a CO_2 laser was used to ablate a cavity in the polymer down to the 18-μm Cu back-side metallization for the chip to be mounted in. For this step the back-side metal functions as a CO_2 laser stop layer. The laser cutting leaves behind some carbonized LCP residue in a small region around the cavity. This was first removed using acetone and isopropyl alcohol and then oxygen plasma was used to remove this thin residue. Next, the chip was mounted in the cavity with a high temperature inorganic conductive silver paste and wire bonded to the package.

Shown in Figure 45 is a die photograph of version 1 of the VCO, the circuit area

of which measures .55 mm x .82 mm. Figure 46 is a photograph of the packaged millimeter-wave CMOS oscillator. The CPW transmission line on the LCP package was designed using 3-D EM simulations performed in HFSS^{TM} to capture the effects of wire bonds. Figure 47 is a screen shot of the HFSS simulation setup that shows the modeling of the wire bond ribbons connecting the CPW interfaces on the CMOS chip substrate and the LCP substrate alongside a photograph of the actual wire bonds. Chip-package co-simulation was performed by de-embedding the wire bond/package s-parameter response to the interface of the wire bonds and the chip pads and generating an s2p file to import into the oscillator circuit simulation environment.

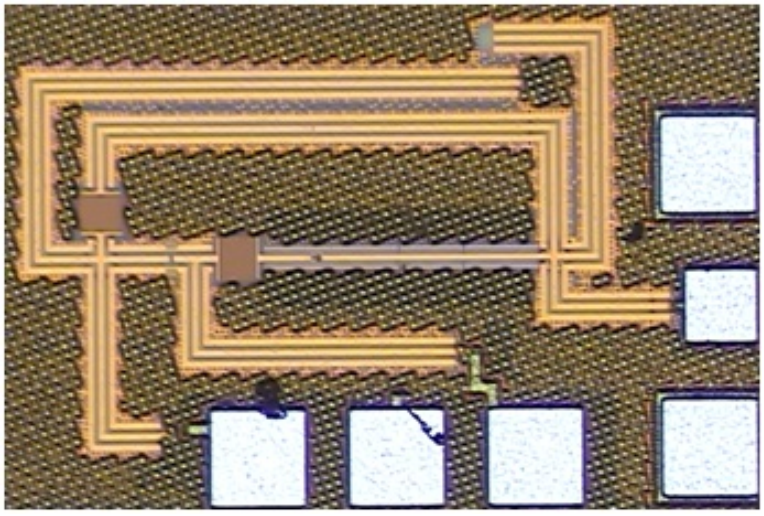


Figure 45: Class-E VCO version 1 die photograph.

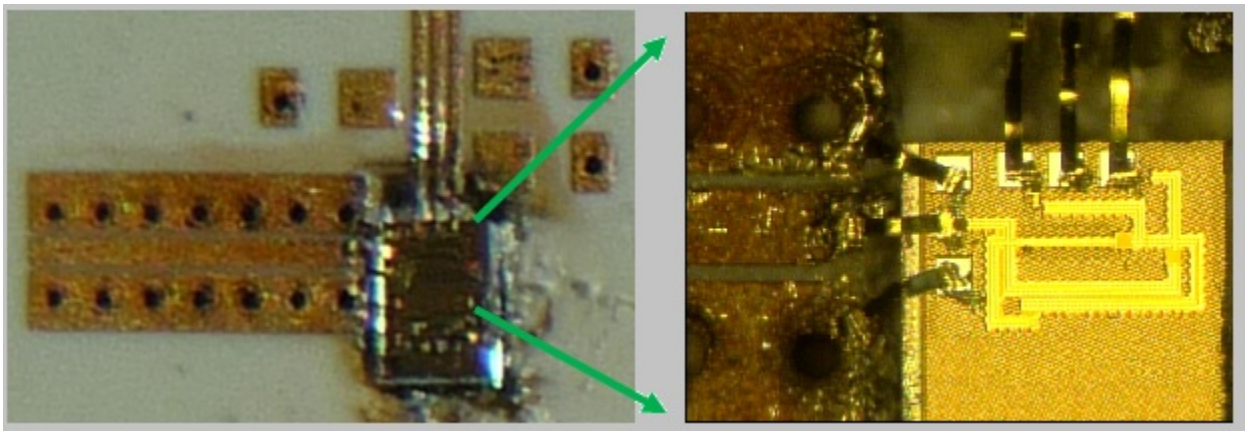
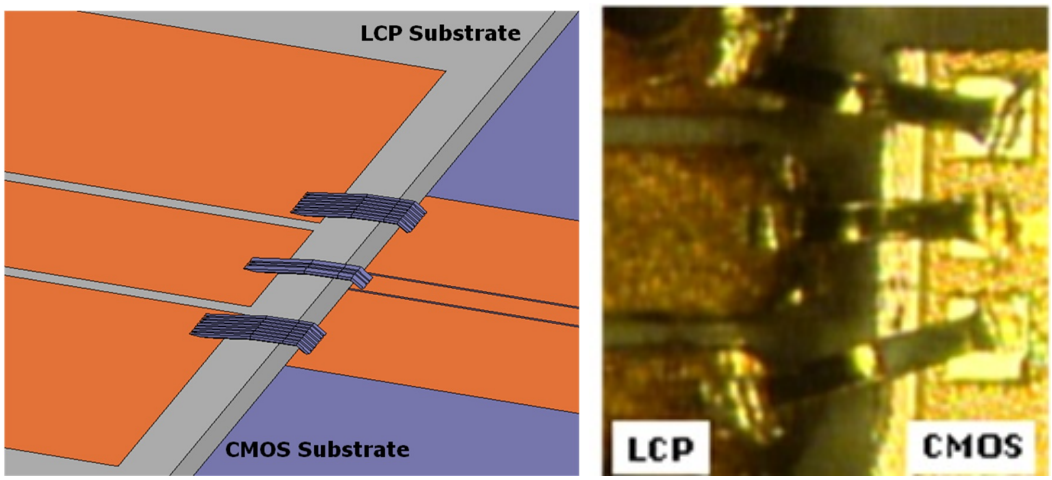


Figure 46: Class-E VCO packaged on LCP substrate.



(a) (b)

Figure 47: Screen shot of the HFSS simulation setup, (a), and photograph of the wire bonds, (b).

HFSS simulations indicated significant degradation of the impedance matching due to the series inductive effect of the wire bonds used to connect the CMOS die to the transmission line on the LCP substrate. In order to compensate for this and improve the input matching the CMOS chip will see at the wire bond interface, capacitive stubs were added to transmission line on the LCP substrate, as depicted in

Figure 48. The optimized stubs measured 20 μm wide by 500 μm long and improved the package input matching in simulation by $>$ 5 dB near the oscillator center frequency of 41 GHz. Figure 49 shows the simulated results of the packaging input matching with and without the capacitive compensation stubs. Unfortunately, the manufacturing precision did not allow for fabrication of these compensation stubs.

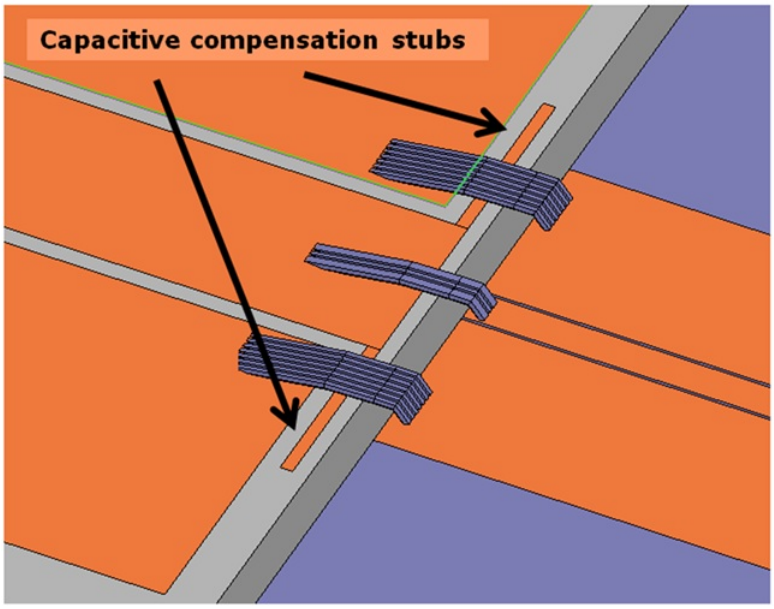


Figure 48: HFSS screen shot showing capacitive compensation stubs.

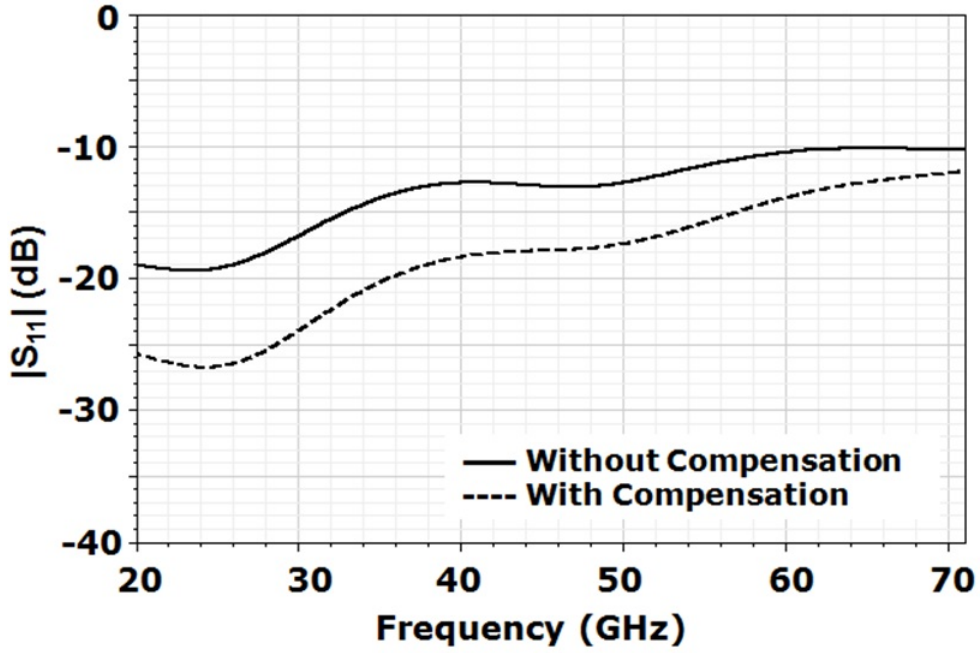


Figure 49: Simulated results of the packaging input reflection coefficient with and without the capacitive compensation stub.

4.2.4 Millimeter-wave Class-E VCO Measured Results

4.2.4.1 Millimeter-Wave VCO Version 1

The oscillator performance was measured both packaged and unpackaged to determine the effects of the LCP packaging [58]. Plots of the measured output spectrum for the unpackaged and packaged cases are shown in Figs. 50 and 51, respectively. Note: the spectra do not include power deembedding of the measurement setup. Seen in Figure 52 is the simulated and measured data for output frequency versus tuning voltage.

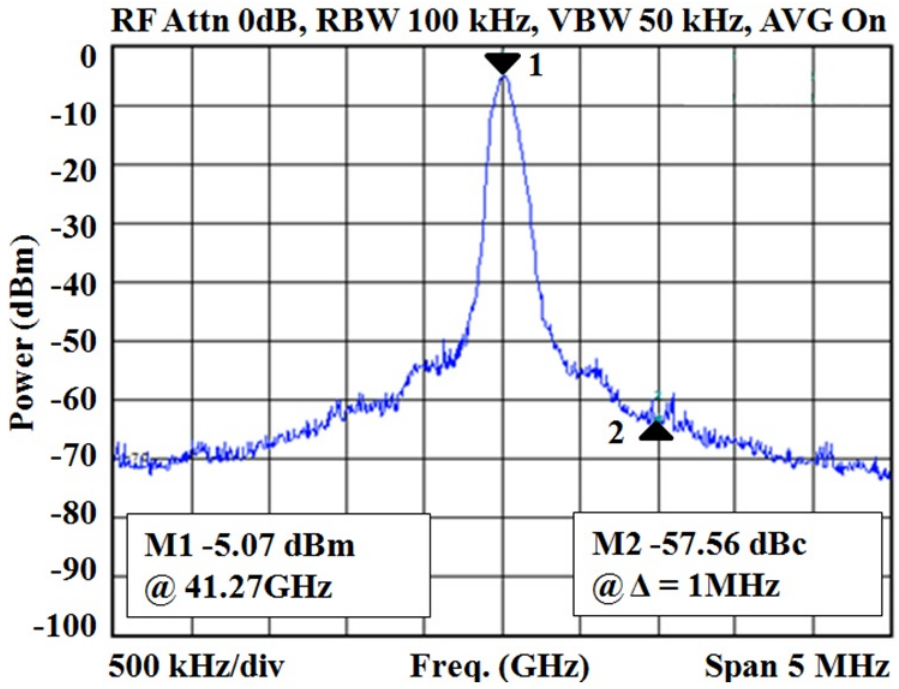


Figure 50: Class-E VCO version 1 measured output spectrum, unpackaged.

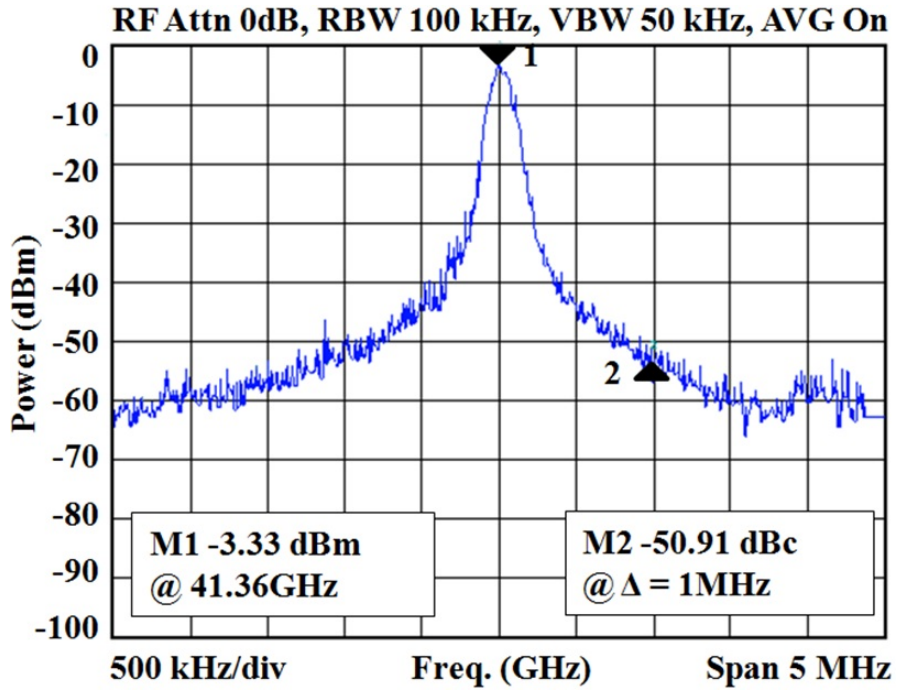


Figure 51: Class-E VCO version 1 measured output spectrum, packaged.

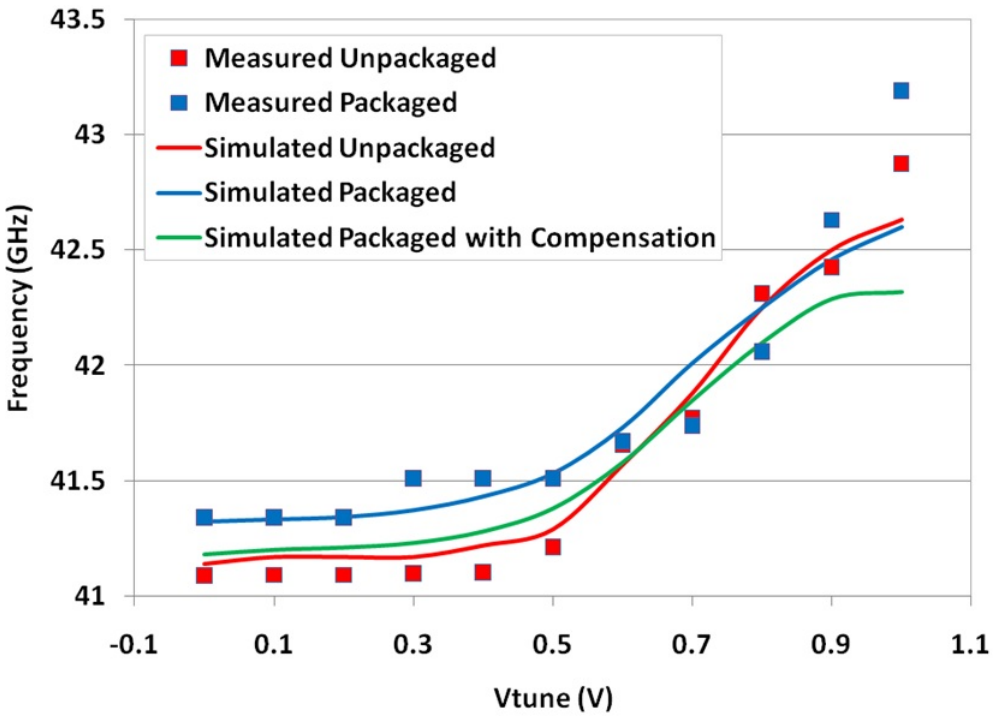


Figure 52: Class-E VCO version 1 output frequency, packaged versus unpackaged.

There is a 250-MHz up-shift in frequency for the packaged oscillator, which is consistent with the predictions of the simulator. The oscillator is tunable between 41.08 and 42.07 GHz for the unpackaged case and 41.32 and 42.60 GHz for the packaged case. Figure 53 shows the simulated and measured data for output power versus tuning voltage. As is predicted by equations (18) and (19) a drop-off in power is observed for higher tuning voltages, corresponding to lower varactor capacitances. This power drop-off was experienced at lower frequencies than anticipated due to a downshift in the loop frequency resulting from the unavailability of accurate millimeter-wave circuit element models prior to CMOS fabrication. The LCP packaging results in a < 1 dB loss of output power for most of the tuning range, which is also consistent with the simulated data. The measured phase noises for the unpackaged and packaged oscillator are shown in Figs. 54 and 55, respectively. The phase noise measurements were taken at 41.08 GHz for the unpackaged oscillator and 41.63 GHz for

the packaged oscillator. In both cases these measurements were taken inside the low-frequency/high-power regions of the tuning curves. Table 3 summarizes the oscillator performance for both the packaged and unpackaged cases.

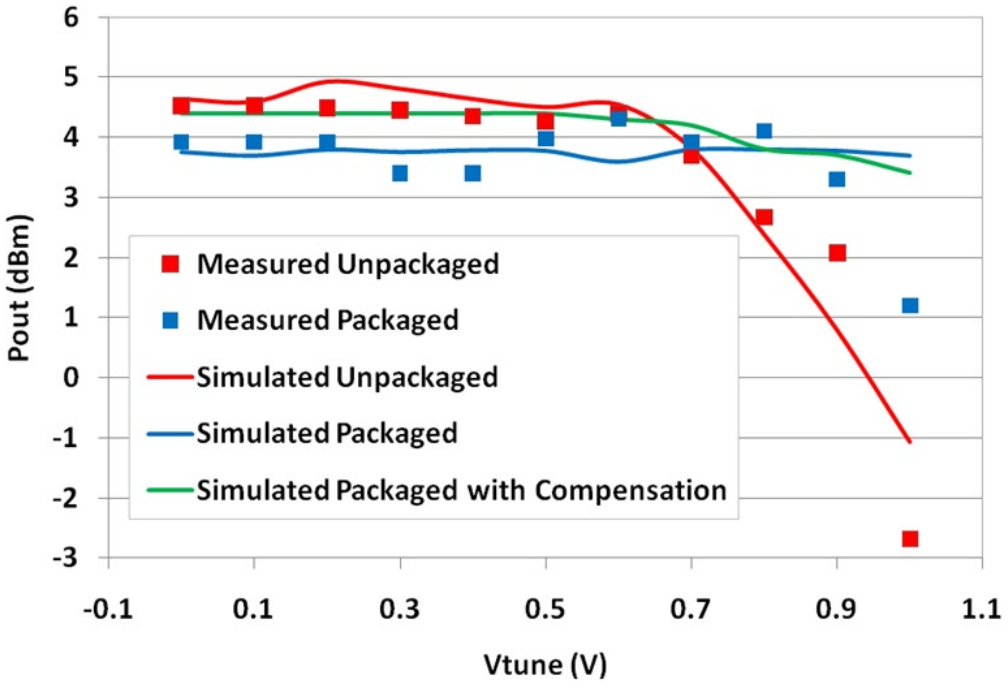


Figure 53: Class-E VCO version 1 output power, packaged versus unpackaged.

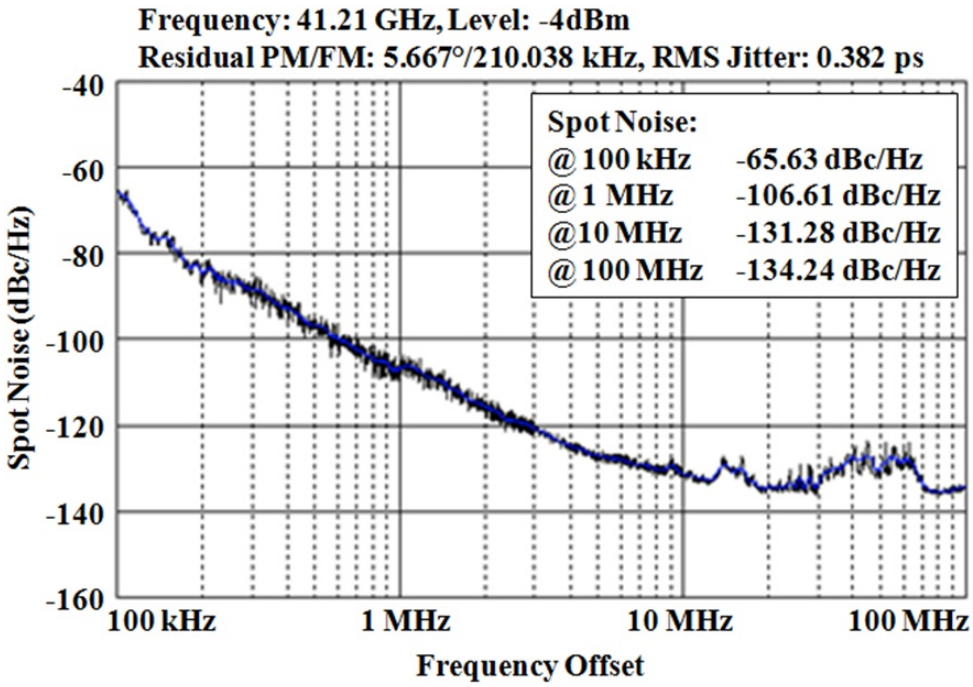


Figure 54: Class-E VCO version 1 measured phase noise, unpackaged.

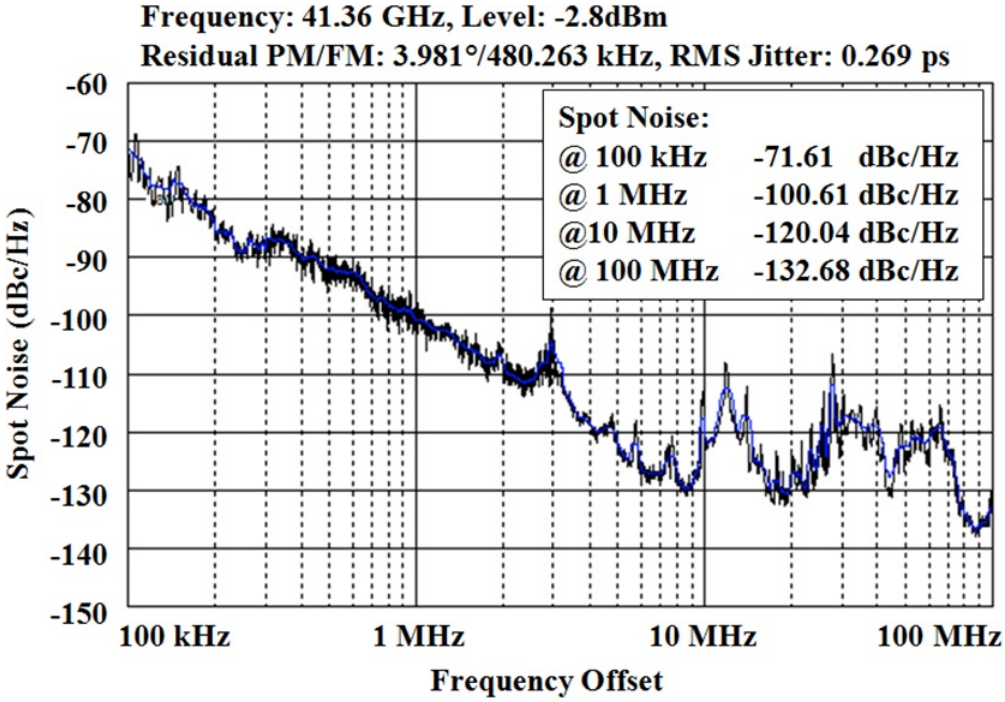


Figure 55: Class-E VCO version 1 measured phase noise, packaged.

Table 3: Class-E VCO version 1 performance comparison packaged versus unpackaged.

Characteristic	Unpackaged Die	Packaged on LCP
Efficiency	11.54%	9.89%
Frequency	41.08-42.87 GHz	41.32-43.20 GHz
Pout Max.	+4.6 dBm	+4.2 dBm
Ph. Noise @ 1 MHz	-106.61 dBc/Hz	-100.61 dBc/Hz

4.2.4.2 Millimeter-Wave VCO Version 2

Figure 56 shows a die photograph of the VCO version 2. Figure 57 and Figure 58 show the VCO measured output spectrum and phase noise, respectively. Note that the spectrum does not include any power deembedding from the measurement setup. Figure 59 shows the measured oscillation frequency and output power versus Vtune for both simulated and measured cases. The VCO achieves a peak output power of 8.2 dBm while consuming 42.24 mW of DC power, yielding a peak efficiency of 15.64%. The tunable range is 45.5-47.5 GHz. Table 4 compares the performance of this design with other silicon-based monolithic millimeter-wave VCOs with high reported efficiencies. Although the standard oscillator figure of merit (28) does not reward high power efficiency, which is the novelty of this work, it has been included in the table for fair comparison.

$$FOM = L(\Delta f) + 20log\left(\frac{\Delta f}{f_0}\right) + 10log\left(\frac{P_{DC}}{1mW}\right) \tag{28}$$

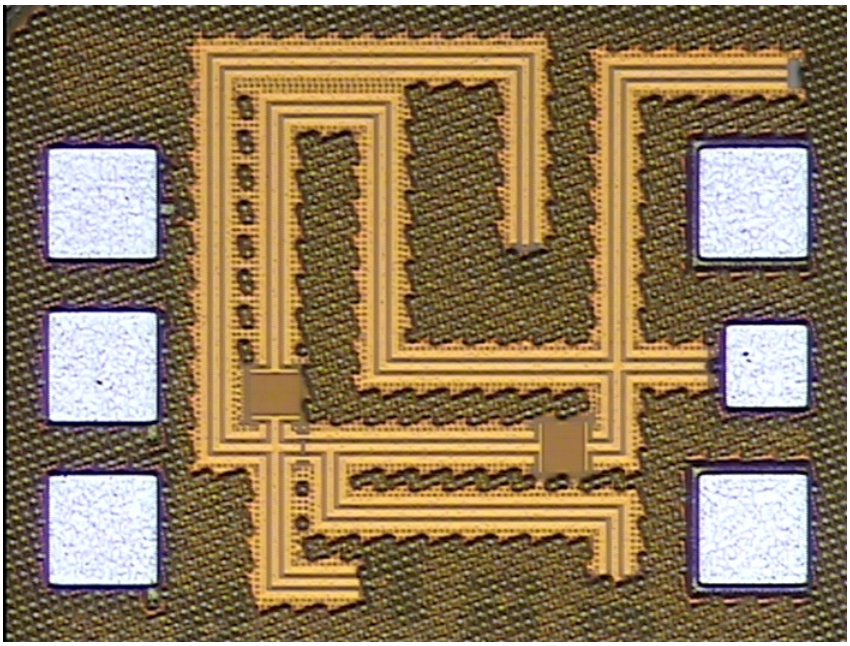


Figure 56: Class-E VCO version 2 die photograph.

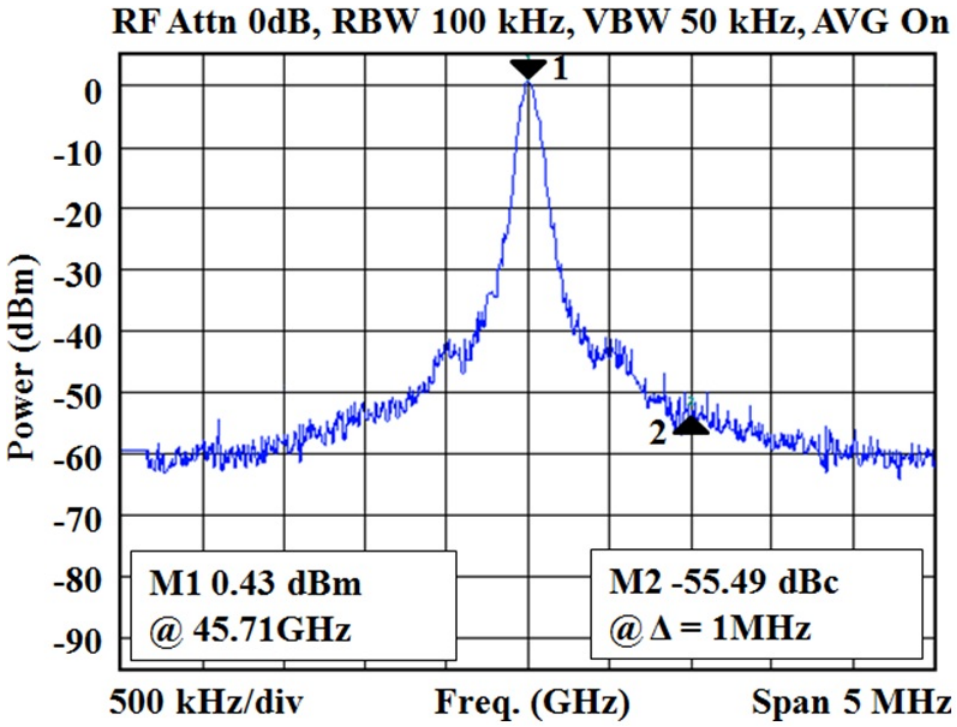


Figure 57: Class-E VCO version 2 measured output spectrum.

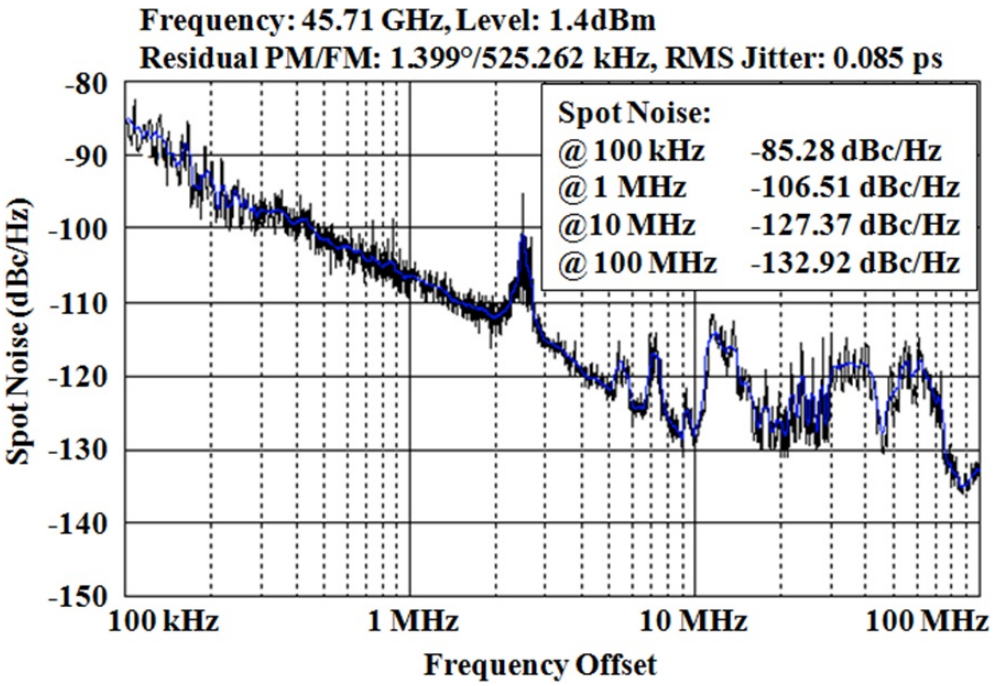


Figure 58: Class-E VCO version 2 measured phase noise.

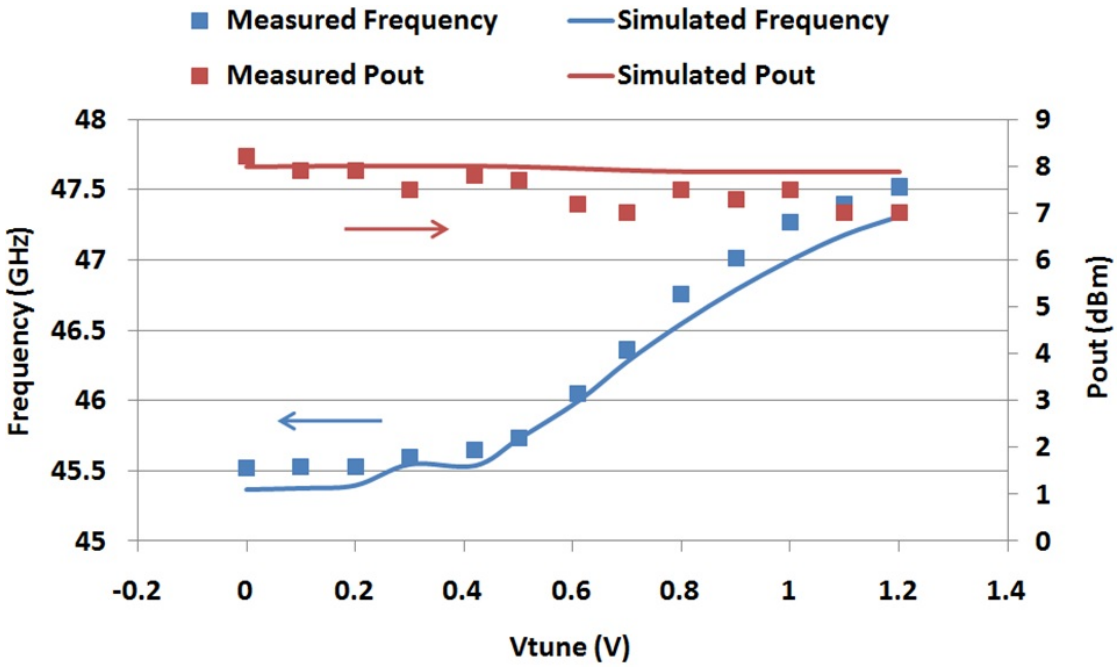


Figure 59: Class-E VCO version 2 measured versus simulated output power and frequency.

Table 4: Class-E VCO version 2 performance versus recent publications.

Reference	This Work	[59]	[60]	[61]
Efficiency	15.64%	21.8%	8.95%	6.57%
Frequency	45.5-47.5 GHz	55.5-62.9 GHz	26.85-27.5 GHz	41-44.5 GHz
Pout. Max.	+8.2 dBm	-6.8 dBm	-3.5 dBm	-2 dBm
Ph. Noise @ 1 MHz	-106.51 dBc/Hz	-94 dBc/Hz	-113 dBc/Hz	-106 dBc/Hz
FOM	-183.4 dBc/Hz	-179.7 dBc/Hz	-194.6 dBc/Hz	-192.7 dBc/Hz
Die Area	.58 mm x.71 mm	.30 mm x.25 mm	.58 mm x.55 mm	.70 mm x.40 mm
CMOS Process	45-nm SOI	90-nm SOI	130-nm	65-nm

4.3 Injection-Locked Oscillator

4.3.1 Injection-Locked Oscillator Design

The schematic of the injection-locked oscillator can be seen in Figure 60. It consists of a cross-coupled NMOS core where the LC tank is formed by micro-strip transmission line inductances and the parasitic gate and drain capacitances of the active devices themselves. All transistors and lumped passive elements use the millimeter-wave modeling approach described in Chapter 2. The core drives common-source output buffers optimized to drive a 50-Ω load. For measurement purposes, one phase of the differential output is terminated on-chip with a 50-Ω load. Signal injection is performed by a pseudo-differential common-source NMOS pair that share drain connections with the cross-coupled pair. The gates of the injecting devices are matched to 50 Ω to interface with the integrated Marchand balun, which allows for a single-ended input. This allows single-ended LO distribution across a chip which can simplify signal routing

and save die area.

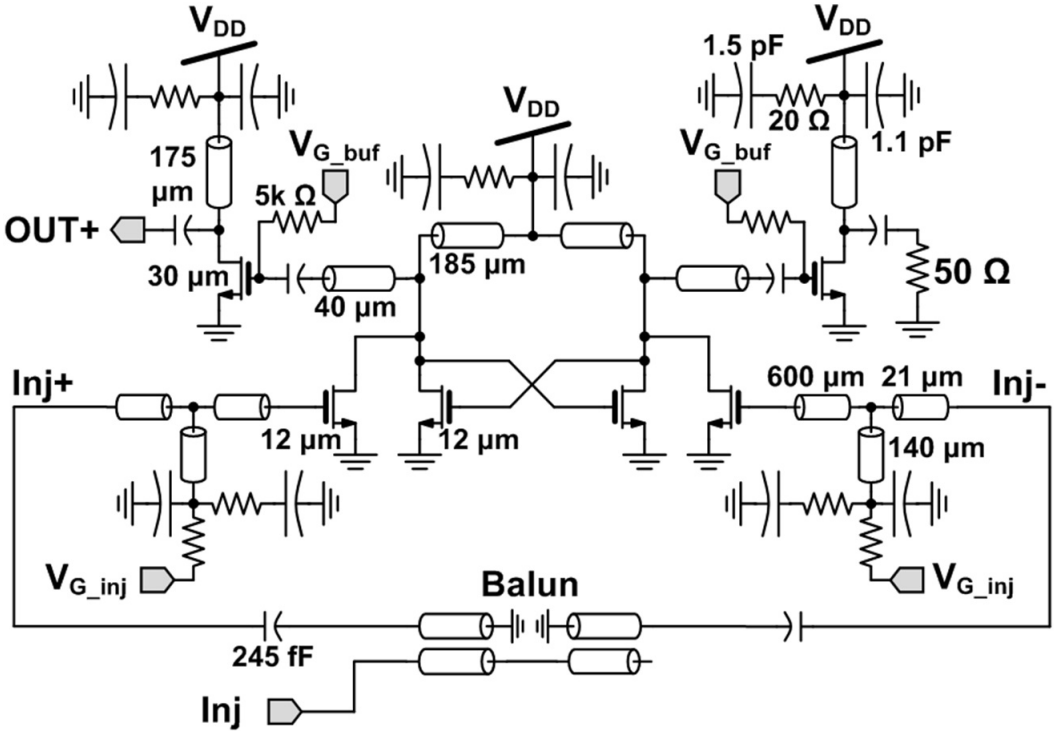


Figure 60: Millimeter-wave ILO schematic.

4.3.2 Injection-Locked Oscillator Measured Results

The die area of the ILO is .55 mm x .82 mm. Figure 61 shows a die photograph of the ILO. The Marchand balun can be seen clearly on the left side of the die after the GSG input pads. As was mentioned before, only one phase of the differential output is taken off-chip for measurement purposes while the other is terminated on-chip. Figure 62 and Figure 63 show the ILO output spectrum and phase noise plots, respectively, where the ILO has been locked to an external signal source whose specified and typical phase noise levels are -97 dBc/Hz and -103 dBc/Hz at a 100-kHz offset from the main tone, respectively. At a 1-MHz offset the specified and typical values are -118 dBc/Hz and -125 dBc/Hz, respectively. Figure 64 shows the minimum input power versus frequency required to lock the oscillator as well as the measured output power resulting from the minimum injected power at each frequency. The output

power is taken to be 3-dB higher than was actually measured since one phase of the differential output was terminated on-chip. The ILO consumes 54.3 mW of DC power (21 mW in the core) and has a maximum output power of 5.2 dBm. This results in a power-added efficiency (PAE) of 6.1% for the minimum locking power at the oscillator center frequency, which is competitive with state of the art millimeter-wave power amplifiers. The ILO exhibits a locking range of 3 GHz for an input power of -10 dBm As given by (12), for the system of Figure 25 and assuming a corporate feed network with 0.6 dB of insertion loss per power divider, the presented VCO+ILO could support a 32-element array.

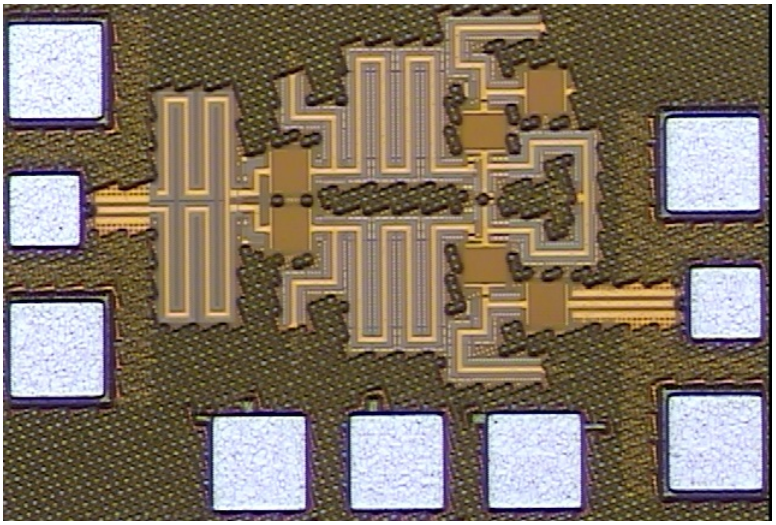


Figure 61: ILO die photograph.

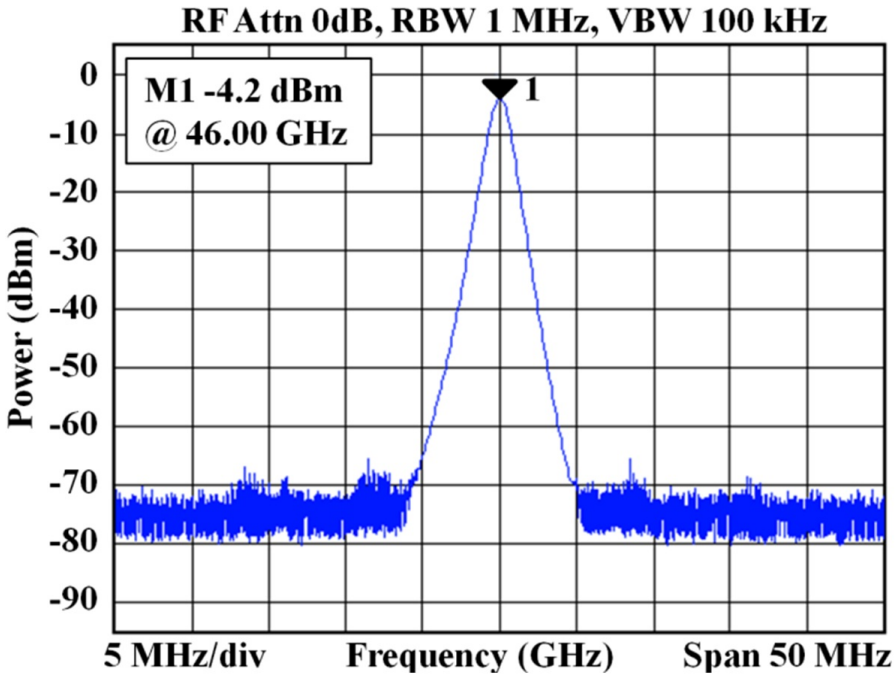


Figure 62: ILO locked output spectrum.

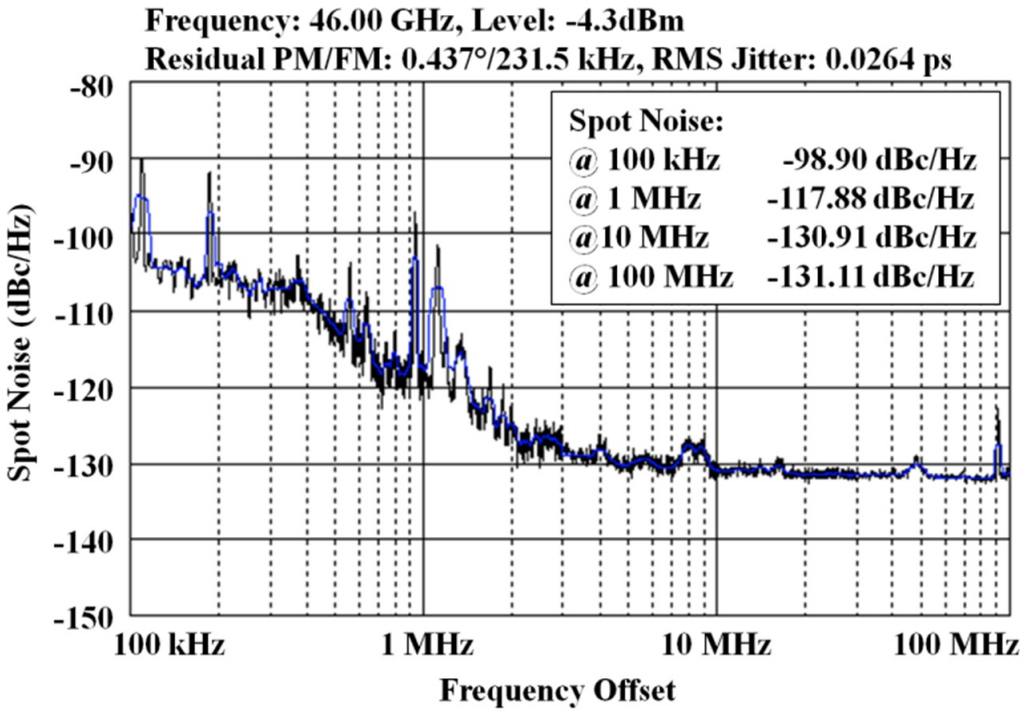


Figure 63: ILO locked phase noise.

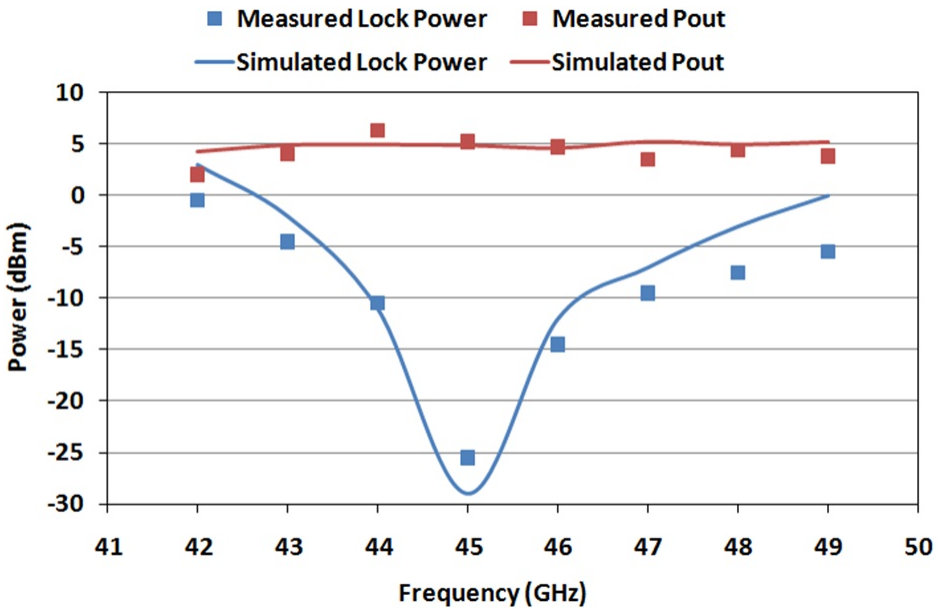


Figure 64: ILO locking injected and output power levels versus frequency.

CHAPTER V

45-GHZ 2-CHANNEL VECTOR MODULATOR FOR LINC/BEAM-FORMING TRANSMITTERS

Most recent silicon-based millimeter wave transceivers in the communications realm have focused on simple single-carrier modulation schemes like BPSK [62], [63], OOK [41], [43], and QPSK [64] due to their low complexity and because they do not require a (highly) linear transmitter. For higher-order, non-constant-envelope modulation formats like 16-QAM or multiple-carrier air interfaces such as OFDM, a linear power amplifier would need to be operated with sufficient backoff so as to not distort the output signal [65], [66]. When designing a system to be included in a mobile device, this loss of efficiency and transmitted power is an undesirable tradeoff [67]. Nevertheless, millimeter-wave communications specifications, such as those drafted by the WiGig alliance for the 60-GHz band [28], support the inclusion of such higher-order modulation schemes. These concerns motivated the design of a LINC transmitter at 60 GHz employing free-space power combining in [68]. In this work continuous 360° degree millimeter-wave phase shifters are employed to enable outphasing modulation using a linear amplification using non-linear components (LINC) architecture [69], [70]. This allows for the use of non-linear and high-efficiency PAs while maintaining linear signal amplification.

There have been many millimeter-wave phase-shifters reported recently but most have targeted beamforming architectures and therefore may have less than 360° tuning ranges [71]-[75], or have discrete tuning steps [76]-[78]. Either precludes their use in an outphasing modulator. Digitally controlled artificial dielectric (DiCAD) phase shifters were used to implement a flexible direct frequency modulator in [79]. The

modulator itself is very low power (< 10 mW), however, the phase-shifter limitations require that a quadrant I/III vector sum modulation be used. Therefore there will be a substantial loss in efficiency by having to use a backed-off linear PA to amplify the combined signals if a non-constant-envelope modulation scheme is used.

This work presents the design of a 2-channel 45-GHz vector modulator in 45-nm SOI CMOS that can be combined with high-efficiency non-linear power amplifiers, integrated or external, to achieve a high-efficiency, high-linearity LINC transmitter. In addition to its application in an outphasing modulation, the design is readily scalable to support an architecture with a higher number of phase-shifted outputs such as a beam-forming system. Also designed is a 45-GHz Wilkinson power combiner on a liquid crystal polymer (LCP) substrate. The CMOS die was mounted in the LCP substrate and driven via external DACs to have flexible modulation capabilities. To the best of the author's knowledge, this is the first work that demonstrates a silicon-based outphasing 16-QAM modulation in the Q-band.

5.1 LINC/Outphasing Background

Any phase/amplitude modulated signal can be decomposed into two constant amplitude signals with phase differences proportional to original signal amplitude [69], [70]. These component signals now carry no information in their amplitude and can be amplified by a non-linear, high-efficiency amplifier. After this amplification stage the components can be summed to produce a linearly amplified version of the original signal as described by (29)-(31). The classical LINC architecture is shown in Figure 65(a) where the modulated signal $S(t)$ is split into its constituent waveforms $S_1(t)$ and $S_2(t)$ by a dedicated block. An alternative approach is shown in Figure 65(b) where $S(t)$ is generated by summing the outputs of two independently modulated phase shifters. This work presents the design of a 2-channel vector modulator to support the latter architecture.

$$\begin{aligned} S(t) &= A(t)cos(\omega t + \phi(t)) \\ &= S_1(t) + S_2(t) \end{aligned} \tag{29}$$

Where,

$$S_1(t) = \frac{A_{max}}{2} cos(\omega t + \phi(t) + \theta(t)) \tag{30a}$$

$$S_2(t) = \frac{A_{max}}{2} cos(\omega t + \phi(t) - \theta(t)) \tag{30b}$$

$$\theta(t) = cos^{-1}\left(\frac{A}{A_{max}}\right) \tag{31}$$

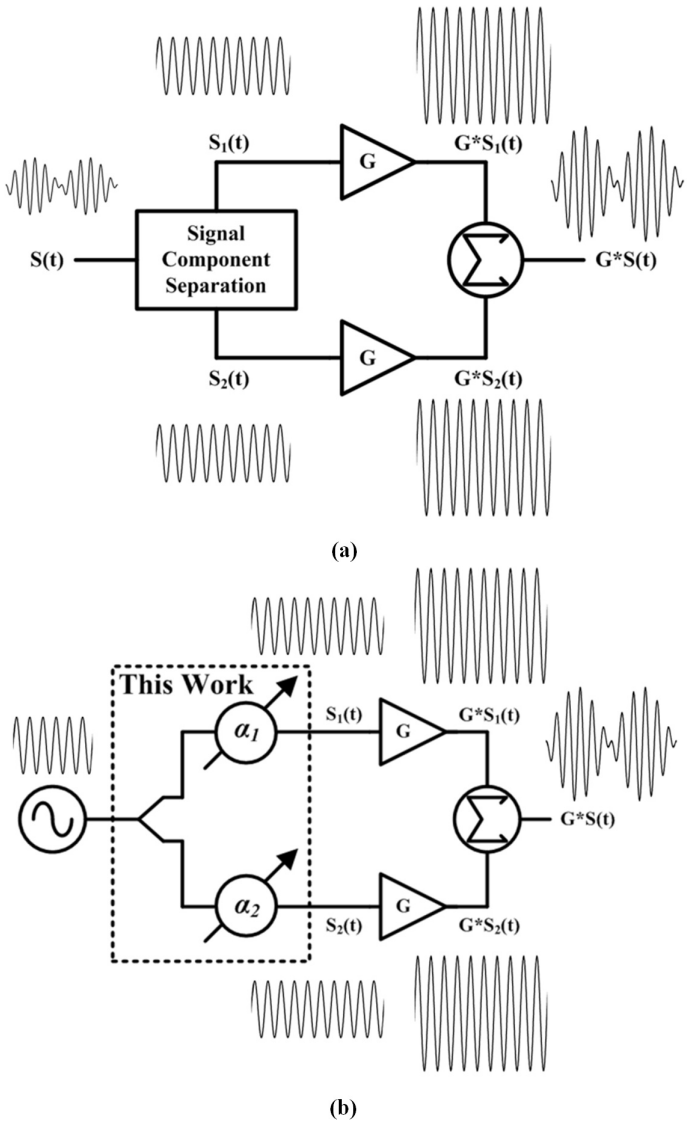


Figure 65: (a) Classical LINC architecture (b) Phase modulation LINC.

5.2 Low-Power 2-Channel CMOS Millimeter-Wave Vector Modulator for LINC Transmitters

The millimeter-wave vector modulator consists of two identical channels that can be independently modulated with continuous 360° vector rotation. A block diagram can be seen in Figure 66. The system is optimized to receive a single tone input at 45 GHz and produce two independently modulated outputs that can be combined to support an outphasing modulation scheme. However, the system can be easily scaled

to a higher number of outputs to support a beam-forming architecture, wherein the input would be a modulated carrier. For the purpose of discussion, the system can be divided into the passive IQ generation network and the active Gilbert cell modulators.

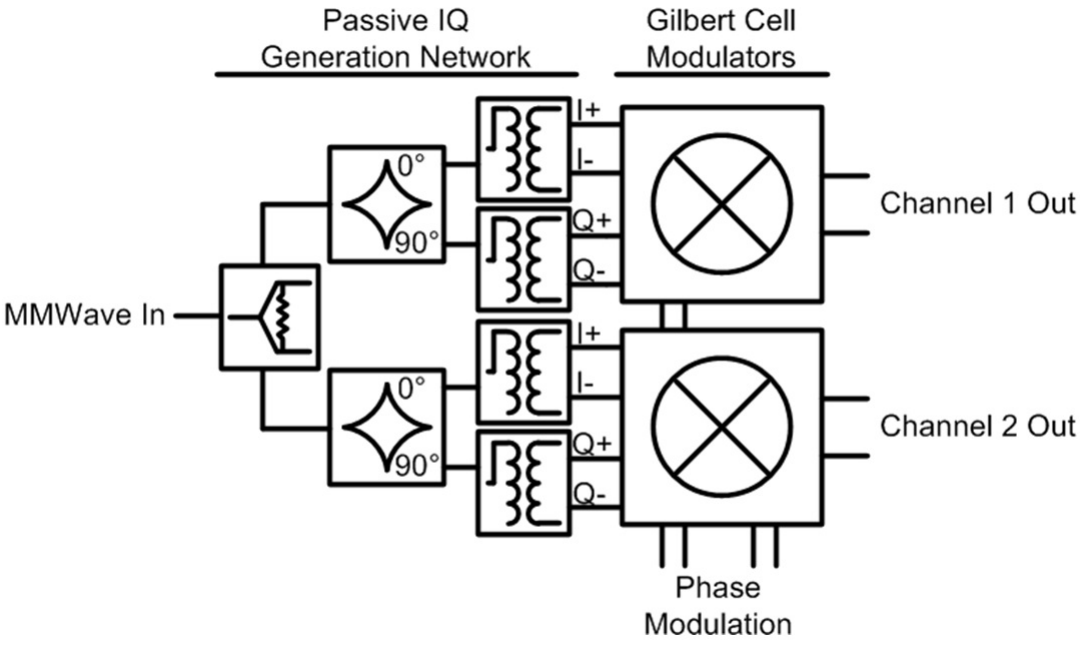


Figure 66: 2-Channel millimeter-wave vector modulator block diagram.

5.2.1 Passive Quadrature Generation and Signal Distribution

The input signal to the modulator is split between the two channels using a Wilkinson power divider implemented with micro-strip transmission line where the signal line was in the thick top metal and the ground plane consisted of a lower, thin-metal mesh. The schematic for the Wilkinson power divider is shown in Figure 67. Quadrature signals are then generated using a 90° hybrid implemented by a branchline coupler with coplanar waveguide transmission line with signal and ground paths in the thick top metal, the schematic of which can be seen in Figure 68. Metal line width rules for the design kit dictated that the high-impedance ($50\sqrt{2}\ \Omega$) lines for the Wilkinson divider, and the low impedance ($50/\sqrt{2}\ \Omega$) lines for the branchline coupler be designed using different transmission-line structures. The balun was implemented as a

vertically coupled structure using the top two thick metals of the design kit. Figure 69 shows the schematic for the Marchand balun.

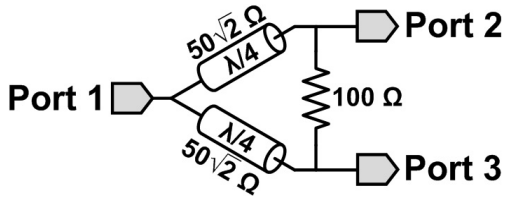


Figure 67: CMOS Wilkinson power divider schematic.

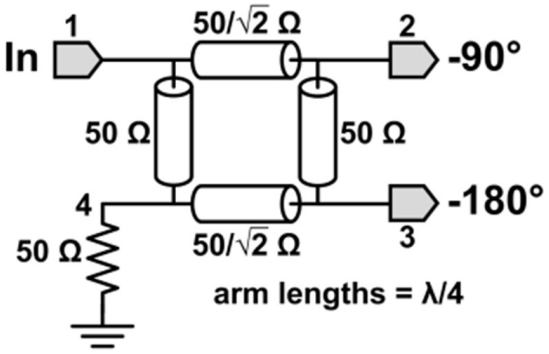


Figure 68: CMOS branchline coupler 90° hybrid schematic.

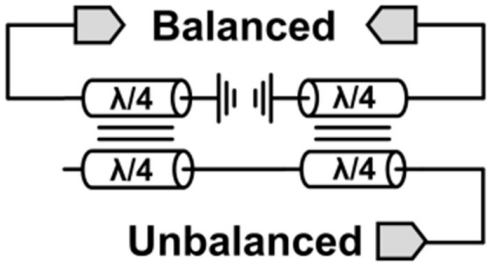


Figure 69: CMOS Marchand balun schematic.

The passive distribution networks were designed using Mentor IE3D^{TM} and Agilent ADS^{TM} . Shown in Figs. 70- 76 are the simulated S-parameters for the CMOS Wilkinson power divider, Marchand balun, and 90° hybrid branchline coupler. The

Wilkinson power divider shows better than -12-dB input matching on all ports and an insertion loss of 1.9 dB at 45 GHz. The Marchand balun has better than -22-dB matching at its unbalanced port and -7-dB matching on its balanced port. The insertion loss of the balun is 1.7 dB at 45 GHz. The quadrature hybrid has 2.75 dB of insertion loss at 45 GHz.

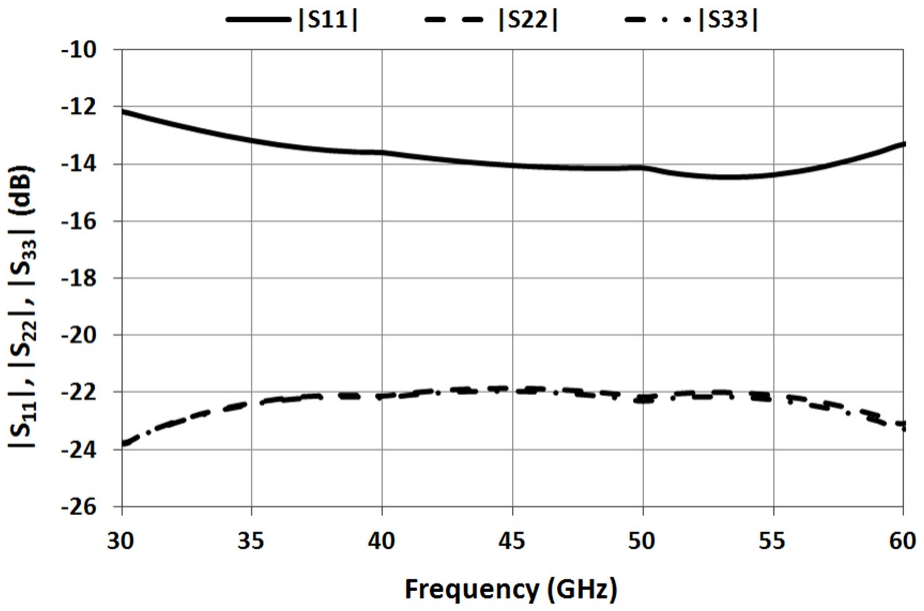


Figure 70: CMOS Wilkinson power divider simulated $|S_{11}|$, $|S_{22}|$, and $|S_{33}|$.

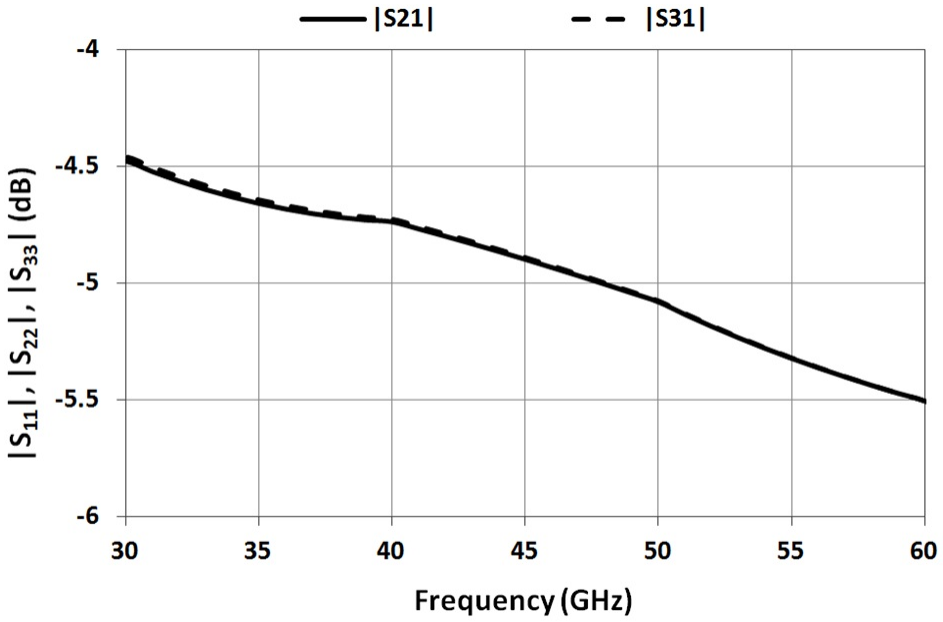


Figure 71: CMOS Wilkinson power divider simulated $|S_{21}|$ and $|S_{31}|$.

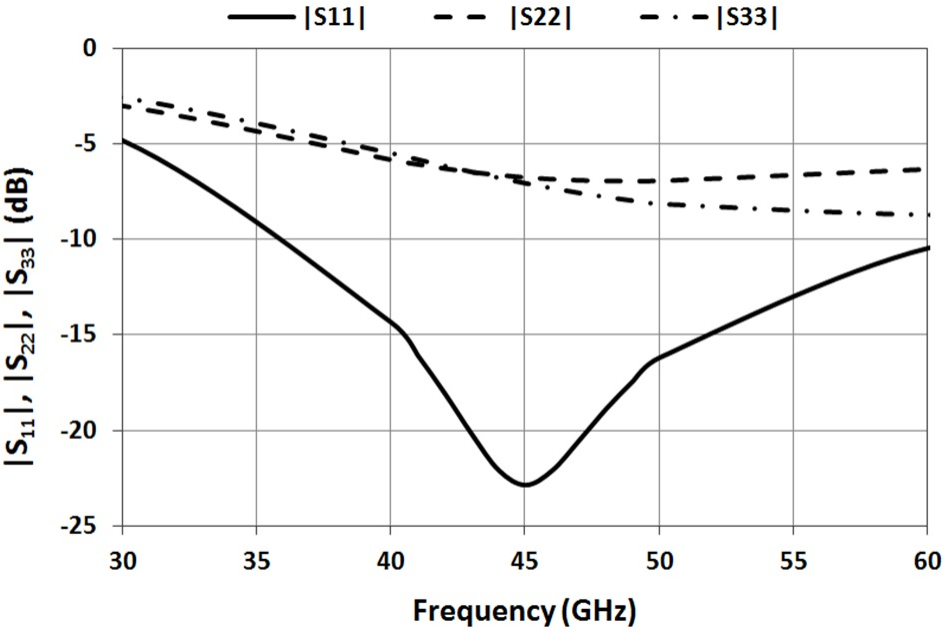


Figure 72: Balun simulated $|S_{11}|$, $|S_{22}|$, $|S_{33}|$.

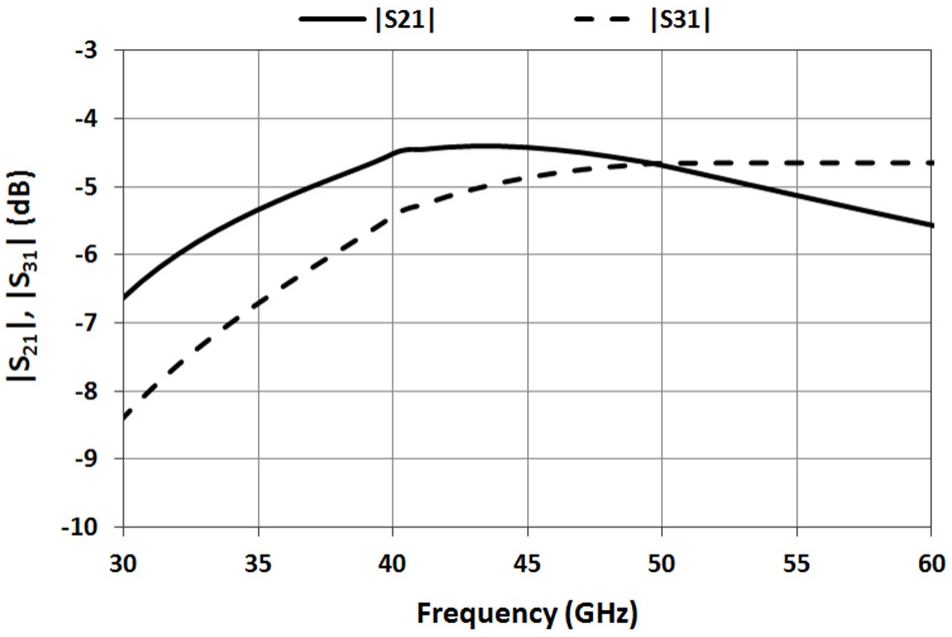


Figure 73: Balun simulated $|S_{21}|$ and $|S_{31}|$.

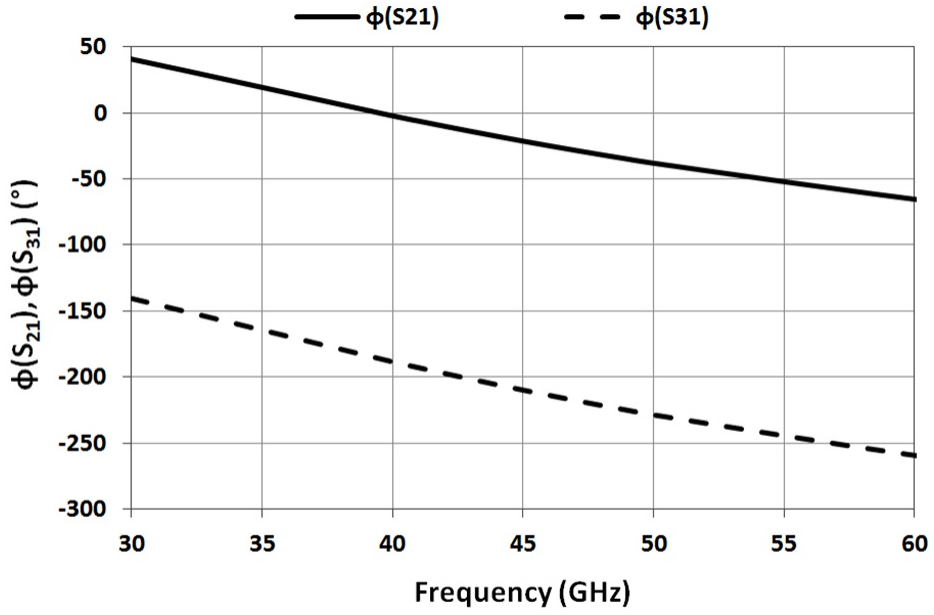


Figure 74: Balun simulated $\phi(S_{21})$ and $\phi(S_{31})$.

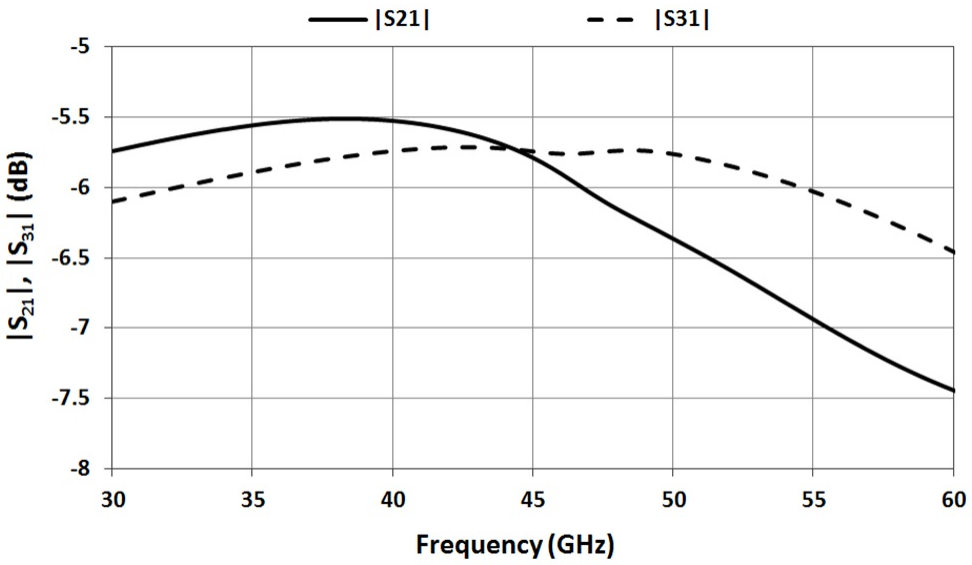


Figure 75: Quadrature hybrid simulated $|S_{21}|$ and $|S_{31}|$.

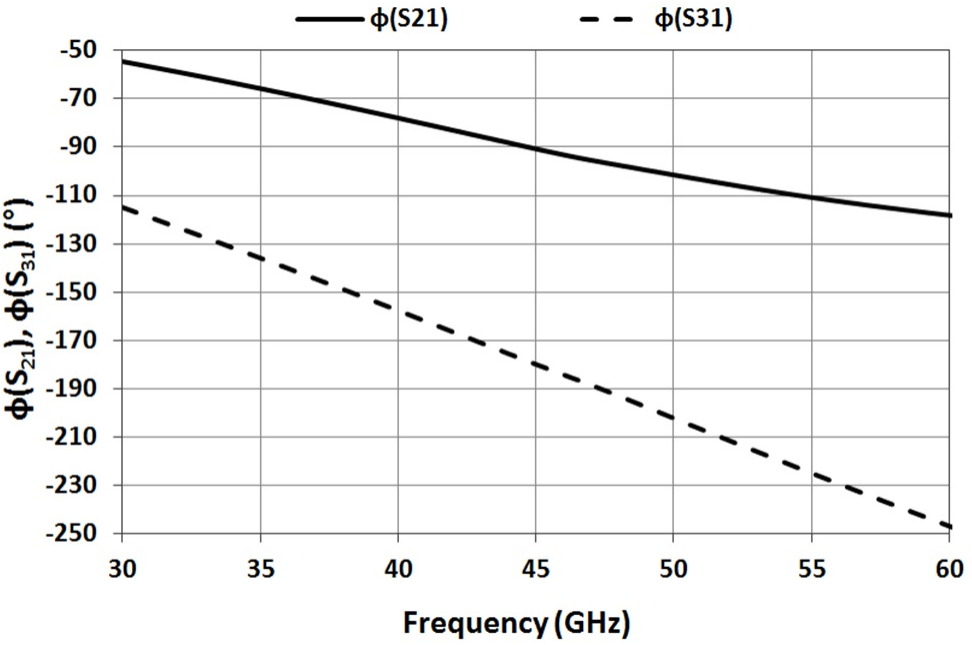


Figure 76: Quadrature hybrid simulated $\phi(S_{21})$ and $\phi(S_{31})$.

5.2.2 Vector Modulator Active Core

Vector rotation is performed using a double-balanced Gilbert cell core, wherein the differential quadrature signals (I±,Q±) generated by the passive network are weighted by the differential inputs to the tail transistors (i±, q±) and summed. This allows for continuous 360° vector generation. The circuit schematic of the Gilbert cell modulator is seen in Figure 77. The series resistors at the gates of the tail transistors serve as ESD protection. Otherwise these nodes would connect directly to the chip pads. The limitation this places on the baseband bandwidth of the circuit is more than an order of magnitude greater than the capability of the measurement setup. Input and output matching networks were designed using coplanar waveguide transmission line constructed using the thick top metal lines as in the branchline coupler. In order to support a flexible testing environment, external DACs were used to drive the tail transistors of the Gilbert cells.

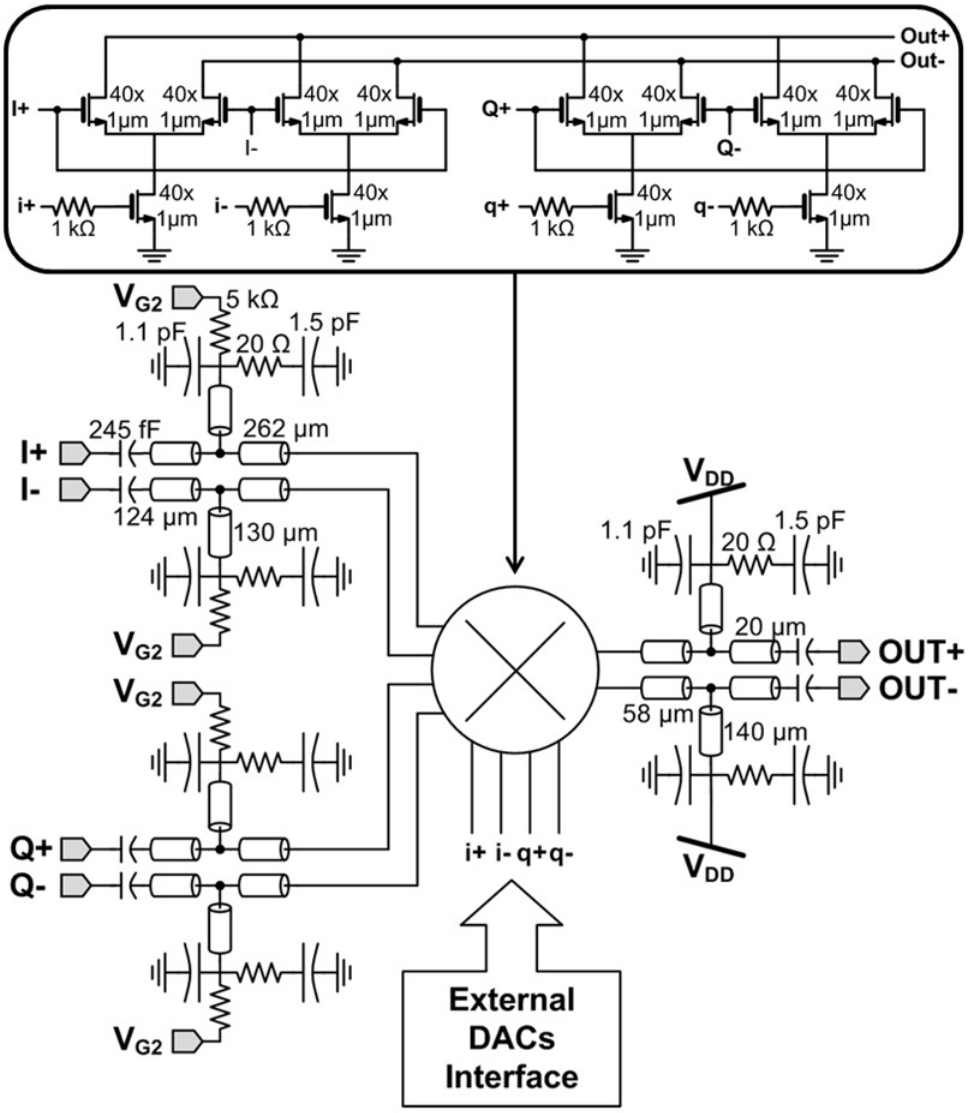


Figure 77: Vector modulator Gilbert-cell core.

A simulation was performed to compare 16-QAM symbols generated by the outphasing modulator with the set of ideal constellation points. S-parameter blocks for the passive network components generated by their EM simulators were used and the baseband signals were restricted to 8-bit resolution, which would be the case in measurement. Figure 78 shows a constellation diagram comparing ideal symbol locations for 16-QAM with those generated by simulation. The deviations from ideal locations are due to the imperfect nature of the passive generation network as well as

the changing input impedance of the Gilbert cell switching-quad devices as a function of tail transistor bias. The effect of the latter can be mitigated by including buffer stages between the passive networks and the Gilbert cells. However, to achieve a low-power design these were omitted for this work. The simulated RMS error-vector magnitude (EVM) is 9.59% or -20.36 dB. For 16-QAM, this corresponds to a bit error rate $< 10^{-6}$ [80].

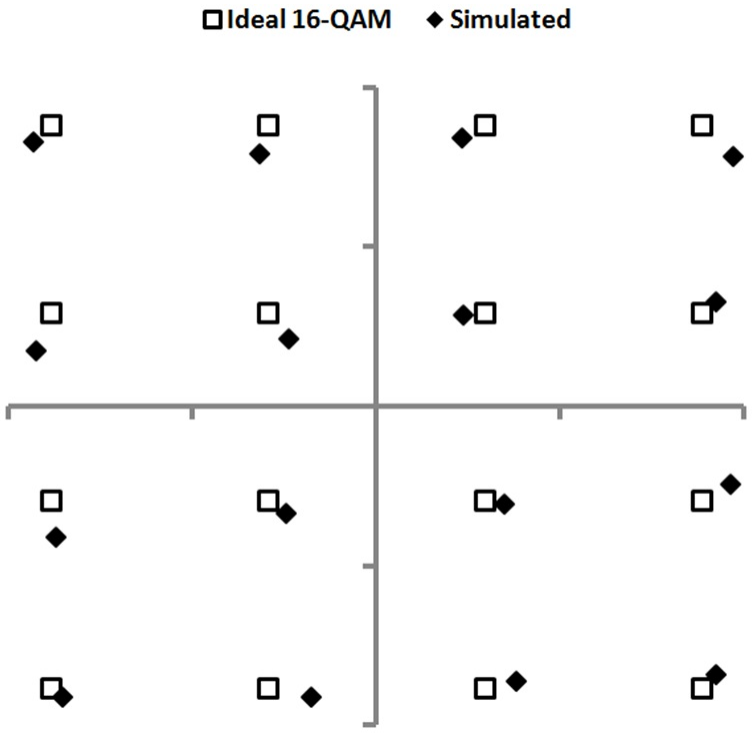


Figure 78: Ideal versus simulated 16-QAM.

5.3 Measured Results

Shown in Figure 79 is a die photograph of the 2-channel vector modulator with its constituent sub-circuits identified. The die area excluding pads for each channel is 0.56 mm^2. For measurement purposes, one phase of the differential output of each of the vector modulators was terminated with a 50-Ω resistor on chip, which reduces the output swing by a factor of two but does not fundamentally change the modulation

mechanism.

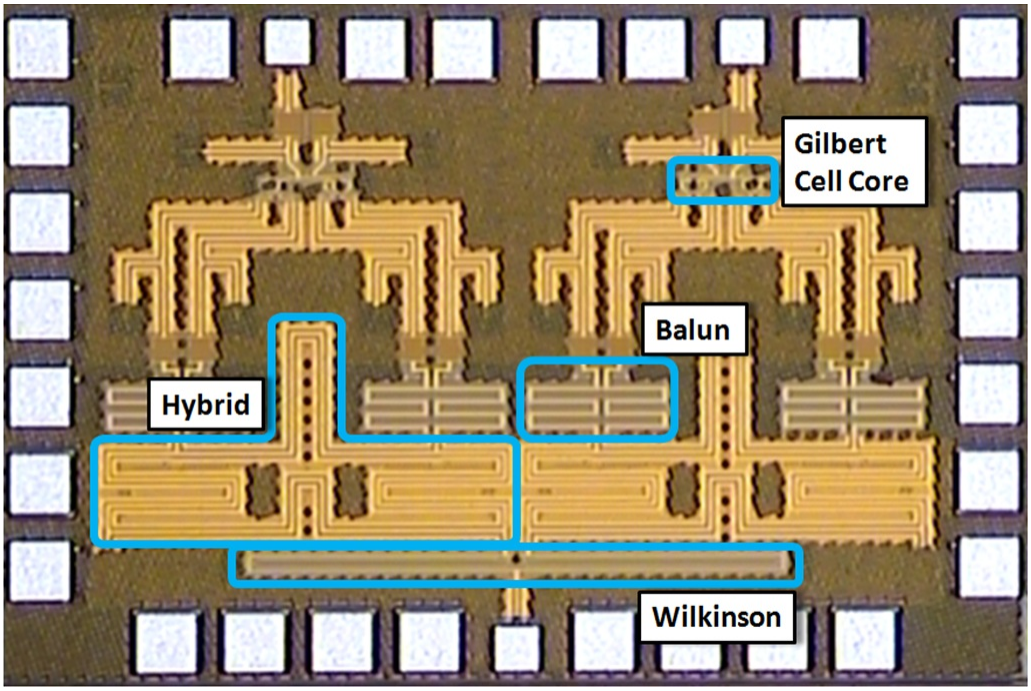


Figure 79: 2-Channel vector modulator die photograph.

5.3.1 Single Channel Vector Modulator Calibration

Depending on the precision requirements of the application, calibration may need to be applied to correct for phase and amplitude imbalances in the 90° hybrid and amplitude imbalances in the balun and/or Gilbert cell modulator due to mismatch. Note that since a single-ended output is taken for ease of experiment, the effects of differential imbalance from mismatch are likely more pronounced and such correction may not be required in the real operating case.

Many previous works have focused in detail on open and closed loop calibration for LINC architectures [81]-[83]. For the purposes of measurement in this work, a set of calibration coefficients and equations is defined similar to what would exist inside such a full system implementation.

Since this 2-channel vector modulator will be used to implement outphasing modulation it is convenient to write the input voltage signals in terms of the output vector angles to be generated by each channel for a given symbol. The normalized ideal differential signal voltages to drive the modulator as a function of desired output phase are given by (32)-(35) where, for example, i_{1n} denotes the differential voltage for the i± inputs of channel 1 for the nth symbol.

$$i_{1n} = cos(\theta_{1n}) \tag{32}$$

$$q_{1n} = sin(\theta_{1n}) \tag{33}$$

$$i_{2n} = cos(\theta_{2n}) \tag{34}$$

$$q_{2n} = sin(\theta_{2n}) \tag{35}$$

The calibrated differential signal voltages are given by (36)-(39). DC offset and amplitude imbalances are corrected for by shifting and scaling the differential input swing whereas the IQ imbalance is corrected by adding a component iq_{corr} to the i vector proportional to the IQ imbalance and the magnitude of the q vector. This results in a magnitude error given by 1-cos($\Delta\theta$), which amounts to an error of less than 1.52% for an IQ imbalance $\Delta\theta$ of 10°. The IQ imbalance correction is depicted graphically in Figure 80. All equations associated with channel 2 include a coefficient ϕ to correct for any phase difference between channels 1 and 2.

$$i_{1n,c} = (i_{1,max} - i_{1,DC})cos(\theta_{1n}) + i_{1,DC} + iq_{corr,1} \tag{36}$$

$$q_{1n,c} = (q_{1,max} - q_{1,DC})sin(\theta_{1n}) + q_{1,DC} \tag{37}$$

$$i_{2n,c} = (i_{2,max} - i_{2,DC})cos(\theta_{2n} + \phi) + i_{2,DC} + iq_{corr,2} \tag{38}$$

$$q_{2n,c} = (q_{2,max} - q_{2,DC})sin(\theta_{2n} + \phi) + q_{2,DC} \tag{39}$$

Where,

$$iq_{corr,1} = sin(\Delta\theta_1)[(q_{1,max} - q_{1,DC})sin(\theta_{1n}) + q_{1,DC}] \tag{40}$$

$$iq_{corr,2} = sin(\Delta\theta_2)[(q_{2,max} - q_{2,DC})sin(\theta_{2n} + \phi) + q_{2,DC}] \tag{41}$$

and,

$i_{1,max}$ is the channel 1 i-path maximum swing,

$q_{1,max}$ is the channel 1 q-path maximum swing,

$i_{1,DC}$ is the channel 1 i-path DC offset,

$q_{1,DC}$ is the channel 1 q-path DC offset,

(analogous terms for channel 2)

$\Delta\theta_1$ is the channel 1 IQ imbalance,

$\Delta\theta_2$ is the channel 2 IQ imbalance,

ϕ is the phase difference between the two channels.

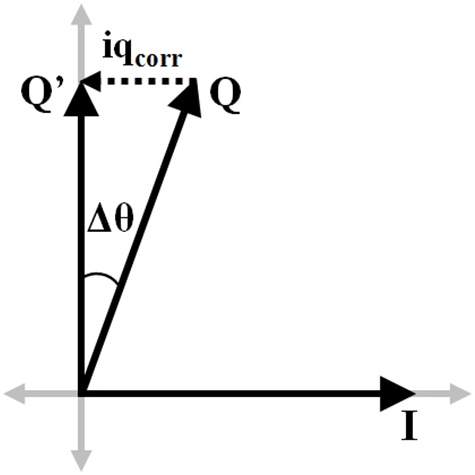


Figure 80: IQ imbalance correction illustrated graphically.

5.3.2 Single Channel Vector Modulator Measured Results

The coefficients for (36)- (39) were determined manually through power measurements on a set of test vectors. The DC offset terms $i_{1,DC}$, $q_{1,DC}$, $i_{2,DC}$, and $q_{2,DC}$ were found by varying the differential biases of the I and Q vector paths for both channels until perfect cancellation was achieved and there was a zero-vector output. Coefficients $i_{1,max}$, $q_{1,max}$, $i_{2,max}$, and $q_{2,max}$ were then determined by finding the weakest vector from all channels (I_1, Q_1, I_2, or Q_2) and normalizing the others to this power level. Next, the IQ imbalance terms were found by changing their value such that the 45°, 135°, 225°, and 315° vectors had the same power levels. This is illustrated by Figure 81 where the 45° and 225° vectors have larger magnitudes than the 135° and 315° vectors resulting from IQ imbalance prior to calibration.

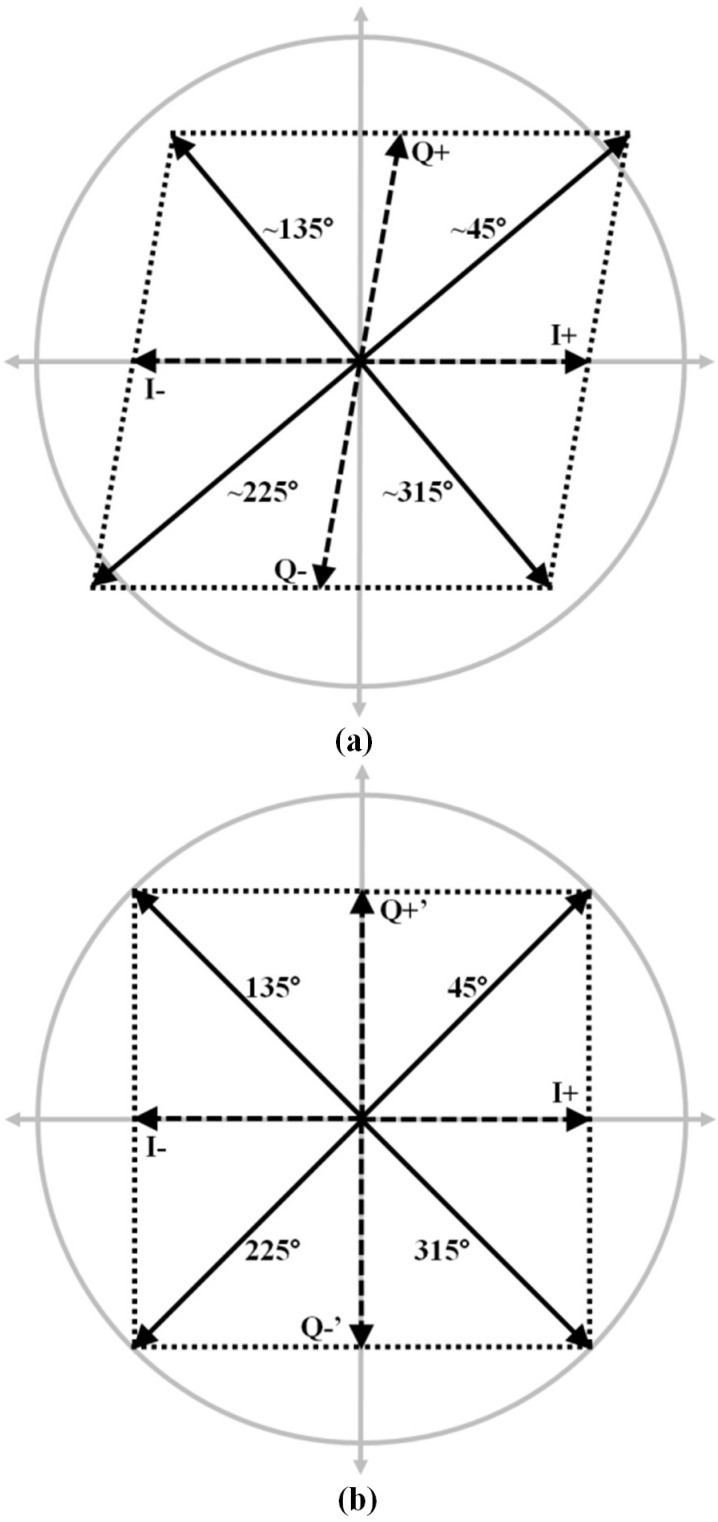


Figure 81: Using the relative magnitudes of the 45°, 135°, 225°, and 315° test vectors to correct for IQ imbalance (a) Uncalibrated (b) Calibrated.

From [84], the RMS gain and phase errors are defined by (42) and (43), respectively. Shown in Figures 82 and 83 are the measured RMS gain and phase errors versus frequency, respectively. In both plots, RMS errors are given for the uncalibrated vector modulator, as well as after calibration at 45 GHz. For the frequency range of 42-48 GHz, the RMS gain error is < 1.3 dB for the uncalibrated case and < 0.5 dB after calibration. For the same frequency range the RMS phase error is $< 10^\circ$ uncalibrated and $< 5^\circ$ calibrated. Figure 84 and Figure 85 show the calibrated measured phase shift and gain versus frequency throughout the tuning range, respectively. The vector modulator is capable of a continuous 360° phase rotation, has an average gain of -13.7 dB and consumes 18 mW of DC power from a 1-V supply. Table 5 compares this work to other silicon-based 360° phase shifters, showing low power consumption and very low RMS gain and phase errors following simple open loop calibration.

$$A_{error,RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}|\Delta A_i|^2} \tag{42}$$

$$\theta_{error,RMS} = \sqrt{\frac{1}{N-1}\sum_{i=2}^{N}|\Delta \theta_i|^2} \tag{43}$$

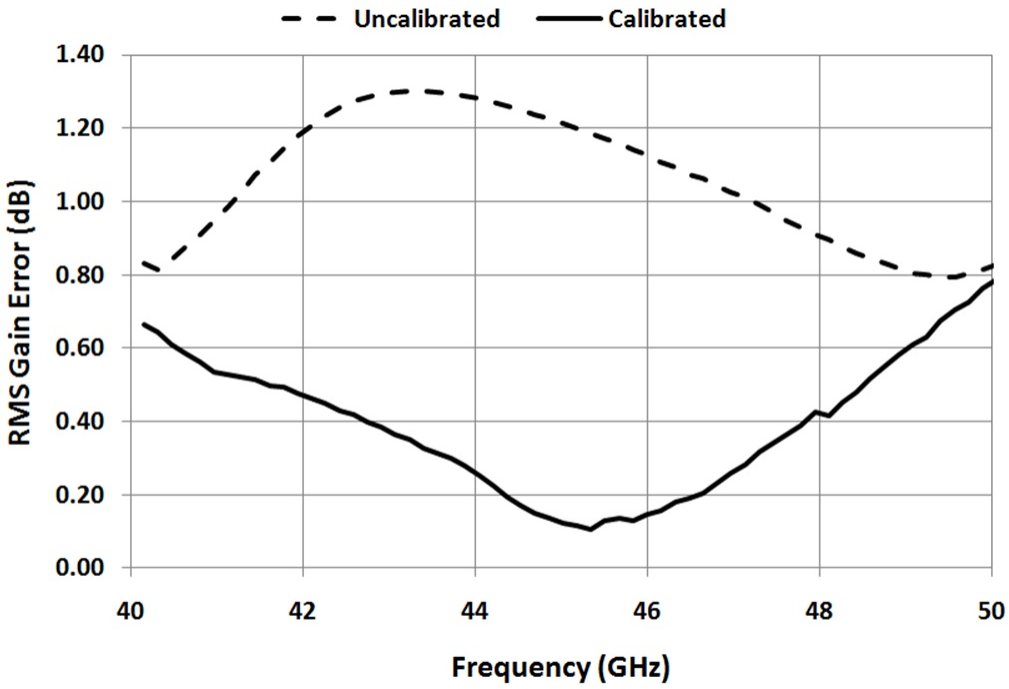


Figure 82: Vector modulator RMS gain error, calibrated verus uncalibrated.

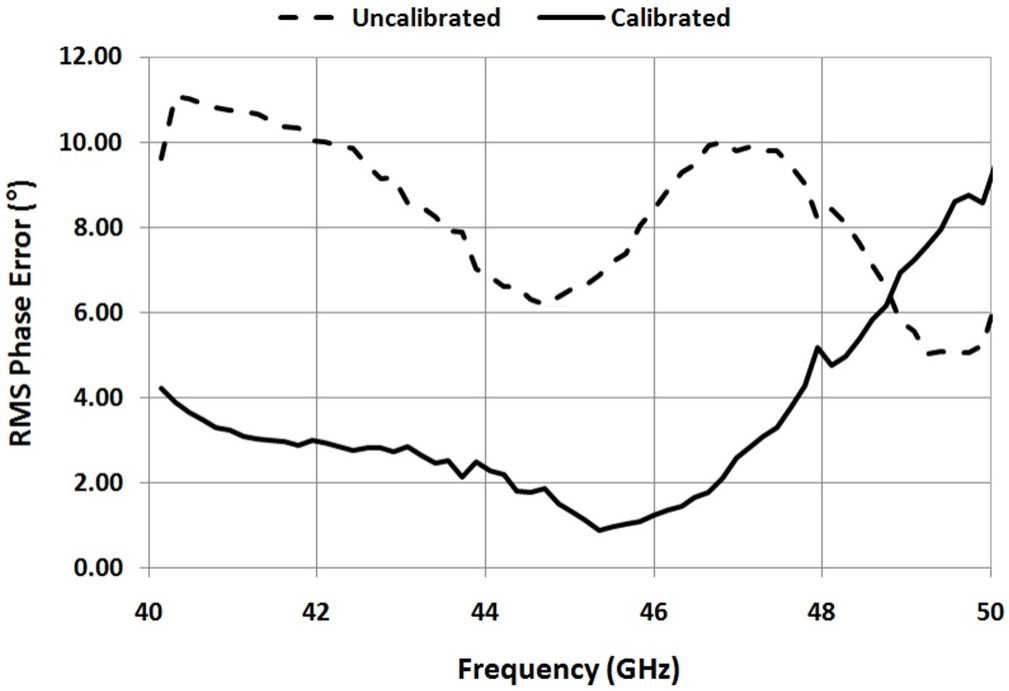


Figure 83: Vector modulator RMS phase error, calibrated versus uncalibrated.

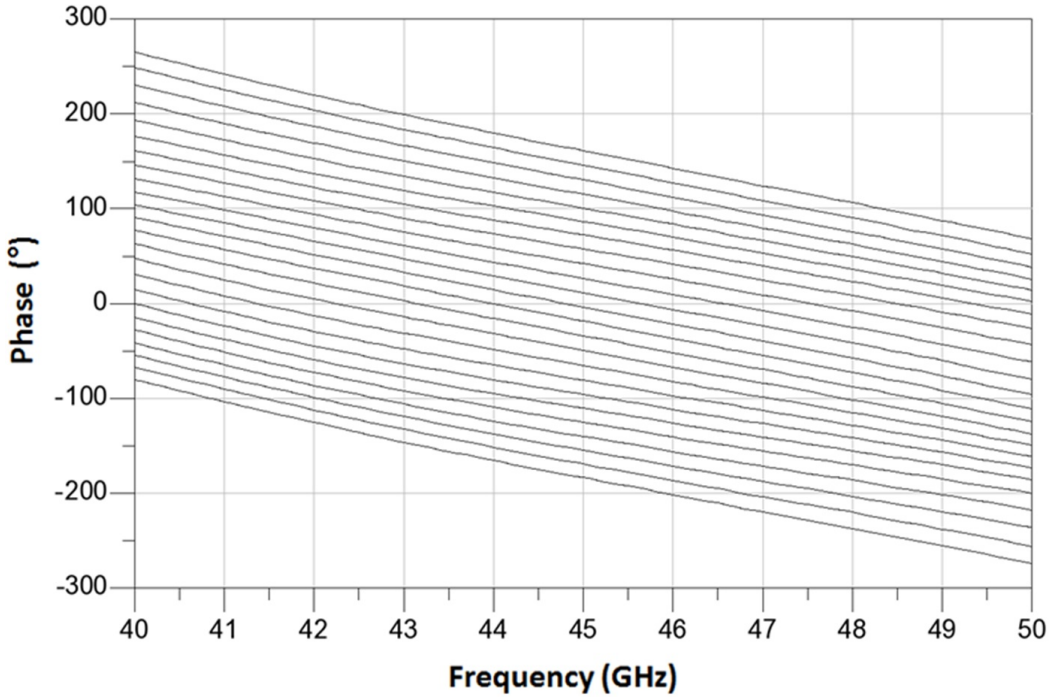


Figure 84: Vector modulator phase shift for different tuning voltages, calibrated.

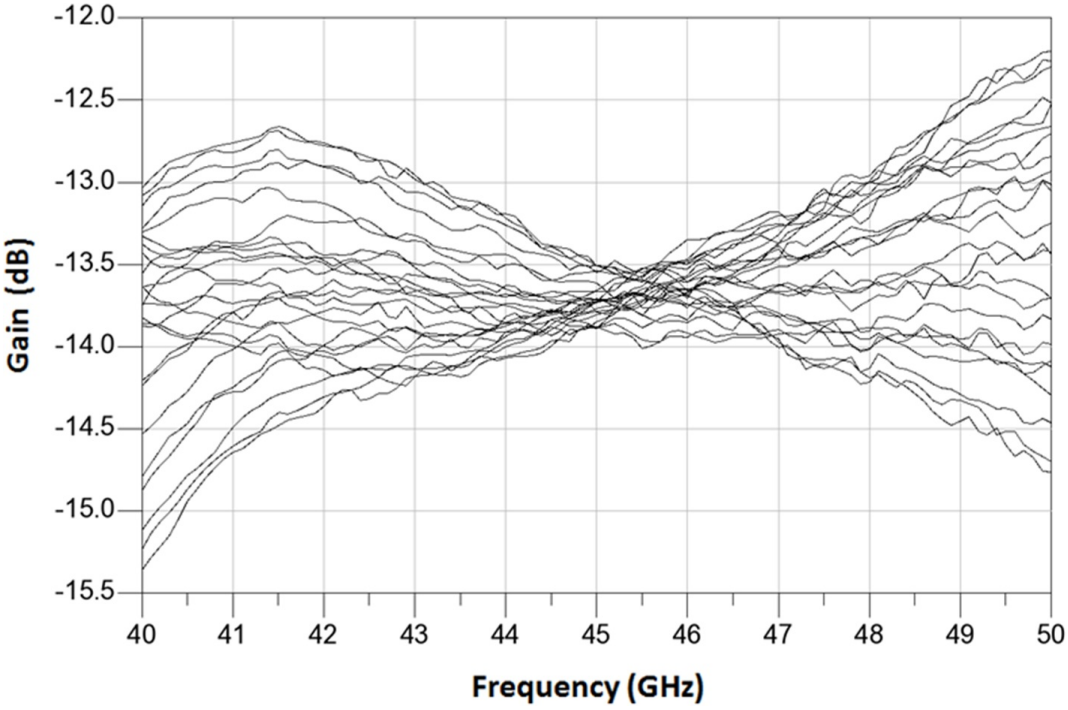


Figure 85: Vector modulator gain for different tuning voltages, calibrated.

Table 5: 360° Vector modulator performance comparison.

Reference	This Work	[76]	[77]	[78]	[85]	[86]
Frequency (GHz)	42-48	30-38	67-78	57-64	50-56	48
Phase Resolution (°)	Cont.	22.5	22.5	22.5	Cont.	Cont.
Average Gain (dB)	-13.7	-12	-19.2	-5.4	-13.5	0
RMS Phase Error (°)	<1.3, <0.5*	<2.4	<3	<1.2	<1.76	-
RMS Gain Error (dB)	<10, <5*	<7.5	<14	<10.5	<21	-
Area (mm^2)	0.56	0.15	0.135	0.25	0.17	-
DC Power (mW)	18	0	0	34	6	105
Technology	45-nm SOI CMOS	0.12-μm BiCMOS	0.12-μm BiCMOS	65-nm CMOS	90-nm CMOS	0.25-μm BiCMOS

*calibrated at 45 GHz

5.3.3 Wilkinson Power Combiner on LCP

In order to demonstrate the outphasing modulation capability while maintaining the ability to measure each channel output independently, signal power combining at 45 GHz was performed off-chip using a Wilkinson power combiner on LCP. The Wilkinson power combiner was designed using Ansys HFSS where the 100-Ω surface-mount resistor was modeled with a sheet resistance. The simulation setup can be seen in Figure 86. The circuit was fabricated by patterning copper traces on a 4-mil

copper-backed LCP substrate. The surface-mount resistors were mounted using silver epoxy. A 4-mil substrate was chosen so that the circuit dimensions would allow for interfacing with the vector modulator on CMOS.

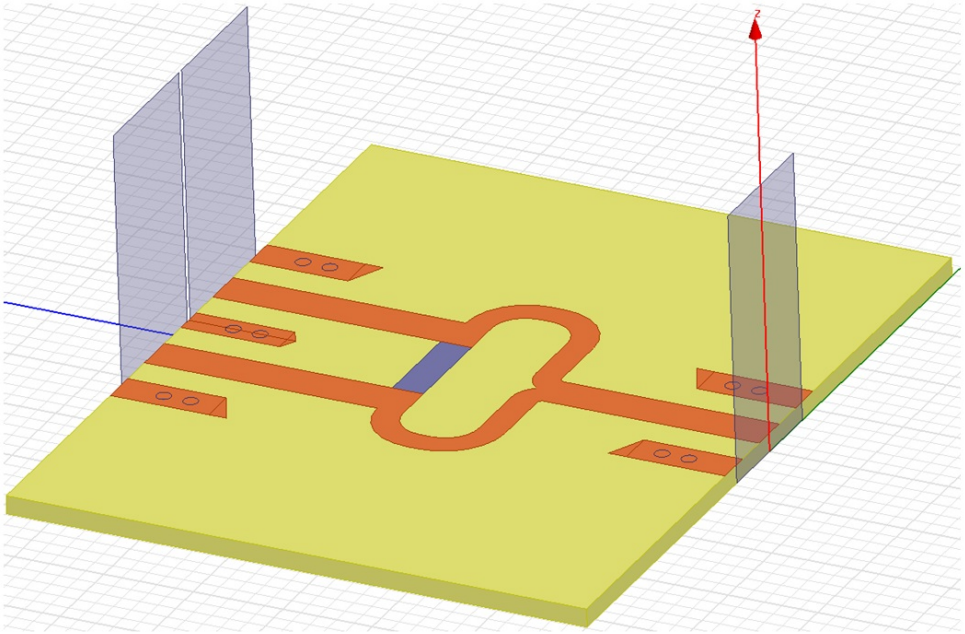


Figure 86: HFSS simulation setup for the Wilkinson power combiner on LCP.

The Wilkinson power combiner was measured by terminating one of the split-power outputs with parallel 100-Ω surface mount resistors and probing the other ports, as seen in Figure 87. The measured versus simulated $|S_{11}|$ and $|S_{22}|$ are shown in Figure 88. The downshift in matching frequency is attributed to both the simplistic modeling of the 100-Ω resistor and under-etching of the metal traces during fabrication, resulting in wider signal lines. Although S-parameter data for the surface mount resistor was not available to create a more realistic model, the 8-fF maximum capacitance specified by the manufacturer would alone be enough to shift $|S_{22}|$ down by more than 30%. Even with these implementation non-idealities the wideband design exhibits $|S_{11}| <$ -11 dB and $|S_{22}| <$ -17 dB for the entire band of interest. Figure 89 shows the measured versus simulated $|S_{12}|$ exhibiting an insertion loss $<$ 0.7 dB.

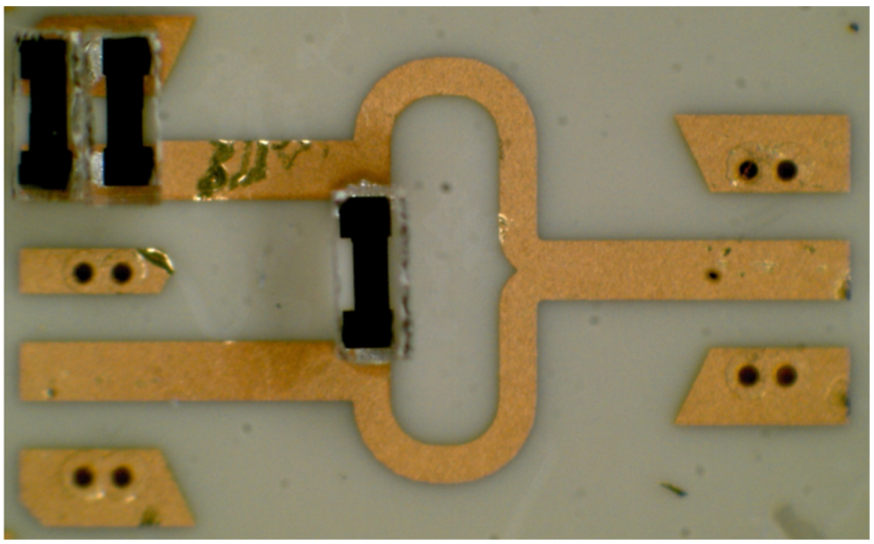


Figure 87: Wilkinson power combiner on LCP, with port 3 terminated using surface mount resistors.

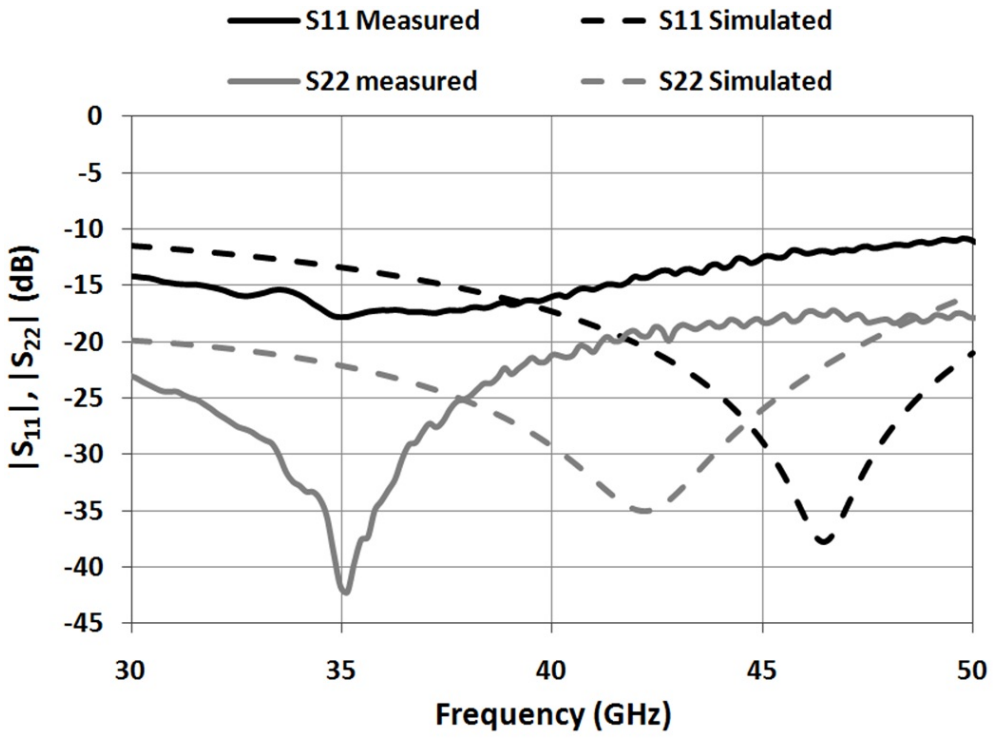


Figure 88: Measured versus simulated $|S_{11}|$ and $|S_{22}|$ for the Wilkinson power combiner on LCP.

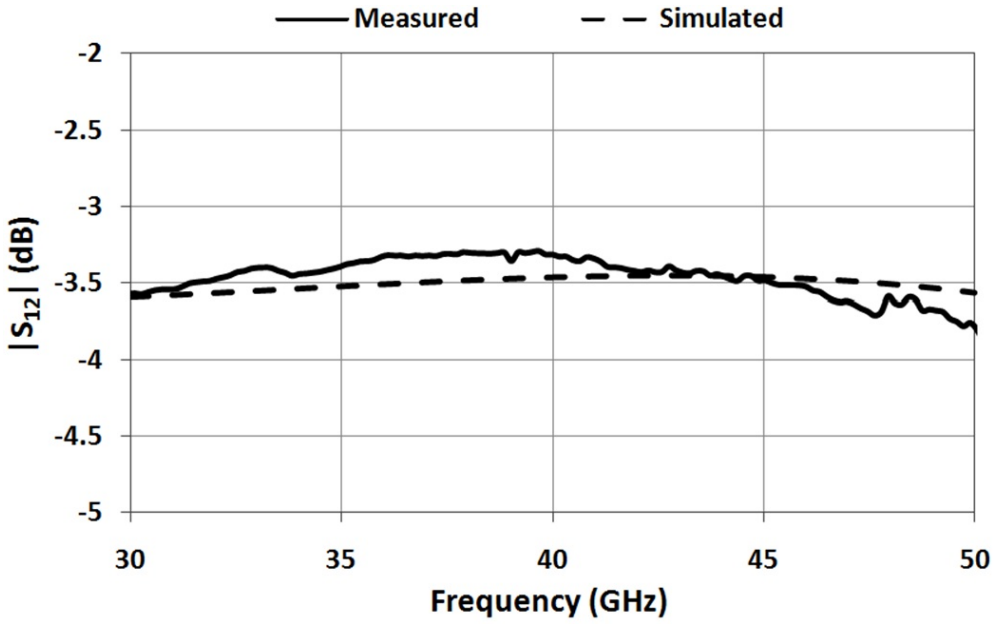


Figure 89: Measured versus simulated $|S_{12}|$ for the Wilkinson combiner on LCP.

5.3.4 LINC Measured Results

Figure 90 shows a photograph of the CMOS die containing the 2-channel vector modulator packaged within the LCP substrate containing the Wilkinson power combiner.

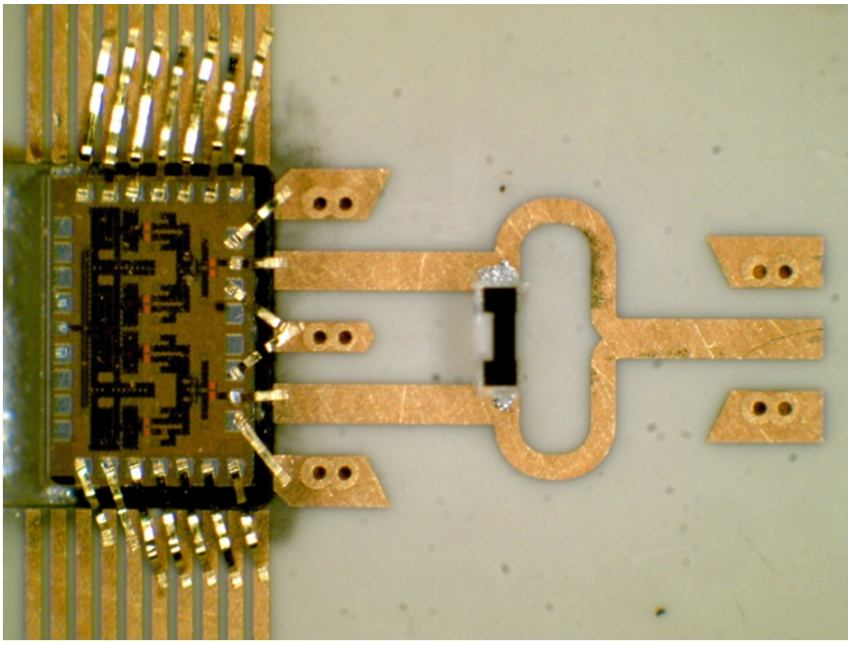


Figure 90: Vector modulator die packaged with Wilkinson combiner on LCP.

Figure 91 shows the test setup used to evaluate the outphasing modulation capability. MATLAB^{TM} code incorporating the calibration equations discussed above was used to generate the modulation and control the Tektronix DG2020A digital waveform generator. This drove 4 parallel 8-bit DACs with differential outputs on evaluation boards. The DAC outputs were connected to the Gilbert cell modulator inputs as shown in Figure 77. The vector modulator has a simulated baseband bandwidth of approximately 2.5 GHz. However, the external DACs used in the measurement setup exhibited a long settling time that limited the producible symbol rate to approximately 1 Msps.

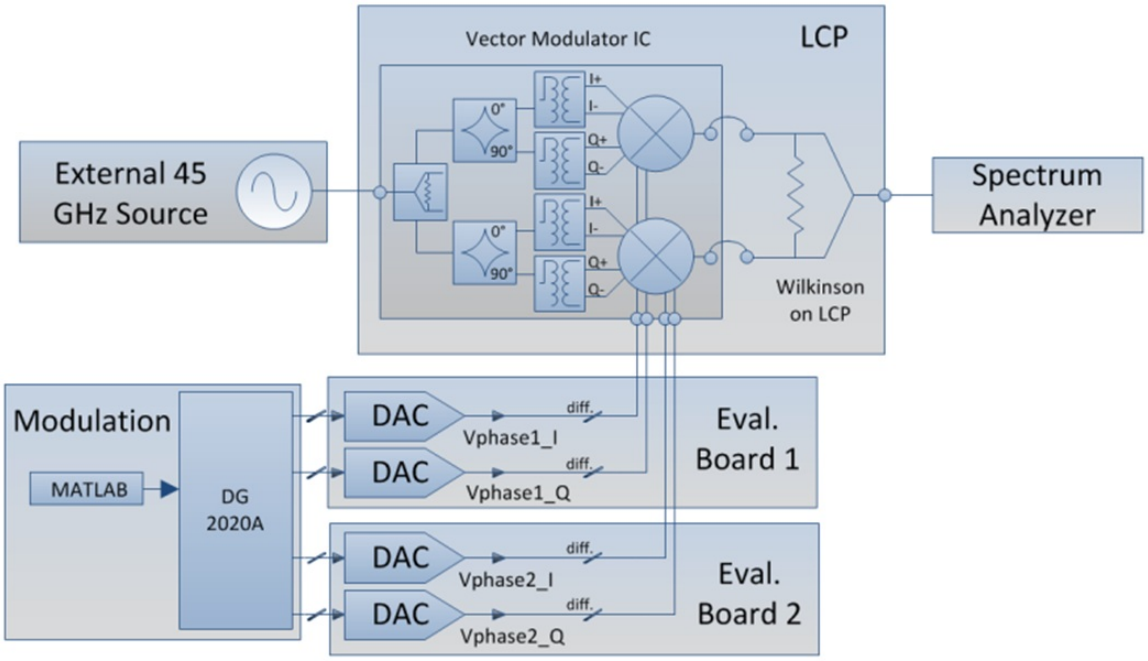


Figure 91: LINC measurement setup.

Figure 92 shows the measured constellation diagram for outphasing-generated 16-QAM for a symbol rate of 1 Msps prior to any calibration, illustrating the need for correction. Seen in Figure 93 is 1-Msps 16-QAM with amplitude correction, but no phase correction applied. Figure 94 shows the measured constellation diagram for 1-Msps 16-QAM after full calibration was applied. The fully calibrated modulation exhibits and RMS EVM of 9.43%, which corresponds very well to the simulated value of 9.59% and is sufficient with margin for contemporary wireless communication standards [87]. For comparison, an EVM of 11.48% was achieved by [68] for free-space combining and 8.32% with post-processed phase adjustment and combining in MATLAB. The fully calibrated measured output spectrum for 1-Msps 16-QAM is shown in Figure 95. The DC power consumption for the entire IC was 36 mW from a 1-V supply. To the author's knowledge, this demonstrates the first ever outphasing modulation for a non-constant envelope modulation scheme in a CMOS based technology in the Q-band for LINC applications.

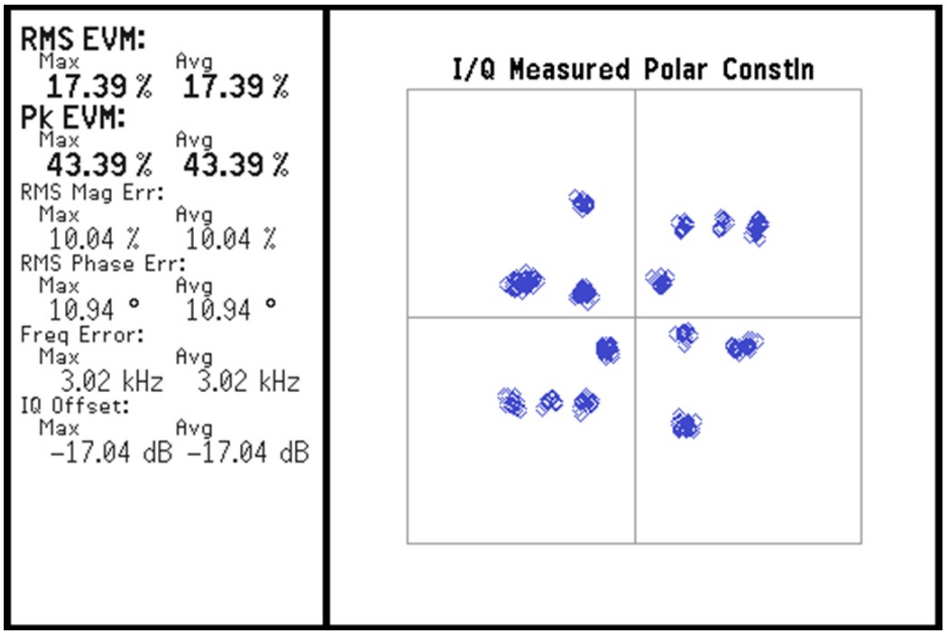


Figure 92: Measured 16-QAM constellation, uncalibrated (1 Msps).

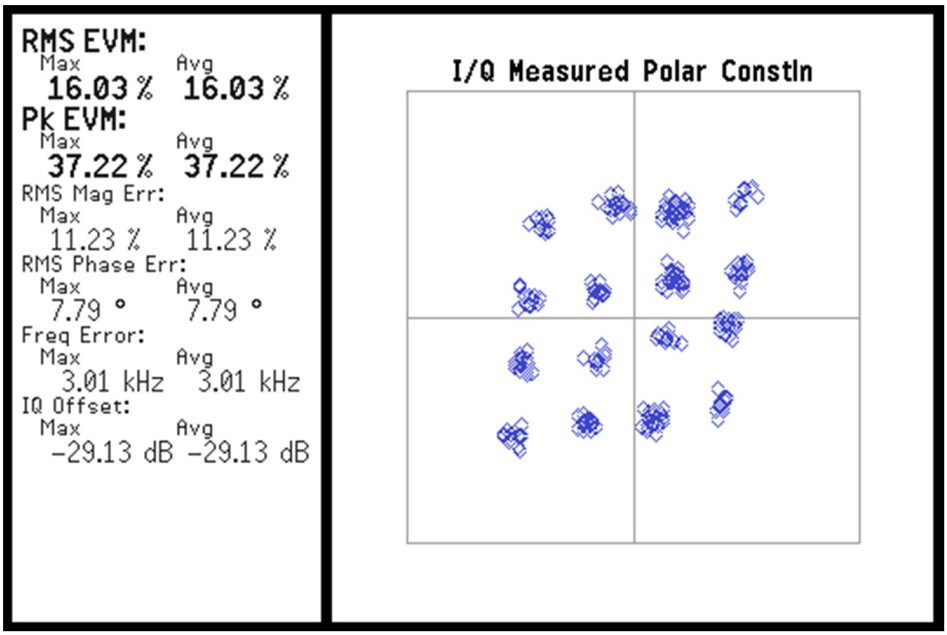


Figure 93: Measured 16-QAM constellation, vector magnitude cal. only (1 Msps).

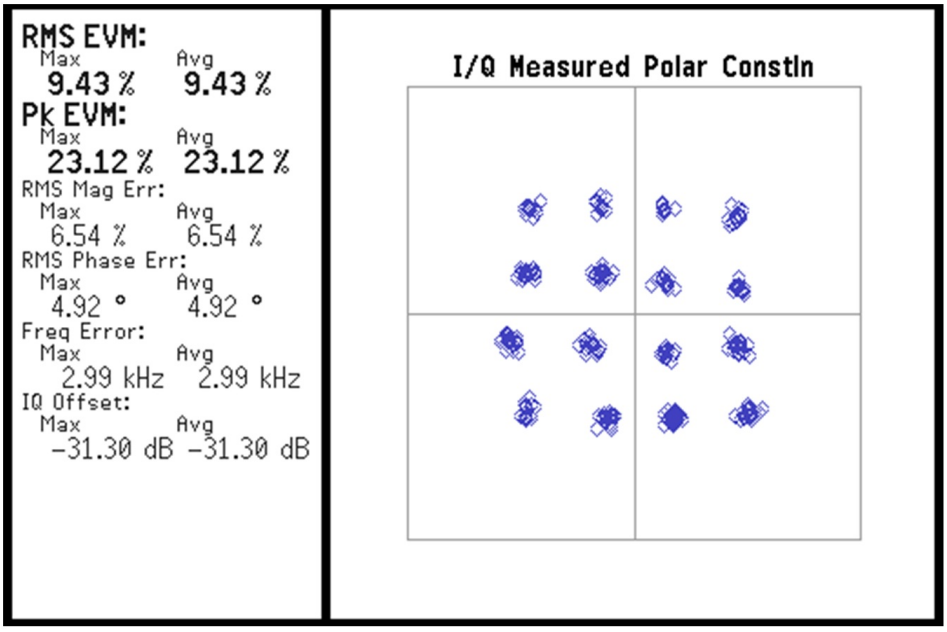


Figure 94: Measured 16-QAM constellation, full calibration (1 Msps).

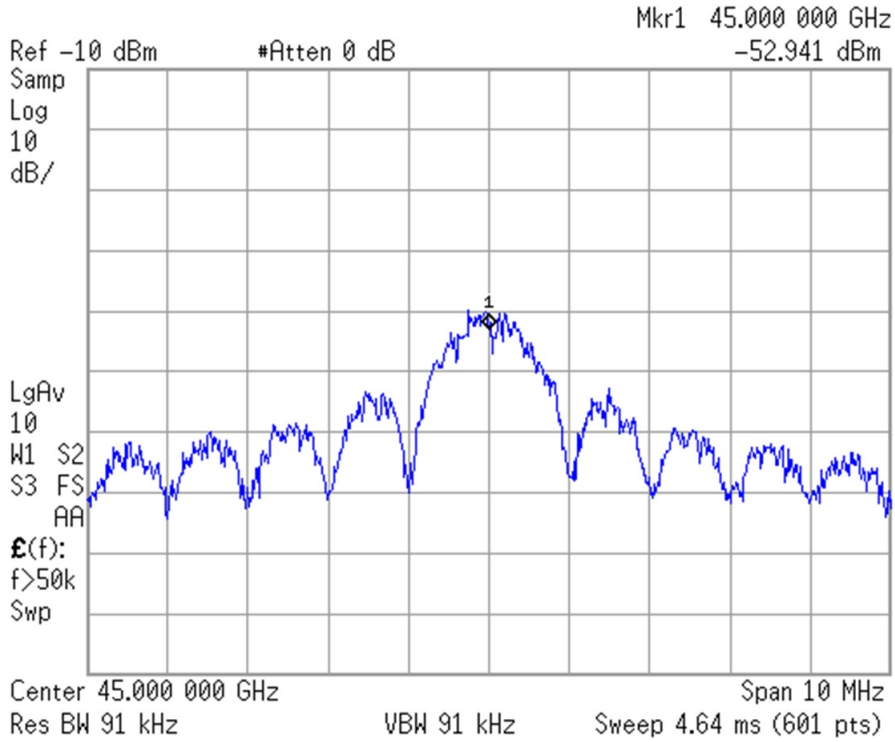


Figure 95: Measured output spectrum with fully calibrated 16-QAM.

Since the measurement setup limited the symbol-rate of 16-QAM modulation to 1-Msps, measurements were taken where BPSK was generated using a single channel to demonstrate capability into the Gbps range. Shown in Figure 96 are the measured constellation and eye diagrams for demodulated 100-Mbps BPSK, which demonstrate an RMS EVM of 12.3%. Figure 97 shows the corresponding output spectrum. Shown in Figures 98 and 99 are the BPSK modulation spectra at 500 Mbps and 1 Gbps, respectively. Since these data rates were above the signal analysis bandwidth of the specrum analyzer, only output spectra could be captured.

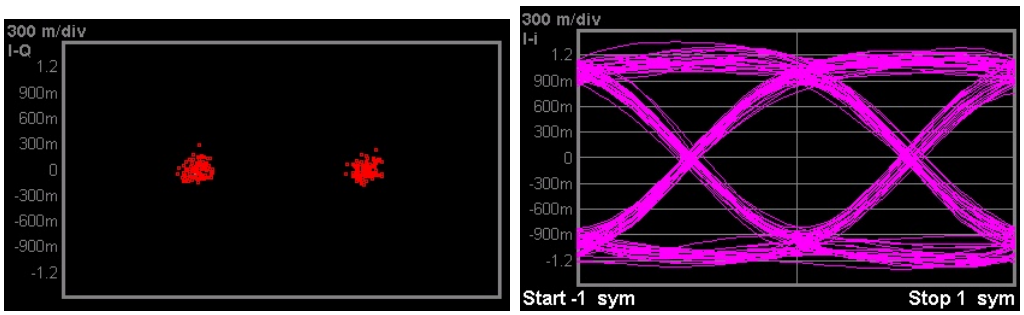


Figure 96: Measured constellation and eye diagram for 100-Mbps BPSK.

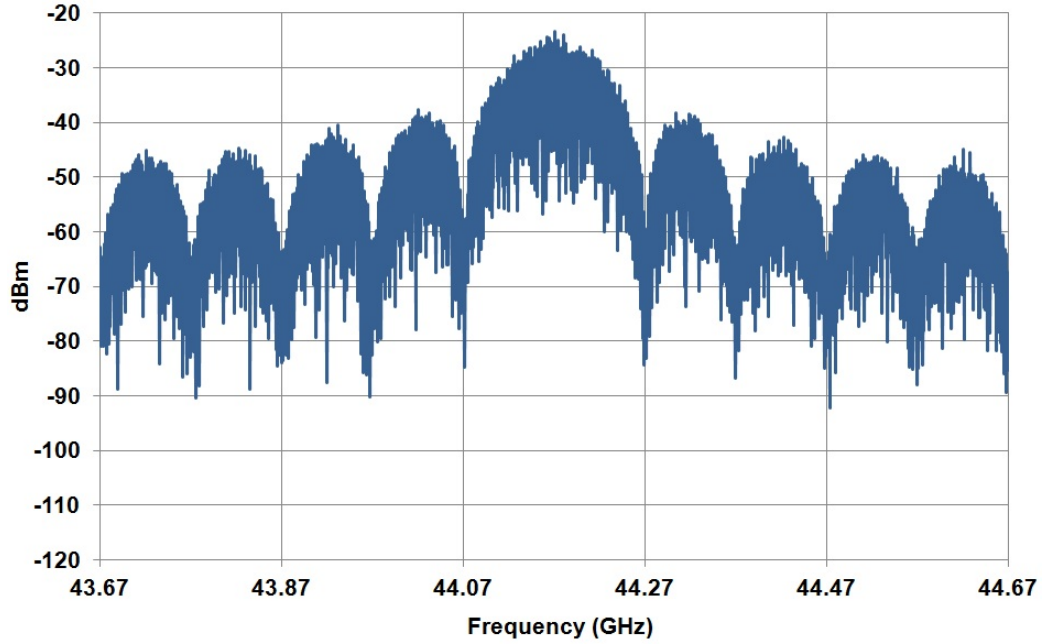


Figure 97: Measured 100-Mbps BPSK spectrum.

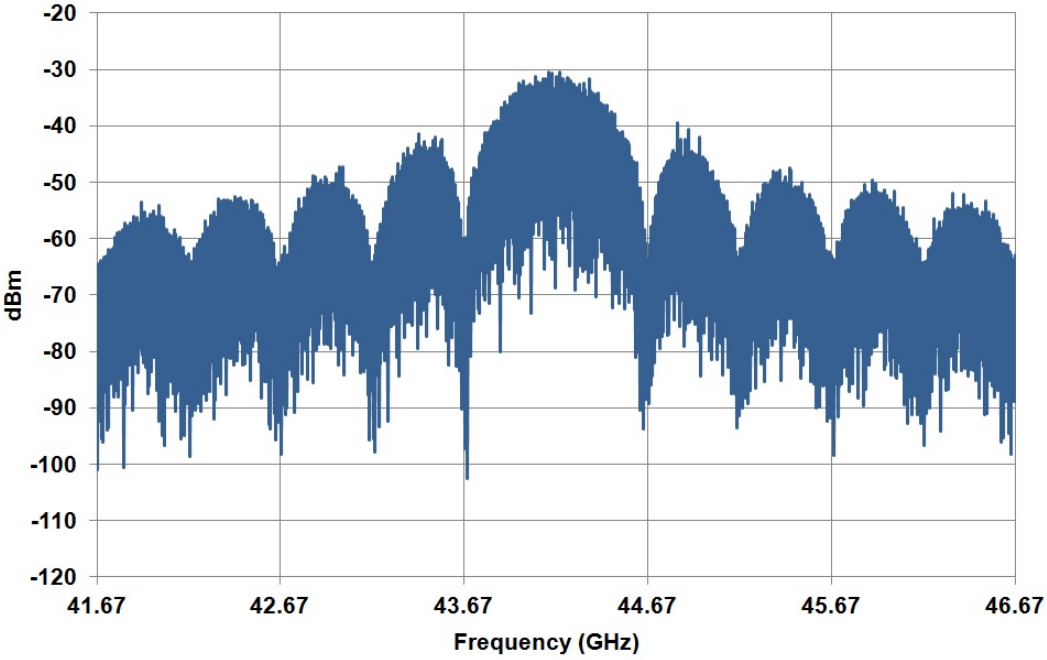


Figure 98: Measured 500-Mbps BPSK spectrum.

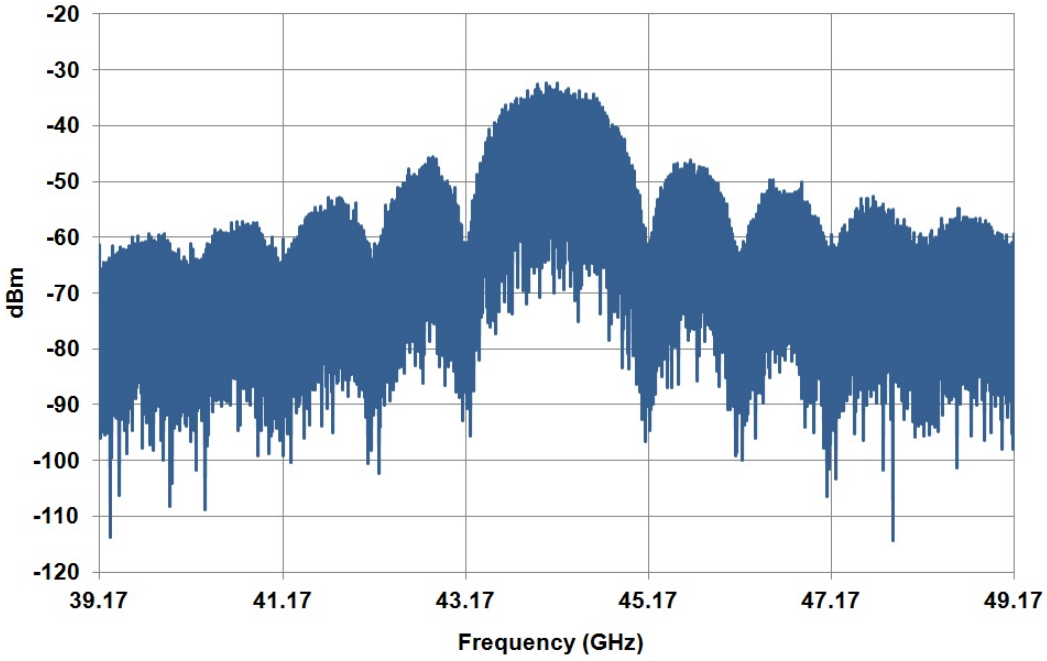


Figure 99: Measured 1-Gbps BPSK spectrum.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

6.1 Technical Contributions

- Full integration of a low-Power 60-GHz to bits CMOS OOK receiver in 90-nm CMOS technology. The use of non-coherent OOK demodulation by a novel demodulator enables a data throughput of 3.5 Gbps and resulted in the lowest power budget (31pJ/bit) for integrated 60-GHz CMOS OOK receivers at the time of publication.

- First reported CMOS millimeter-wave VCO based upon a class-E power amplifier in a feedback configuration. This design achieves the highest output power (8.2 dBm) and efficiency (15.64%) to date for monolithic silicon-based millimeter-wave VCOs.

- First demonstration of the performance of a CMOS millimeter-wave VCO packaged on low-cost, organic liquid crystal polymer substrate.

- First 16-QAM generated by outphasing modulation for LINC transmitters in the Q-band in CMOS technology. A 2-channel 45-GHz vector modulator is implemented in 45-nm SOI CMOS. The zero-power passive IQ generation network and a low-power Gilbert cell modulator are used to enable continuous 360° vector generation. The IC is packaged with a Wilkinson power combiner on LCP and driven by external DACs to demonstrate to demonstrate high-order non-constant envelope modulation with the aid of a simple open-loop calibration scheme.

6.2 Suggestions for Future Work

Several of the contributions of this dissertation are the enabling pieces of larger millimeter-wave transceivers. The logical extension of this work would be to develop and integrate the additional building blocks necessary to implement complete systems.

The target application for the high-efficiency, high-power millimeter-wave VCO and ILO described in Chapter 4 is LO distribution for multi-element transceivers such as phased arrays. Therefore, additional blocks that would need to be developed to implement a phased array transceiver in 45-nm CMOS would include mixers, amplifiers, and a passive LO distribution tree.

The high-efficiency VCO could also find application for inexpensive millimeter-wave therapy as described in section 1.3.6. This would require the development of a package solution in LCP or another suitable technology that included the VCO, a power source, and a compact millimeter-wave antenna with a radiation pattern suitable for medical purposes.

The 2-channel 45-GHz vector modulator described in Chapter 5 demonstrates the core millimeter-wave blocks that can enable outphasing modulation for a LINC transmitter architecture. The next step in implementing a full LINC transmitter in CMOS is the development of high-efficiency amplifiers to be driven by the modulator as in Figure 65. In fact, the class-E PA core of the millimeter-wave VCO described in Chapter 4 can serve this purpose. The peak output power of the VCO is 8.2 dBm, which is the power level following an equal spit where half of the power coming out of the PA core is fed back to the input to enable positive feedback. If the feedback loop is removed and the input is driven sufficiently, an output power of >11 dBm could be expected from such an amplifier. If the modulator is to be used in a system requiring sufficiently higher output power, beyond the current reach of millimeter-wave CMOS PA technology, the modulator could be integrated on LCP substrate with high-power

commercially available PAs in a III-V semiconductor technology.

The second step would be to develop a millimeter-wave coupler and power detector such that a measure of the output power at 45-GHz could be fed back to a calibration system that could determine the coefficients used in the presented calibration equations. It is in this regard that the development of a millimeter-wave front-end in 45-nm CMOS becomes very advantageous since the digital back end for calibration and other digital signal processing will also have state of the art size and efficiency. Finally, high-speed DACs can also be integrated on the same die to drive the modulator in a flexible manner to support many different standards.

Also, as mentioned in Chapter 5, the vector modulator was designed to be scalable for use in multi-element transmitter architectures such as phased arrays. In this application, it would be advantageous to investigate circuit area reduction techniques, particularly in the passive distribution network as employed in [64], since in a phased-array architecture the area savings in the vector modulator would be multiplied by the number of redundant structures in the multi-element transmitter.

APPENDIX A

ACRONYM LIST

ADS	Advanced Design System
BER	Bit Error Rate
BiCMOS	BipolarComplimentary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BPSK	Binary Phase-Shift Keying
CMOS	Complimentary Metal Oxide Semiconductor
FCC	Federal Communications Commission (US)
FD	Fully Depleted
GaAs	Gallium Arsenide
HFSS	High Frequency Structural Simulator
ILO	Injection-Locked Oscillator
InP	Indium Phosphide
LCP	Liquid Crystal Polymer
LINC	Linear Amplification Using Non-linear Components
LNA	Low Noise Amplifier
MAC	Medium Access Control

MMIC	Monolithic Microwave Integrated Circuit
OOK	On-Off Keying
PA	Power Amplifier
PD	Partially Depleted
PDK	Process Design Kit
PEX	Parasitic Extraction
PHY	Physical Layer
PRBS	Pseudo-Random Binary Sequence
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase-Shift Keying
RF	Radio Frequency
SiGe	Silicon Germanium
SOI	Silicon-on-Insulator
VCO	Voltage Controlled Oscillator
WiGig	Wireless Gigabit (Alliance)
WHDI	Wireless Home Digital Interface (Consortium)
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

APPENDIX B

MATLAB CODE

The following is the MATLAB code used to generate calibrated 16-QAM using the 2-channel vector modulator:

```
disp('running...')

obj_dg2020a = instrfind('Type', 'gpib', 'BoardIndex', 0,
 'PrimaryAddress', 1, 'Tag', '');

    % Create the GPIB object if it does not exist
    % otherwise use the object that was found.
    if isempty(obj_dg2020a)
        obj_dg2020a = gpib('NI', 0, 1);
    else
        fclose(obj_dg2020a);
        obj_dg2020a = obj_dg2020a(1);
    end

    % Connect to instrument object, obj_dg2020a.
    fopen(obj_dg2020a);

    %Set DG2020A Voltage Levels
    vhigh = '3V';
    vlow = '0.0V';
```

```
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH0:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH0:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH1:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH1:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH2:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH2:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH3:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH3:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH4:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH4:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH5:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH5:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH6:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH6:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH7:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH7:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH8:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH8:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH9:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH9:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH10:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH10:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH11:HIGH 3.0V', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODA:CH11:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH0:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH0:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH1:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH1:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH2:HIGH %s', vhigh));
```

```
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH2:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH3:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH3:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH4:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH4:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH5:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH5:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH6:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH6:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH7:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH7:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH8:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH8:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH9:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH9:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH10:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH10:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH11:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODB:CH11:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH0:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH0:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH1:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH1:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH2:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH2:LOW %s', vlow));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH3:HIGH %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH3:LOW %s', vlow))
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH4:High %s', vhigh));
fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH4:LOW %s', vlow));
```

```
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH5:HIGH %s', vhigh));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH5:LOW %s', vlow));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH6:HIGH %s', vhigh));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH6:LOW %s', vlow));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH7:HIGH %s', vhigh));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH7:LOW %s', vlow));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH8:HIGH %s', vhigh));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH8:LOW %s', vlow));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH9:HIGH %s', vhigh));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH9:LOW %s', vlow));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH10:HIGH %s', vhigh));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH10:LOW %s', vlow));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH11:HIGH %s', vhigh));
    fprintf(obj_dg2020a, sprintf('OUTP:PODC:CH11:LOW %s', vlow));

    %Set Internal Frequency
    fprintf(obj_dg2020a, 'SOUR:OSC:SOUR INT');
    fprintf(obj_dg2020a, 'SOUR:OSC:INT:FREQ 1MHz');

    %Run Mode
    fprintf(obj_dg2020a, 'mode:state repeat');
    fprintf(obj_dg2020a, 'stop');       %Stop output before changing values

a=127;       %Channel1 I zero vector
b=127;       %Channel1 Q zero vector
c=127;       %Channel2 I zero vector
d=127;       %Channel2 Q zero vector

wp = 255;     %Channel 1 I+ scaled vector value
```

```
wm = 0;       %Channel 1 I- scaled vector value

xp = 255;     %Channel 1 Q+ scaled vector value

xm = 0;       %Channel 1 Q- scaled vector value


yp = 255;     %Channe2 1 I+ scaled vector value

ym = 0;       %Channe2 1 I- scaled vector value

zp = 255;     %Channe2 1 Q+ scaled vector value

zm = 0;       %Channe2 1 Q- scaled vector value


%-------------------------------------------------------------QPSK Channel 1

symbols = 4;

size = 256;


theta1_0 = 90;

theta1_1 = 135;

theta1_2 = 225;

theta1_3 = 315; % remember to zero out Channel 2 below in "Single Channel

 QPSK" section


magscale = 1.0;


delta_ip1 = 1*magscale;      delta_ip2 = 1*magscale;

delta_im1 = 1*magscale;      delta_im2 = 1*magscale;

delta_qp1 = 1*magscale;      delta_qp2 = 1*magscale;

delta_qm1 = 1*magscale;      delta_qm2 = 1*magscale;


iqimbal1 = 0;       iqimbal2 = 0;

%-------------------------------------------------------------------------%
```

```
% ------------------------------------------------------------QPSK Channel 2
symbols = 4;
size = 256;

theta2_0 = 45;
theta2_1 = 135;
theta2_2 = 225;
theta2_3 = 315; % remember to zero out Channel 1 below in "Single Channel
 QPSK" section
magscale = 1;

delta_ip1 = 1*magscale;      delta_ip2 = 1.05*magscale;
delta_im1 = 1*magscale;      delta_im2 = .85*magscale;
delta_qp1 = 1*magscale;      delta_qp2 = 1.0*1.025*magscale;
delta_qm1 = 1*magscale;      delta_qm2 = .90*1.025*magscale;

iqimbal1 = 0;         iqimbal2 = 0;
% ------------------------------------------------------------------------%

% ------------------------------------------------------------16QAM
symbols = 16;
size = 256;

theta1_0 = 135;             theta2_0 = 135;             %corner
theta1_1 = 150.25;     theta2_1 = 66.62;
theta1_2 = 113.38;      theta2_2 = 29.75;
theta1_3 = 45;              theta2_3 = 45;              %corner
theta1_4 = 203.38;     theta2_4 = 119.75;
theta1_5 = 205.53;        theta2_5 = 64.47;
```

```
theta1_6 = 115.53;          theta2_6 = 334.47;
theta1_7 = 60.25;       theta2_7 = 336.62;
theta1_8 = 23.37;      theta2_8 = 299.75;
theta1_9 = 25.53;         theta2_9 = 244.47;
theta1_10 = 295.53;        theta2_10 = 154.47;
theta1_11 = 240.25;     theta2_11 = 156.62;
theta1_12 = 225;             theta2_12 = 225;            %corner
theta1_13 = 330.25;     theta2_13 = 246.62;
theta1_14 = 293.38;     theta2_14 = 209.75;
theta1_15 = 315;             theta2_15 = 315;            %corner

magscale = 1;
delta_ip1 = 1*magscale;       delta_ip2 = 1*magscale;
delta_im1 = 1*magscale;       delta_im2 = 1*magscale;
delta_qp1 = 1*magscale;       delta_qp2 = 1*magscale;
delta_qm1 = 1*magscale;       delta_qm2 = 1*magscale;
iqimbal1 = 0;          iqimbal2 = 0;
% ------------------------------------------------------------------------%

% symbols = 2;

%------------------------------------------------ Channel 1 angle to symbol
for s = 0:symbols-1
    if  or(eval(sprintf('theta1_%d',s)) <= 90,
     eval(sprintf('theta1_%d',s)) >= 271)
           result = round(delta_ip1*(wp-a)*cosd(eval(sprintf('theta1_%d',s)))
            +a);
           eval(['symbi1_' num2str(s) '= result'])
    elseif and(eval(sprintf('theta1_%d',s)) >= 91,
```

```
 eval(sprintf('theta1_%d',s)) <= 270)
       result = round(delta_im1*(a-wm)*cosd(eval(sprintf('theta1_%d',s)))
        +a);
       eval(['symbi1_' num2str(s) '= result'])
   else
       disp('ERROR')
       disp(sprintf('theta1_%d',s))
   end

   if  and(eval(sprintf('theta1_%d',s)) >= 0,
    eval(sprintf('theta1_%d',s)) <= 180)
       result = round(delta_qp1*(xp-b)*sind(eval(sprintf('theta1_%d',s)))
        +b);
       eval(['symbq1_' num2str(s) '= result'])
       result2 = sind(iqimbal1)*eval(sprintf('symbq1_%d',s));
       eval(['symbi1_' num2str(s) '= symbi1_' num2str(s) '+ result2;'])
   elseif eval(sprintf('theta1_%d',s)) >= 181
       result = round(delta_qm1*(b-xm)*sind(eval(sprintf('theta1_%d',s)))
        +b);
       eval(['symbq1_' num2str(s) '= result'])
       result2 = sind(iqimbal1)*eval(sprintf('symbq1_%d',s));
       eval(['symbi1_' num2str(s) '= symbi1_' num2str(s) '- result2;'])
   else
       disp('ERROR')
       disp(sprintf('theta1_%d',s))
   end
end
%-------------------------------------------------------------------------%
```

```
%------------------------------------------------ Channel 2 angle to symbol
for s = 0:symbols-1
    if  or(eval(sprintf('theta2_%d',s)) <= 90,
     eval(sprintf('theta2_%d',s)) >= 271)
           result = round(delta_ip2*(yp-c)*cosd(eval(sprintf('theta2_%d',s)))
            +c);
           eval(['symbi2_' num2str(s) '= result;'])
    elseif and(eval(sprintf('theta2_%d',s)) >= 91,
     eval(sprintf('theta2_%d',s)) <= 270)
           result = round(delta_im2*(c-ym)*cosd(eval(sprintf('theta2_%d',s)))
            +c);
           eval(['symbi2_' num2str(s) '= result;'])
    else
           disp('ERROR')
           disp(sprintf('theta2_%d',s))
    end

    if  and(eval(sprintf('theta2_%d',s)) >= 0,
     eval(sprintf('theta2_%d',s)) <= 180)
           result = round(delta_qp2*(zp-d)*sind(eval(sprintf('theta2_%d',s)))
            +d);
           eval(['symbq2_' num2str(s) '= result;'])
           result2 = sind(iqimbal2)*eval(sprintf('symbq2_%d',s));
           eval(['symbi2_' num2str(s) '= symbi2_' num2str(s) '+ result2;'])
    elseif eval(sprintf('theta2_%d',s)) >= 181
           result = round(delta_qm2*(d-zm)*sind(eval(sprintf('theta2_%d',s)))
            +d);
           eval(['symbq2_' num2str(s) '= result;'])
           result2 = sind(iqimbal2)*eval(sprintf('symbq2_%d',s));
```

```
            eval(['symbi2_' num2str(s) '= symbi2_' num2str(s) '- result2;'])
    else
        disp('ERROR')
        disp(sprintf('theta2_%d',s))
    end
end
%-------------------------------------------------------------------------%


%-----------------------------------------------Single Channel QPSK
% symbi1_0 = a; symbq1_0 = b; %Uncomment for Channel 2 Only QPSK
% symbi1_1 = a; symbq1_1 = b; %Uncomment for Channel 2 Only QPSK
% symbi1_2 = a; symbq1_2 = b; %Uncomment for Channel 2 Only QPSK
% symbi1_3 = a; symbq1_3 = b; %Uncomment for Channel 2 Only QPSK


% symbi2_0 = c; symbq2_0 = d; %Uncomment for Channel 1 Only QPSK
% symbi2_1 = c; symbq2_1 = d; %Uncomment for Channel 1 Only QPSK
% symbi2_2 = c; symbq2_2 = d; %Uncomment for Channel 1 Only QPSK
% symbi2_3 = c; symbq2_3 = d; %Uncomment for Channel 1 Only QPSK
%-----------------------------------------------------------------%


%--------------------------------Make sure chip stays within safety limits
dangerflag=0;
safehigh = 240;
safelow = 15;
for s = 0:symbols-1
    if or(eval(sprintf('symbi1_%d',s)) > safehigh, eval(sprintf('symbi1_%d',s))
```

```
     < safelow)
             disp('DANGER -- BIAS POINT BEYOND SAFE LIMITS!!!!!!!!!')
             sprintf('symbi1_%d',s)
             dangerflag = 1;
    elseif or(eval(sprintf('symbq1_%d',s)) > safehigh, eval(sprintf('symbq1_%d',s))
     < safelow)
             disp('DANGER -- BIAS POINT BEYOND SAFE LIMITS!!!!!!!!!')
             sprintf('symbi1_%d',s)
             dangerflag = 1;
    elseif or(eval(sprintf('symbi2_%d',s)) > safehigh, eval(sprintf('symbi2_%d',s))
     < safelow)
             disp('DANGER -- BIAS POINT BEYOND SAFE LIMITS!!!!!!!!!')
             sprintf('symbi1_%d',s)
             dangerflag = 1;
    elseif or(eval(sprintf('symbq2_%d',s)) > safehigh, eval(sprintf('symbq2_%d',s))
     < safelow)
             disp('DANGER -- BIAS POINT BEYOND SAFE LIMITS!!!!!!!!!')
             sprintf('symbi1_%d',s)
             dangerflag = 1;
    end
end
%-------------------------------------------------------------------------%

%------------------------Concatenates all the binary bytes to binary words
    w3 = zeros(symbols,32);
    for n = 1:symbols
        str4 = strcat(dec2bin(eval(sprintf('symbi1_%d',n-1)),8),
        dec2bin(eval(sprintf('symbq1_%d',n-1)),8),
        dec2bin(eval(sprintf('symbi2_%d',n-1)),8),
```

```
        dec2bin(eval(sprintf('symbq2_%d',n-1)),8) );
        for k = 1:32
            w3(n,k) = str2num(str4(k));
        end
    end
%-------------------------------------------------------------------------%

%---------------------sets up the (random) symbols to be input to DG2020A
    array4 = zeros(32,size);          %zeros out the word matrix
    for k = 1:2:size-1                %sets up the matrix with random word order
        rand = randi(symbols);
        array4(:,k) = eval(sprintf('w3(%d,:)',rand));
        array4(:,k+1) = eval(sprintf('w3(%d,:)',rand));
    end
%-------------------------------------------------------------------------%

fprintf(obj_dg2020a, sprintf('data:msize %d', size));   %# of symbols in the pattern

%-----------------------------------------------writes DAC1 bits wordwise (size)
    word = '0';
    address = 0;
       position = 2;         %bit position index
                for j=1:size
                    word(j) = num2str(array4(position-1, j));
                end
                fprintf(obj_dg2020a, sprintf('DATA:PATTERN:BIT %d,%d,%d,#3%d%s',
                 19, address, size, size, word))
       for position = 3:10         %bit position index
                for j=1:size
```

```
                    word(j) = num2str(array4(position-1, j));
                end
                fprintf(obj_dg2020a, sprintf('DATA:PATTERN:BIT %d,%d,%d,#3%d%s',
                 position, address, size, size, word))
        end
        for position = 3:18         %bit position index
                for j=1:size
                    word(j) = num2str(array4(position-1, j));
                end
                fprintf(obj_dg2020a, sprintf('DATA:PATTERN:BIT %d,%d,%d,#3%d%s',
                 position, address, size, size, word))
        end
%-------------------------------------------------------------------------%

%-----------------------------------------writes DAC2 bits wordwise
     word = '0';
    address = 0;
       for position = 20:35         %bit position index
                for j=1:size
                    word(j) = num2str(array4(position-3, j));
                end
                fprintf(obj_dg2020a, sprintf('DATA:PATTERN:BIT %d,%d,%d,#3%d%s',
                 position, address, size, size, word))
        end
%-------------------------------------------------------------------------%

%-----------------------------------------------------writes clock wordwise
 clock = '0';
 position = 11;                          %CLK
```

```
            %for address = 0:8:size-8
            address = 0;
                for j=1:2:size-1
                    clock(j) = '0';
                    clock(j+1) = '1';
                end
                fprintf(obj_dg2020a, sprintf('DATA:PATTERN:BIT %d,%d,%d,#3%d%s',
                 position, address, size, size, clock))
%-------------------------------------------------------------------------%

%-----------------------------------clears control word latch bits wordwise
clear = '0';
for j=1:size
        clear(j) = '0';
   end
   address = 0;
   position = 0;
   fprintf(obj_dg2020a, sprintf('DATA:PATTERN:BIT %d,%d,%d,#3%d%s', position,
    address, size, size, clear))

   position = 1;
   fprintf(obj_dg2020a, sprintf('DATA:PATTERN:BIT %d,%d,%d,#3%d%s', position,
    address, size, size, clear))
%-------------------------------------------------------------------------%

%---------------------------------------Check for danger flag
if dangerflag == 1
    disp('DANGER -- BIAS POINT BEYOND SAFE LIMITS!!!!!!!!!')
else
```

```
    fprintf(obj_dg2020a, 'start');
end
%-------------------------------------------------------------------------%

fclose(obj_dg2020a);                    %Close connection to DG2020A

beep                                    %Alert that script is complete
disp('done')
```

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RELATED PUBLICATIONS

[1] **E. Juntunen**, C. Patterson, W. Khan, S. Bhattacharya, D. Dawn, J. Laskar, J. Papapolymerou, "A low-Power 2-Channel CMOS Millimeter-Wave Vector Modulator for LINC Transmitters," *Submitted to the IEEE Transactions on Microwave Theory and Techniques*

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PATENT APPLICATIONS

[1] US Patent Application Serial No 12/850,481. "Multi-Gigabit Millimeter Wave Receiver System and Demodulator System."' Filing Date: 04 August 2010. GTRC Ref. No. 4197.

VITA

Eric Andrew Juntunen was born in Ann Arbor, MI, USA in 1980. He received his bachelor of science in electrical engineering from Western Michigan University, Kalamazoo, MI, USA in 2003, and his master of science in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA in 2009. During his Ph.D. program, he held an internship position at BAE Systems, Merrimack, NH in 2009. He held a part-time position with Samsung Electro-Mechanics America, Inc. in Atlanta, GA in 2010-2011 and a full-time position with Peraso Technologies, Inc. in Toronto, ON, Canada in 2011-2012. He has authored or co-authored 8 IEEE publications and served as a reviewer for the IEEE Transactions on Microwave Theory and Techniques and Analog Integrated Circuits and Signal Processing. He has one patent application filed.