DESIGN AND DEMONSTRATION OF ULTRA-MINIATURIZED GLASS-BASED 3D IPD DIPLEXERS AND 3D IPAC RF FRONT-END MODULES FOR LTE APPLICATIONS

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DESIGN AND DEMONSTRATION OF ULTRA-MINIATURIZED GLASS-BASED 3D IPD DIPLEXERS AND 3D IPAC RF FRONT-END MODULES FOR LTE APPLICATIONS

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To my family and friends

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LIST OF ABBREVIATIONS

2D	Two-dimensional
3D	Three-dimensional
4G	Fourth generation
5G	Fifth generation
ADS	Advanced design system
BAW	Bulk acoustic wave
BEOL	Back end of line
BGA	Ball grid array
BT	Bluetooth
CTE	Coefficient of thermal expansion
CA	Carrier aggregation
CDMA	Code division multiple access
CMOS	Complementary metal–oxide–semiconductor
CMP	Chemical mechanical polishing
Cu	Copper
Div FEM	Diversity front-end module
CO_2	Carbon dioxide
DPDT	Double-pole-double-through
EM	Electromagnetic
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ENIG	Electroless nickel immersion gold
FEM	Front-end module

FEMiD	Front-end module with integrated duplexer
GPS	Global positioning system
GSM	Global system for mobile
GSG	Ground-signal-ground
HBF	High-band filter
HFSS	High frequency structural simulator
HPF	High-pass filter
IC	Integrated circuit
IF	Intermediate frequency
IL	Insertion loss
IoT	Internet-of-Things
IPAC	Integrated passive and active component
IPD	Integrated passive device
LC	Inductor and capacitor
LCP	Liquid crystal polymer
LNA	Low-noise amplifier
LBF	Low-band filter
LPF	Low-pass filter
LTCC	Low-temperature cofired ceramics
LTE	Long-term evolution
MCM	Multi-chip module
MIM	Metal-insulator-metal
MIMO	Multiple-input-multiple-output
PECVD	Plasma-enhanced chemical vapor deposition
Q	Quality

RDL	Redistribution layer
PA	Power amplifier
PAiD	Power amplifier with integrated duplexer
PCB	Printed circuit board
RF	Radio frequency
RL	Return loss
SAW	Surface acoustic wave
SAP	Semi-additive process
SMD	Surface-mounted device
SMT	Surface mount technology
SRF	Self-resonant frequency
SESUB	Semiconductor embedded in substrate
Si_3N_4	Silicon Nitride
SOC	System-on-chip
SPDT	Single-pole-double-through
SSN	Simultaneous switching noise
TGV	Through-glass via
TPV	Through-package via
Ti	Titanium
UV	Ultraviolet
VNA	Vector network analyzer
WLAN	Wireless local area network

SUMMARY

The objective of this research is to design and demonstrate three-dimensional integrated passive device (3D IPD) diplexers and three-dimensional integrated passive and active component (3D IPAC) packages with ultra-miniaturized glass substrates for radio frequency (RF) fourth generation long-term evolution (4G LTE) front-end modules (FEMs).

This research overcomes the short comings of current FEMs in many ways. These include 1) substrate thickness minimization to as small as 100 μm; 2) high-Q inductors and low-loss ultra-high density thinfilm capacitors embedding into ultra-thin glass substrates; 3) precision passives manufacturing and low-cost panel-level component assembly on double sides of substrates; and 4) systematic study on process-induced variations and RF design sensitivity.

First, both circuit-level and full-wave electromagnetic (EM) simulations were employed to design the LTE diplexers and modules. Leveraging the low loss of glass substrates and their ability to provide precision fine features and through-vias, high-density high-quality factor inductors and capacitors were designed for filtering and impedance matching circuits. More than 5 nH / mm^2 inductance densities were achieved on 50-200 μm thick glass with Q factors better than 60 in LTE bands. Ultra-high density (>300 pF /mm^2) high-Q thinfilm capacitors have also been designed on glass substrates. With these breakthroughs, the designed LTE filters and diplexers on ultra-thin glass substrates feature low passband insertion loss (IL) and high out-of-band rejection attributes. The designed LTE FEMs with substrate-embedded impedance matching

networks and electromagnetic interference (EMI) shields, as well as surface-assembled discrete acoustic wave filters on glass showed improved system performance and miniaturization compared to traditional laminate technologies.

Second, glass substrate processes were developed to demonstrate the designed passive components and modules. The key process innovations are low-cost, reliable, through-package via formation, thinfilm passive integration, precision fabrication with better than 5% variation and double-side chip-level assembly on 50-100 μm thick ultra-thin glass, much beyond prior work in 3D glass packages. The performance metrics of demonstrated 3D IPDs and FEMs were characterized, and excellent correlation between modelling and measured results were observed. Superior electrical performance and miniaturized package size in both vertical and lateral dimensions compared to traditional two-dimensional (2D) packages were demonstrated with the proposed 3D glass packages.

In addition, a comprehensive analysis was also conducted to quantify the process-induced variations and evaluate the performance sensitivities of designed diplexers to these fluctuations. Three-dimensional microscopy was used to quantify the differences between fabricated samples and designs in terms of conductors' linewidth, spacing, and thickness, dielectric layer thickness, and multi-layer alignment accuracy. EM simulations were conducted to analyze the sensitivity of various factors that affect the performance of glass-substrate embedded passives. Process improvement solutions for large-scale manufacturing were also proposed and evaluated.

Finally, both electrical and package design ground rules for 3D glass packaging with substrate-embedded passives and double-side surface-assembled devices were proposed to achieve system-level miniaturization and improved performance.

CHAPTER 1

INTRODUCTION

The growing demands to access vast quantities of information and realize fast data-exchange for mobile networks, autonomous driving, sensing and Internet-of-Things (IoT) are driving the proliferation of wireless communication systems. It is estimated that tens of billions of these devices will be connected through these networks, as shown in Figure 1.1. Wireless connectivity is established with multiple communication standards. Traditional communication standards such as global system for mobile (GSM) communications, wireless local area network (WLAN), global positioning system (GPS), and Bluetooth should coexist with emerging fifth generation (5G) standards in future RF systems [1]. All of these are driving the need for ultra-miniaturized, high-performance and diverse RF modules.

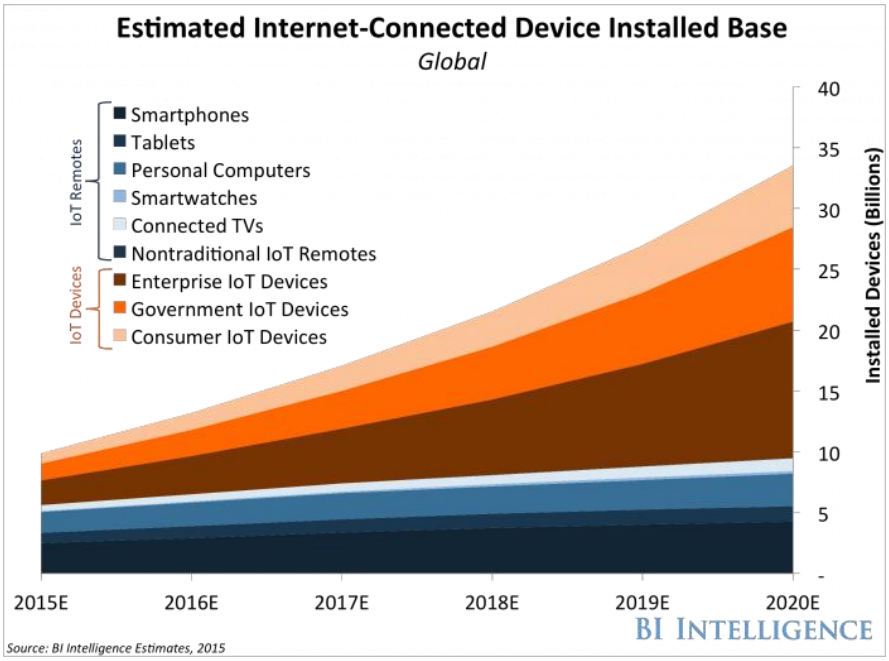


Figure 1.1. Proliferation of electronic systems connected through wireless networks [2].

1.1 RF Module Roadmap

A critical need for the wireless systems is to reach the peak connectivity speeds and offer high-quality user experience, such as enjoying smooth streaming of video, virtual reality and other data-intensive applications. Driven by such demands, the next-generation 5G wireless communication system will enable multi-gigabit data rates. However, the establishment of the 5G network does not overthrow current 4G cellular infrastructure, but rather leverage today's innovations in advanced 4G network to enable a broad range of future applications by expanding the available spectrum with wide contiguous carrier bandwidths [3]. New carrier frequencies below 6 GHz in the near future, as well as millimeter wave frequencies in the long-term need to be developed [4]. In addition to the exploration and employment of new carrier frequencies, core technologies such as carrier aggregation (CA) in current advanced 4G-LTE networks will be a key enabler to achieve high data rates for 5G infrastructures and thus will be further exploited in the future.

CA was proposed to offer higher uplink and downlink data rates within the existing spectrum [5]. Conceptually, this has been realized through the combination of simultaneously operated multiple LTE component carriers, each within a narrow bandwidth, to increase the overall capacity of the wireless networks. Major challenges that are faced by the hardware lie in the development of system-level integration technologies that could effectively increase the component density in a miniaturized RF FEM and meanwhile sufficiently suppress the crosstalk over multiple bands.

An example of RF FEM schematic diagram is sketched in Figure 1.2. Passives like filters or diplexers at multiple LTE bands are integrated with antenna switches and low-

noise amplifiers (LNAs) for receivers and power amplifiers (PAs) for transmitters. Together, they form FEMs, with one end connected to antennas while the other end is connected to the RF-to-digital interface for baseband processing.

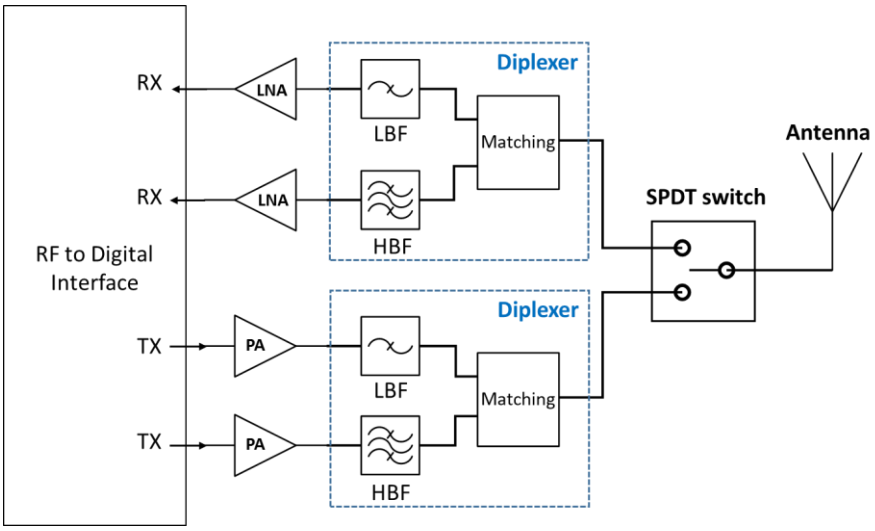


Figure 1.2. An example of RF FEM architecture.

Conventionally, front-end components are integrated as homogeneous functional blocks, examples of which are antenna switch banks, and diplexer banks, as shown in Figure 1.3. With an increasing need for form-factor reduction and more functionality in RF modules, system-level integration across different functional blocks within low, medium and high bands is essential for multiband FEMs with improved performance.

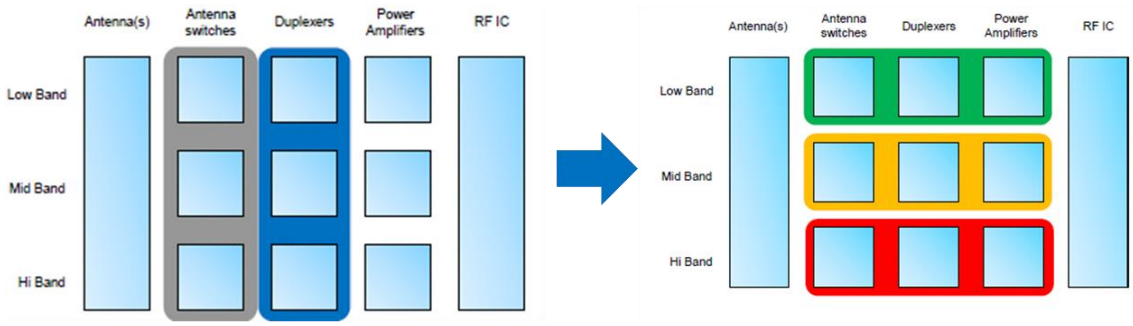
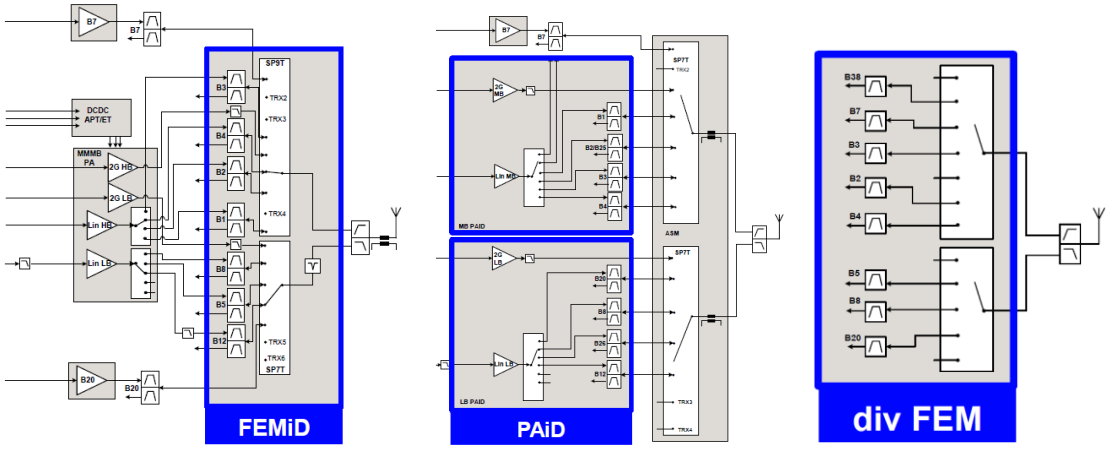


Figure 1.3. RF module trend from integration of similar functional blocks to system integration across different functional blocks (Courtesy: Dr. Christian Hoffman, Qualcomm).

In response to the need for band-level integration, a variety of FEMs are emerging in consumer markets [6]. Some of these FEMs are illustrated in Figure 1.4, including a front-end module with an integrated duplexer (FEMiD), a power amplifier with an integrated duplexer (PAiD) and a diversity front-end module (Div FEM). These FEMs are customized into different categories to meet the functionality requirement for different user architectures, while also providing the flexibility to enable further integration with the rest of the system. Multiband FEMs with CA is bound to increase the component density by an order of magnitude, without increasing the form-factor or power consumption. To meet these immediate needs, manufacturers are striving to enhance the quality factor of components, and achieve higher component densities with minimal interference. Innovations in passive components as well as their integration with actives forms the key R&D focus for future RF systems.



(a) (b) (c)

Figure 1.4. Block diagrams of FEMs subdivision: a) FEMiD, b) PAiD and c) Div FEM (Courtesy: Dr. Christian Hoffman, Qualcomm).

1.2 State-of-the-art RF Module Technologies

Today's RF modules primarily interconnect separately-packaged passive and active components to perform the FEM functions. These discrete devices are assembled onto substrates or printed circuit boards (PCBs) side-by-side, forming 2D FEMs. Several passive components are needed to perform system functionalities such as filtering, impedance matching and decoupling. These passive components typically outnumber the active components by more than 10 times, therefore, increasing the package footprint.

Traditional RF passives and substrates are manufactured with multilayered and cofired ceramic and conductor layers. Referred to as low-temperature cofired ceramics (LTCC), this technology has matured over the past few decades, and utilized for both passives and RF module substrates. With LTCC module substrates, the multiple ceramic layers not only can provide interconnections for signal and power delivery to the system, but can also be utilized to embed passive components so that the interconnection loss is mitigated. Despite its superiority in overall electrical performance, LTCC has its limitations in thickness reduction and large-scale manufacturing for low cost.

Proliferation of laminate-based packaging technologies aided by their low-cost and large-area manufacturing at 700mm x 700mm panel size made them the mainstream integrated circuit (IC) packaging solution. Discrete devices are assembled onto the organic package substrates or PCBs side-by-side in 2D architectures as multi-chip modules (MCMs). An example of such module is shown in Figure 1.5, which depicts a Skyworks 2.4GHz WLAN/Bluetooth (BT) front-end module used in HTC One.

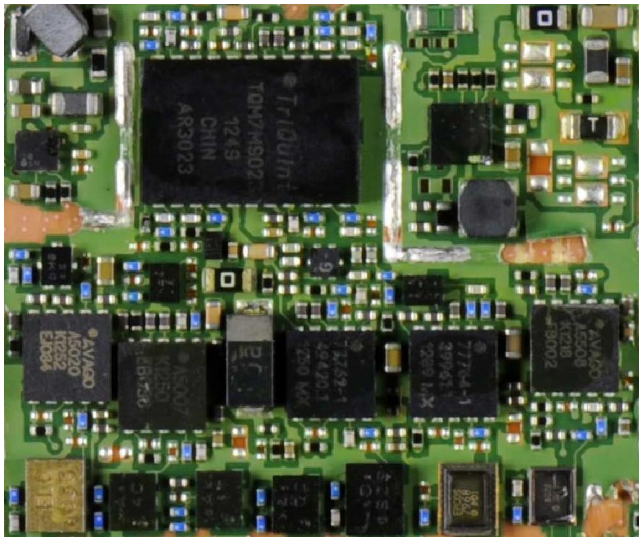


Figure 1.5. A Skyworks 85302-11 2.4 GHz WLAN/BT front end module in HTC One [7].

The side-by-side placement of these components requires long interconnections through the substrates, which generates additional losses. Their performance and form-factors fail to meet the compactness and multi-functionality needs for emerging consumer electronic products. This led to the evolution of new technologies for integration of passive devices as well as modules [8]. At component level, IPDs have been developed to allow the integration of several passive components into a single substrate. This reduces the pick-and-place costs, package footprint, routing issues and interconnection parasitics. These IPDs are realized on LTCC substrates [9], on laminate substrates [10] or in the form of thinfilms on silicon wafer [11] or in glass substrates [12]. These have been widely pursued in recent RF systems for higher functional densities.

Since the ultimate goal of passive components is to serve the active devices to provide various power and RF functions, it is important both to miniaturize the passives and also integrate them close to the active devices. This led to the focus in 3D or embedded modules. The primary motivation for embedded packaging is to reduce the package

footprint and thickness, and also shorten the interconnection length for improved electrical performance by reducing the insertion losses and loop inductance. In addition, embedding allows complete integration of modules for multiple bands in a single package with heterogeneous components. Embedded RF modules originally started with thin-film passive components in the substrate for matching networks, while semiconductor chips and other discrete components are assembled onto these passive-embedded substrates to form modules [13, 14]. However, actives embedding with fan-out technologies has become mainstream technology recently, either as wafer-level fan-out with molded and reconstructed wafers, or as panel fan-out in laminates. Discrete passives and other components are assembled onto these low-profile active-embedded substrates. A prominent example is SESUB or "semiconductor embedded in substrate", enabling multi-functional and miniaturized solutions for RF applications [15]. Multiple semiconductor chips are embedded side-by-side in a fully-molded laminate but with backside device surfaces accessible for cooling. The substrates, with embedded 50 μm thin ICs, are as thin as 300 μm or less, on top of which discrete components are assembled. Georgia Tech advanced this concept further with chip-last embedded and fan-out power and RF modules [16]. In this approach, the core and build-up layers of the substrates are also used to embed thinfilm passives such as filters, along with interconnect layers that include transmission lines. Build-up layers with laser-ablated cavities are laminated onto these core layers. ICs were assembled into these cavities at low temperatures. LNA, PA and switch were embedded inside pre-fabricated cavities in organic substrates to form RF modules. Figure 1.6 depicts the evolution of RF packaging technologies in both passive components and module integration [17-20].

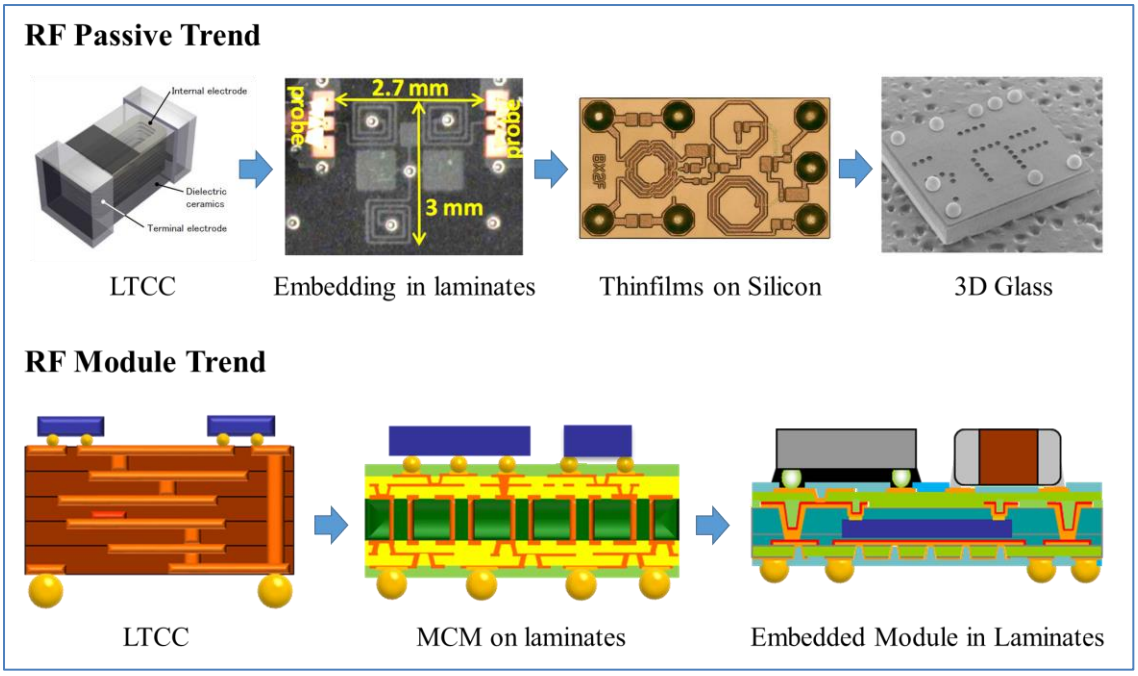


Figure 1.6. Evolution of RF passives and module integration technologies.

While the state-of-the-art embedding technologies have made great progress in terms of system miniaturization and performance enhancement, several challenges still remain. With LTCC substrates, thickness reduction and poor precision during multilayer fabrication limit the miniaturization of RF components and modules. Traditional organic substrates offer a low-cost alternative because of their large-scale manufacturability with cheaper materials, but are limited by its dielectric losses and dimensional instabilities, which lead to poor tolerance, making them difficult to meet high-performance requirements. While the back end of line (BEOL) processes that have been used in silicon IPDs can offer the best tolerance control in fabrication, the poor electrical insulation of silicon creates additional substrate losses that degrade the IPD performance. Glass-based passive devices were also developed but with single-side thinfilm components. A complete RF system integration technology, that can both improve the performance and reduce the form factor, has not been pursued yet.

1.3 3D Glass-based Integrated RF Packages

To overcome the shortcomings of existing RF module technologies on LTCC and laminates, glass is emerging as a promising next-generation substrate material because of its several superior attributes:

1) low loss and high resistivity, which are key enablers for high-Q passives design, high data transfer rates at lower power consumption, and low crosstalk;
2) superior dimensional stability for well-controlled layer-to-layer circuitry registration, and smooth surfaces for precise circuitry patterning even with small feature size;
3) tailorable coefficient of thermal expansion (CTE) from 3 ppm/K - 9 ppm/K for improved reliability of both first-level interconnections with silicon chips and second-level assembly onto PCBs;
4) low-cost panel-level manufacturability that is compatible with existing laminate substrate manufacturing infrastructures;
5) capability for double-side component integration with through glass vias (TGVs) at low warpage.

To further enhance the component densities and system performance with glass substrates, a new concept based on 3D IPAC was proposed by Prof. Rao R. Tummala [21]. With the 3D IPAC concept, passive components are either double-side assembled onto the module substrates or directly embedded as thinfilms in the module substrates. The passive components can also be double-side integrated as thinfilms onto glass substrates to form stand-alone 3D IPDs [22]. Active or passive component integration is realized through panel-level double-side assembly onto these passive-embedded ultra-

thin glass substrates. A cross-sectional view of the proposed 3D IPAC glass packages for RF FEMs is illustrated in Figure 1.7.

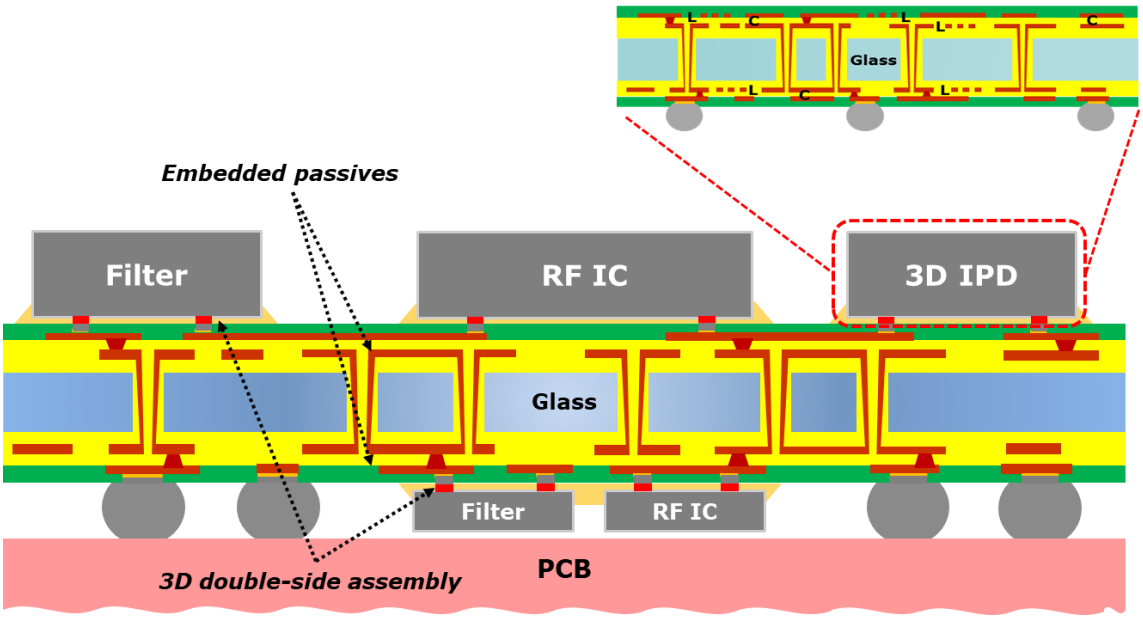


Figure 1.7. Proposed 3D IPAC glass packages for RF FEMs.

About 2X miniaturization in lateral dimensions is achieved with 3D IPAC by assembling surface-mountable active and passive devices on both sides of the substrate, and interconnecting them with ultra-short reliable TPVs. Further miniaturization is achieved by embedding passive components such as impedance matching networks into glass substrates. Glass also facilitates higher quality (Q) factor and precision fabrication for both substrate-embedded passives and 3D IPDs, owing to its attributes such as low loss and high modulus. Moreover, thinfilm technologies that have been previously applied on silicon or organic substrates are also compatible with glass substrates process. Hence, embedded or integrated passives in glass substrates can achieve higher density than conventional discrete components.

1.4 Research Objectives, Challenges and Tasks

1.4.1 Research Objectives

The objectives of the proposed research are to design, fabricate and characterize ultra-miniaturized 3D IPD LTE diplexers and 3D IPAC LTE modules with:

1) superior electrical performance;
2) miniaturized footprint and reduced thickness;
3) low manufacturing cost;

enabled by design and technology advances in precision low-loss thinfilm passives on ultra-thin glass substrates and double-side assembly. Table 1 lists the details of research objectives.

Table 1.1. Objectives of proposed research

Topics	Metrics	Prior Art	Objectives
3D IPD Diplexers	Performance	• IL = 0.6 dB • RL = 15 dB • Isolation = 20 dB	• IL < 0.6 dB • RL > 15 dB • Isolation > 20 dB
	Miniaturization	• Z = 1 mm • X-Y = 2mm x 2.5 mm	• Z < 0.3 mm • X-Y < 2 mm x 2.5 mm
3D IPAC Modules	Performance	• IL = 2 dB • RL = 14 dB • Q < 50	• IL < 2 dB • RL > 14 dB • Q > 60
	Miniaturization	• Volume ~ 5-10 mm^3 (Z > 600 μm) • Substrate thickness > 200 μm	• Volume ~ 1-3 mm^3 (Z < 500 μm) • Substrate thickness < 100 μm

1.4.2 Technical Challenges

<u>3D IPD Diplexers</u>

Key challenges in both electrical design and substrate fabrication need to be addressed to achieve the low loss and miniaturization targets for glass-based 3D IPD diplexers.

Tradeoff Between Performance and Size

The key performance metrics for diplexers are passband insertion loss, stopband rejection and band-to-band isolation. Lumped elements are typically used in WLAN and LTE bands for compactness while higher filter orders are favored for better selectivity. However, high-order filter designs usually come at the cost of larger package size and additional insertion loss, since more inductors and capacitors are needed. As illustrated in Figure 1.8, a bandpass filter with fourth order shows better stopband rejection than a second order design, but suffers from higher passband insertion loss.

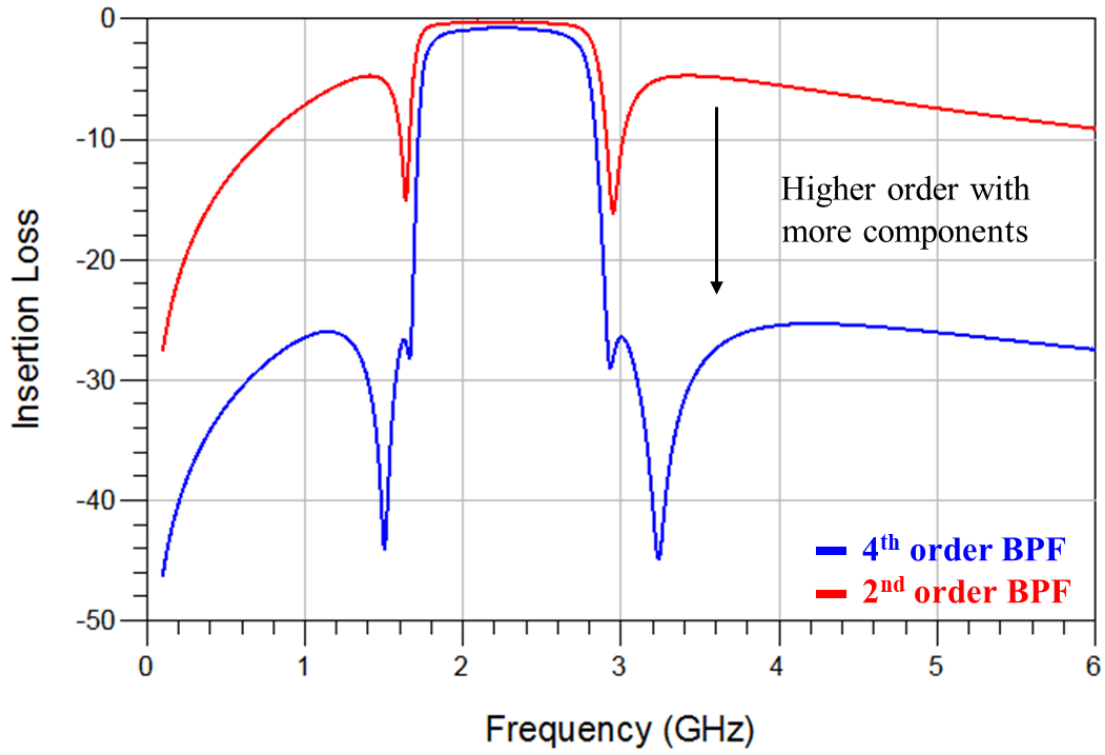


Figure 1.8. Performance comparison of a bandpass filter with different filter orders.

Substrate thickness and footprint targets further constrain the topology selection. In addition, in contrast to conventional IPDs on single-sided silicon or glass wafers, the 3D substrate architecture requires careful floor planning of passive components to minimize

crosstalk between passive circuits on either sides of the thin glass substrates and also suppress higher-order harmonics.

Process-induced Variations

RF circuits are sensitive to process-induced variations, and without a rigorous control, performance degradation from increased insertion loss, frequency-shift and band-spread are common issues faced by designers and manufacturers. This is illustrated in Figure 1.9. A 5% variation without any post-trimming is typically required. Stringent process control applies to both dielectric thinfilms that are a few hundred nanometers to a few micron meters thick, but also to multilayer fine-line RF circuitry patterning.

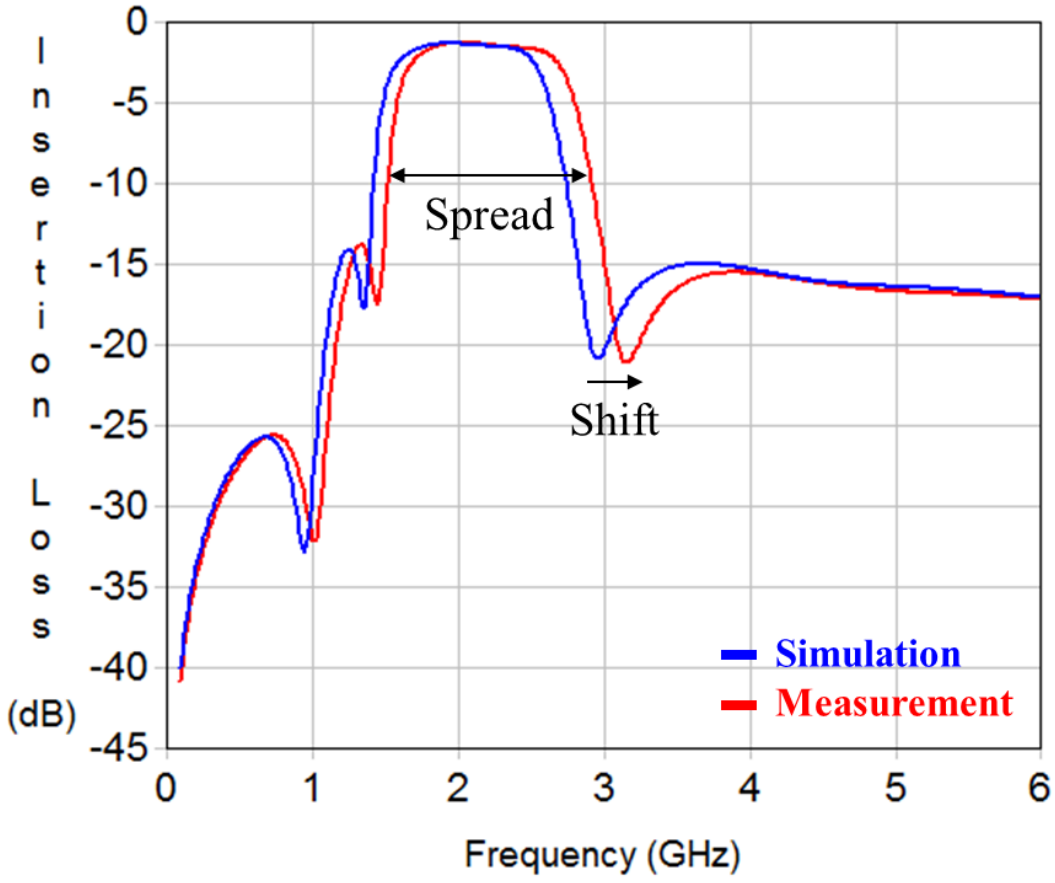


Figure 1.9. Process-induced band spread and frequency shift on a bandpass filter.

3D IPAC LTE Modules

Challenges in RF module integration on ultra-thin 3D glass packages predominantly come from electrical design, which includes high-Q inductors and component-level EMI shields as well as process development of panel-scale double-side flip-chip assembly on ultra-thin glass substrates.

Quality Factor Degradation and Proximity-induced EMI in Ultra-thin Substrates

In 3D IPAC LTE modules, impedance matching networks are embedded in ultra-thin glass packages. Inductors are critical building blocks for the matching networks. Although off-chip inductors benefit from the availability of low-cost package real-estate, they suffer because of additional losses that arise from increased interconnection lengths. To compensate for this additional loss from longer interconnects, low-loss inductors with Q factors that are two to three times higher than those from on-chip inductors are required. Achieving high Quality factors with thin glass substrates and smaller footprints is a major challenge. On ultra-thin 50-100 μm thick glass substrates, the copper (Cu) conductor thickness is further constrained by the fabrication processes and stress induced from the CTE mismatch between glass and copper. This limits the lowest equivalent series resistance that the inductors can achieve. Integrating magnetic materials into inductors can boost the magnetic flux and thus enhance the quality factors of inductors. However, most of the nanomagnetic film materials show high loss at in the GHz operation range and are not suitable for WLAN and LTE applications. With these constraints, design of high-quality factor inductors without compromising the package footprint is a major challenge.

In the proposed high-density 3D architectures in ultra-thin packages, system components are brought in close physical proximity to each other in both lateral and vertical directions, making them sensitive to electromagnetic interference from each other. The resulting parasitic effects can alter the circuit functionality and may also damages the victim devices. EMI shields are needed to suppress the electromagnetic radiations within the RF packages so that they can meet the electromagnetic compatibility (EMC) requirements.

Ultra-thin Glass Substrate Process

The substrate process challenges are similar to those described in the 3D IPD section. Fabrication of ultra-thin glass packages with 50 μm thick glass is an additional challenge that will be addressed in this task.

Double-side Integration of Components on Glass Substrates

Panel-scale double-side flip-chip assembly on ultra-thin glass substrates faces challenges associated with ball grid array (BGA) ball height to accommodate backside components, backside assembly without glass cracking and reflow conditions. Assembly-induced warpage in ultra-thin glass substrates, and package singulation-induced glass cracking also create additional challenges. A customized and novel process-flow is required to address these challenges.

1.4.3 Research Tasks

3D IPD Diplexers

High-performance 3D IPD Diplexer Design

Insertion loss reduction of a diplexer can be addressed by both achieving good impedance match in signals' passbands and designing high quality-factor passive components. Inorganic thinfilm technology is introduced with glass substrate fabrication, since it can bring more than 100 times increase in capacitance density as well as enhance the Q factor. It is critical that diplexer design not only addresses the trade-offs between filter order, footprint and performance, but also achieves this with a minimum number of inductors and inductance. High-Q inductor design is also essential to improve the overall diplexer performance. However, size reduction and Q factor improvement of inductors continue to face fundamental challenges. Therefore, from electrical design point of view, inductors become the bottleneck for diplexer's performance.

Precision Glass Substrate Fabrication

Process-induced variations at each fabrication stage must be quantified. Experimental characterization results such as dielectric thickness, conductor thickness and dimensions, and layer-to-layer mis-registration are documented, and refined electrical models are built with the actual geometries. The simulation results of this new model are compared to both original design as well as the measurement results on fabricated samples. By analyzing the correlation and discrepancy between these results, sensitivity of diplexer performance to process variations is studied. More importantly, sensitive material and design parameters that degrade the performance of diplexers are identified.

After identifying the sensitive factors that impact the diplexers' performance, fabrication processes were optimized to mitigate the mismatch between simulations and measurements. This study provides design guidelines to RF designers so that they can incorporate process variations into their electrical designs.

The research challenges and tasks for 3D IPD diplexer demonstration are summarized in Table 1.2.

Table 1.2. Research tasks for 3D IPD diplexers

Topics	Metrics	Objectives	Challenges	Tasks
3D IPD Diplexers	Performance	• IL < 0.6 dB • RL > 15 dB • Isolation > 20 dB	• Trade-off between performance and size • Process-induced variations of thinfilm passives fabrication	• ***High-performance 3D IPD diplexer design***: Design and integration of compact high-Q inductors and thinfilm capacitors in glass substrates • ***Precision glass substrate fabrication***: a) Quantitation of process variations and diplexer sensitivity study b) Process optimization for precise passive fabrication
	Miniaturization	• Z < 0.3 mm • X-Y < 2 mm × 2.5 mm		

3D IPAC LTE Modules

Miniaturized 3D Module Design

Fundamental limitations in designing high-Q inductors in ultra-thin glass substrates are studied through EM simulations and analysis. Different inductor design topologies, including planar spiral inductors, multilayer inductors and 3D solenoid inductors will be explored and compared in terms of inductance density, performance metrics and manufacturability.

Component-level EMI shielding techniques are also investigated to isolate the inductors in impedance matching circuits, as well as to reduce the crosstalk between double-side integrated components. Optimal EMI shielding structures with minimum degradation of inductors' Q factor will be designed. Ultra-miniaturized EMI shielded high-Q inductors in ultra-thin glass substrates will be proposed.

Ultra-thin Glass Substrate Fabrication

Panel-level processes of double-side passives embedding on 50 -100 μm thick glass are to be developed and demonstrated. In particular, substrate warpage and cracking issues on 50 μm thick glass are to be addressed with advances in substrate stack-up design and double-side processes.

Double-side Assembly on 3D Glass Packages

A manufacturable assembly process flow with optimal assembly sequence is proposed. Unit steps such as panel-scale BGA balling, double-side assembly and direct 3D glass package to PCB attachment will be developed. Concerns such as process yield from potential ultra-thin glass substrate cracking, RDL delamination and dicing-induced defects are monitored. Optimized process guidelines for double-side assembly on ultra-thin glass substrates will be provided. The research challenges and tasks for 3D IPAC module demonstration are summarized in Table 1.3.

Table 1.3. Research tasks to design and demonstrate 3D IPAC LTE modules

	Metrics	**Objectives**	**Challenges**	**Tasks**
3D IPAC Modules	Performance	• IL < 2 dB • RL > 14 dB • Q > 60	• Quality factor degradation of inductors in ultra-thin substrates and proximity-induced EMI • Ultra-thin glass substrate process • Double-side integration of components on ultra-thin glass substrates	• ***Miniaturized 3D module design***: Integrating high-Q embedded inductors and EMI shields on 50 μm thick glass • ***Ultra-thin glass substrate fabrication***: Precision component integration on ultra-thin glass substrates • ***Double-side assembly on 3D glass packages***: Panel-level BGA balling and flip-chip mass reflow for double-side assembly at low package warpage
	Miniaturization	• Z < 500 μm • Substrate thickness < 100 μm		

1.5 Dissertation Organization

The following chapters are organized as follows. Chapter 2 compiles the literature survey of RF passive and module technologies. Chapter 3 describes the design and demonstration of two types of thinfilm glass-based 3D IPD diplexers. Chapter 4 presents the research on design and demonstration of 3D IPAC RF modules with ultra-thin 50-100 μm thick glass. Finally, research summary, major scientific contributions, and suggestions for future work are compiled in Chapter 5.

CHAPTER 2

LITERATURE SURVEY

Innovations in passive and active components, and their high-density integration technologies are the principal enablers for breakthroughs in today's RF modules. This chapter reviews the most recent works that are related to these two building blocks. The first part discusses the progress in advanced passives, including thinfilm capacitors, high-Q inductors, filters and diplexers. The second part summarizes the evolution of the RF module integration technologies.

2.1 Advanced Passives

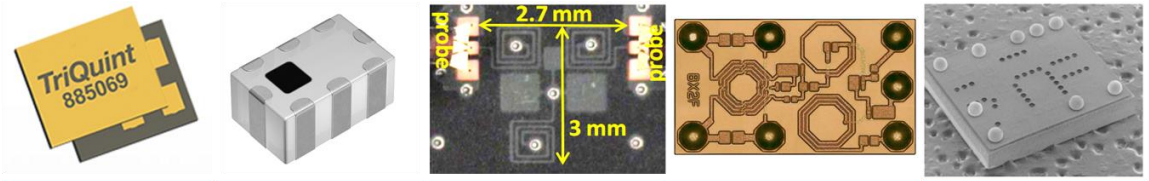
RF modules comprise of multiple passive components, which typically outnumber the actives by about 10:1. These passives can be classified into acoustic wave and planar electromagnetic types, depending on their fundamental working mechanism.

Acoustic wave devices are manufactured on the piezoelectric substrate materials, such as quartz, and they are usually packaged as discrete surface-mount devices (SMDs). Due to their superiority in low loss, small form-factor and high-precision, acoustic wave technologies are commonly utilized in making high performance filters, resonators and oscillators, and have found many applications in 4G-LTE networks [23].

On the other hand, RF passives in planar type show their advantages in high-frequency and wideband operation capability, flexibility as either discrete SMD components or embedded passives in substrates, and low-cost manufacturability. They are typically implemented in the form of distributed circuits or discrete lumped elements. Distributed circuits are usually constructed by transmission lines and waveguides, and they tend to

give high quality factors in microwave bandwidth. Lumped elements are zero-dimensional by definition, and they work perfectly in low RF frequencies such as below 10GHz. Since the wavelengths of electromagnetic waves in WLAN and LTE bands are relatively large, distributed circuits are not space-efficient[24]. Hence, lumped elements are extensively adopted for system miniaturization. Three essential elements of lumped elements are resistors, inductors and capacitors, and they can be discrete, integrated or embedded on substrates with a variety of design architectures.

In this chapter, RF passives can be classified into five categories by their integration technologies as summarized in Figure 2.1, and prior art in each category are discussed.



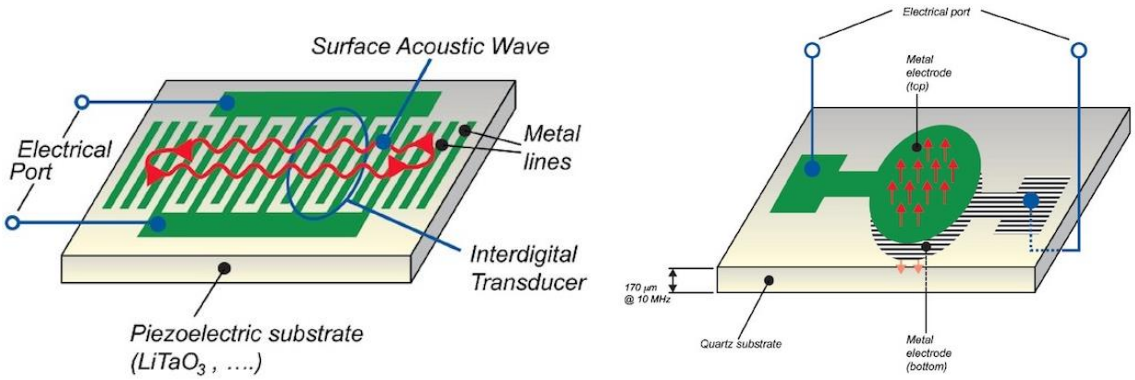
Acoustic Wave	LTCC	Laminate	Silicon	3D Glass
High selectivity	Low loss	Substrate loss	Substrate loss	Low loss
Thin	Thick	Thin	Thin	Thin
Small footprint	Small footprint	Moderate footprint	Moderate footprint	Small footprint
High density	Low density	Moderate density	Moderate density	High density
High cost	Mass production	Less in demand	High cost	Not in market

Figure 2.1. Summary of RF passive technologies [17, 19, 20, 25, 26].

2.1.1 Acoustic Wave Passives

Acoustic wave technology has been widely used for wireless communication in mobile phones over 20 years, and has been the key enabler to guarantee spectral integrity of RF signals. It has been widely adopted in making passive components such as resonators and filters. Acoustic wave filters can be classified into surface acoustic wave (SAW) filters and bulk acoustic wave (BAW) filters [27]. They are named and

distinguished by the direction of acoustic wave movement on the piezoelectric substrates. The fundamental working principle of acoustic wave filters is to perform a conversion between electrical energy and mechanical energy when voltage is applied to the crystal material. Since the efficiency of this energy conversion is extremely high, high quality factor and low insertion loss can be achieved. Therefore, narrow-band high-selectivity filters can be constructed, which require higher order designs that are not achievable by other technologies since they cannot afford the penalty of increased loss. Simplified examples of SAW and BAW filters are shown in Figure 2.2.



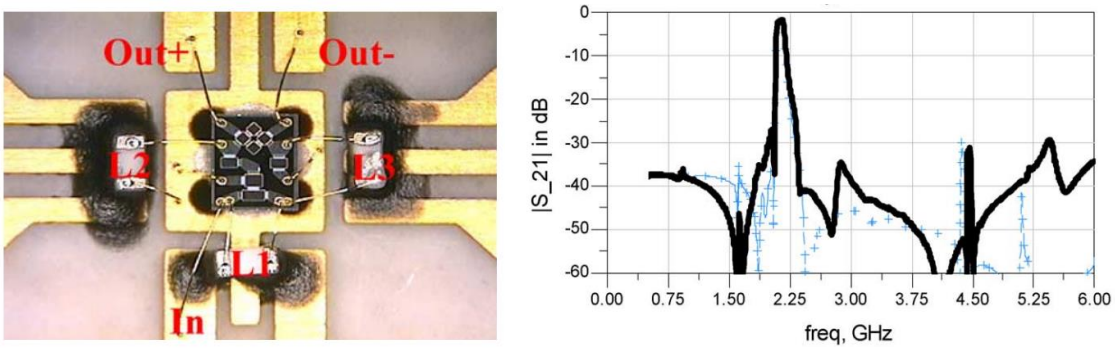
(a) (b)

Figure 2.2. Examples of acoustic wave passives: (a) a SAW filter, and (b) a BAW filter [28].

In SAW filters, acoustic waves propagate along the surface of the substrate, and dimensions of metal lines are directly correlated to the wavelengths of incoming RF signals. Since these metal lines are patterned by photolithography, it becomes challenging to fabricate SAW filters in high frequencies. BAW filters overcome this limitation by altering the excitation of acoustic waves to the vertical direction between two metal electrodes. This transfers the dimension requirement from lateral linewidth to vertical distance, and the thickness between the two metal electrodes becomes the bottleneck for

the operation frequency. Owing to the thinfilm deposition technologies, micron or sub-micron thick piezo layers can be achieved, offering high-frequency operation capability to BAW filters. Because of their excellent electrical performance, small form factor and compatibility with semiconductor manufacturing processes or standard MEMS fabrication processes, acoustic wave devices are widely utilized for filters.

An example of BAW bandpass filter is illustrated in Figure 2.3. The BAW filter had a passband between 2095 MHz to 2155 MHz with 60 MHz bandwidth, less than 2.1 dB passband insertion loss and more than 30 dB out-of-band signal rejection. The size of one individual BAW filter chip was only 1.0 mm × 0.8 mm laterally [29].



(a) (b)

Figure 2.3. Demonstration of a BAW bandpass filter: (a) diced BAW filter chip and auxiliary SMT inductors, and (b) transmission characteristics.

This filter design fully utilized the advantages of both ladder and lattice structures by using a balun to realize the electrical coupling between a single-ended ladder section at its input and a balanced lattice section at its output.

Although acoustic wave filters have their superiority in miniaturization, low insertion loss and high selectivity, they are restricted to narrow-band operation due to limited electromechanical coupling coefficient, which is determined by its design topology and

piezoelectric materials [30]. In addition, for high-frequency operation where BAW filters are particularly used, the manufacturing challenges due to constrained process precision tolerance and complexity of processes introduce additional cost.

2.1.2 LTCC Passives

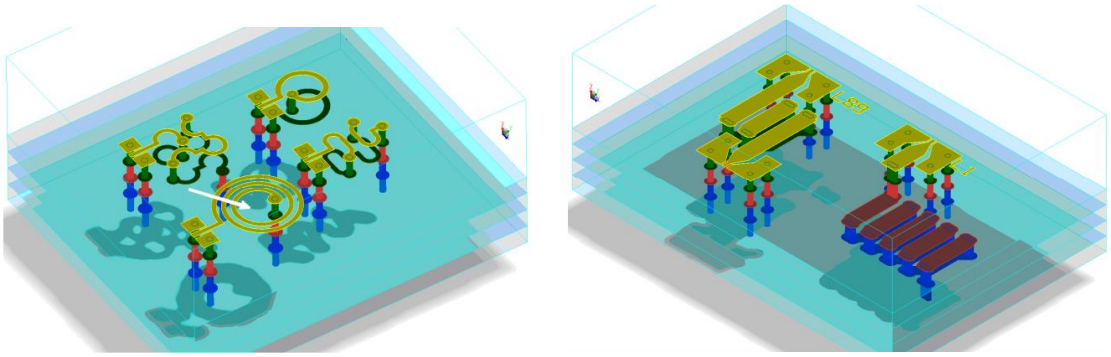
LTCC substrates typically use glass-ceramics as the dielectric and copper or silver as conductors to build high-quality factor passives and low-loss interconnects. Multiple ceramic layers are stacked and co-fired simultaneously, resulting in 3D circuits. LTCC passives are in the form of discrete elements, such as individual inductors and capacitors, or as IPDs, such as filters and diplexers. Individually-packaged discrete components and IPDs are surface-mounted onto substrates or PCBs. They have been extensively employed for building RF modules for decades.

High-Q LTCC Inductors

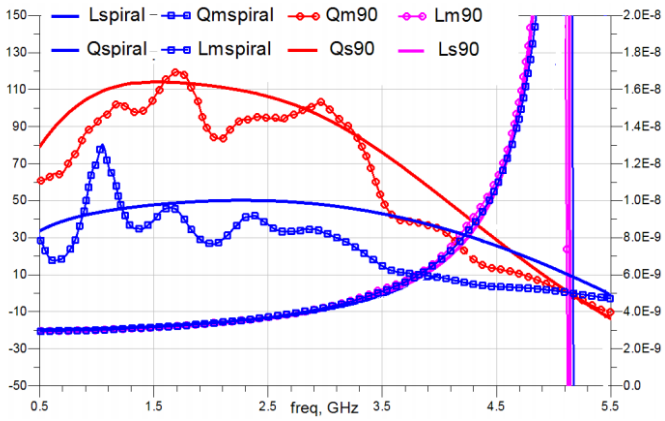
Inductance, Q factor and self-resonant frequency (SRF) are three major electrical attributes that depict electrical performance of an inductor. For high-performance applications, small-size high-Q inductors are imperative. Inductors can be classified into 2D planar types and 3D solenoid types by their physical geometries, and they are typically embedded into multilayers of ceramic substrates.

A study on performance comparison between spiral inductors and horizontal solenoid inductors on LTCC substrates was recently reported [31]. As shown in Figure 2.3, various inductors are designed with the same inductance and SRF, occupying two metal layers without counting the testing structures. From the performance metrics comparison shown in Figure 2.4 (c), the Q factor of a solenoid inductor doubled that of a spiral inductor from 0.5 GHz to 2.5 GHz, and peaked at around 1.5 GHz with a value of more

than 110. The enhancement of Q factor in a 3D configuration came from both reduced resistance with fatter metal traces and suppressed capacitance coupling between adjacent loops. In inductors design where lateral dimensions are fixed, 3D inductors generally offer higher Q factors than 2D types.



(a) (b)



(c)

Figure 2.4. Performance comparison of inductors on LTCC substrates: (a) layout of spiral inductors, (b) layout of horizontal solenoid inductors, and (c) performance metrics.

It is also worthy to mention that the designed LTCC high-Q horizontal solenoid inductors required large footprint size and yielded low inductance density (< 2 nH / mm^2). Because of this, they may not be suitable to be used in ultra-miniaturized RF systems.

To reduce the size, inductors are also favored to be designed in a vertical solenoid configuration, fully exploiting the advantages of multiple ceramic layers in a LTCC substrate. These inductors feature high Q factors and high inductance density per unit area. Therefore, they are commonly adopted in building low-loss IPDs and RF modules, in which thickness is not closely confined. A commercialized LTCC high-Q inductor is shown in Figure 2.5 [18].

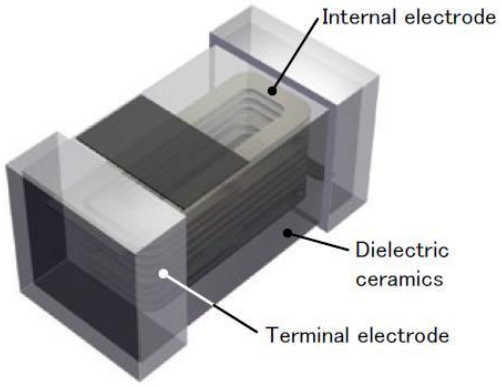


Figure 2.5. A LTCC high-Q vertical solenoid inductor.

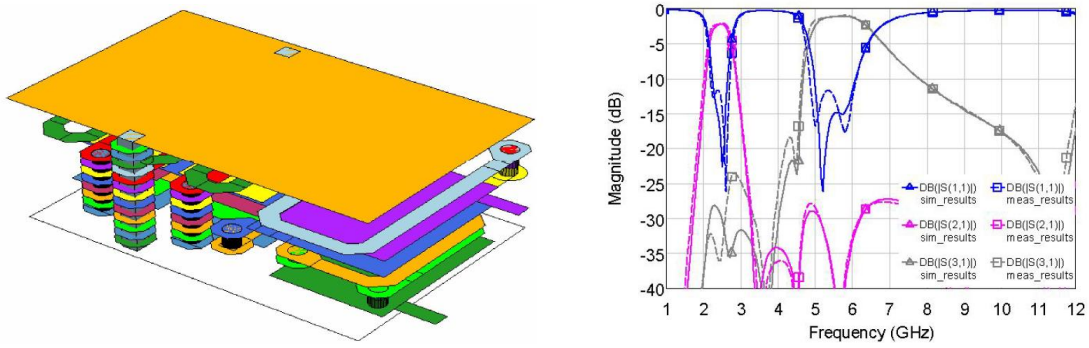
High-performance LTCC IPDs

A LTCC IPD integrates lumped inductors and capacitors all together into a single packaged substrate, where these embedded individual components are interconnected laterally or vertically through multiple ceramic layers. Depending on design complexity, the number of stacked layers can be different. Because of the low loss nature of ceramic and 3D substrate stack-up architecture, higher-performance IPDs can be designed in LTCC substrates.

Recent advances in LTCC IPDs demonstrated a diplexer with high band-selectivity and isolation on a six-layer LTCC substrate with a size of $3.45 \times 4.0 \times 0.7$ mm^3 [32]. A high-pass filter (HPF) and a low-pass filter (LPF) were used to separate the GSM and

code division multiple access (CDMA) bands. High isolation was achieved by introducing a transmission zero at the stopband of the LPF. The insertion loss and return loss (RL) of GSM bands were -0.54 dB and -10.5 dB respectively, while in the CDMA band, they were -1.13 dB and -6.16dB.

TDK-EPCOS demonstrated various compact WLAN diplexers on LTCC substrates with design innovations. By tuning the output admittances Y_{low} and Y_{high} of both low-band filter (LBF) and high-band filter (HBF) to be complex conjugates at the corresponding frequency bands, the size of the diplexer can be miniaturized since the impedance matching network can be eliminated [33]. A dual-band diplexer was also demonstrated by connecting a simple diplexer in series with a dual-band filter after shifting the notches of a broad-band filter [34]. More than 1 GHz bandwidth was achieved in HBF. Such a dual-band diplexer had a size of 2.1 mm ×1.5 mm × 0.56 mm, and was fabricated on a fourteen-layer LTCC substrate, as shown in Figure 2.6.



(a) (b)

Figure 2.6. A LTCC WLAN diplexer: (a) 3D layout, and (b) transmission characteristics.

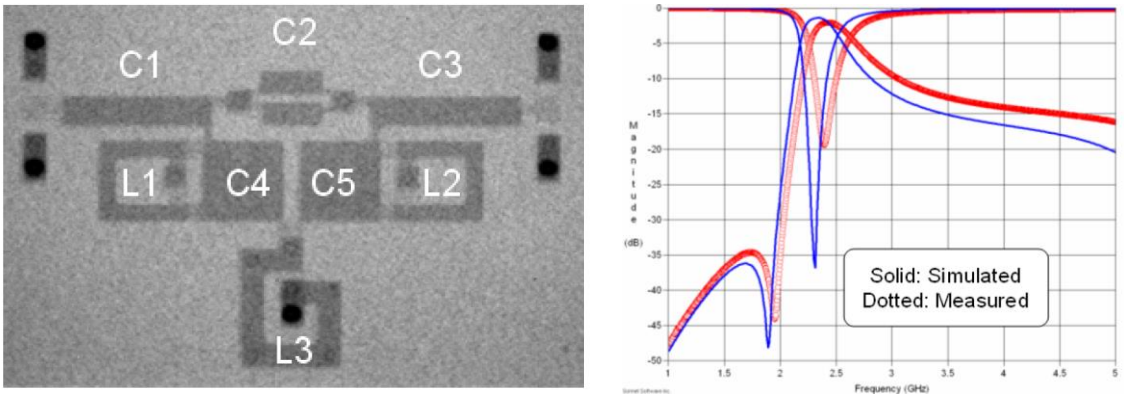
It has been proven that high-performance IPDs can be built on LTCC substrates. The remaining challenges are thickness reduction and high-density integration into a

miniaturized RF module. To build thin LTCC IPDs, ceramic layers need to be thinned and the layer count needs to be minimized, both leading to performance degradation. Conventionally, these components are mounted onto a laminate substrate with additional interconnections, which not only consume space, but also generate additional losses. Although embedding technologies are being pursued nowadays, the feasibility of embedding LTCC passives into laminate substrates is still questioned.

2.1.3 Laminate Passives

The need for cost and thickness reduction of passive components drove the development of laminate-based passive integration technology. By embedding the passive circuits into multiple build-up films and RDL layers of organic laminate substrates, higher component density can be achieved. As the films on laminate substrates are thinner and the layers are fewer compared to LTCC substrates, laminate substrates lead to reduction in the thickness of passive circuits [35].

Multiple BPFs at 2.4 GHz and 5 GHz have been demonstrated in four-metal-layer low-loss RXP substrates at Georgia Tech [36]. These filters were designed with second-order for compactness. Specific transmission zeros were included to achieve high stop-band rejection. The filters were implemented with spiral inductors and stitched capacitors, and were fabricated with 115 μm thick RXP core and four 20 μm thick build-up layers. An example of demonstrated bandpass filter is presented in Figure 2.7, and it had a size of 3.6 mm × 2.4 mm × 0.2 mm.



(a) (b)

Figure 2.7. A BPF on RXP substrate: (a) X-ray photo, and (b) transmission characteristics.

In contrast to LTCC substrates, where inductor and capacitor (LC) components can be stacked vertically in different layers, layout for lumped elements in laminate substrates is usually planned in lateral dimensions, constrained by fewer build-up layers. Hence, the footprint of IPDs on laminate substrate can be huge unless the density of LC components is significantly improved. The miniaturization of laminate IPDs is contingent on small features and thin films. Since the intrinsic mechanical instability of organic materials hinders fabrication of fine structures, manufacturing of high-density passives with precision thus becomes challenging.

2.1.4 Thinfilm Passives on Silicon and Glass

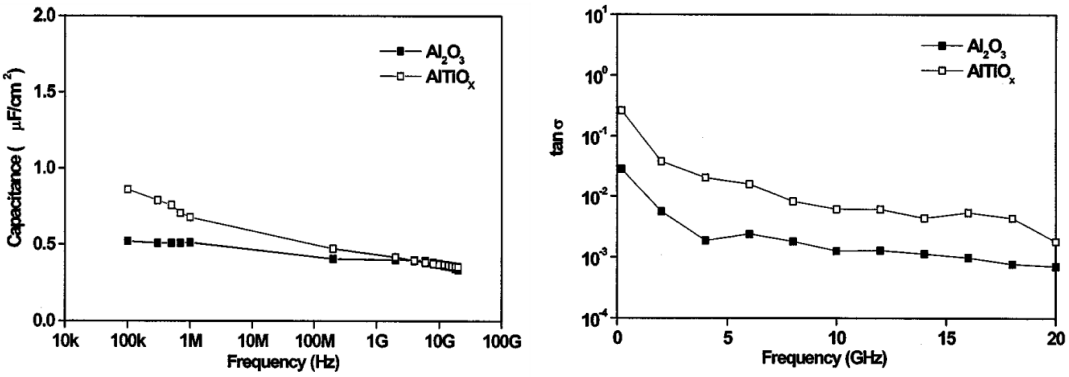
To further miniaturize the size of the lumped passive components and improve the multilayer process precision that is encountered with laminate substrates, thinfilm technologies have been introduced to passives fabrication. They were first implemented on silicon substrates due to the process capability with existing Complementary metal–

oxide–semiconductor (CMOS) technologies. Utilizing thinfilm dielectrics, the size of capacitors can be remarkably reduced.

Thinfilm Capacitors

The density and performance of capacitors are dependent on the thickness and properties of dielectrics between capacitor electrodes. To enhance the capacitance density, thinfilms with 5-10 μm thick organic polymers, or sub-micron thick inorganic dielectrics such as silicon nitride and alumina oxide are used for capacitor design. The later ones are referred to metal-insulator-metal (MIM) capacitors [37, 38], which have been widely used in silicon-based passive circuits.

S.B. Chen investigated the electrical properties of Al_2O_3 and $AlTiO_x$ MIM capacitors from intermediate frequency (IF) (100 KHz) to RF (20 GHz) frequency range [24]. Electrical characteristics such as capacitance density, loss tangent, leakage current and reliability for both capacitors were studied. Two types of MIM capacitors were both fabricated on silicon substrates with their dielectric layers deposited at a thickness of 12 nm. Frequency-dependent capacitance density and loss tangent are plotted in Figure 2.8. To be used in RF filtering networks, MIM capacitors should have both stable capacitance and low loss within their operation bandwidth. It was found that Al_2O_3 offered better capacitance stability than $AlTiO_x$ in RF frequencies as well as lower tangent loss. MIM capacitors with Al_2O_3 dielectric layer are good candidates for RF filters and diplexers design.



(a) (b)

Figure 2.8. Frequency-dependent characteristics of Al2O3 and AlTiOx: (a) capacitance density, and (b) tangent loss.

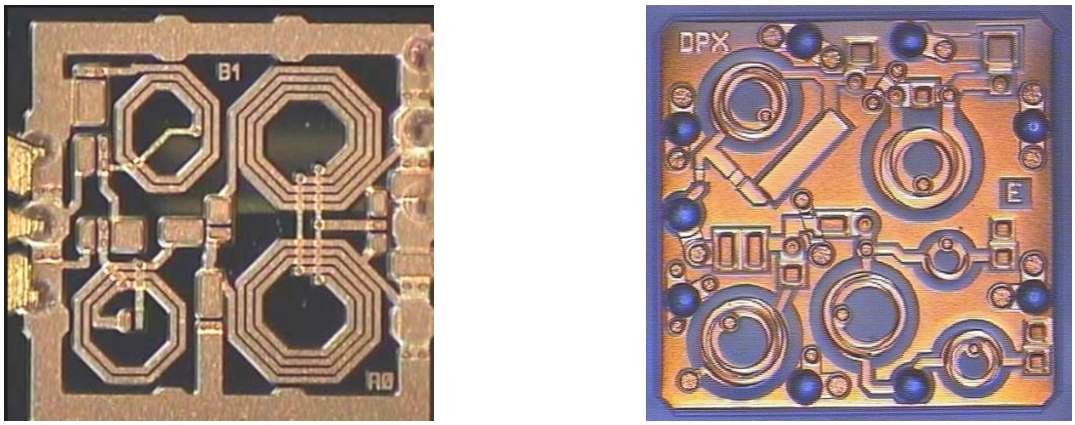
The exponential growth of capacitance density of MIM capacitors makes their physical dimensions insignificant when compared to inductors in a thinfilm IPD design. Hence, the size of a lumped-element IPD can be miniaturized by integrating thinfilm technologies.

Thinfilm IPDs

The availability of high-density thinfilm capacitors enables small-size IPDs implementation on silicon or glass wafers. Conventionally, passive circuits are patterned on single side of a wafer, where BEOL processes are utilized to deposit thinfilms and metalize the conductors. Due to the constraint of build-up layer thickness and manufacturing cost, inductors are typically implemented as 2D planar types, such as multi-turn spiral inductors.

Intel presented a transmit diplexer in 2.3-2.7 GHz low band and 3.3-3.8 GHz high band on silicon and glass substrates [39], as shown in Figure 2.9. By integrating ultra-high density MIM capacitors, the size of diplexers on silicon and glass was as compact as 1.55 mm ×1.55 mm × 0.25 mm and 1.63 mm ×1.61 mm × 0.3 mm respectively. At 2

GHz, MIM capacitors with silicon nitride dielectric on silicon offered a Q factor of 300, while on glass, MIM capacitors with tantalum nitride dielectric had a Q factor of 150. In terms of inductor design, coplanar spiral inductors were implemented on silicon while vertical solenoid inductors were designed on glass. A 2 nH inductor, for instance, has a Q factor of 25 on silicon and 60 on glass. In comparison, a twelve-layer LTCC diplexer was also designed and manufactured with the same electrical specifications and its physical dimensions were 1.63 mm ×1.61 mm × 0.5 mm. The LTCC diplexer was in similar footprint as silicon and glass diplexers, but was much thicker. The electrical performance of the three diplexers were compared against each other. LTCC diplexer had slightly lower insertion loss compared to silicon and glass diplexers due to higher Q factors of its passive components.



(a) (b)

Figure 2.9. Tinfilm diplexers integrated on (a) silicon substrates, and (b) glass substrates.

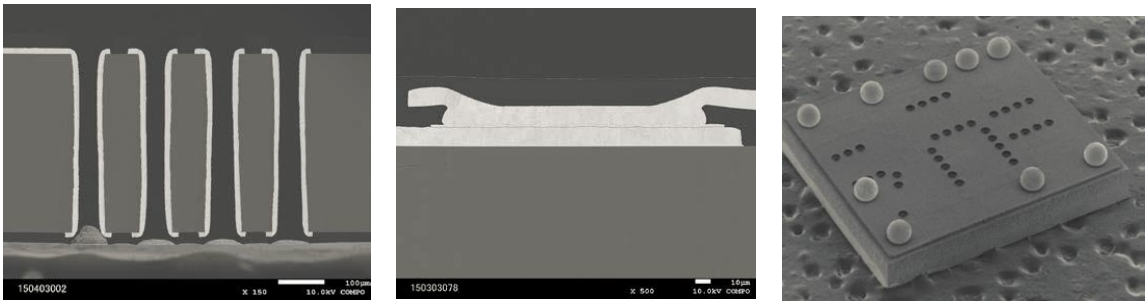
In this study, all the thinfilm passives were integrated only on a single side of the silicon or glass substrates, resulting in an unbalanced mechanical structure. Considering the potential risk of causing stress-induced failures, the number and thickness of build-up layers should be tightly restricted. Consequently, it is extremely difficult to design high-Q

inductors to benchmark those on LTCC substrates, where stringent thickness requirement does not apply.

2.1.5 3D Passives on Glass

As described in Chapter 1, glass-based passive devices have been extensively investigated because of their advantages such as low loss, dimensional stability for precision geometries, and ability to form double-side thinfilm passives connected with low-loss through-vias. Existing thinfilm packaging technologies on silicon and laminates as well as new processes are being investigated on glass.

As an example, Corning demonstrated LC networks for RF applications by leveraging TGVs for high-Q inductors and thinfilm technologies for ultra-high density MIM capacitors [20]. The glass could be fabricated in wafer-scale up to 300 mm diameter or in panel-scale, which could be scaled up to 515mm × 515 mm. Glass with thickness between 0.1 mm to 0.7 mm is durable and TGVs could be made with diameters ranging from 25 μm to 100 μm. Some of the fabrication results are pictured in Figure 2.10. Due to the availability of TGVs, both sides of glass could be metallized and hence 3D passives become feasible on glass.



(a) (b) (c)

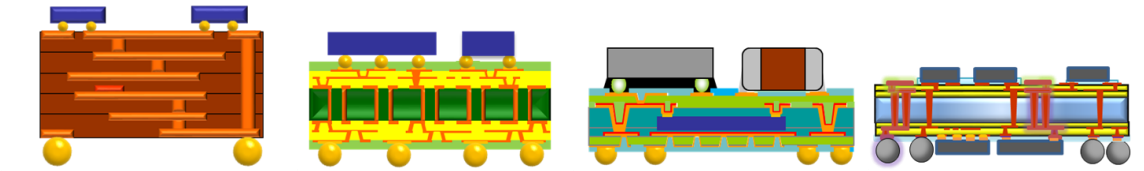
Figure 2.10. 3D RF passives on glass: (a) X-section of a 3D solenoid inductor using TGVs, (b) X-section of a Cu-SiN-Cu MIM capacitor, and (c) a completed LC network.

Prior works have proven that glass is an ideal candidate for high-performance RF passive device applications. However, several aspects such as miniaturization of high-Q passives, high-density inductor and capacitor (LC) integration, IPD performance sensitivity to process-induced variations, and glass substrate manufacturability at large scale are to be studied.

2.2 Advanced RF Modules

In RF FEMs, active components such as switches, PAs, LNAs and passive components such as antennas, diplexers, duplexers, filters and impedance matching networks are integrated to provide functionalities. Chip-level integration technology based on system-on-chip (SOC) concept has been developed for RF modules [40]. It offers accuracy in process and compactness in module size. However, it is limited by its inferior cost and performance. Hence, SOP concept was proposed as a system-level integration solution and has been widely pursued [41]. Heterogeneous system components coexist in SOP RF modules, where the system performance is optimized through advances in actives and passives, low-loss interconnections and innovations in integration techniques.

Module integration can be subdivided into LTCC modules, MCMs on laminates, embedded modules in laminates and 3D modules on glass, which are summarized in Figure 2.11.



LTCC	MCM on Laminates	Embedded Module in Laminates	3D Module on Glass
High performance	Moderate performance	High performance	High performance
Thick	Moderate	Thin	Thin
Small footprint	Moderate footprint	Small footprint	Small footprint
Moderate component density	Low component density	Moderate component density	High component density
Moderate cost	Low cost	Moderate cost	Limited manufacturability

Figure 2.11. Summary of RF module technologies.

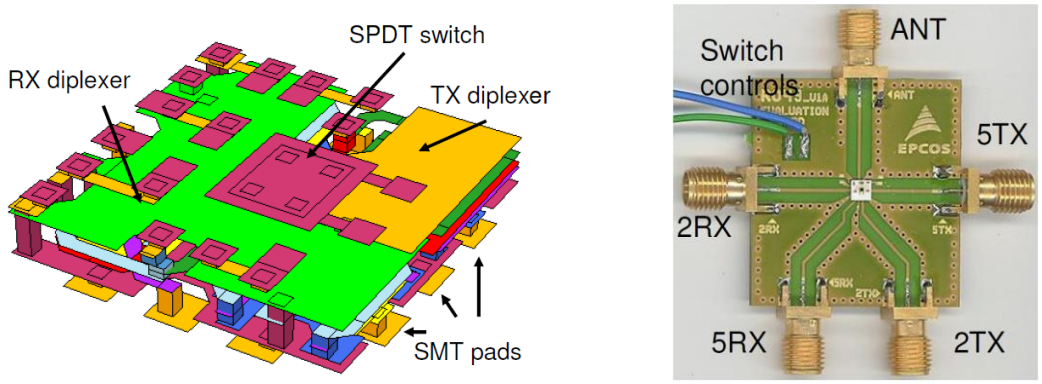
In conventional MCMs, multiple individually-packaged discrete active and passive components are generally interconnected through substrates. Laminate substrates are widely used for MCMs at low cost, and glass substrates are also being explored as potential candidates for the future. Embedding can be implemented with passives that are fabricated along with the laminate, LTCC or glass substrates, or with actives which are embedded into laminate substrates.

2.2.1 RF Modules on LTCC Substrates

Conventional RF modules are primarily built on LTCC substrates for their low loss, low moisture absorption, high mechanical stability and capability to support three-dimensional circuits with high performance. Discrete passives or IPDs such as inductors, filters, baluns, matching circuits and multiplexers can be implemented on multi-layer ceramic substrates and the actives are connected to the substrates through wire bonding, flip-chip assembly and surface mount technology.

EPCOS has presented an ultra-low profile small-size LTCC FEM for WLAN applications [33]. High-rejection Tx and Rx diplexers were embedded into the LTCC

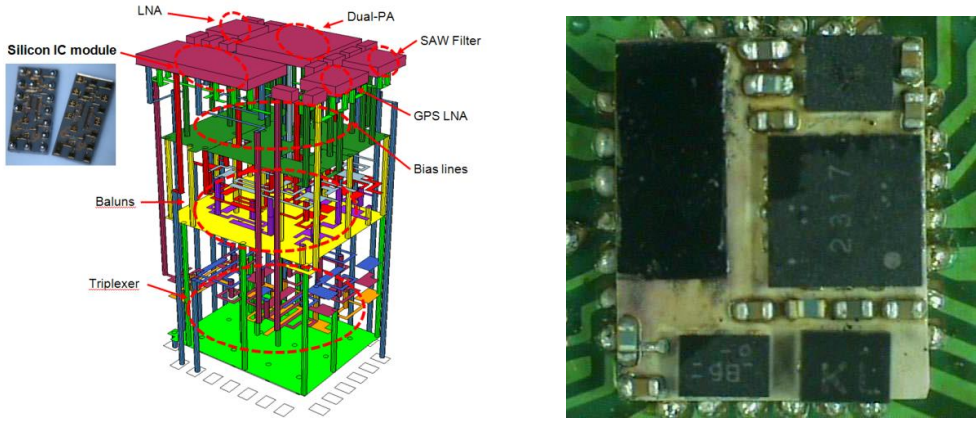
substrates with eleven 30 μm thick dielectric layers. A single-pole-double-through (SPDT) switch was assembled onto the top of the completed substrate through wire bonding. Low passband insertion loss was achieved in both Tx and Rx paths. The overall size of such FEM was 3 mm × 3 mm × 0.95 mm. Both substrate layout and demonstrated FEM sample on testing board are shown in Figure 2.12.



(a) (b)

Figure 2.12. A WLAN FEM on LTCC substrates: (a) substrate layout, and (b) module on an evaluation board.

Packaging Research Center of Korea Electronics Technology Institute has demonstrated a compact 5 mm × 6 mm triple-band triple-mode RF FEM on 0.85 mm thick LTCC substrates for GPS/BT/WiFi applications [42]. Variety of passives, such as baluns, triplexers and bias lines were embedded into multiple ceramic layers. Discrete components, such as actives including LNAs, a PA and a silicon IC module, as well as passives including inductors, capacitors and a SAW filter were either flip-chip assembled or surface mounted onto the LTCC substrates. The module showed low insertion loss and high gain at Rx paths, and good linearity characteristics in Tx paths. The designed and demonstrated FEM is shown in Figure 2.13.



(a) (b)

Figure 2.13. A GPS/BT/WiFi triple-mode FEM on LTCC substrates: (a) substrate layout, and (b) module top view.

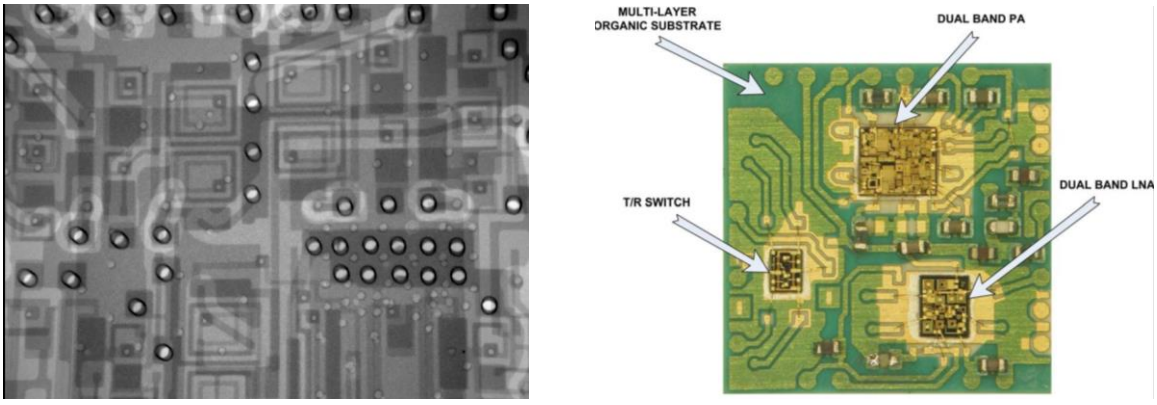
Making use of the low-loss nature of ceramic and multi-layer substrate architecture, high-Q passives could be designed and embedded into a LTCC substrate with effective utilization of space. The discrete components that are placed on the top of the substrate can access the embedded passives with relatively shorter paths so that interconnection loss is suppressed. However, this space-saving module integration approach is at the cost of enlarged module thickness and increased manufacturing cost, making it difficult to be employed in miniaturized mobile devices.

2.2.2 RF Modules on Laminate Substrates

MCMs on laminate substrates were developed and gradually took the place of LTCC modules for their reduced thickness and lower manufacturing cost. In RF MCMs, discrete passives and actives are assembled side-by-side onto the laminate substrates. However, the performance of traditional MCMs was limited by the high moisture absorption and high dielectric loss associated with laminates. These limitations were addressed by using liquid crystal polymer (LCP) laminates for module integration. In addition, the overall

module size could be further reduced by embedding individual passive elements or IPDs into low loss organic substrates.

S. Dalmia from Georgia Tech has demonstrated a dual-band WLAN multiple-input-multiple-output (MIMO) FEM on a six-metal-layer LCP-based substrate [13], as shown in Figure 2.14. Filters, baluns and diplexers were embedded into thick low-loss LCP laminates and integrated into the substrates as IPDs. The FEM also incorporated actives such as PAs, LNAs and a double-pole-double-through (DPDT) switch, and other discrete passives for decoupling and biasing, on top of the substrates. The overall lateral size of demonstrated FEM was 64 mm^2.



(a) (b)

Figure 2.14. WLAN FEM on LCP-based substrates: (a) passives embedding in substrates, and (b) top-view of the assembled FEM.

Compared to LTCC substrates, since fewer layers are employed in the laminate substrates, the module thickness could be reduced. At the same time, the lateral size of the module becomes a problem, which could not be addressed by thickfilms as they impede the miniaturization of embedded passives. Another challenge confronted by laminate substrates is the fabrication precision, because of the mechanical instability and other intrinsic attributes of organic materials. Manufacturing defects such as layer-to-

layer mis-registration and substrate warpage, and limitations in small feature size circuitry patterning are the obstacles in the path of miniaturization of embedded IPDs and further module thickness reduction.

2.2.3 Embedded RF Modules in Laminate Substrates

In contrast to MCMs, embedded modules shorten the interconnection lengths and minimize the parasitics. Therefore, system-level insertion loss is reduced, signal integrity is improved, and the package loop inductance is lowered for better power supply. Integration of appropriate ground planes, shields and conformal metal overmolds can substantially suppress the EMI [43, 44]. Heat-spreaders can be locally integrated for efficient IC cooling. The package size is significantly reduced since the space-consuming discrete components are embedded into the substrate build-up layers. In addition, embedding approach allows heterogeneous integration of system building blocks with different technologies.

Chip-first Embedding

In chip-first embedding, the discrete components are first thinned down and modeled into laminate substrates. This ends up with an artificial substrate where build-up processing can be directly employed to interconnect the embedded components. The interconnection lengths are shortened due to the absence of chip bumps, hence system performance is enhanced and assembly cost is saved.

TDK-EPCOS has developed the most leading-edge SESUB module technologies in the market, as shown in Figure 2.15, enabling a multifunctional and miniaturized solution for RF applications. Multiple semiconductor chips are first embedded side-by-side and fully molded in laminates, with the backside surface accessible for cooling. It is followed

by the growth of redistribution layer (RDL) layers directly on ICs. The semiconductor-embedded substrates could be as thin as 300 μm or less, on top of which discrete components could be assembled [15]. Minimized parasitic effects from short vertical interconnections further improve the system performance.

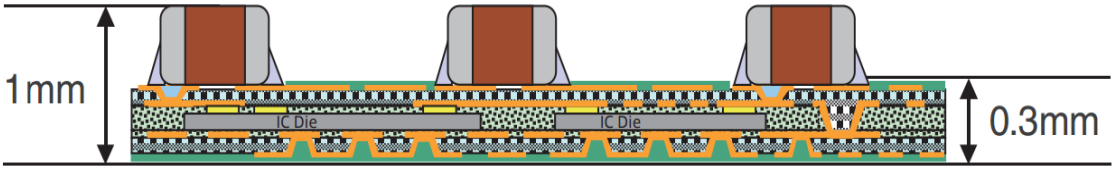


Figure 2.15. Cross-section view of SESUB RF modules.

Chip-last Embedding

The chip-last approach for RF modules was proposed to address the concerns of die-yield loss and technical challenges of heterogeneous components embedding with dissimilar thickness that are faced by chip-first embedding or fan-out packaging technologies. In chip-last embedding, cavities for IC accommodation are first formed inside laminate substrates, and IC chips are flip-chip assembled into yielded cavity-formed substrates. Passive components can be either embedded into the substrates as IPDs or can be mounted onto the surface of finished substrates.

Srikrishna Sitaraman et al., from Georgia Tech demonstrated a RF WLAN receiver module with LNA and a BPF in thin laminate substrates [16]. The BPF was designed and embedded into the build-up layers of a laminate substrate, while the LNA die was lastly embedded into the cavity formed during substrate fabrication. The interconnection between the LNA and the BPF was established laterally through RDLs. The overall thickness of the module was only 160 μm without BGAs. A cross section of such chip-last embedded module is shown in Figure 2.16.

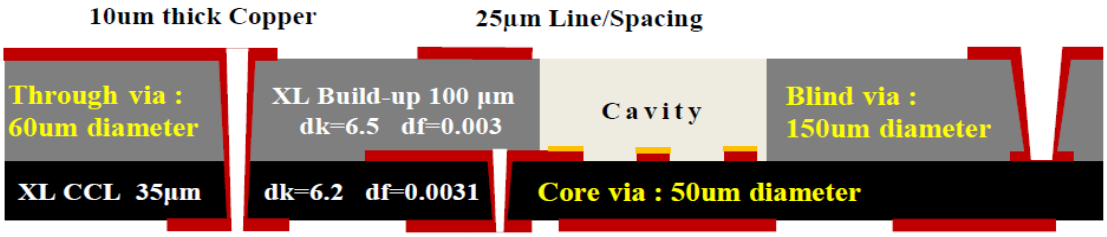


Figure 2.16. Cross-section view of chip-last embedded RF modules.

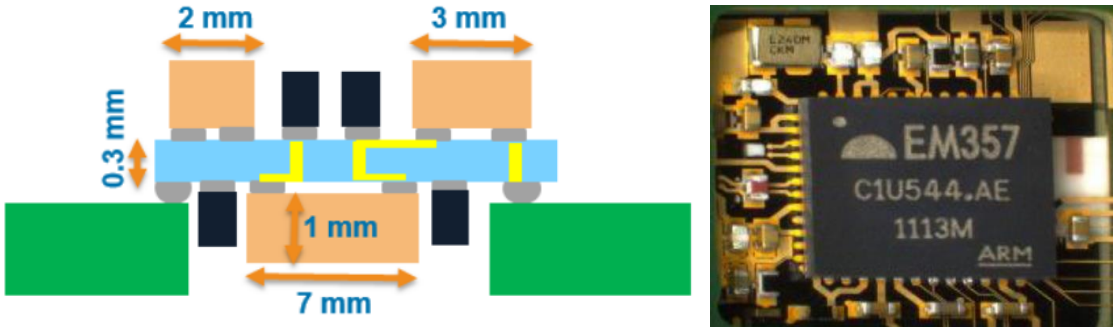
In contrast to vertically-interconnected discrete passives and embedded actives in a chip-first configuration, the chip-last approach embeds both actives and passives side-by-side into laminate substrates, yielding the thinnest RF module. However, the footprint of the chip-last package increases and degrades the performance because of longer interconnection lengths, especially when more functionalities are to be integrated into one single module. Both embedded module technologies share one common bottleneck. The minimum thickness of substrates is constrained by the embedded ICs, which may not always be as thin as required.

2.2.4 3D RF Modules on Glass Substrates

Recently, extensive efforts have been put into glass packaging technologies for their superiorities in many aspects as described in Chapter 1. The compatibility of glass to existing packaging infrastructures gives it the flexibility of substrate thickness control, design topology selection and new packaging architecture exploration. A 3D RF module concept was proposed to minimize the size of package footprint by integrating components on both side of the glass substrates.

TE Connectivity recently demonstrated a 3D glass interposer for RF modules. Glass with 300 µm thickness was used as the substrate material with TGVs interconnecting top and bottom metal layers [45]. Discrete active ICs and passives were assembled onto both

sides of the glass substrate, yielding in a 3D package as shown in Figure 2.17. The glass package was assembled onto a PCB and tested with good electrical performance reported. The demonstrated RF module on glass, when compared to its current layout as a laminate MCM, showed significant size reduction from 28 mm × 19 mm to 15 mm × 13 mm, without compromise in thickness.



(a) (b)

Figure 2.17. A RF module on 3D glass interposer: (a) cross section of the proposed package, and (b) top view of assembled RF module on glass.

In this research, glass showed its robustness during mutiple processes, enabling double-side component assembly as well as direct assembly of glass to PCB. The interconnection loss between system components was also mitigated due to the shortened interconnection lengths through TGVs. Nevertheless, in this proposed 3D package, glass was primarily used for interconnections, power delivery and grounding, without offering additional functionalities. In addition, the back-side assembled active component was too thick, which challenges the solder balling for board-level assembly. Better glass packaging architectures and integration technologies that can leverage the benefits of glass to the greatest extent should be explored.

2.3 Summary of Prior Arts

RF passives and embedding technologies have made profound progress in terms of miniaturization and performance enhancement at both component and system level. However, several challenges remain. First, 2D integration approach fails to utilize the short vertical interconnections from the package, impeding further miniaturization of RF devices and modules. Existing 3D solutions, on the other hand, are restricted to only limited functionalities. Second, sensitivity of RF components to process-induced variations were not systematically studied. Such variations can degrade the system performance if not cautiously considered. To meet the stringent performance requirements for RF systems and to continuously miniaturize the RF module size, innovative passive design and module integration technologies should be explored along with the co-development of advanced materials and processes.

CHAPTER 3
DESIGN AND DEMONSTRATION OF 3D IPD LTE DIPLEXERS

This chapter presents the design, process development, fabrication and characterization of ultra-thin 3D IPD diplexers. Double-side integration of high-performance and high-density inductors and capacitors are used to form filter networks on thin glass substrates, which are interconnected with through-vias. Innovative process enhancements are demonstrated to achieve high performance, with 3X reduction in thickness compared to state-of-the-art inductors.

A diplexer is a three-port passive device which implements frequency-domain multiplexing, and has been widely used in RF filtering networks inside FEMs. It often has one port connected to an antenna, while the other two are connected to transmitters or receivers at different operation bands. Incoming signals received by the antenna are split into two frequency bands through one LBF and HBF. When signals are being transmitted, both high-band and low-band signals can output and coexist on the antenna port without interfering with each other. Low-band filtering is usually executed by a LPF or a BPF, while a BPF or HPF might be made use of high-band filtering. The LBF and HBF are separately designed first and then combined into a diplexer with one common port connected to the antenna. Since impedance matching is typically required during the integration process, it can also be a part of the diplexer. The overall diplexer block diagram is shown in Figure 3.1.

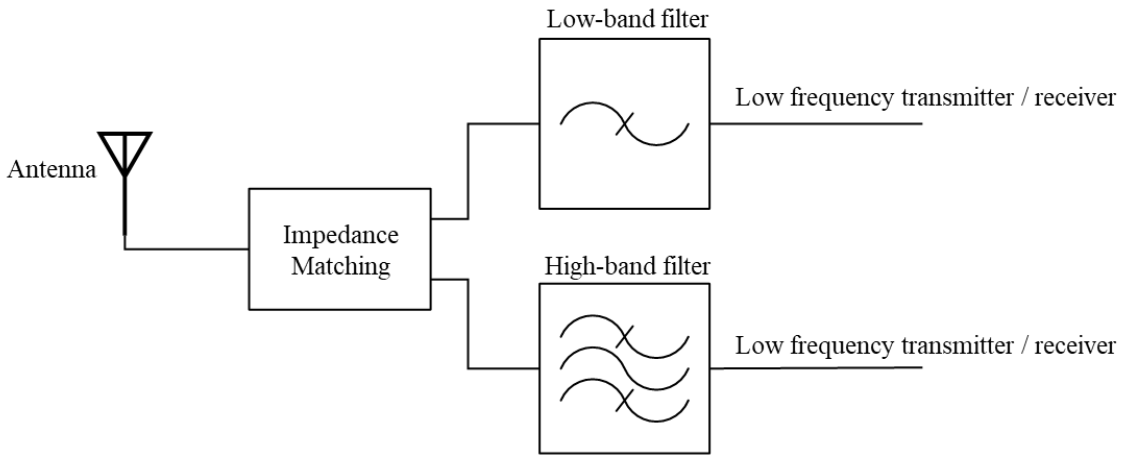


Figure 3.1. Block diagram of a typical diplexer.

In 4G-LTE networks, the wavelengths of signals are in the range of a few centimeters to tens of centimeters. Therefore, the filtering circuits are implemented with lumped LC components for reducing the foot-prints. High-density integration of these lumped passives is being pursued by embedding them into substrates, forming IPDs. These IPDs are conventionally individually packaged into SMT devices that are assembled onto package substrates, and are lately embedded into package substrates when component- and system- level co-design are required.

High performance of an IPD diplexer is defined by its low passband insertion loss, high out-of-band signal rejection and high isolation between LBF to HBF. These attributes are achievable by optimized filter and diplexer design topologies, employment of low loss components, optimized layout on substrates, and high-precision manufacturing. Therefore, innovations in both electrical design and substrate fabrication need to be studied.

The objective is to design and demonstrate high-performance wideband LTE diplexers in an ultra-miniaturized package size, using the proposed innovative 3D IPD approach on

most advanced glass substrates. The diplexers are projected to have three times reduction in thickness with comparable or better electrical performance than LTCC diplexers. Two types of diplexers are designed on 100 -200 μm thick ultra-thin glass, using different implementation methods.

The first half of this chapter presents the design and demonstration of miniaturized organic thinfilm-based 3D IPD diplexers on 100 μm thick glass. Electrical design and modeling of miniaturized filters and diplexer were elaborated in detail. Process development of 3D IPDs with double-side integrated LC networks is then summarized. This is followed by diplexer performance characterization and sensitivity analysis to process-induced variations. Finally, a low-cost and manufacturable process innovation to control process variation is proposed, developed and validated.

The second part presents the design and integration of high-Q inductors and ultra-high-density thinfilm MIM capacitors on glass substrates. Significant performance improvement is achieved in re-designed high-performance thinfilm 3D IPD diplexers on 200 μm thick glass.

3.1 Ultra-miniaturized 3D IPD Diplexers with Organic Thinfilms on Glass

Diplexers are designed to support two bands that allow signals to pass at low insertion loss within low-frequency band at 700 MHz - 960 MHz and high-frequency band at 1710 MHz - 2690 MHz. More than 15 dB out-of-band signal rejection and more than 20 dB high-band to low-band isolation are desirable. The target size of such diplexer is 2.5 mm × 2.5 mm × 0.3 mm. Large-scale manufacturing needs such as small form-factors, compatible process with existing laminate substrate infrastructures and <5% tight process tolerance should be met.

3.1.1 Design of Ultra-miniaturized 3D IPD Diplexers

Circuit-level Design

Circuit-level simulation is the very first step for passive circuit design, through which design topology, filter orders and values of LC component values are decided. Individual LBF and HBF are to be designed first, implemented by a LPF and a BPF respectively, with minimum number of lumped components. This is followed by their integration into a diplexer with additional impedance matching circuits.

Design Topology Selection

Filters that are designed by elliptic functions are preferable in this application because they offer extremely sharp roll-off characteristics at a low count of LC elements. When compared to other conventional filter design topologies including Butterworth, Chebyshev, and Bessel, elliptic-function filter offers the best selectivity, as shown in Figure 3.2. This is because finite-frequency transmission zeros are introduced into the transfer function of an elliptic-function filter. In Equation (3.1), multiple transmission zeros can be specifically designed at Ω_i, allowing zero signal transmission right outside of the filter's passband. However, the high selectivity is at the expense of add-on ripples in both passband and stopband of a filter, which constrains the best achievable electrical performance, such as minimum passband insertion loss. Therefore, trade-offs between a filter's selectivity and insertion loss must be prudently made.

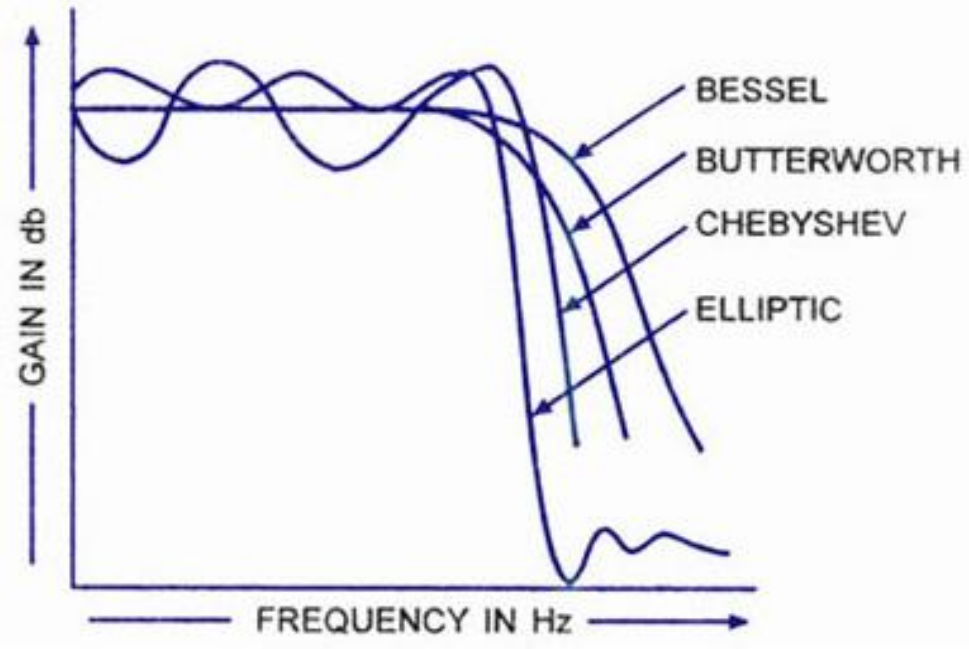
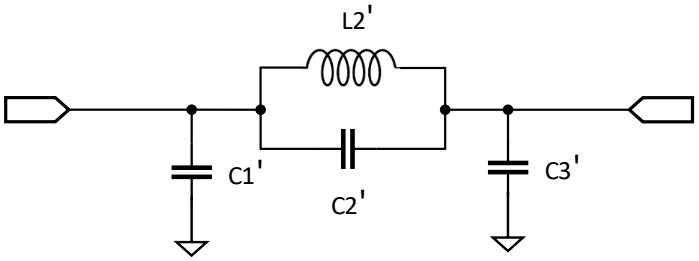


Figure 3.2.Comparison of four commonly used filter design topologies [46].

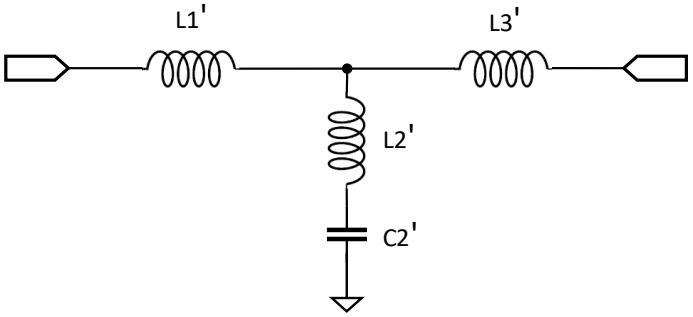
$$F_n(\Omega) = \begin{cases} M \dfrac{\prod_{i=1}^{\frac{n}{2}} (\Omega_i^2 - \Omega^2)}{\prod_{i=1}^{\frac{n}{2}} \left(\frac{\Omega_s^2}{\Omega_i^2 - \Omega^2}\right)} & for\ n\ even \\ N \dfrac{\Omega \prod_{i=1}^{\frac{n-1}{2}} (\Omega_i^2 - \Omega^2)}{\prod_{i=1}^{\frac{n}{2}} \left(\frac{\Omega_s^2}{\Omega_i^2 - \Omega^2}\right)} & for\ n\ (\geq 3) odd \end{cases} \tag{3.1}$$

LPF Design for LBF

The low-band LPF design starts with the prototype LPF selection under some critical design constraints. A 3rd order LPF was decided as a compromise between high selectivity and low LC components count. There are two prototype architectures associated with this and they are shown in Figure 3.3 with π-section on the top and T-section on the bottom [47].



(a)



(b)

Figure 3.3. Prototype 3rd order elliptic-function filters with (a) π-section model and (b) T-section model.

The π-section LPF prototype was selected because it has only one inductor. The physical size of inductors is usually bulky and difficult to be miniaturized for low-loss applications compared to a capacitor. Selected element values are captured in Table 3.1, where normalized equal-ripple cutoff frequency Ω_c is 1 and normalized impedance of both input and output is 1. Symbols n, L_{Ar}, L_{As}, Ω_s, Ω_z are the order of filter, passband ripple, minimum stopband insertion loss, normalized equal-ripple stopband starting frequency, and normalized transmission zero frequency.

Table 3.1. Element values of elliptic-function LPF prototype with $Z_i = Z_o=1$, $\Omega_c =1$ [47]

n	L_{Ar} (dB)	L_{As} (dB)	Ω_s	Ω_z	$C_1' = C_3'$	C_2'	L_2'
3	0.18	15.22	1.4142	1.5710	0.8823	0.5576	0.7267

A transmission zero was set at Ω_z, right outside the filter's passband. Minimum insertion loss of 15.22 dB in stopband was maintained by choosing 0.18 dB passband ripples. The LC values in LPF were then calculated by performing frequency and impedance scaling on obtained prototype values, following equations (3.2).

$$L_k = \frac{L'_k Z_0}{2\pi f_c}$$
$$C_k = \frac{L'_k}{2\pi f_c Z_0} \tag{3.2}$$

Port impedance Z_0 was matched to 50 Ω and 0.18 dB ripple cutoff frequency Ω_c was scaled to 1 GHz. The resultant LPF schematic diagram is shown in Figure 3.4.

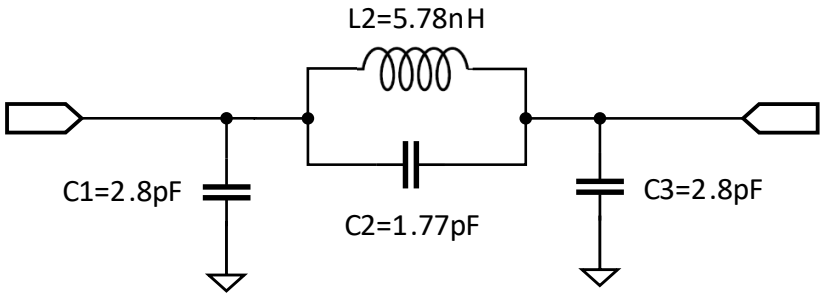


Figure 3.4. Circuit model of designed 3rd order elliptic-function LPF.

The circuit model was built in Keysight ADS with lossless lumped LC elements. A frequency sweep was run from 100 MHz to 8 GHz and the simulated filter's transmission characteristics are shown in Figure 3.5.

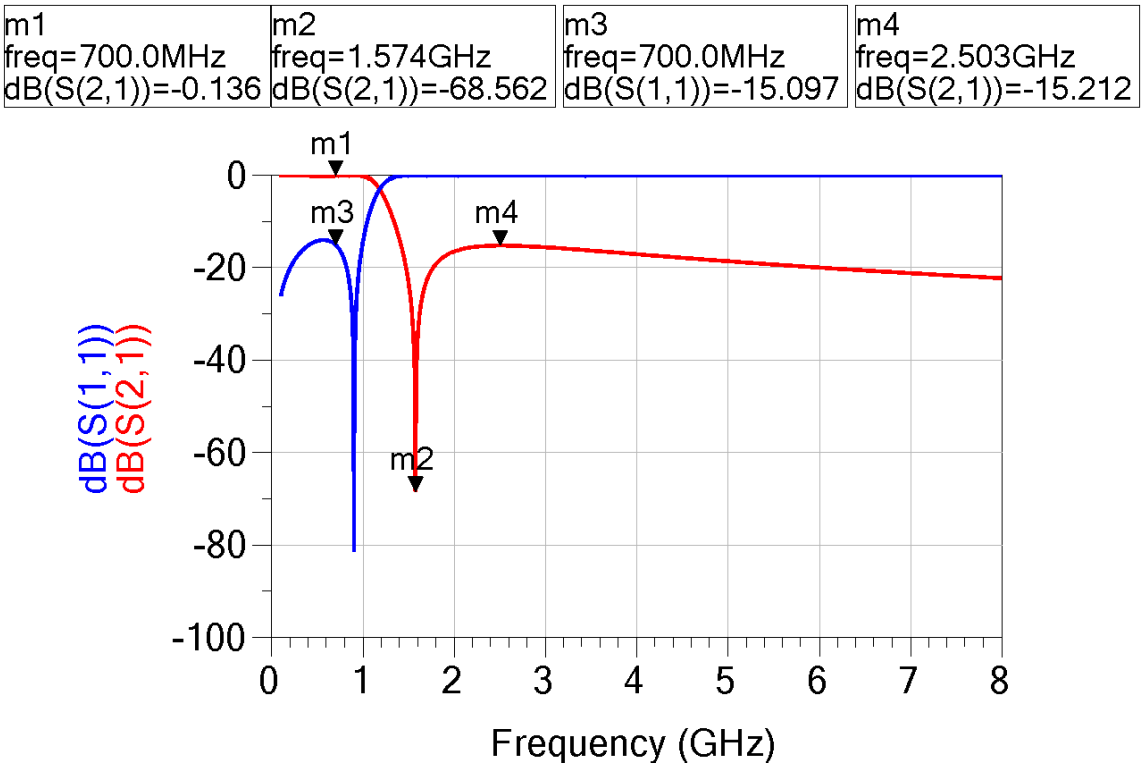


Figure 3.5. Circuit-level simulation results of LPF transmission characteristics.

As has been marked in the graph, the designed LPF had maximum passband insertion loss of 0.14 dB at 700 MHz, one transmission zero at 1.57 GHz, minimum stopband insertion loss of 15 dB, and minimum return loss of 15.1 dB at 700 MHz.

BPF Design for HBF

The high-band BPF design starts from the prototype LPF design, which then goes through a low-pass to band-pass transformation. Design parameters of the selected 3rd order T-section elliptic-function LPF prototype are summarized in Table 3.2.

Table 3.2. Element values of elliptic-function LPF prototype for BPF design with $Z_i = Z_o=1$, $\Omega_c = 1$ [47]

n	L_{Ar} (dB)	L_{As} (dB)	Ω_s	Ω_z	$L_1' = L_3'$	L_2'	C_2'
3	0.18	20.74	1.1482	1.8692	0.9802	0.3320	0.8623

To enable signals with 1710 MHz – 2690 MHz frequencies to be transmitted at low loss, the center frequency f_0 of the passband was defined as 2.2 GHz, and a 3dB bandwidth of 60% was assigned from 1.54 GHz to 2.86 GHz. With these constraints, a low-pass to band-pass transformation was performed following Equations (3.3). An inductor was transformed into an inductor and a capacitor in series, while a capacitor was replaced by an inductor and a capacitor in parallel.

$$\Delta = \frac{f_2 - f_1}{f_0}$$

$$L_j = \frac{L_j' Z_0}{2\pi f_o \Delta}, C_k = \frac{\Delta}{2\pi f_o L_j' Z_0} \quad for\ L\ to\ series\ LC\ transformation \tag{3.3}$$

$$L_k = \frac{\Delta Z_0}{2\pi f_o C_k'}, C_k = \frac{C_k'}{2\pi f_o \Delta Z_0} \quad for\ C\ to\ parallel\ LC\ tranformation$$

Resultant schematic diagram of the BPF after transformation is shown in Figure 3.6. The designed BPF was composed of four inductors and four capacitors.

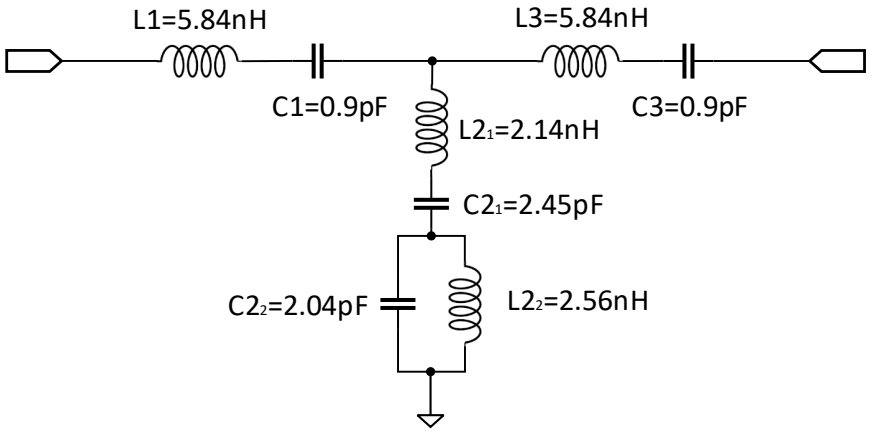


Figure 3.6. Circuit model of designed 3rd order elliptic-function BPF.

The BPF circuit was modelled in ADS and simulated from 100 MHz to 8 GHz. Frequency responses including insertion loss S_{21} and return loss S_{11} are plotted in Figure 3.7, with critical characteristics marked and recorded.

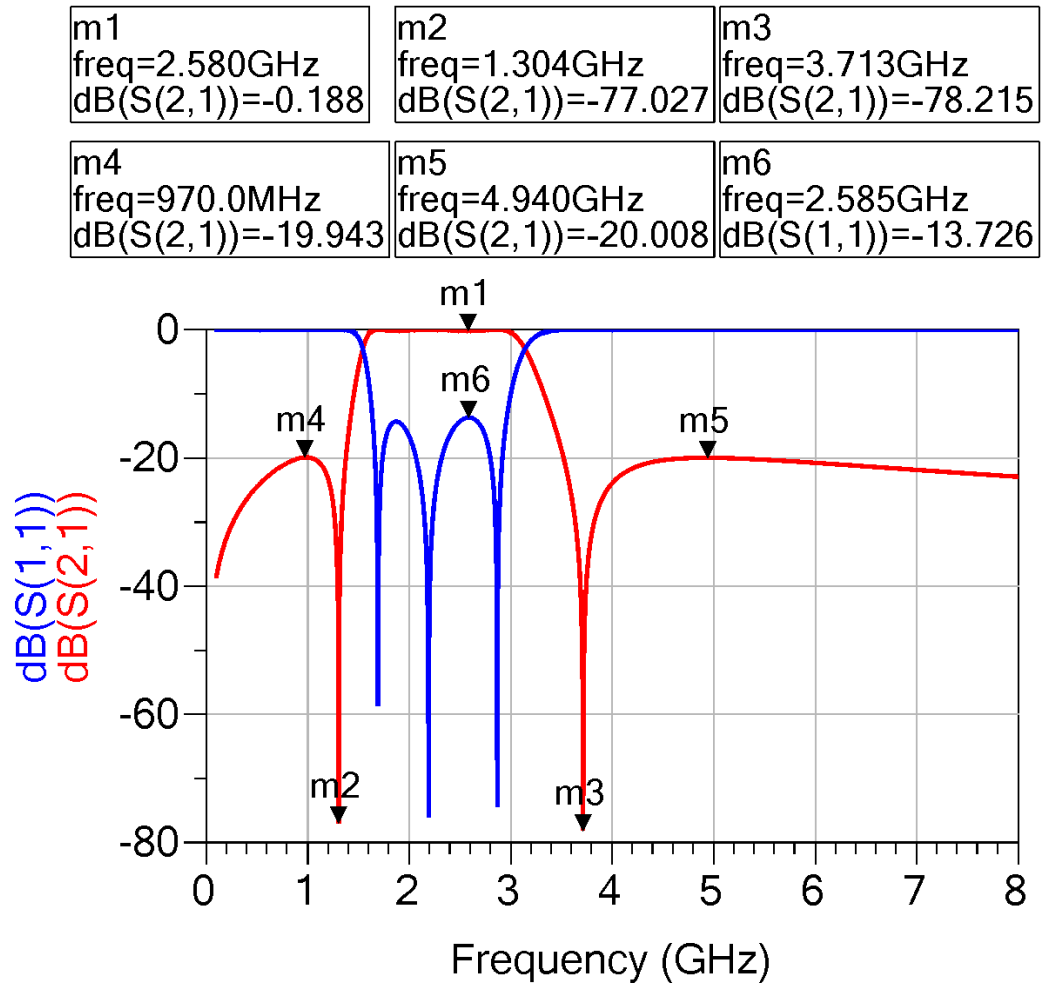


Figure 3.7. Circuit-level simulation results of BPF transmission characteristics.

Two transmission zeros were located at 1.30 GHz and 3.71 GHz respectively, and a good impedance match was achieved around the center frequency of 2.2 GHz. The designed BPF had a minimum passband insertion loss of 0.19 dB, minimum passband return loss of 13.7 dB, and a minimum out-of-band signal rejection of 20 dB.

Diplexer Design

In LBF and HBF designs, impedance matching was independently addressed only in the passband, without considering the impact after they are coupled into a diplexer. Hence, impedance matching elements should be added to the designed LBF and HBF

circuits to mitigate undesired impedance mismatch. The addition of impedance matching elements should engineer the admittance Y_L and Y_H at both filters' input so that they are complex conjugates at the corresponding passbands. The block diagram of a typical diplexer design is shown in Figure 3.8.

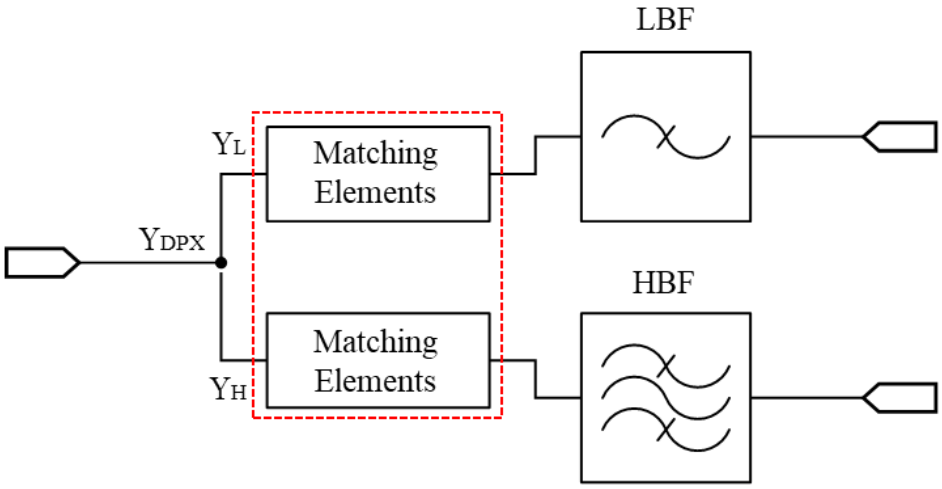
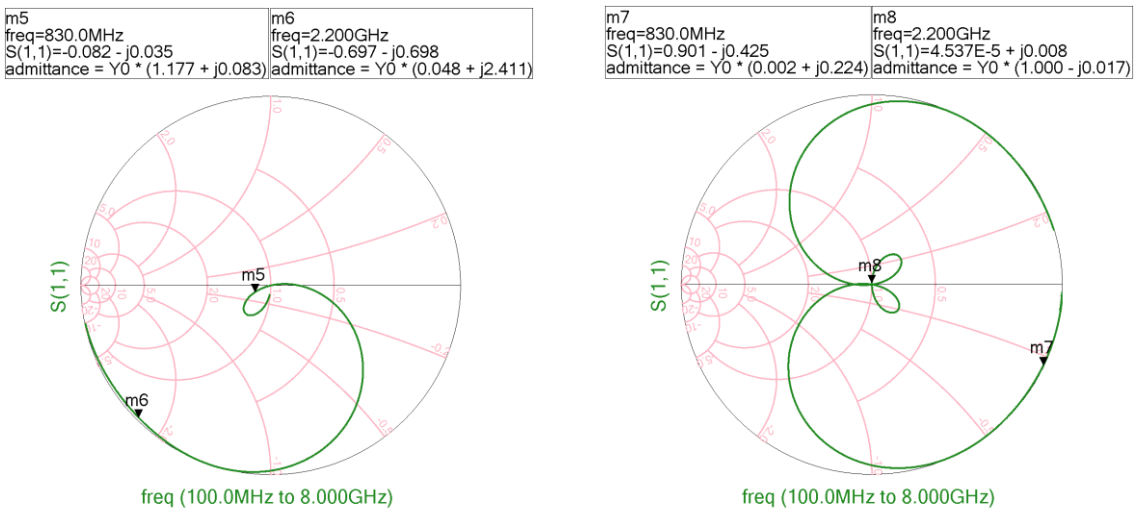


Figure 3.8. Block diagram of diplexer design with impedance matching networks.

Since the addition of impedance matching elements can potentially enlarge the size of the diplexer, their design should be simplified. In Figure 3.9, the Smith Chart shows the terminal admittances of LBF and HBF without impedance matching elements. At 830 MHz in low band, the normalized admittance Y_H = 0.002 + j0.224, both real and imaginary parts of which were relatively small. However, at 2.2 GHz in high band operation, the imaginary part of Y_L = 0.048 + j2.411 could seriously deteriorate the impedance matching. This analysis suggested that the admittance of the LBF should be modified especially in high-band frequencies by introducing additional impedance matching elements. Other optimization measures are also required and could be accomplished by direct modifications of current LC parameters.



(a) (b)

Figure 3.9. Admittance plot on Smith Charts of (a) Y_L for LBF and (b) Y_H for HBF.

Since the imaginary part of Y_L at 2.2 GHz is positive, it could be mitigated by adding inductive elements. For this implementation, a shunt capacitor C_m (0.7 pF) and a series inductor L_m (9 nH) were added in front of the LBF to form its impedance matching network. The HBF's input port is directly connected to the common port, as shown in Figure 3.10.

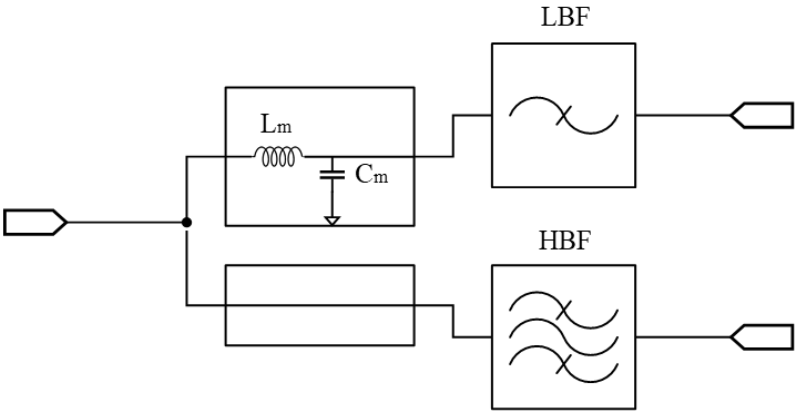


Figure 3.10. The block diagram of impedance matching network implementation in the designed diplexer.

The accomplished circuit model is demonstrated in Figure 3.11. Since C_m and C1 in the LBF circuit were in parallel, they are combined into C_{L1}.

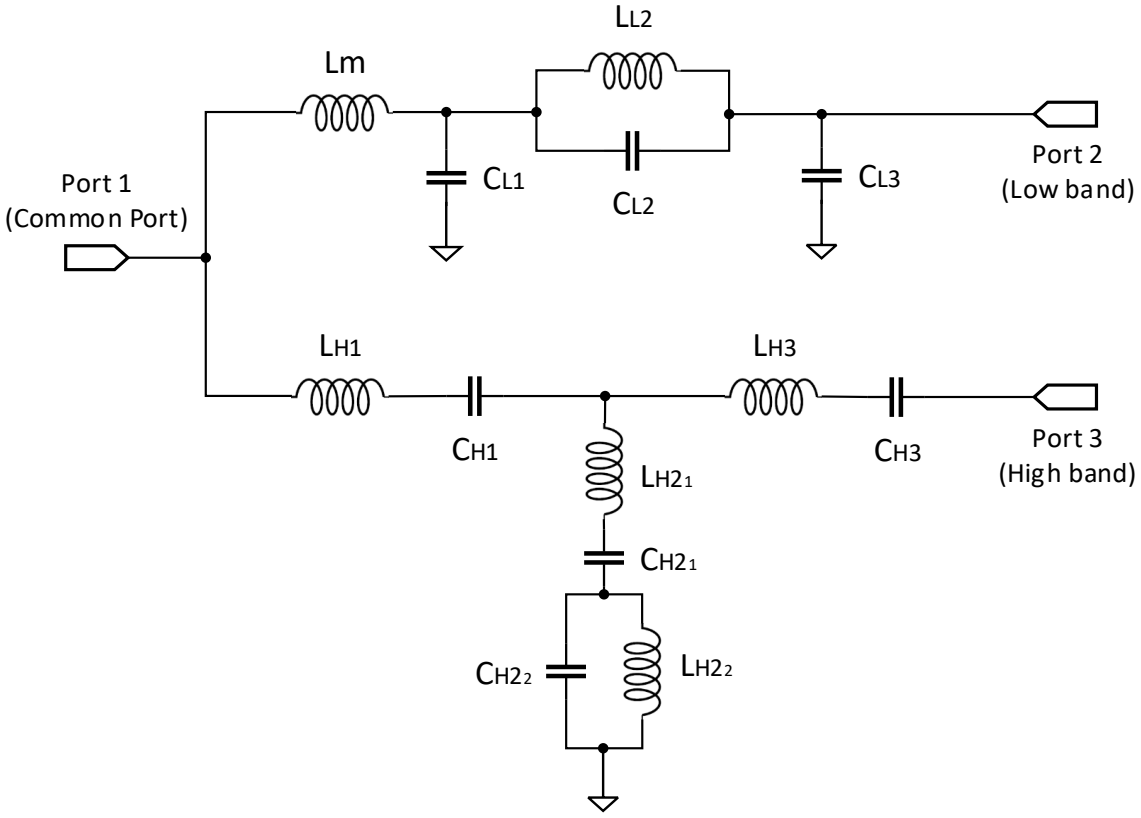


Figure 3.11. Circuit model of designed diplexer.

Design optimization was carried out in ADS and all the component values are documented in Table 3.3.

Table 3.3. Element values of designed diplexer

	Capacitance (pF)		Inductance (nH)	
Low Band	CL1	3.50	Lm	10.0
	CL2	1.77	LL2	5.78
	CL3	0.30		
High Band	CH1	0.90	LH1	5.84
	$CH2_1$	2.45	$LH2_1$	2.14
	$CH2_2$	2.04	$LH2_2$	2.56
	CH3	0.90	LH3	5.84

Circuit-level simulation was conducted and the diplexer's frequency response is plotted in Figure 3.12 below.

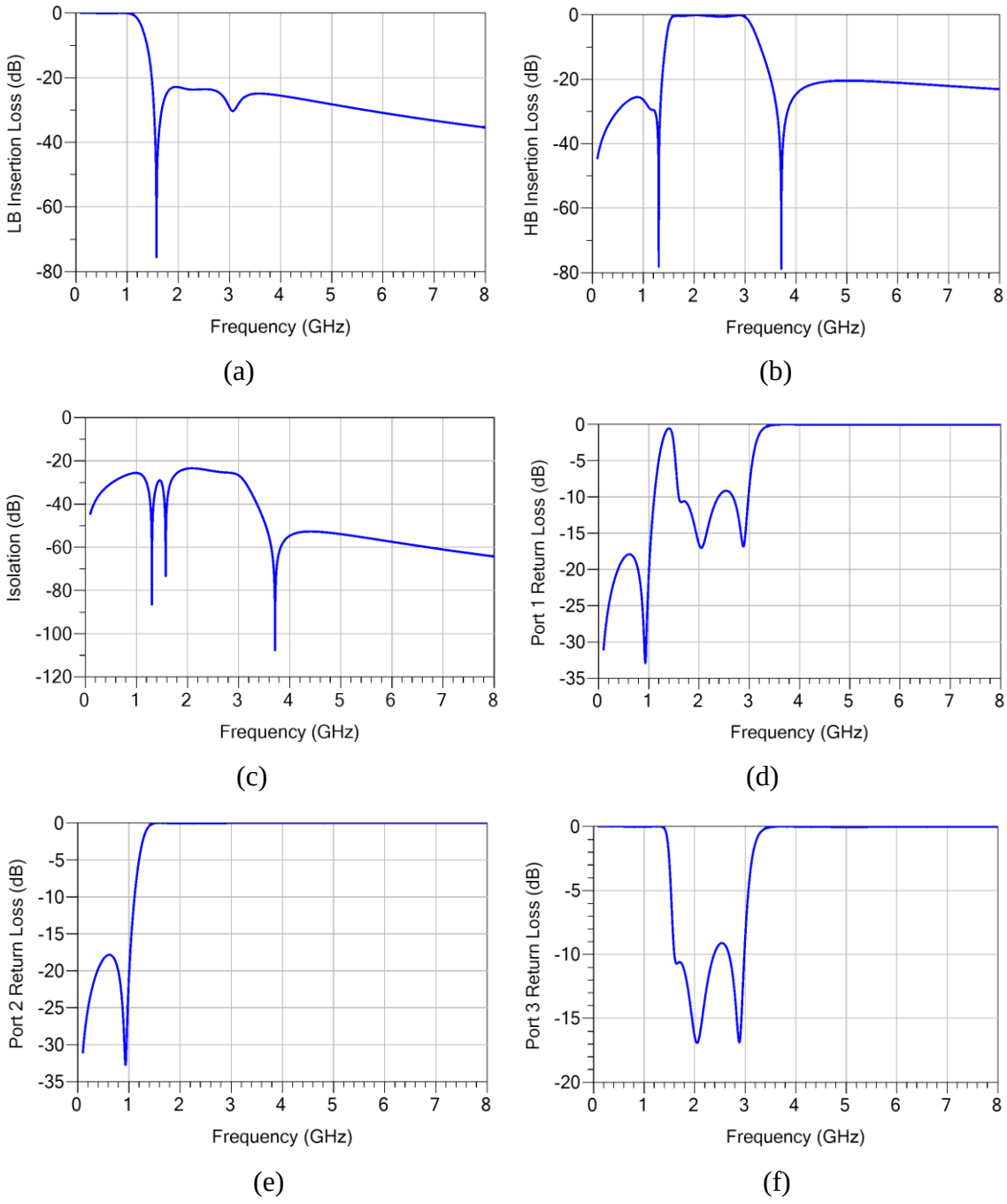


Figure 3.12. Circuit-level simulation results of diplexer transmission characteristics: (a) low-band IL, (b) high-band IL, (c) isolation, (d) Port 1 RL, (e) Port 2 RL, and (f) Port 3 RL.

The maximum passband insertion loss is 0.07 dB and 0.58 dB respectively for the low- and high- frequency band. More than 20 dB out-of-band signal rejection in both operation bands, and higher than 20 dB band-to-band isolation have been obtained.

EM Modeling

To conduct EM simulations, a physical layout of designed 3D IPDs should be modeled based on the substrate stack-up. The proposed substrate design rules and substrate cross sectional image are shown in Figure 3.13.

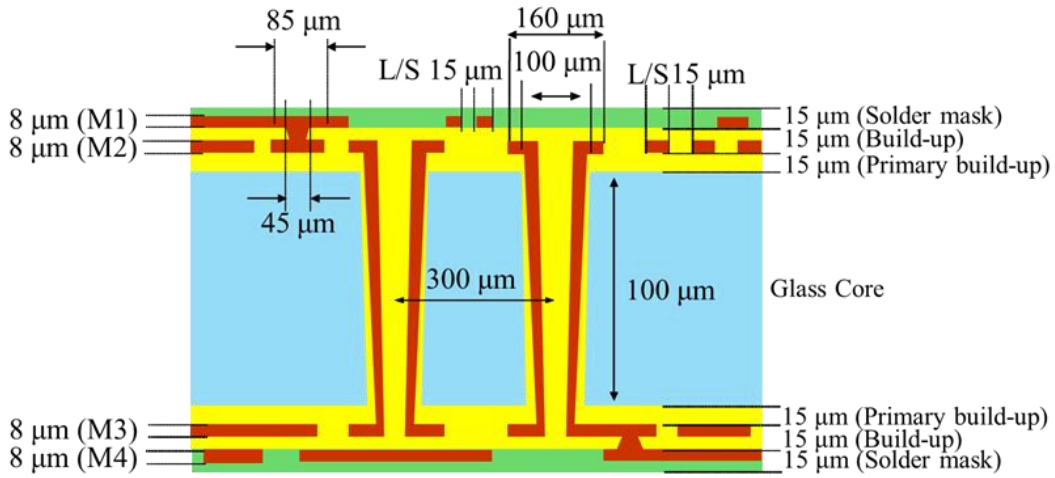


Figure 3.13. Glass substrate stack-up of 3D IPD diplexers with organic thinfilms.

Four layers of dry-film epoxy-based dielectrics Ajinomoto' build-up film ABF with 15 µm thickness are laminated onto both sides of the 100 µm thick glass substrate. In LTE frequencies, the glass substrate has a dielectric constant of 5 and a loss tangent of 0.005, while the build-up dielectrics have a dielectric constant of 3.2 and a loss tangent of 0.0042. These low-loss attributes contribute to performance enhancement of the passive circuits by minimizing substrate-induced insertion loss. The minimum linewidth / space of this design is 25 µm / 15 µm, considering the fabrication precision. The copper circuitry patterning capability on glass substrates at panel-level can be extended to as fine

as below 2 μm / 2 μm in terms of linewidth/spacing with the leading-edge packaging processes that have been developed and demonstrated at Georgia Tech. The diameter of TGVs was 100 μm, maintaining a 1:1 via diameter to substrate thickness aspect ratio. Four metal layers with copper conductors at 8 μm thickness were needed to build the passive circuits.

Based on the proposed substrate architecture, spiral inductors and parallel-plate capacitors were individually modeled as the first step to establish an LC library. Spiral inductors were designed with a minimum of 25 μm linewidth and 15 μm space between two adjacent loops. These inductors had inductance density of over 20 nH / mm^2 and unloaded Q factors of 30~40 at 2 GHz. And because of the use of organic thinfilms, the capacitance density was 3.5 pF/mm^2.

The diplexer modeling was performed in the 3D EM solver ANSYS HFSS. In the layout, the LBF and HBF were embedded separately into the organic thinfilms on double sides of the glass substrates, and interconnected with TGVs. This yielded a 3D IPD configuration, and is shown in Figure 3.14.

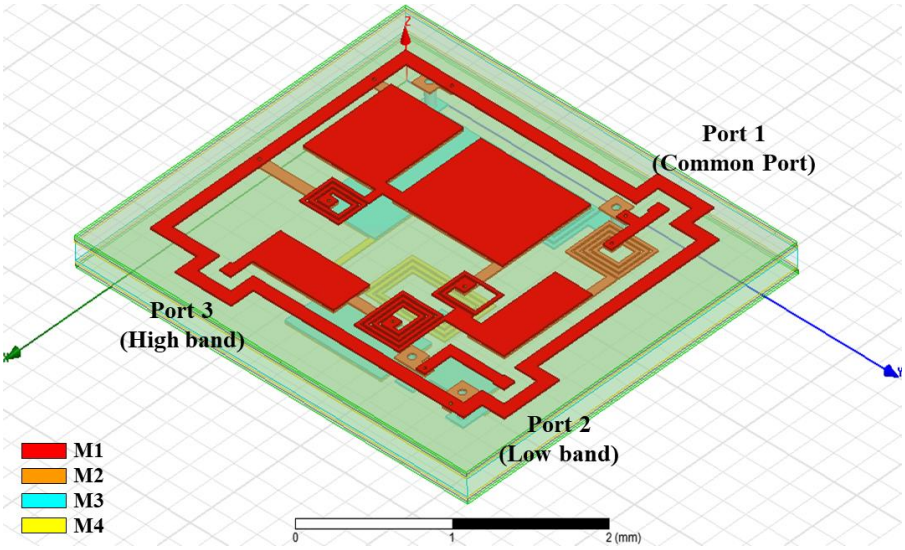
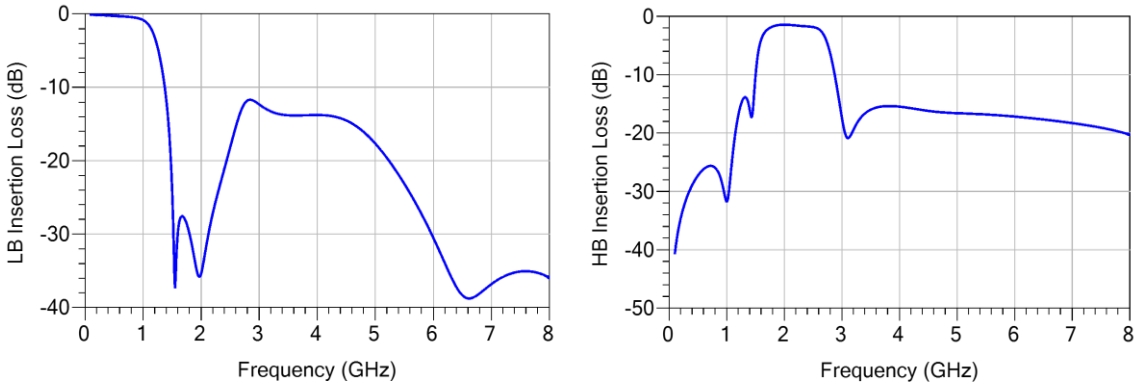


Figure 3.14. Layout of designed diplexer in HFSS.

In details, the HBF network was designed by utilizing two metal layers on the top side of the glass substrate, while the LBF was designed on the bottom side, with its ports extended to the top M1 layer through TGVs and blind vias. A ground frame was designed on the M1 layer surrounding the diplexer and it served as the return path for the current during high-frequency measurements. Wafer-probe testing was enabled by introducing three 250 μm pitch ground-signal-ground (GSG) pads at each port. All three ports were coplanar on M1 metal layer and the signals were fed to the three ports from signal pads through short copper traces. Port 1 was defined as the common port that connected both LBF and HBF, while Port 2 and Port 3 were the low-band and high-band outputs respectively.

Direct superposition of high-band filter directly over the low-band filter was also avoided as much as possible to reduce the proximity-induced EM crosstalk between top and back side components. The designed diplexer had a total thickness of 200 μm, and lateral dimensions 2.3 mm × 2.8 mm, including the testing structures.

EM simulation was conducted with a frequency sweep from 100 MHz to 8 GHz and the simulated transmission characteristics of the designed diplexer are presented in Figure 3.15.



(a) (b)

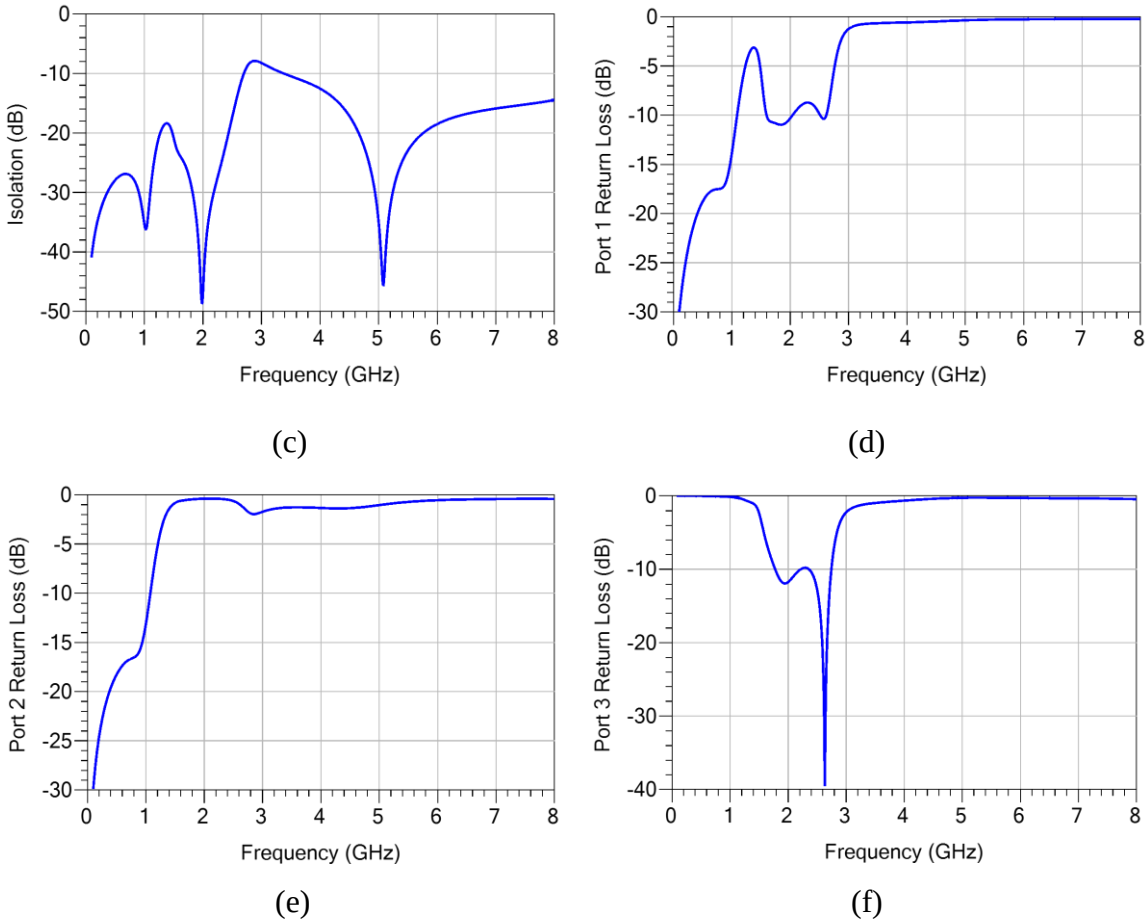


Figure 3.15. EM simulation results of the designed diplexer: (a) low-band IL, (b) high-band IL, (c) isolation, (d) Port 1 RL, (e) Port 2 RL, and (f) Port 3 RL.

The minimum insertion loss achieved in diplexer's passbands were 0.40 dB in low band and 1.44 dB in high band. The discrepancy between EM simulation and circuit-level simulation results was due to several factors that were not captured in the circuit modeling. The existence of factors such as Q factors of lumped elements and EMI induced parasitic effects can alter the filter's performance. This has been particularly serious in ultra-miniaturized systems, in which high-Q components are difficult to design and components in proximity crosstalk with each other. Therefore, sustained attention is required in each engineering step.

3.1.2 Diplexer Fabrication on Glass Substrates

Process Flow

In order to allow low-cost and large-area panel-scale manufacturing of the proposed glass-based 3D IPDs, laminate-substrate-compatible processes were proposed for the glass substrates fabrication. Detailed process flow is illustrated in Figure 3.16.

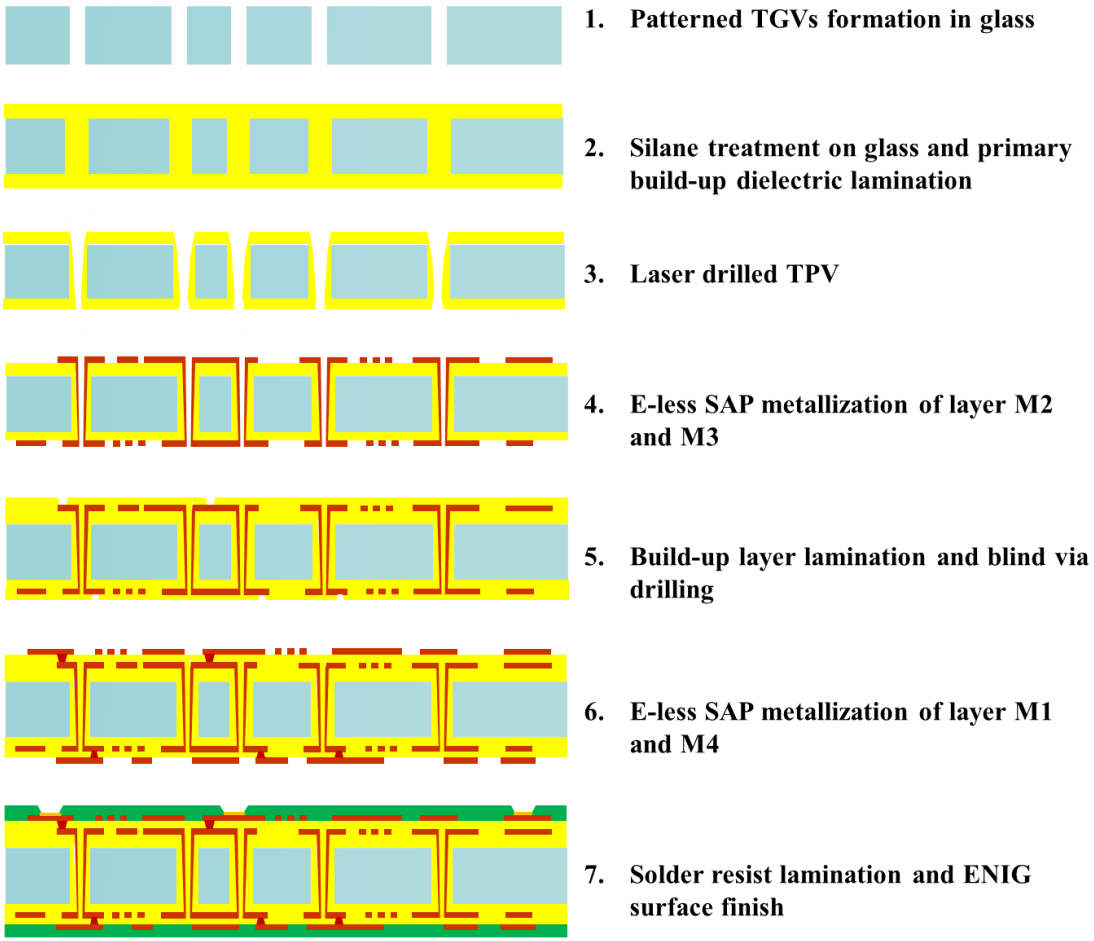


Figure 3.16. Glass substrate fabrication process-flow for 3D IPD diplexers.

TGVs of 100 μm diameters were formed in bare Corning glass with laser ablation and laser-assisted chemical etching. Glass surfaces were treated with 3-aminopropyltrimethoxysilane to improve their adhesion to polymer. To enable glass-handling for large-scale manufacturing, dry film polymers were laminated onto the glass

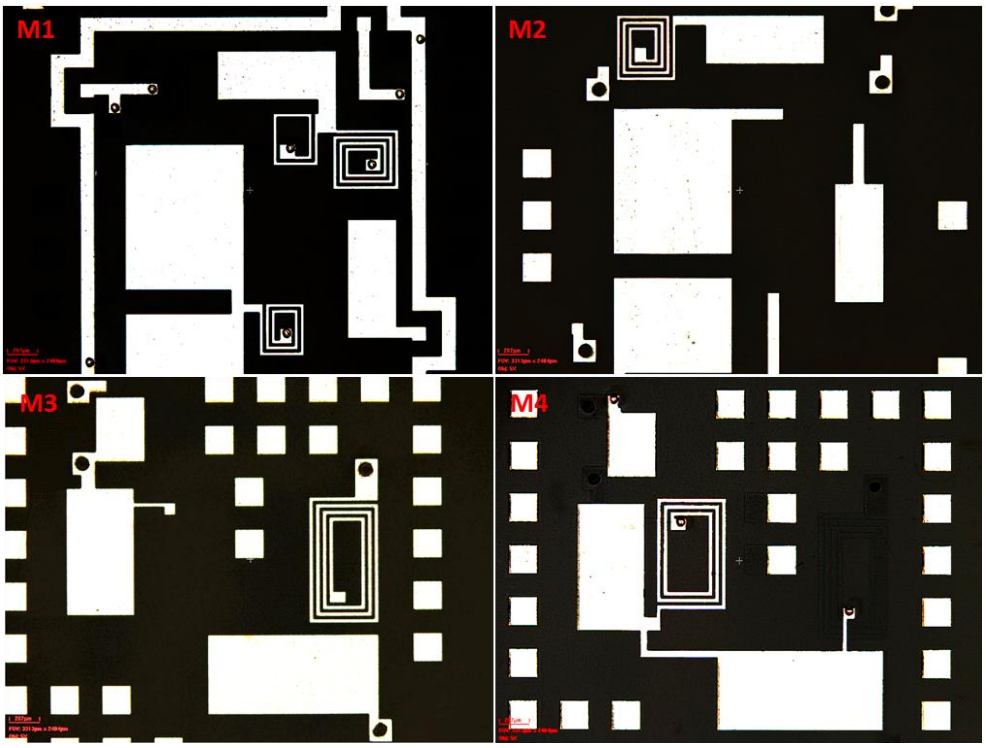
to form primary build-up layers. The polymers attain low viscosity that allows them to flow during their curing process, and fill up the TGVs of the designed size. Through-vias are formed by drilling through the polymer-filled vias. A carbon dioxide (CO_2) laser was used to drill through these polymer-fills and form through-package vias (TPVs) at a relatively smaller diameter compared to the pre-fabricated vias. As the glass surface, including the TGV sidewalls, is completely coated with polymers, a low-cost wet metallization process electroless (E-less) plating can be used to deposit the seed layer on polymers with good adhesion. This eliminates the need for sputtering processes, which are typically used in BEOL technology for silicon wafers, and are associated with higher tooling cost and comparatively lower throughput.

Copper circuits were formed with semi-additive patterning (SAP) process using ultraviolet (UV) dry film lithography and electroplating. The solder mask layer was then laminated to cover the circuitry and prevent contamination and oxidation, while only leaving the GSG pads for probing purpose. Electroless nickel immersion gold (ENIG) surface finish was applied to the probe pads to reduce the contact ohmic loss during testing. The fabricated diplexers were singulated from the glass substrate panel by mechanical dicing using a diamond blade.

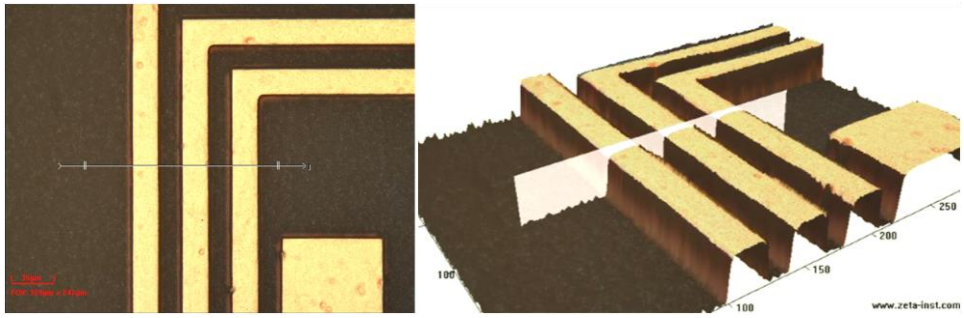
Fabrication Results

Patterned diplexer circuitry on each metal layer is shown in Figure 3.17. Several 0.2 mm × 0.2 mm isolated metal squares were placed around the design structures at each metal layer in order to balance the copper distribution uniformity. This implementation also allowed a uniform copper plating over structures of varying sizes, because of which the copper thickness differences between inductors and capacitors were minimized. In the

microscopy image of one fabricated inductor, straight copper trace edges and sharp corners were featured, owing to high-precision photolithography and advanced SAP metallization methods.



(a)

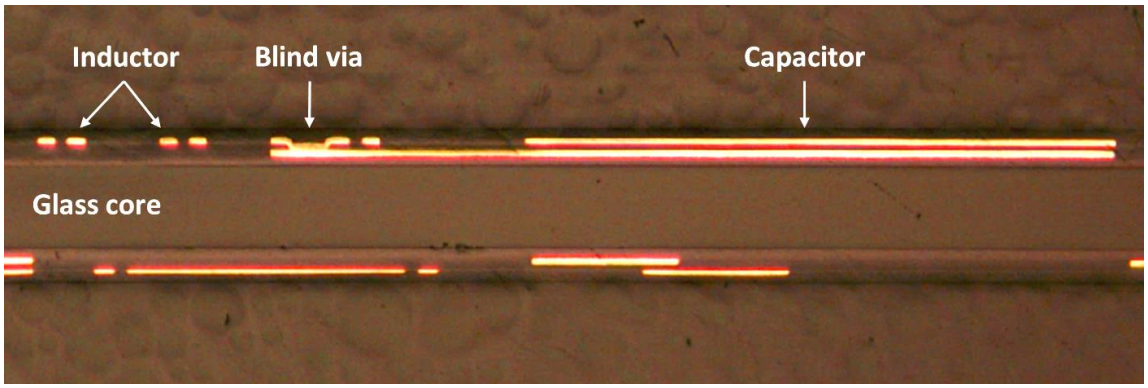


(b)

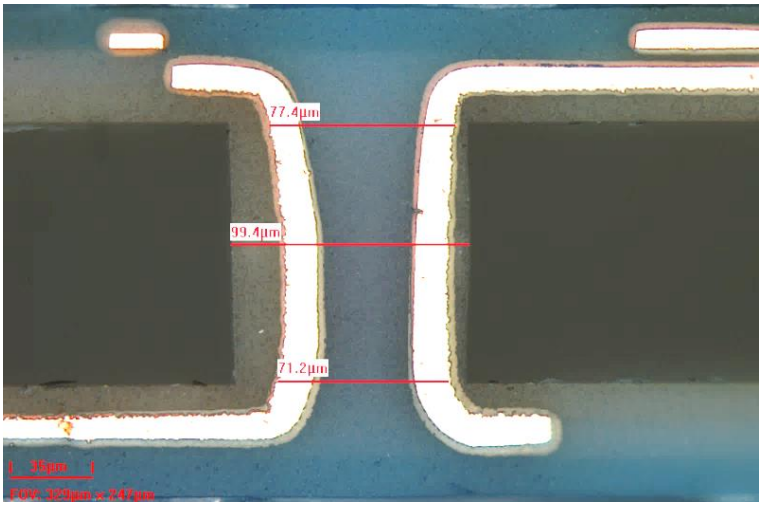
Figure 3.17. Electroless and SAP metallization results of fabricated diplexers: (a) overview of M1-M4 layers, and (b) a spiral inductor imaged by 3D microcopy.

Cross-sectional images of designed diplexers are pictured in Figure 3.18. The substrate maintained its flatness due to high modulus of glass. In a TGV structure, the polymer

coated on the vertical sidewalls of the glass vias not only enabled the electroless copper plating, but also served as a buffer layer to release the stress between copper and glass. In addition, the lamination of second build-up dielectrics also filled the void space in conformal plated vias, further enhancing the reliability of these TGVs.



(a)



(b)

Figure 3.18. Cross-sectional images of fabricated diplexers: (a) double-side embedded passives on glass, and (b) a TGV structure for interconnection.

The glass panel size for this lab-scale demonstration was 150 mm × 150 mm, using processes that can be potentially scaled up to 500 mm × 500 mm for mass production by substrate manufacturers. A magnified image of the fabricated 3D IPD diplexers on glass substrate is shown in Figure 3.19.

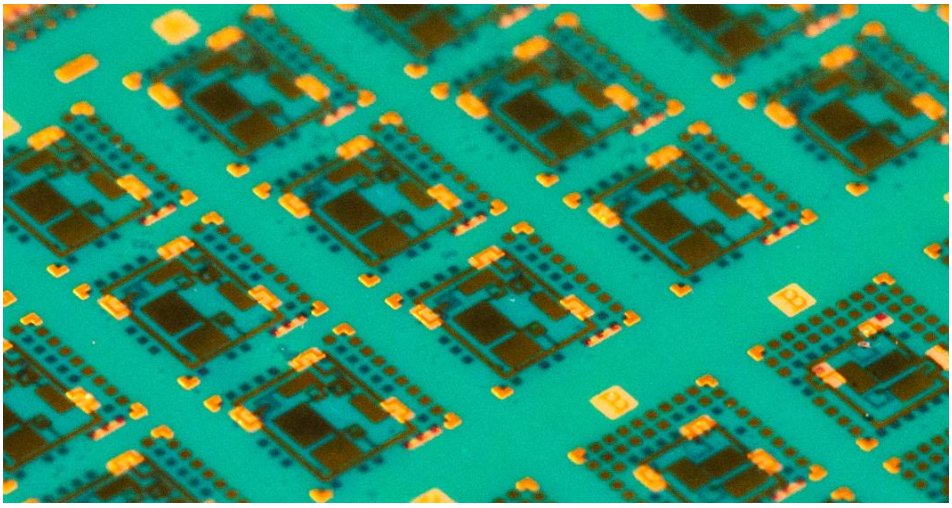


Figure 3.19. Demonstrated 3D IPD diplexers on glass substrates.

These diplexers could be integrated into an RF module either as discrete components with bumped solder balls so that they could be assembled onto a module substrate, or as substrate-embedded passives that are fabricated along with the glass module substrate. Particularly, when used in the proposed 3D IPAC glass packages, both integration approaches are executable. As discrete components, since the CTE mismatch between device and module substrate is eliminated, assembly-induced reliability concern is relieved. This approach could also be extended to embedding because diplexers could be co-designed with the module substrates because of the compatible glass substrate technologies.

3.1.3 Diplexer Performance Characterization

The performance of the fabricated diplexers was measured using a vector network analyzer (VNA) that could support up to millimeter wave frequencies. A probe station with three-port measurements was set up using three GSG probes at 250 μm pitch. The measured performance metrics were plotted together with the EM simulation results of the HFSS model for correlation analysis, as shown in Figure 3.20.

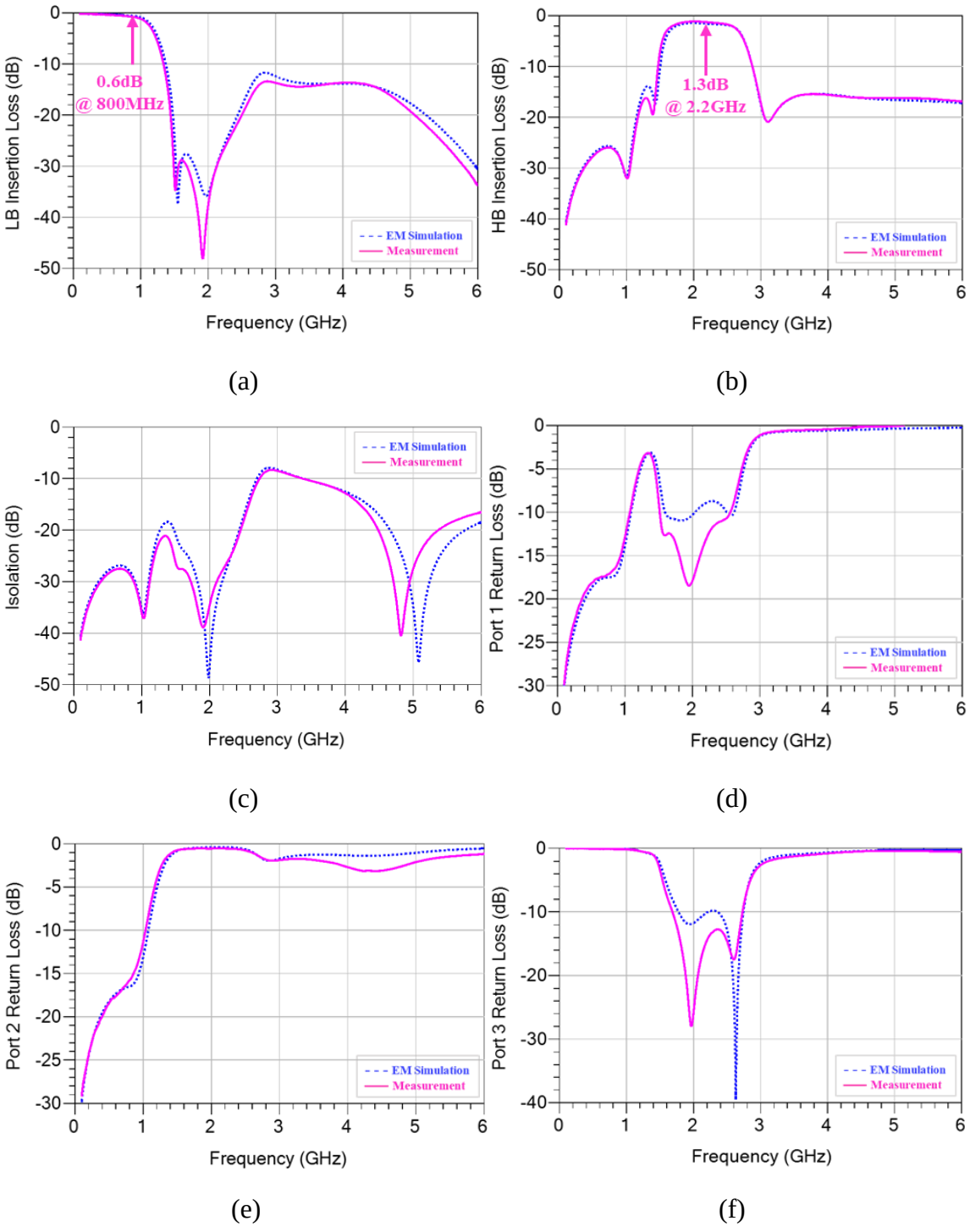


Figure 3.20. Correlation between diplexer EM simulation and measurement results: (a) low-band IL, (b) high-band IL, (c) isolation, (d) Port 1 RL, (e) Port 2 RL, and (f) Port 3 RL.

A good measurement-to-simulation agreement was observed, indicating the successful modeling and fabrication of the proposed diplexers. The feasibility of designing 3D IPDs with organic thinfilms on ultra-thin glass substrates is thus shown. The measured electrical performance metrics of the proposed diplexer are summarized in Table 3.4.

Table 3.4. Measured 3D IPD diplexer performance metrics

	Specification	Frequency (MHz)	Magnitude (dB)
Low Band	Insertion loss	700 - 960	< 0.9
	Return loss	700 - 960	> 14
	Rejection	1500 -1700	> 23
	Rejection	1710 - 2690	> 16
	Isolation	1710 - 2690	> 13
High Band	Insertion loss	1710 - 2690	< 2.9
	Return loss	1710 - 2690	> 12
	Rejection	700 - 960	> 26
	Rejection	4000 - 6000	> 16
	Isolation	700 - 960	> 27

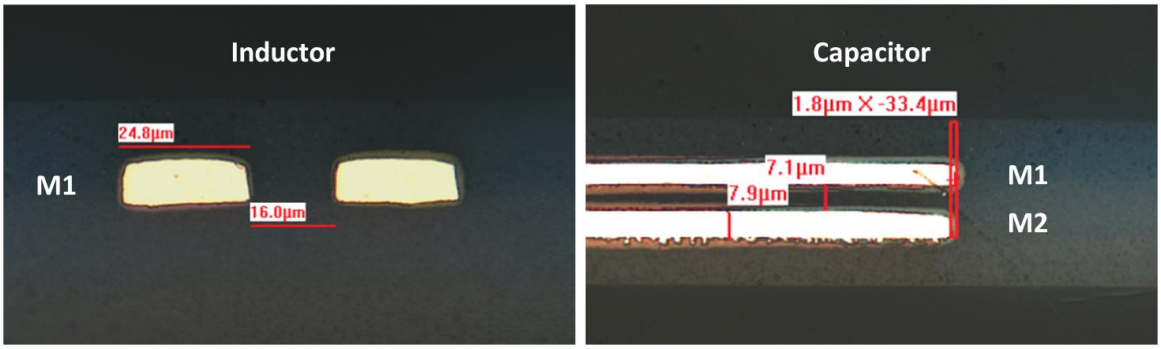
3.1.4 Diplexer Performance Sensitivity Analysis

The performance of passive circuits is sensitive to many factors. This requires deliberate considerations at each design and manufacturing step so that the proposed technology can be transferred to large-scale manufacturing. Due to the inevitable challenges with process control during device manufacturing, process-induced variations could deviate the behavior of RF circuits from what they are designed. These variations should be quantified by extensive experiments, then analyzed by a combination of modeling and characterization, and finally be minimized with optimization solutions. Better than 5% process tolerance is targeted for large-scale manufacturing.

Process-induced Variations

In this diplexer design with ultra-thin polymer dielectric films, the acceptable process error margin is narrow because of smaller structure and feature sizes. Sub-micron change in dimensions could exert a significant influence on diplexer performance. Although fabrication imperfections cannot be avoided, it is still valuable to figure out the dominant factors and optimize the designs through process innovations to minimize their sensitivity towards the performance.

Inductors and capacitors are the major components in a diplexer, and their sensitivity to process errors directly influences the diplexer's performance. However, in this design, the spiral inductors and organic thinfilm parallel-plate capacitors react to process-induced variations differently, and they should be studied separately. For instance, cross-sectional images of one inductor and one capacitor sample on previously tested diplexer are shown Figure 3.21. Measured physical dimensions of linewidth/spacing, metal thickness, dielectric thickness and layer-to-layer mis-registration are recorded in Table 3.5.



(a) (b)

Figure 3.21. Cross-sectional images of previously tested diplexer: (a) a one-turn spiral inductor, and (b) a capacitor.

Table 3.5. Quantified process variations of the demonstrated diplexer

Items	Design	Measurement
Linewidth / Space	25 μm / 15 μm	24.8 μm / 16 μm
Dielectric thickness	7 μm	7.1 μm
M2 thickness	8 μm	7.9 μm
Layer-to-layer mis-registration	0	1.8 μm

In the case of spiral inductors, where fine lines and spaces are used, photolithography accuracy and copper trace sidewall etching during seed-layer removal could modify their characteristics such as quality factor and self-resonant frequency. The measurement data from Table 3.5 showed excellent lithography precision with 5% fine-line resolution accuracy. Precision in copper trace geometry was also maintained during seed-layer removal with innovative differential etching, which selectively etches the seed-layer without inducing lateral undercut of copper sidewalls.

The performance of capacitors, however, is more sensitive to process variations compared to inductors. Unlike spiral inductors, where only one winding metal layer is critical for magnetic flux generation, parallel-plate capacitors use two electrodes on different layers that are face to face and separated by a dielectric film. The dielectric film thickness directly affects the electrical characteristics of the capacitors.

One of the challenges for multilayer processing is the layer-to-layer mis-registration. In the current diplexer topology, the two electrodes of each capacitor are designed to be equal in size with zero tolerance to misalignment. This allows to test and evaluate the diplexer performance sensitivity with the proposed ultra-thin glass substrate technology. A key characteristic of glass is its dimensional stability from high modulus and elastic behavior with no permanent deformation from viscoelastic or viscoplastic behavior,

which effectively impedes the dimensional change while also maintaining substrate flatness during processing. In this diplexer sample, the layer-to-layer mis-registration was less than 2 μm, considering ±1 μm alignment tolerance. Even for the smallest capacitor C_{L3} whose physical dimension was 335 μm × 440 μm, the capacitance variation from mis-registration was within 1%.

However, capacitance can significantly shift on account of variation in dielectric thickness. Figure 3.22 illustrates the mechanism by which dielectric thickness could vary because of the variation in plated copper thickness during substrate fabrication process.

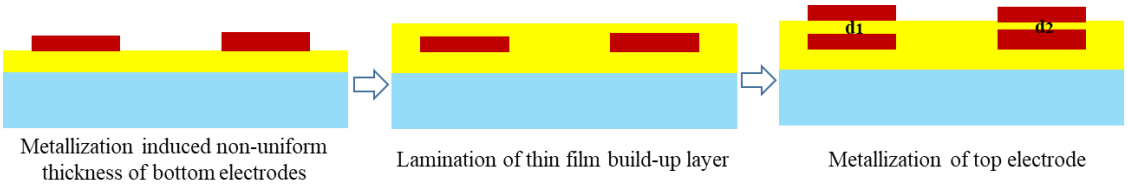


Figure 3.22. Dielectric thickness variation during substrate fabrication.

Thickness uniformity of electrolytic plated copper is a major challenge during large-area panel processing. If the bottom electrode thickness varies across the panel, it will directly impact the dielectric thickness, resulting in different thicknesses at different locations. Small deviation in thinfilm dielectric thickness could cause a huge percentage change in capacitance. To verify this hypothesis, experimental quantification was conducted on ten fabricated diplexer samples. As much as ± 0.5 μm thickness variation on build-up dielectric and copper was observed, exceeding the 5% tolerance requirement.

Diplexer Sensitivity to Process Variations

To understand the sensitivity of the designed 3D IPD diplexer, EM models were built and simulated to quantify the deviation of diplexer's performance from process variations. The study was primarily focused on M2 copper and the corresponding

dielectric thickness. The capacitors were initially designed with 8 µm thick copper electrodes and 7 µm thick dielectrics in between the two electrodes. In diplexer EM models, ± 0.3 µm thickness variations were captured. The diplexer was simulated, and its sensitivity to these thickness variables is reflected in the high-band insertion loss, as plotted in Figure 3.23.

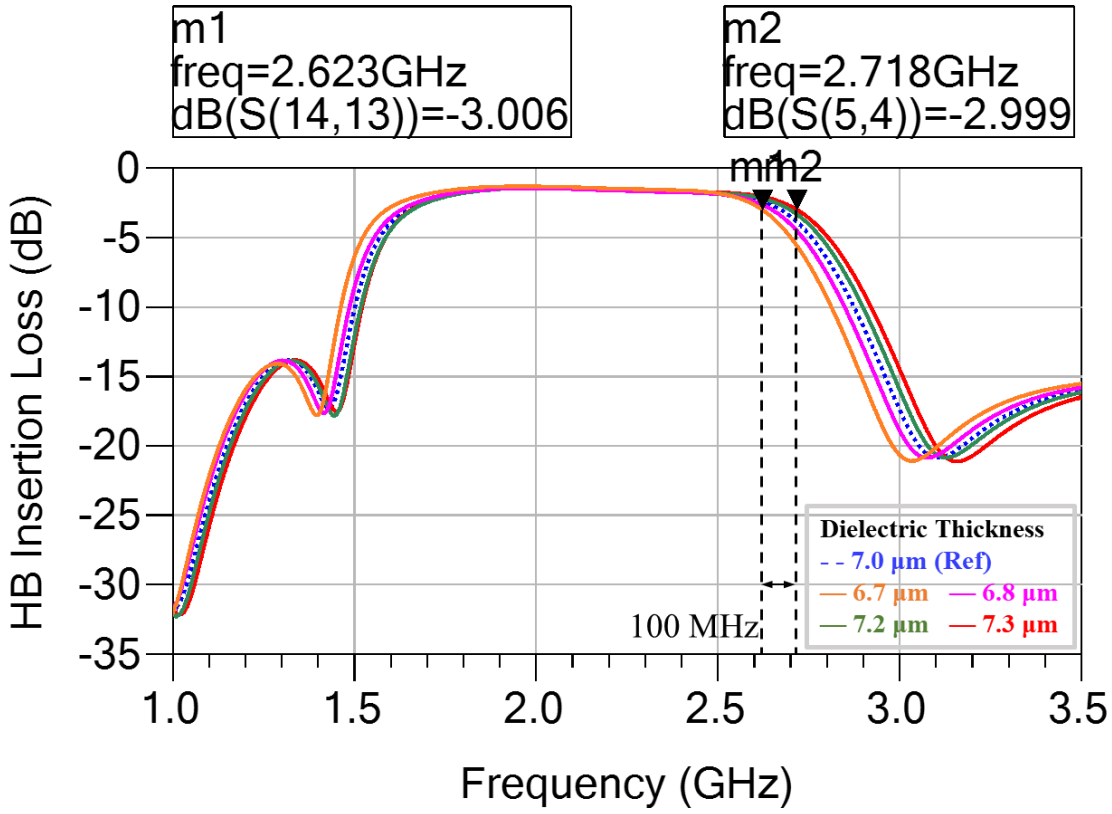


Figure 3.23. Thickness variation-induced diplexer high-band IL deviation.

When the dielectric thickness varied, the upper 3 dB cut-off frequency of the HBF showed a spread of as much as 100 MHz, equivalent to 10% of the bandwidth. This indicated that the diplexer performance was sensitive to the build-up dielectric thickness variation due to its impact on capacitance values. It was also observed that the passband insertion loss was not affected much with this thickness variation, as the Q factors of LC elements were not sensitive to these thickness variations.

Process Optimization

To mitigate the critical frequency-shift or band-spread issue, both dielectric and copper thickness should be well-controlled. A surface planarization method was proposed by using a diamond blade to mechanically cut the excessive thickness of copper and dielectrics. This is a low-cost approach compared to expensive chemical mechanical polishing (CMP) that has been widely used in BEOL processes on silicon wafers. Step 4 and 5 in the previous process flow shown in Figure 3.16 were modified to incorporate this surface planarization process, and these modifications were illustrated in Figure 3.24.

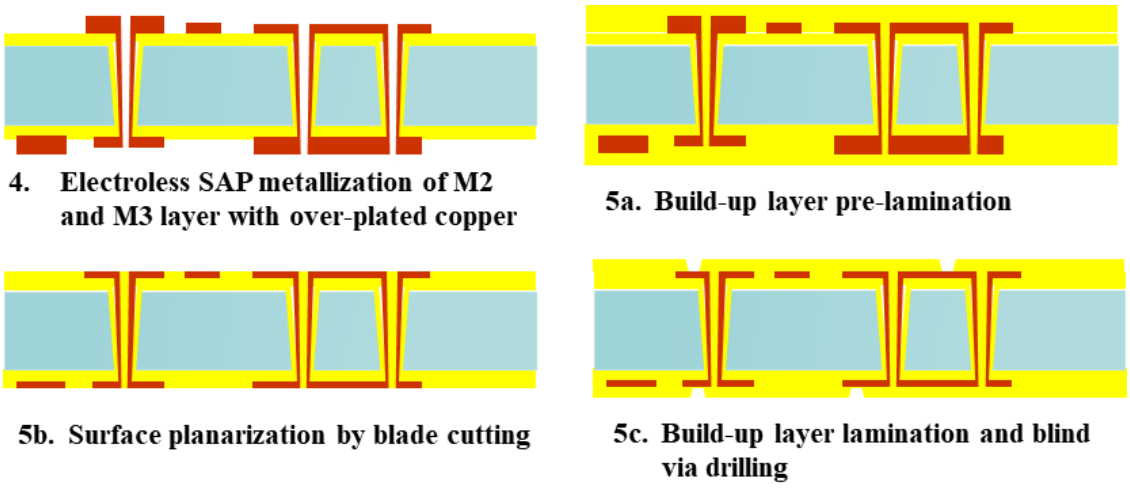


Figure 3.24. Modified build-up layer lamination process with the introduction of surface planarization process for thickness control.

During the metallization process of M2 and M3 layers, the copper was over-plated by as much as 4 μm on purpose, ensuring all the copper structures on the glass panel were thicker than target thickness. Then, build-up dielectric films were pre-laminated on double sides of the glass substrates to embed the copper circuitry, and were half-cured at room temperature for 24 hours. Both sides of the substrate were then planarized by a blade-cutter machine provided by Disco, and excessive thickness of dielectric and copper

was simultaneously removed, until all the embedded copper circuitries were exposed and copper thickness target was met. Smooth and flat substrate surfaces were yielded with uniform copper thickness along the panel. Results of planarized copper circuitry are shown in Figure 3.25. On top of these planarized substrate surfaces, build-up dielectrics were laminated. Since the gaps between copper structures had been filled with pre-laminated dielectrics, the build-up layer suffered zero thickness variation after curing. Hence, process-induced copper and dielectric thickness variation was minimized.

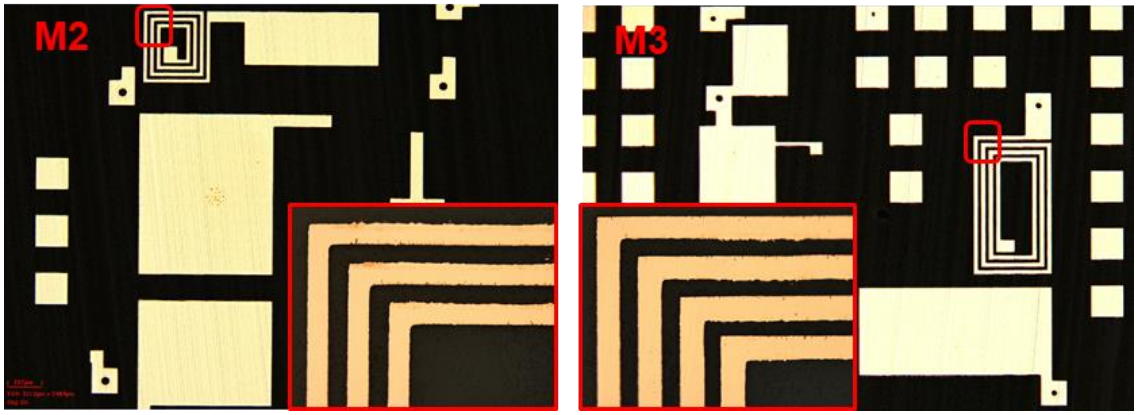
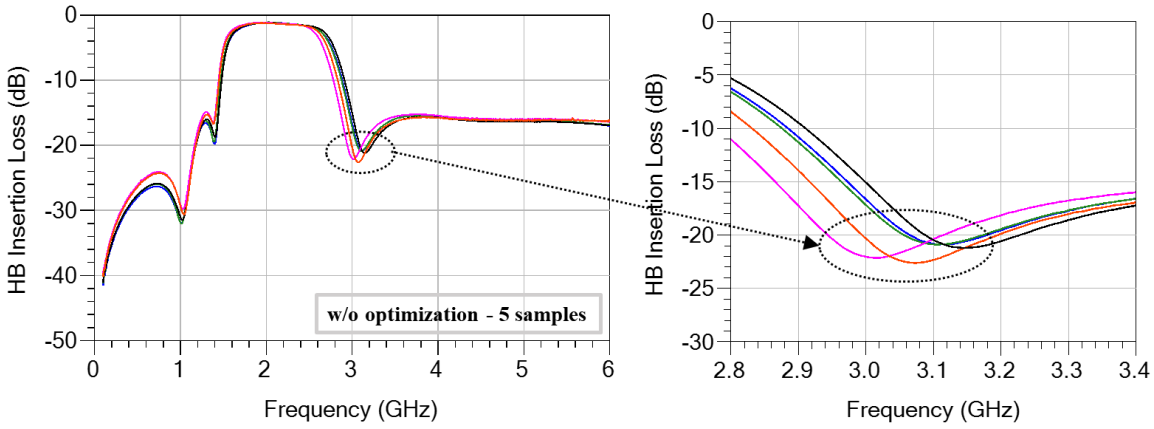
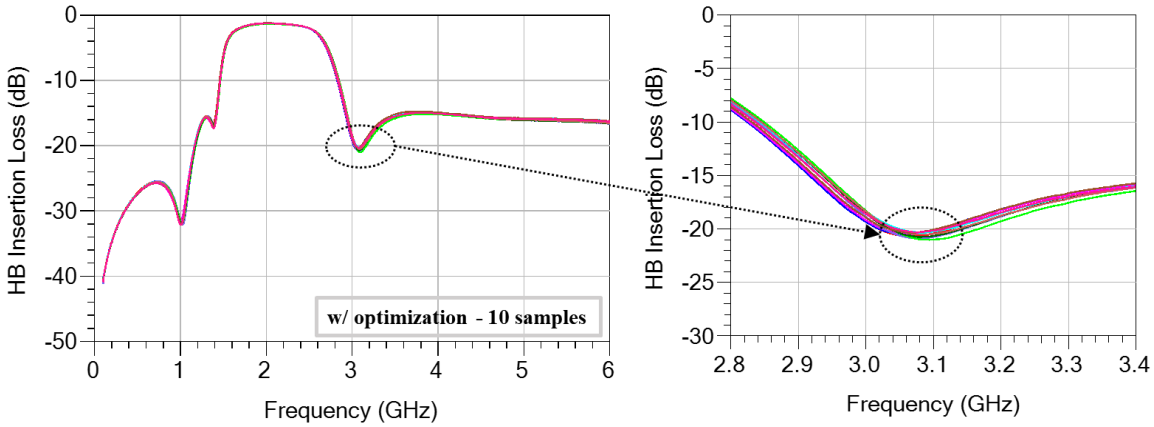


Figure 3.25. Surface planarized M2 and M3 layers.

To verify the effectiveness this optimization approach, the electrical performance of re-fabricated diplexer samples was measured and compared to previous results, as shown in Figure 3.26. The graphs suggest that, without surface planarization, the notch frequency spread from five samples was 150 MHz. This number, however, was minimized to 39 MHz on ten measured samples, after employing the optimization approach.



(a)



(b)

Figure 3.26. Comparison of HBF S31 IL: (a) first batch of samples without process optimization, and (b) second batch of samples with process optimization.

Excellent fabrication repeatability was achieved with the introduction of surface planarization process. The dielectric thickness variation significantly impacts the diplexer's attributes. Potential large-scale manufacturing of the proposed 3D IPDs with organic thinfilms on glass can be enabled by precise control over the build-up dielectric thickness. Surface planarization by a blade cutting approach is one promising low-cost solution for such application.

3.1.4 Summary

The very first ultra-miniaturized 3D IPD LTE diplexer was successfully designed and demonstrated with organic thinfims on ultra-thin glass substrates. Major accomplishments of the demonstrated diplexer are summarized in Table 3.6.

Table 3.6. Accomplishment of demonstrated 3D IPD diplexer

Topic	Metrics	Objectives	Accomplishment
3D IPD Diplexers	Performance	• IL < 0.6 dB • RL > 15 dB • Isolation > 20 dB	• IL - Min 0.5 dB @ LB - Min 1.3 dB @ HB • RL - > 15 dB @ LB - > 12 dB @ HB • Isolation - > 26 dB @ LB - > 16 dB @ HB
	Miniaturization	• Z < 0.3 mm • X-Y < 2 mm × 2.5 mm	• Z = 0.2 mm • X-Y = 2.3 mm × 2.8 mm

Process-induced variations were quantified and analyzed. The process variation study for the proposed approach suggested that the diplexer performance is sensitive to build-up dielectric layer thickness. The degradation of diplexer performance is reflected as a frequency-shift and band-spread, particularly at high frequencies. A process control solution was proposed with the introduction of an additional surface planarization process during build-up layer lamination. Re-fabricated diplexers showed excellent consistency, demonstrating that the glass 3D IPD technologies are suitable for large-scale manufacturing. With design optimization and process innovations, electrical performance of the diplexer could be further improved.

3.2 High-performance 3D IPD Diplexers with High-Q Thinfilms on Glass

The performance metrics of previously demonstrated diplexers are to be further improved with new design and technologies. To reduce the insertion loss, high-Q components are required. The enhancement of inductor Q factor is always at a cost of decreased density, and hence the inductor size becomes a major constraint. This could be potentially compensated with smaller capacitors, optimized design topology and space-saving floor-plan techniques. High-Q inductors could be realized by using 3D architecture such as solenoid types to replace the 2D spiral types. While for high-density and high-Q capacitors, thinfilm high-K dielectrics are key enablers. Traditional organic thinfims fail to meet these needs due to their limited dielectric constant and their inability to form sub-micron films with high yield. On the other hand, inorganic materials can eliminate these concerns and have been widely used as the dielectric layers for ultra-high density MIM capacitors. The integration of both high-Q inductors and ultra-high density MIM capacitors on low-loss glass substrates has become a promising solution to enhance the diplexer performance.

3.2.1 Thinfim Passive Components

<u>High-Q Inductors</u>

Inductor Basics

The Q factor of an inductor is defined as ratio of energy stored over the energy dissipated, and these two parameters are correlated to its inductance and resistance. A two-port inductor on a substrate can be equalized to a π-type lumped circuit model, as shown below in Figure 3.27(a) [48]. In the equivalent circuit, L_S is the inductance of the inductor, and R_S indicates the series resistance. In a typical inductor design, multiple coils

are wound and coupled with each other, which yields capacitance C_S. Other parameters such as C_{d1} and C_{d2} are the capacitance between the inductor wires and the substrate, while C_{sub} and R_{sub} are the capacitance and resistance in the substrates. These lumped elements could also be transferred to Y-parameters so that the frequency-dependent characteristics are manifested. An equivalent Y-parameter model is drawn in Figure 3.27 (b) [48].

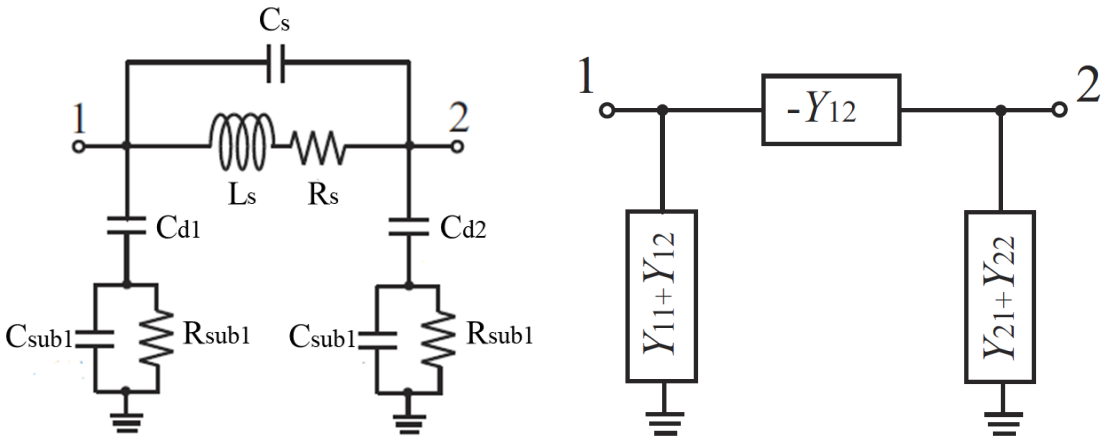


Figure 3.27. Equivalent π-model circuit of an inductor with: (a) lumped elements, and (b) Y-parameters.

When one port of the inductor is shorted to ground, then $-Y_{12}$ and $Y_{11}+Y_{12}$ are in parallel, yielding only Y_{11} between Port 1 and ground. Equations in (3.4) define the inductance and Q factor.

$$L = \frac{Im(1/Y_{11})}{w}$$
$$Q = \frac{Im(1/Y_{11})}{Re(1/Y_{11})} \tag{3.4}$$

It is easy to relate Y_{11} with lumped elements in Figure 3.27(a). For inductors designed on low-loss glass substrates, parasitic elements such as C_d, C_{sub} and R_{sub} can be ignored especially at low frequencies. The expression for Y_{11} and Q factor can be approximately expressed in the forms shown in equation (3.5). Both R_S and L_S are frequency dependent and could be extracted from Y-parameters. To enhance to the Q factor at a fixed inductance, conductor resistance must be minimized.

$$\frac{1}{Y_{11}} \sim R_s + jwL_s$$
$$Q = \frac{wL_s}{R_s} \tag{3.5}$$

High-Q Inductor Design

Lateral 3D solenoid inductors were considered which could efficiently leverage the space in three dimensions [49]. These inductors were designed on 200 µm thick glass with the substrate stack-up shown below in Figure 3.28. The glass substrate was double-side laminated with 15 µm low loss Ajinomoto's ABF GY-11 series dielectric films. Two copper layers were utilized and interconnected with 60 µm diameter TGVs at 150 µm pitch.

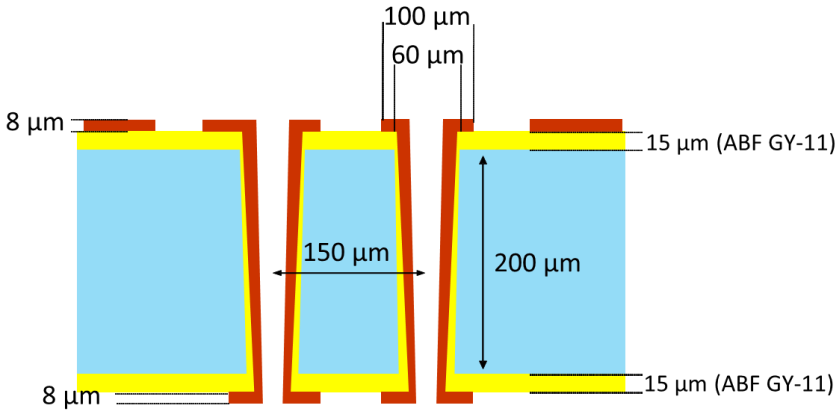


Figure 3.28. Glass substrate stack-up for high-Q solenoid inductors.

An example of a designed solenoid inductor model is pictured in Figure 3.29. The inductor had 2.5 turns of coils, and the winding in lateral direction was enabled by six TGVs. Lumped ports were set at two terminals, referring to a ground frame that serves as the current return path. The inductor had a physical dimension of 1 mm × 1 mm.

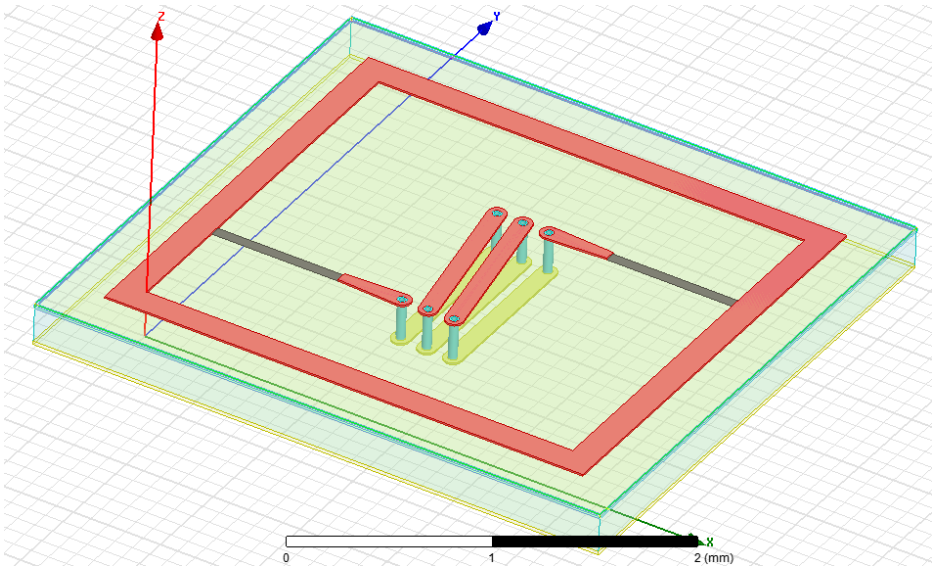


Figure 3.29. An example of designed solenoid inductor on glass.

The inductance and Q factor were extracted and calculated out of the Y-parameters based on Equations (3.4), and are plotted in Figure 3.30.

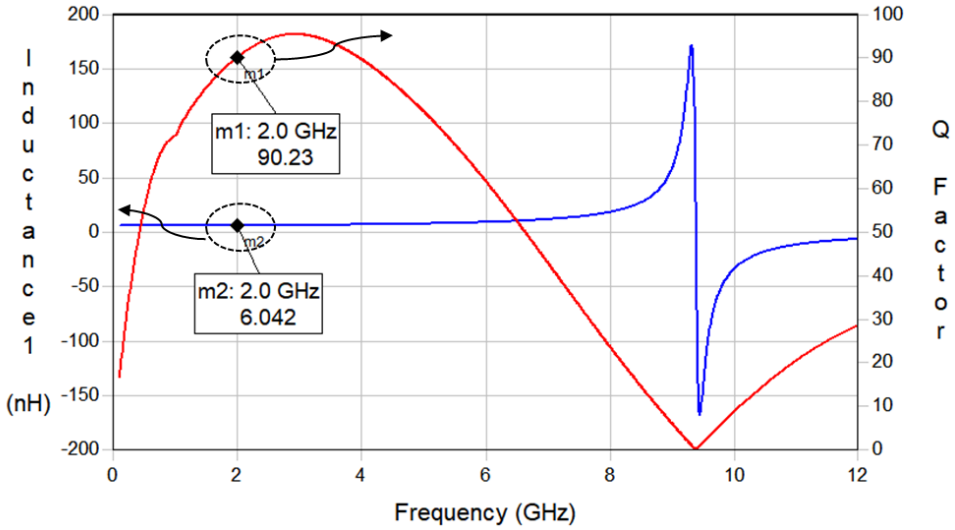


Figure 3.30. Frequency response of the designed solenoid inductor.

The designed inductor had an inductance of 6.04 nH and a Q factor of 60 at 1 GHz and 90 at 2 GHz. The SRF of such inductor was at 9.31 GHz, which is more than four times the frequency of interest. EM modeling and simulation has proved that solenoid inductors significantly improve the Q factor.

Ultra-high Density Thinfilm Capacitors

MIM Capacitor Integration on Glass

MIM capacitors have been widely used in analog, mixed signal and RF IC circuits, for their stable capacitance, high capacitance density and low parasitics. Owing to the high-K sub-micron thick dielectrics, the capacitance density of MIM capacitors could be 50 X or higher than that of conventional organic thinfilm capacitors. Their integration on glass would certainly help the performance enhancement of filters and diplexers.

Silicon Nitride (Si_3N_4) was selected as the primary insulator material between two copper electrodes, and a unique MIM capacitor structure on glass has been proposed and shown in Figure 3.31.

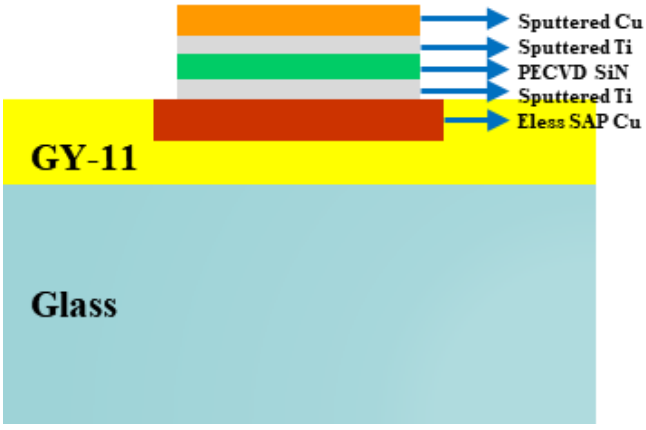


Figure 3.31. Proposed MIM capacitor structure on glass substrate.

Multiple thin metal and dielectric layers are stacked on the glass substrate with the process flow illustrated in Figure 3.32.

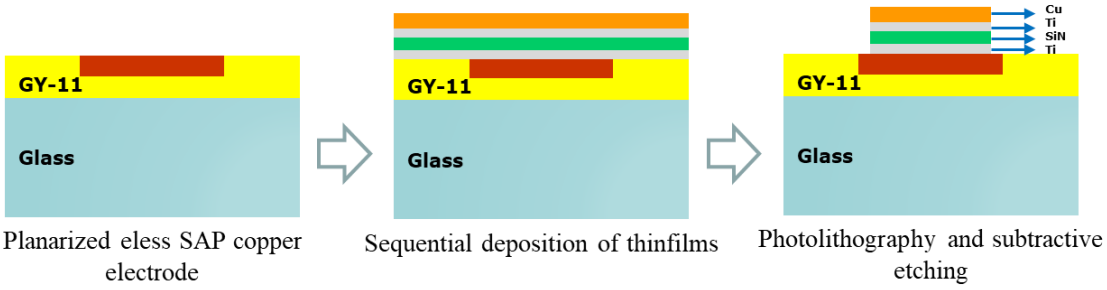


Figure 3.32. Process flow of MIM capacitor integration on glass substrate.

The bottom electrode was first metalized by electroless SAP and embedded into organic dielectrics by surface planarization, referring to the processes from Step 4 to Step 5b, as have been mentioned in Figure 3.24. This would allow the thickness of bottom electrode layer be controllable so that other coplanar metal structures could be utilized for low-loss interconnections or as parts of high-Q inductors in a filter or diplexer design.

A sequential disposition of titanium (Ti), Si_3N_4, Ti and Cu was then applied. Thin layers of Ti were introduced in between copper and silicon nitride layers by deposition. It was necessary to have Ti for several reasons. First, thin layer of Ti could serve as the adhesion promoter at Cu - SiN interfaces. It also functioned as a barrier that prevented copper oxidation and inter-diffusion between silicon nitride and copper oxide. In addition, the presence of Ti minimized the losses from interfacial reactions and inter-diffusion. The Si_3N_4 layer was formed by plasma-enhanced chemical vapor deposition (PECVD). Since the quality of the thinfilm Si_3N_4 depends on the deposition temperature, more than 200 °C was needed for pin-hole free and dense films with low loss. On the top of thinfilm Si_3N_4, top electrode of the capacitor was metalized by sputtering Ti and Cu at the same temperature of 250 °C.

To pattern the MIM capacitors, the top electrode was first defined by photolithography, with photoresist covering the surface of copper electrode. Cu in

uncovered area was removed by wet-etching, and then a dry etching process using CHF_3/O_2 plasma was employed to remove the Ti, Si_3N_4 and Ti sequentially in a single process step. Zero undercut was expected by the dry-etching process, which prevented potential short circuits risk between the top and bottom electrodes. After stripping the photoresist, the MIM capacitor was formed, with its both electrodes accessible using standard processes integration.

Characterization of MIM Capacitors

Before designing MIM capacitors, design rules must be identified and critical electrical properties of Si_3N_4 film such as relative dielectric constant D_k and loss tangent D_f should be quantified so that these MIM capacitors could meet both performance and manufacturing needs.

As has been discussed previously, the capacitance of a thinfilm capacitor is vulnerable to its dielectric thickness change. Because of this concern, the proposed PECVD Si_3N_4 thinfilm approach should be qualified first. An experiment was conducted on a 150 mm × 150 mm substrate, whose ultra-smooth surface helped eliminate the measurement errors due to surface roughness. About 1800 Å thick Si_3N_4 was deposited by PECVD with Ti barrier layer in between. The thickness of Si_3N_4 film was measured at different locations on the panel, with the results presented in Figure 3.33. An excellent 1% thickness uniformity was achieved locally within those 3 cm × 3 cm sampling regions, and the largest thickness spread measured on the substrate was 87 Å, accounting for less than 5% variation in worst case scenario. This experiment demonstrated that the proposed PECVD thinfilm Si_3N_4 based MIM capacitors could be potentially used in high-performance RF passive circuits due to their precise thickness control.

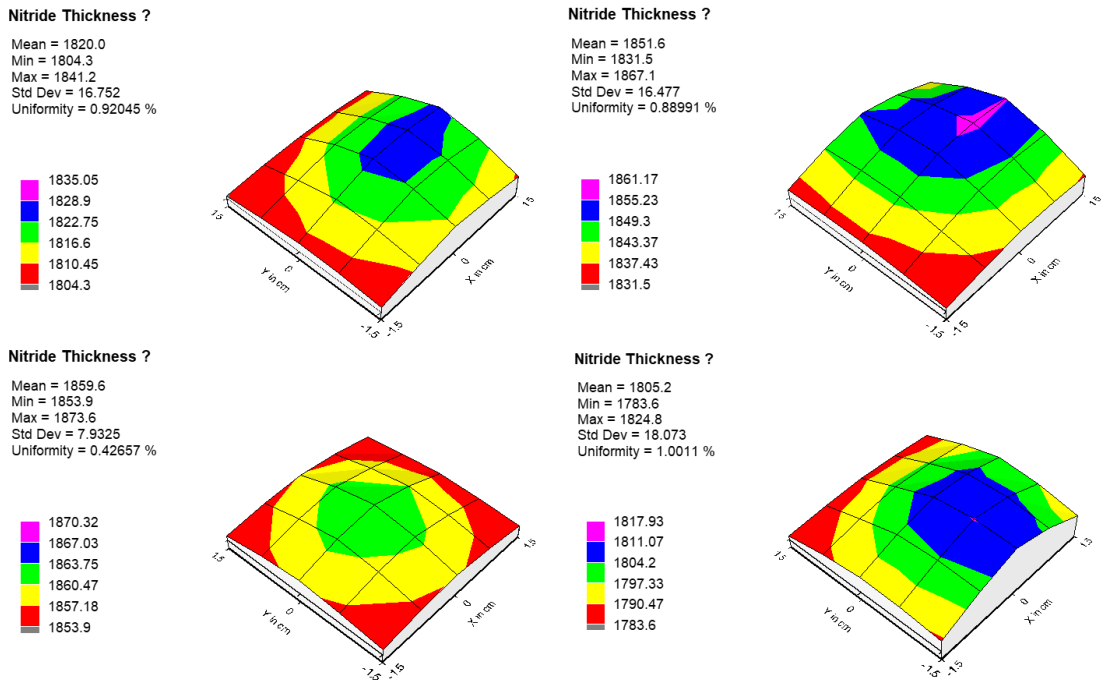


Figure 3.33. Measured thickness variation of PECVD Si_3N_4 on glass.

In order to extract the frequency-dependent electrical properties of the PECVD Si_3N_4, a VNA is required to test the frequency response of the fabricated MIM capacitors. For this purpose, a two-port MIM capacitor testing structure has been proposed and its substrate cross section is shown in Figure 3.34.

Figure 3.34. Proposed substrate stack-up for MIM capacitor testing structures

The MIM capacitor fabrication on glass process strictly followed the process flow that has been shown in Figure 3.32. The bottom electrode was embedded into the ABF GY-11

dielectric film, and it was designed to be 8 μm thick. After surface planarization, the bottom electrode on M2 metal layer had an average surface roughness of 21.6 nm. The thinfilm Si_3N_4 was deposited with a thickness of 180 nm (1800 Å), and the top electrode was deposited to achieve a thickness of 200 nm. The fabricated MIM capacitor is pictured in Figure 3.35 (a). Probe testing with an LCR meter was used. The measured D_k and D_f were 7 and 0.001 respectively at a few MHz frequencies. The PECVD Si_3N_4 deposition at 170 °C deposition temperature on copper, with Ti barrier layer, is thus shown to yield a low loss tangent.

A photosensitive dry-film dielectric, TOK IF, was laminated onto the substrate and photo-imageable blind vias were formed directly onto the top electrode and onto M2 layer pad, which was connected to the bottom electrode. Since both electrodes were accessible using through-vias, two GSG ports were introduced to M1 layer, each connected to an electrode. A fabricated MIM capacitor and its testing structure are shown in Figure 3.35. The utilization of photo-sensitive dry film as the second build-up layer avoided the laser ablation method for via making, which could potentially damage the sputtered ultra-thin top electrode and thinfilms.

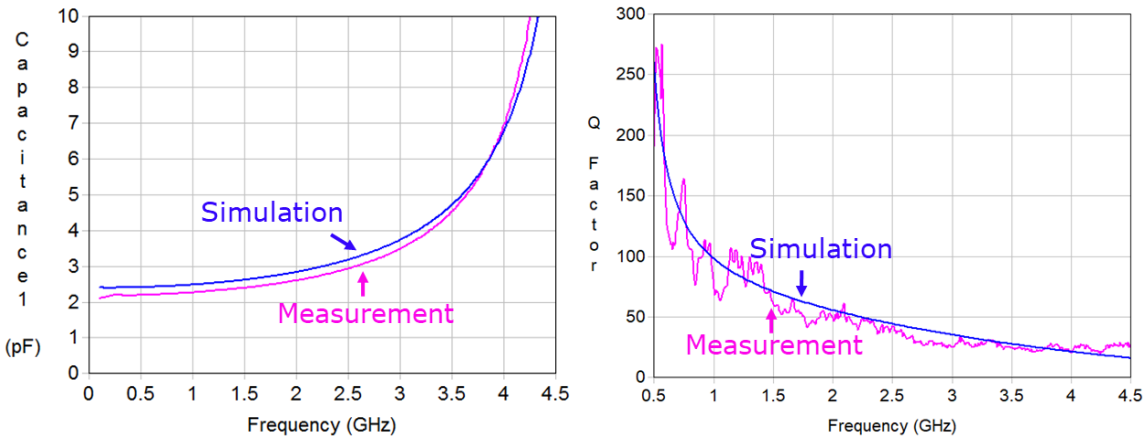
(a) (b)

Figure 3.35. (a) A MIM capacitor, and (b) its testing structure on glass.

Wafer probe testing was performed on a VNA to obtain the Y-parameters. The performance metrics of a capacitor could be extracted as a function of Y_{11} by Equation (3.6).

$$C = \frac{1}{w\, Im(1/Y_{11})}$$
$$Q = mag\{\frac{Im(1/Y_{11})}{Re(1/Y_{11})}\} \tag{3.6}$$

Both D_k and D_f were extracted by a curving-fitting approach. The measured capacitance and Q factor curves were plotted first, and frequency-dependent material properties of thinfilm Si_3N_4 in the EM model were then modified so that the simulation correlates with the measurement results. The curve fitting results on capacitance and Q factor are plotted in Figure 3.36.



(a) (b)

Figure 3.36. Curve fitting results of (a) capacitance frequency response, and (b) Q factor frequency response.

Given the film thickness, the capacitance was primarily dependent on D_k. By setting D_k = 7 in the EM model, a capacitance curve with the best fit was obtained. The

extraction of D_f was based on the Q factor. Given the best Q factor curve fitting result, estimated D_f was below 0.005 under 3 GHz, and gradually rose to 0.01 at 4.5 GHz.

The extraction of D_k and D_f provides design guidelines for MIM capacitors with PECVD Si_3N_4. The demonstrated thinfilm capacitors could achieve a high Q factor as much as 100 at 1 GHz and 50 at 2 GHz. With 200 nm thick Si_3N_4, more than 250 pF/mm^2 capacitance density could be achieved.

The proposed processes for MIM capacitor embedding in glass substrates offers several manufacturing and performance advantages such as: 1) minimal process steps for high throughput, 2) precise capacitor patterning by advanced zero-undercut thinfilm subtractive etching and PECVD thinfilm Si_3N_4, 3) compatibility with low-cost organic film passive manufacturing processes so that heterogeneous technology integration is enabled, and 4) high-Q factor and high-density capacitors for miniaturized high-performance RF designs.

3.2.2 Design of High-performance 3D IPD Diplexers

Circuit-level Design

Similar to the organic thinfilm diplexer design, 3rd order elliptic-function filters were selected for both LBF and HBF. Several design innovations were implemented to improve the diplexer design, including the consideration of Q factors of each component and improvement of impedance matching of filters' passbands.

LPF Design for LBF

The transmission zero of the LPF was moved from 1.5 GHz in previous design to 2 GHz, right inside the high-frequency passband. This was performed to improve the signal rejection of the LPF when high-band signals were received so that the insertion loss of

high-band signals could be reduced. Based on 20 dB minimum out-of-band signal rejection requirement, a π-section LPF was designed. To improve the circuit model accuracy, Q factors were assigned to each lumped LC elements. Consistent with the results achieved with high-Q solenoid inductors and thinfilm capacitors, Q factors of 60 and 100 were assigned to inductors and capacitors respectively. The circuit model was then optimized in ADS and shown in Figure 3.37.

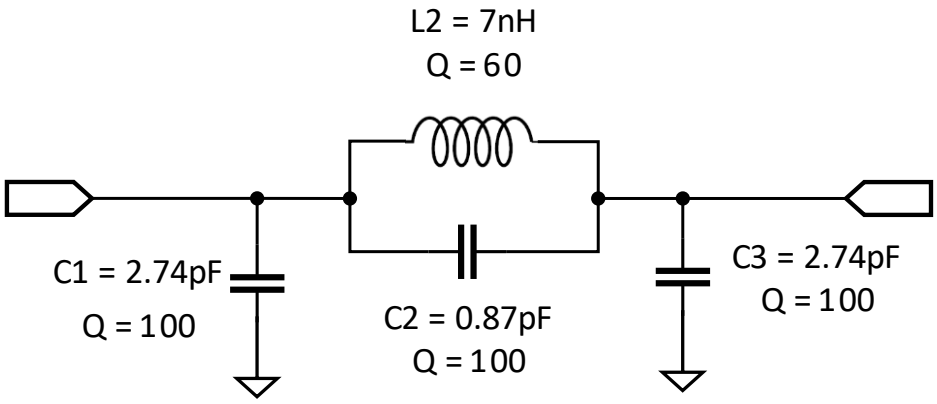


Figure 3.37. Circuit model of re-designed 3rd order elliptic-function LPF with Q factor assignment.

Circuit-level simulation results of the designed LBF were plotted in Figure 3.38. In its 700 MHz – 960MHz passband, a maximum insertion loss of 0.21 dB, and a minimum return loss of 16.6 dB were obtained. In addition, a transmission zero was successfully moved to HBF's passband at 2.05 GHz and the out-of-band signal rejection was more than 20 dB.

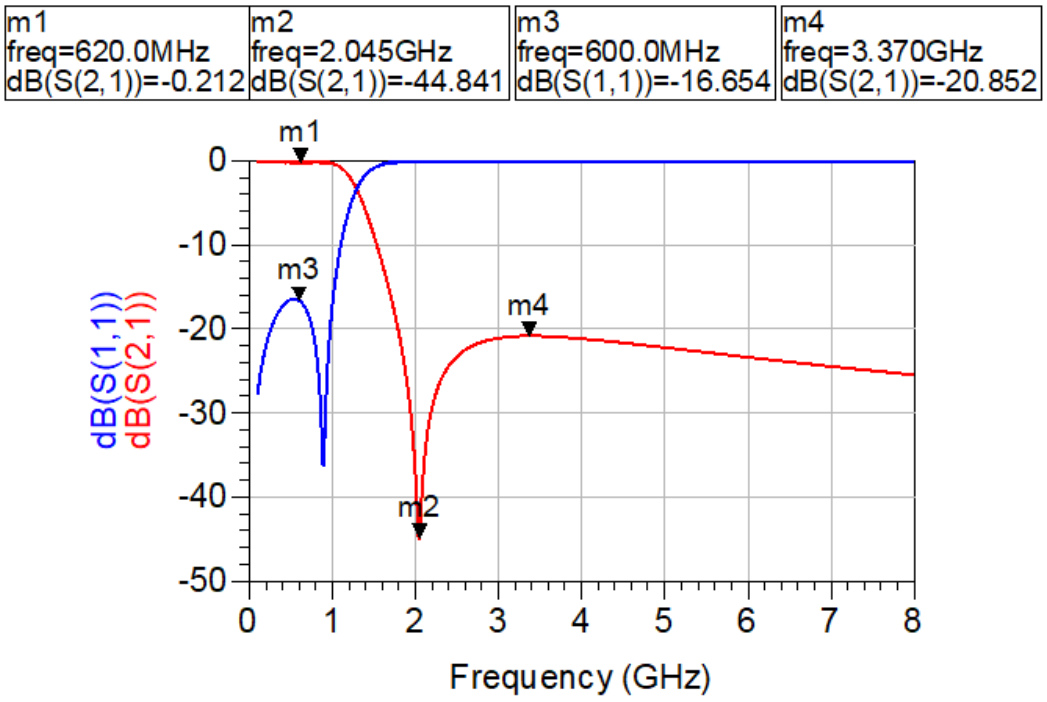
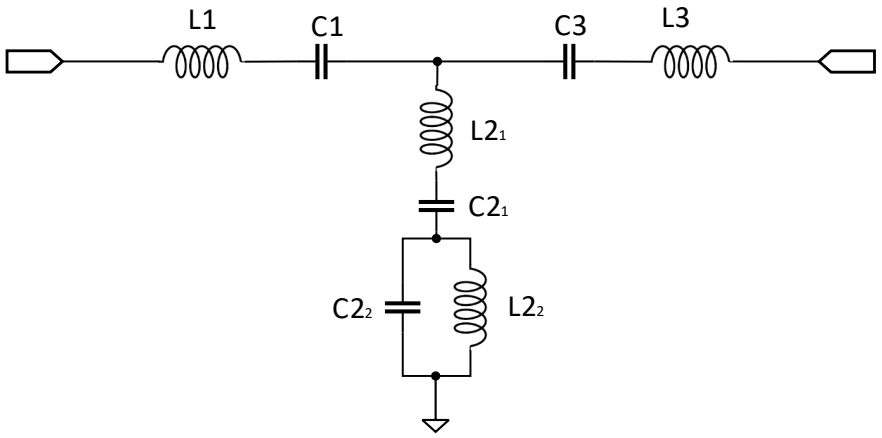


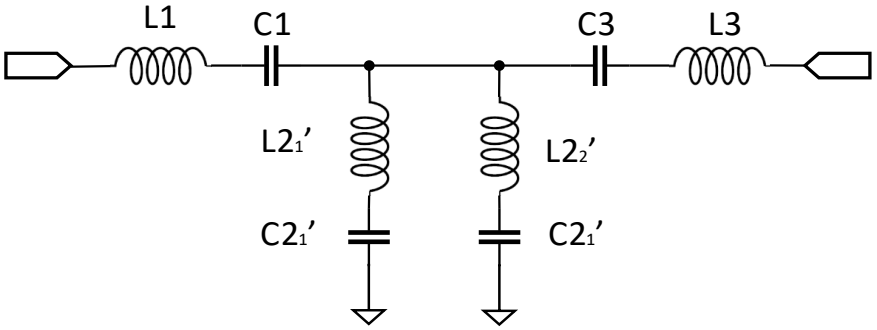
Figure 3.38. Circuit-level simulation results of re-designed LPF.

BPF Design for HBF

A 3rd order elliptic BPF was designed based on a T-section LPF prototype, which offered more than 20 dB out-of-band rejection and more than 15 dB return loss. The LPF was than transformed into a BPF, following the same procedures from the previous BPF design, which have been elaborated in detail. This resulted in a BPF schematic diagram as has been shown in Figure 3.39 (a), however, it is not convenient for practical implementation. Since the physical dimensions of ultra-high-density thinfilm capacitors are very small when compared to inductors, their parallel placement would require long interconnections, which are not preferable for both parasitic loss and space saving. Hence, $C2_2$ and $L2_2$ in parallel should be avoided. The circuit model was transformed into its equivalent form in Figure 3.39 (b), following equations (3.7) [50].



(a)



(b)

Figure 3.39. BPF circuit model transformation from (a) to (b) for easy practical implementation.

$$
\begin{gathered}
a = L2_1 L2_2 C2_1 C2_2 \, , b = L2_1 C2_1 + L2_2 C2_2 + L2_1 C2_2 \\
c = L2_1 C2_1 C2_2 \, , d = C2_2 \, , e = \frac{b + \sqrt{b^2 - 4a}}{2} \\
L2_1' = \frac{a(a - e^2)}{e(ad - ce)} \, , C2_1' = \frac{ad - ce}{a - e^2} \\
L2_2' = \frac{a - e^2}{c - de} \, , C2_2' = \frac{e(c - de)}{a - e^2}
\end{gathered}
\tag{3.7}
$$

The shunt branch in the original design with $L2_1$, $C2_1$, $L2_2$, and $C2_2$ was replaced by two parallel shunt branches. Each of these branches had an inductor and a capacitor in

series, and transmission zeros were located exactly at the LC resonant frequencies. The Q factors of inductors and capacitors were then assigned as 90 and 50 respectively, consistent with the previous analysis. The circuit model was then simulated and optimized in ADS, with the resultant LC values recorded in Table 3.7.

Table 3.7. Documentation of LC values in the designed BPF

Filter type	Capacitance (pF)		Inductance (nH)	
BPF	C1	1.00	L1	5.50
	$C2_1$'	3.00	$L2_1$'	6.05
	$C2_2$'	0.95	$L2_2$'	1.70
	C3	1.00	L3	5.50

Circuit-level simulation results of the designed BPF are presented in Figure 3.40. It had a maximum insertion loss of 1.00 dB, minimum return loss of 17.4 dB and minimum out-of-band rejection of 23 dB.

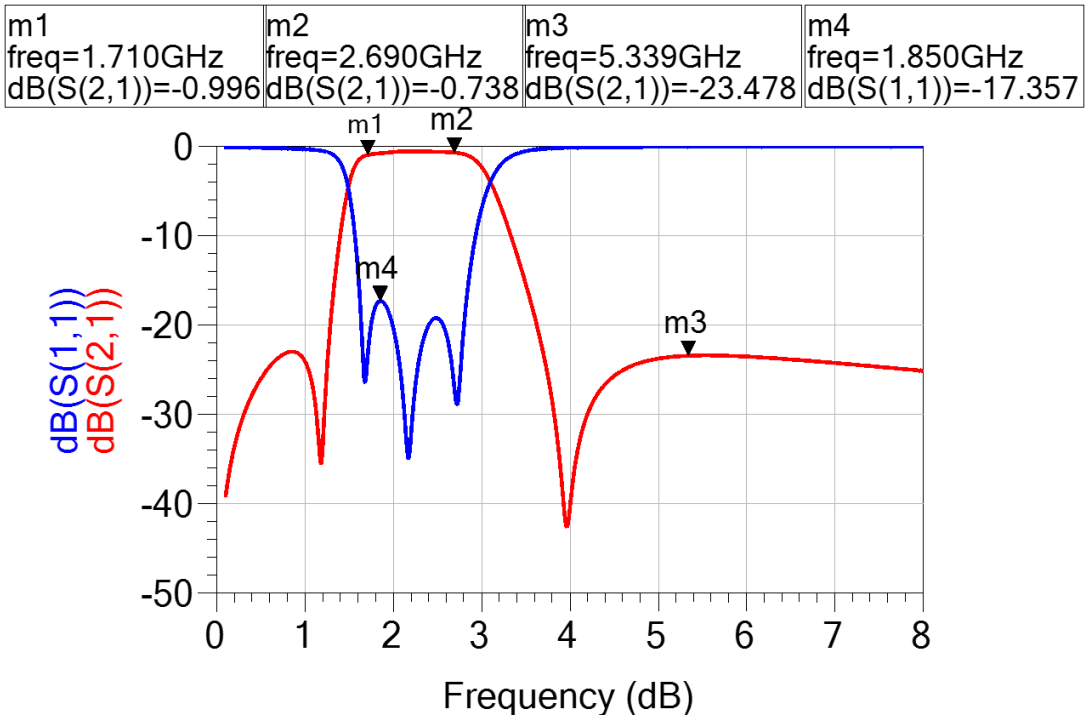


Figure 3.40. Circuit-level simulation results of re-designed BPF.

Diplexer Design

When the designed LBF and HBF were connected to share one common port, impedance matching is required to minimize the signal reflection in filters' passbands. A series inductor L_{L0} was added in front of capacitor C_{L1} in the LBF and a shunt capacitor C_{H0} was introduced right after the inductor L_{H1} in the HBF. The "L" shape impedance matching network is seen from the common port in both low and high bands, as shown in Figure 3.41. The values of C_{L1} and C_{H0} were to be modified along with the additional LC components, so that the input admittance of LBF and HBF were conjugated at the corresponding bands.

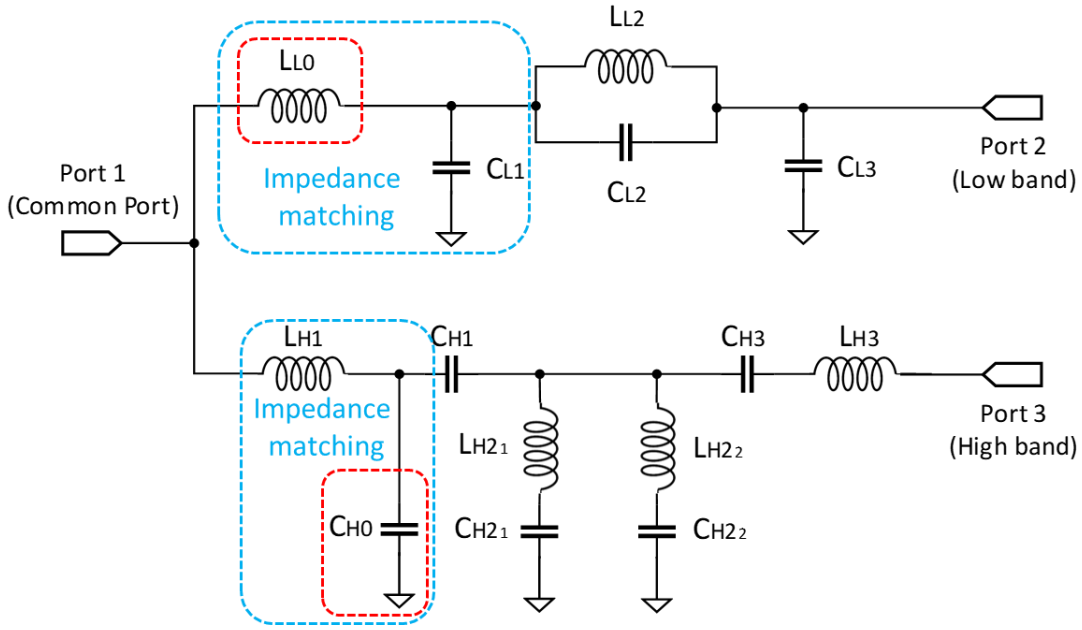


Figure 3.41. Circuit model of the re-designed diplexer.

The diplexer comprises of six inductors and eight capacitors as its essential building blocks. After assigning Q factors to each LC components, design optimization was carried out in ADS for best performance. The optimized LC values are documented in Table 3.8.

Table 3.8. Optimized LC values in re-designed diplexer

	Capacitance (pF)		Inductance (nH)	
Low Band	C_{L1}	4.00	L_{L0}	8.50
	C_{L2}	1.00	L_{L2}	7.00
	C_{L3}	1.70		
High Band	C_{H0}	0.10		
	C_{H1}	1.00	L_{H1}	4.00
	C_{H2_1}	3.00	L_{H2_1}	6.05
	C_{H2_2}	0.95	L_{H2_2}	1.70
	C_{H3}	1.00	L_{H3}	6.00

The port 1 impedance is plotted on a Smith Chart as shown in Figure 3.42. Good impedance matching was achieved in both the low-frequency and high-frequency passbands, with the magnitude of normalized input impedance close to 1. Therefore, return loss was improved.

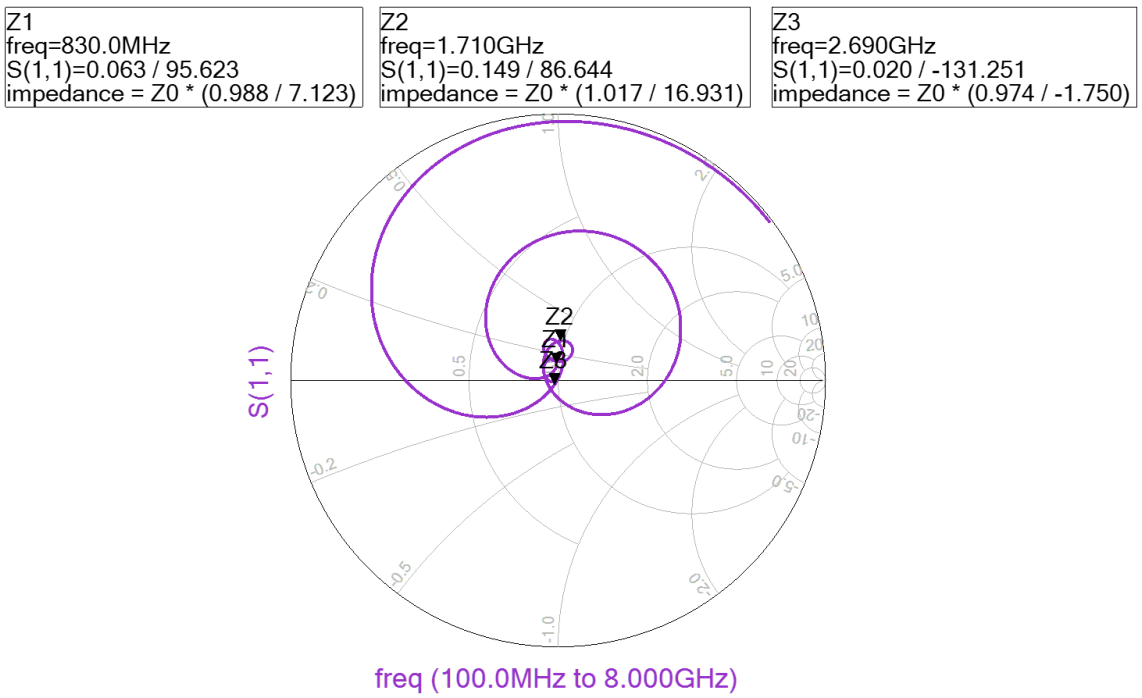


Figure 3.42. Port 1 impedance plot on a Smith Chart.

The frequency response of the new diplexer design is plotted in Figure 3.43.

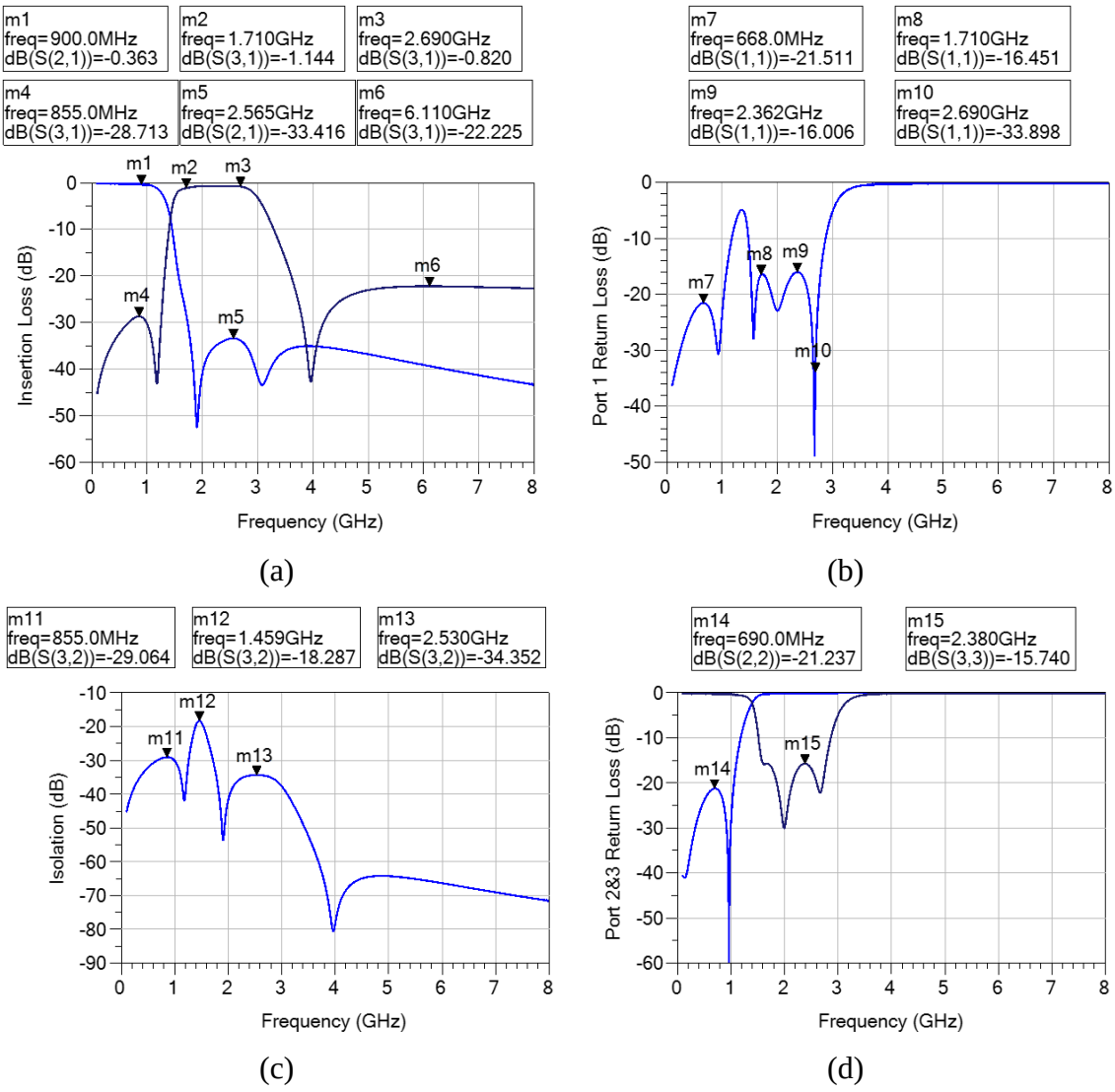


Figure 3.43. Circuit-level simulation results of diplexer transmission characteristics: (a) low-band and high-band IL, (b) Port 1 RL, (c) isolation, and (d) Port 2&3 RL.

A maximum passband insertion loss of 0.36 dB and 1.14 dB were simulated in low-band and high-band respectively. Return loss was improved to be more than 15 dB for all the three ports. Low- to high- band isolation was maintained to be more than 18 dB for all frequencies and better than 29 dB in the diplexer's passbands.

EM Modeling of Re-designed 3D IPDs

Based on previous high-Q inductor design and demonstration of MIM capacitors, an innovative substrate architecture that could integrate and maximize the advantages of both component technologies were proposed. The substrate stack-up is illustrated in Figure 3.44, and its details are documented in Table 3.9.

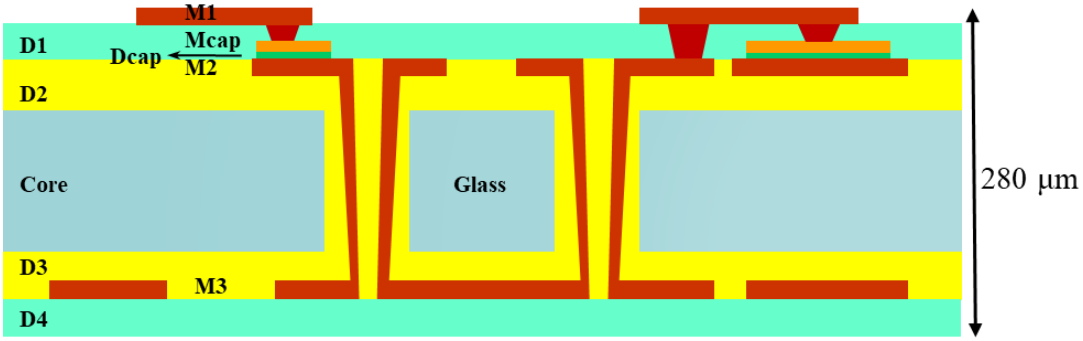


Figure 3.44. Proposed substrate stack-up for re-designed 3D IPDs.

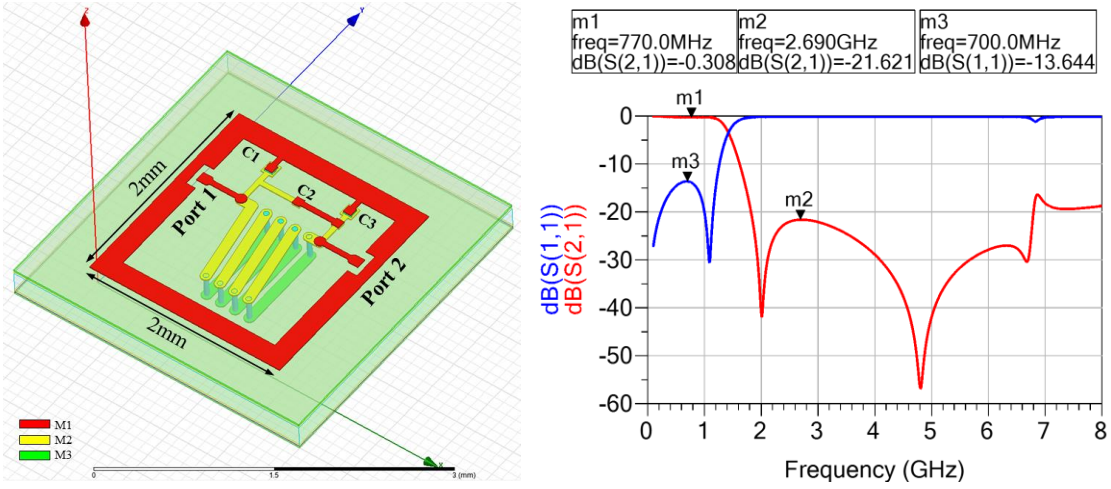
Table 3.9. Optimized LC values for the new diplexer design

Layer	Material	ε_r	tanδ	Thickness	Technology
M1	Cu	-	-	10 µm	Sputtering - SAP
D1	TOK IF	3.5	0.03	10 µm	Photosensitive dry film
Mcap	Cu	-	-	0.2 µm	Sputtering
Dcap	Si_3N_4	7	0.003 @ 0.5 GHz 0.012 @ 4.5 GHz	0.2 µm	PECVD
M2	Cu	-	-	10 µm	Electroless - SAP
D3	GY-11	3.2	0.004	25 µm	Dry-film polymer
Core	Glass	5.5	0.005	200 µm	Asahi glass
D3	GY-11	3.2	0.004	25 µm	Dry-film polymer
M2	Cu	-	-	10 µm	Electroless - SAP
D4	TOK IF	3.5	0.03	10 µm	Photosensitive dry film

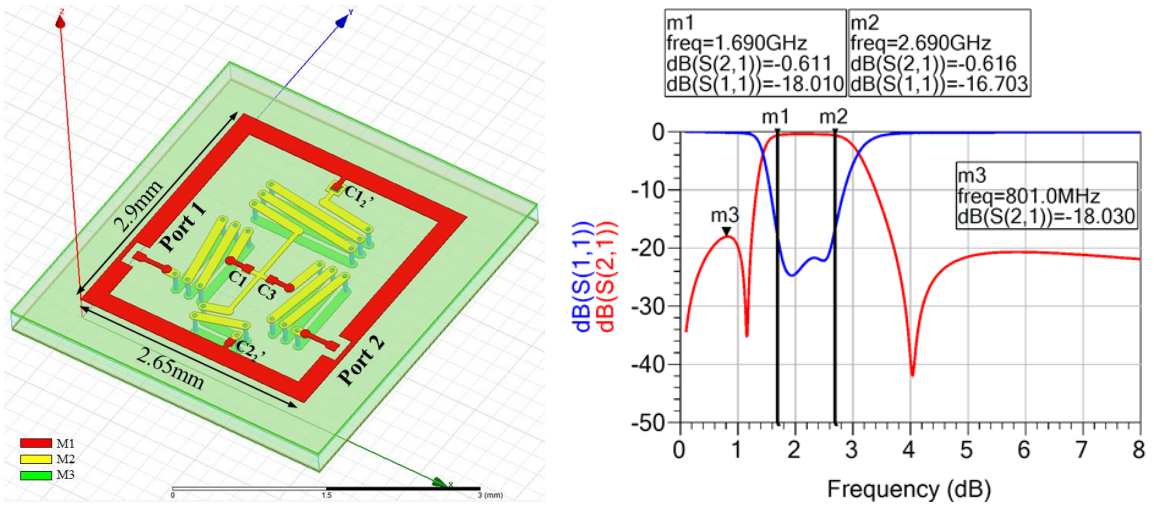
Both sides of the glass substrate are used for passives embedding. Metal layer M2 and M3, as well as TGVs were employed for high-Q inductor designs. Thinfilm capacitors are embedded into the build-up dielectric layers on the top side of the substrate. Since the

bottom electrodes of capacitors are designed on metal layer M2, capacitors can be built directly onto the inductors so that their interconnection losses are minimized, especially in an LC series circuit. The thickness of M2 layer is also flexible and can be well-controlled by surface planarization. In addition, the access to capacitors' top electrodes as well as the inductors can be realized on the M1 layer through photo-imaged and metalized blind vias. Hence, both high-Q inductors and thinfilm capacitors are integrated onto the glass substrates with the proposed approach, leveraging the advances from both design and manufacturing aspects.

With the proposed substrate stack-up, high-Q inductors were designed with 60 μm - diameter and 150 μm - pitch TGVs, and MIM capacitors were designed using 200 nm thick Si_3N_4 as the dielectric. Following these, re-designed LPF and BPF were modeled and simulated in the 3D full-wave EM solver HFSS. Their substrate layouts and simulation results are presented in Figure 3.45. The lateral dimensions of the LPF, BPF and diplexer were 2 mm × 2 mm and 2.65 mm × 2.9 mm respectively, including the GSG probe pads, feedlines, and ground frame.



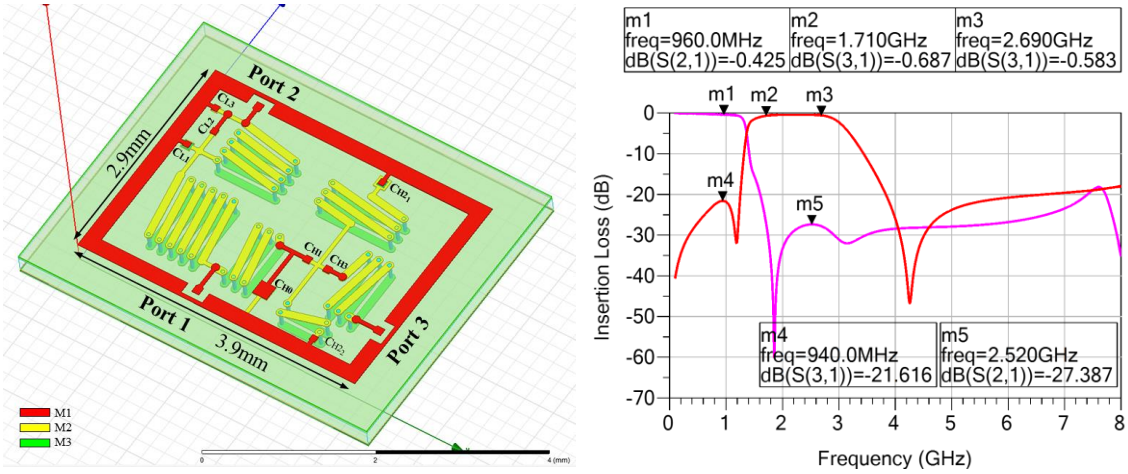
(a)



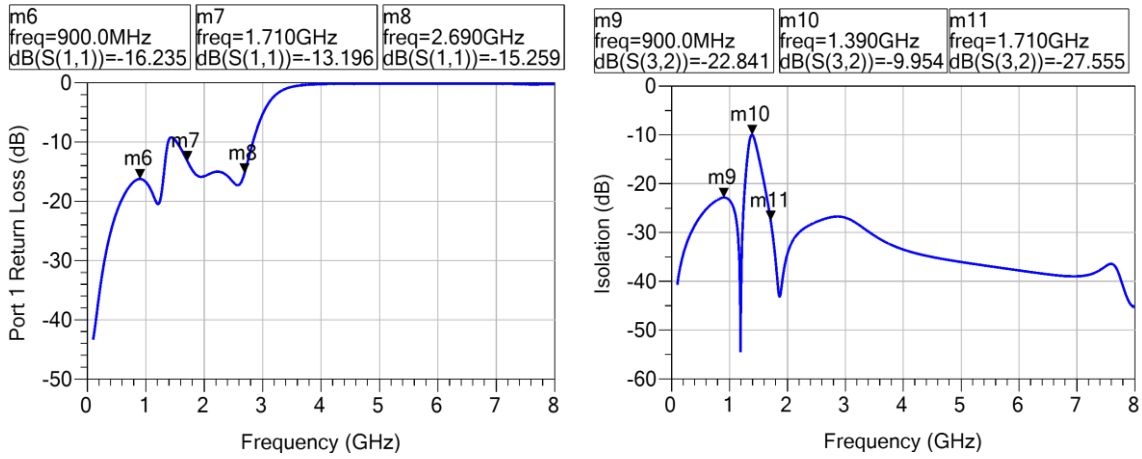
(b)

Figure 3.45. EM model and simulation results of re-designed (a) LPF, and (b) BPF.

In the diplexer layout, since capacitor C_{H0} has the smallest capacitance of 0.1 pF, it is difficult to pattern it with good tolerance if designed as thinfilm type. Instead, this capacitor employs the 10 μm thick photosensitive build-up film as its dielectric layer. The diplexer's 3D model and EM simulation results are presented in Figure 3.46. The diplexer is 2.9 mm × 3.9 mm in size, including testing structures.



(a) (b)



(c) (d)

Figure 3.46. EM model and simulation results of re-designed diplexers: (a) layout; (b) low-band and high-band insertion loss; (c) Port 1 RL and (d) Isolation.

The simulated performance metrics of the re-designed 3D IPD diplexer with high-Q thinfilms on glass are summarized in Table 3.10.

Table 3.10. Simulated performance metrics of re-designed 3D IPD diplexer

	Specification	Frequency (MHz)	Magnitude (dB)
Low Band	Insertion loss	700 - 960	0.43
	Return loss	700 - 960	16
	Rejection	1500 -1700	15
	Rejection	1710 - 2690	27
	Isolation	1710 - 2690	27
High Band	Insertion loss	1710 - 2690	0.69
	Return loss	1710 - 2690	13
	Rejection	700 - 960	22
	Rejection	4000 - 6000	26
	Isolation	700 - 960	23

Good electrical performance was achieved with the re-designed 3D IPD diplexer with high-Q thinfilm passives on glass. It has low insertion loss in both low- and high-frequency passbands and high selectivity.

3.2.3 Summary

A high-performance 3D IPD diplexer was designed with the integration of high-Q inductors and thinfilm MIM capacitors on glass substrates. Key performance and size attributes of the designed diplexer are summarized in Table 3.11.

Table 3.11. Accomplishment of redesigned high-performance 3D IPD diplexer

Topic	Metrics	Objectives	Accomplishment
3D IPD Diplexers	Performance	• IL < 0.6 dB • RL > 15 dB • Isolation > 20 dB	• IL - < 0.43 dB @ LB - < 0.69 dB @ HB • RL - > 16 dB @ LB - > 13 dB @ HB • Isolation - > 23 dB @ LB - > 27 dB @ HB
	Miniaturization	• Z < 0.3 mm • X-Y < 2 mm × 2.5 mm	• Z = 0.28 mm • X-Y = 2.9 mm × 3.9 mm

High-Q solenoid inductors based on TGVs were designed on 200 μm thick glass. A Q factor of 90 was achieved at 2 GHz and the inductance density was more than 5 nH/mm^2. A low-cost MIM capacitor fabrication process was developed on glass substrates with PECVD thinfilm Si_3N_4, featuring less than 5% thickness uniformity. These LC components integration yielded a re-designed 3D IPD diplexer, showing significant improvement in its electrical performance. Since the diplexer size is dominated by the inductors, further miniaturization could possibly be achieved using fine-pitch and high-aspect-ratio TGVs.

CHAPTER 4

DESIGN AND DEMONSTRATION OF 3D IPAC LTE MODULES

RF front-end modules typically include active devices such as PAs, LNAs, and RF switches, and passive components such as filters and diplexers. In addition to these devices, several other passive components are needed to provide actual system functionalities and also improve the performance. Some of these components have been widely used to implement impedance matching functions in between system components that are at different impedance levels. Other components such as decoupling capacitors are widely used in power distribution networks to mitigate the power integrity issues caused by the simultaneous switching noise (SSN). These additional passive elements always outnumber those active components by many times. In today's MCM RF modules, these add-on passives are primarily implemented as SMT-type LTCC lumped components and are assembled side-by-side with other discrete components onto substrates or PCBs. Therefore, the package footprint is increased, and the resultant long interconnections through substrates generate additional losses. To address these issues, advanced thin-film passive components and their integration with actives to form high-density modules are required.

The objectives of this research task are to design and demonstrate RF FEMs with high-Q substrate-embedded thinfilm impedance matching network circuits and double-side integration of discrete components using the 3D IPAC concept. The modules are designed to achieve significant improvement in the passband insertion loss of LTE filters, less than 200 μm substrate thickness, and miniaturized package footprint, while also providing integrated shielding functions.

This chapter firstly focuses on the process demonstration of miniaturized 3D glass packages utilizing 100 μm thick glass. Miniaturized impedance matching networks design and process development of double-side assembly are discussed in detail. Secondly, the evolution of 3D RF modules towards higher performance and smaller thickness is presented, with both design innovations in high-Q inductors, component-level shielding, as well as process advances in handling 50 μm ultra-thin glass.

4.1 Small-size 3D LTE Modules on 100 μm Thin Glass

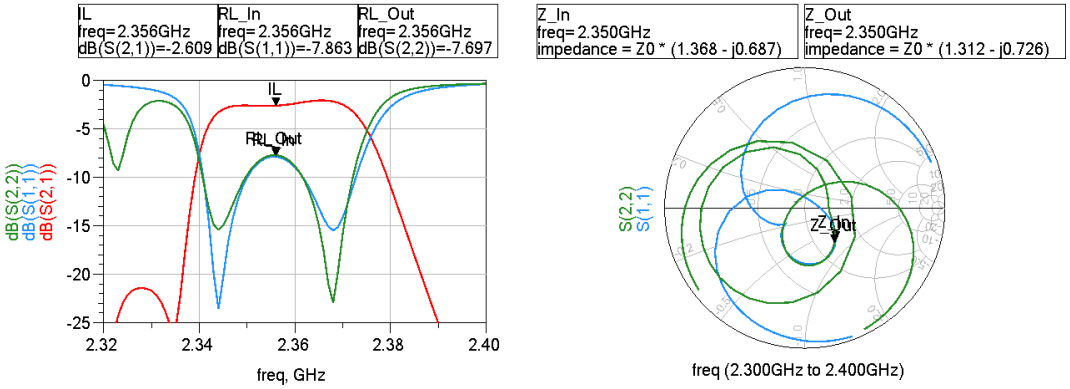
Narrowband filters are essential building blocks of FEMs to address the need for carrier aggregation in advanced 4G-LTE. These narrow band filters are typically acoustic wave devices due to their unparalleled superiority in band selectivity that other filter technologies fail to offer. Therefore, two types of commercial acoustic wave devices from TDK-EPCOS, a SAW filter and a BAW filter, are selected. They are designated for LTE mobile telephones in Band 30 and Band 41B respectively, and are packaged for surface mount technology (SMT) with their terminals bumped with BGAs. To validate the proposed 3D RF module concept and study the performance of glass substrate-embedded impedance matching networks, these two filters are to be flip-chip bonded onto either sides of the glass substrates, and their impedance matching networks are embedded into the substrates, directly underneath the footprint of each filter.

4.1.1 Design of 3D LTE Modules

Circuit-level Design

The S-parameters of both tested stand-alone SAW and BAW filters were provided by the suppliers. Each filter had one input port, one output port and four other ports for

ground. The circuit-model of both filters were built in ADS and 50 Ω termination was used on all the signal ports. The simulated frequency-dependent characteristics, such as passband insertion loss, input and output port return loss and port impedance of both filters are sketched in Figure 4.1 below.



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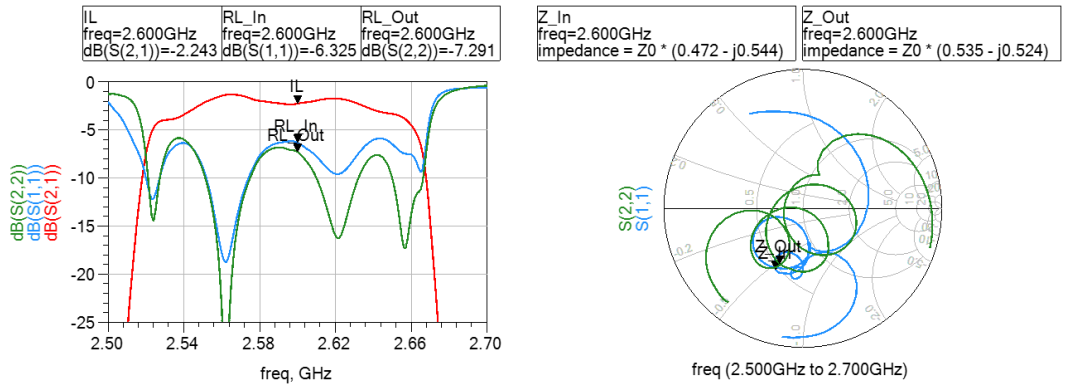
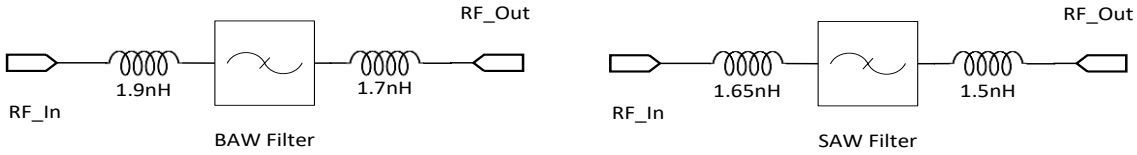


(b)

Figure 4.1. Stand-alone frequency response of (a) a BAW filter and (b) a SAW filter.

It was observed that both filters had a narrow 3 dB bandwidth less than 100 MHz. The center frequency of the BAW and SAW filter was 2.356 GHz and 2.6 GHz, respectively. However, the poor return loss observed on both filters indicated an impedance mismatch between the filters' signal ports and the 50 Ω termination. The port impedance was detailed in the Smith Chart, and both input and output ports on each filter were shown to

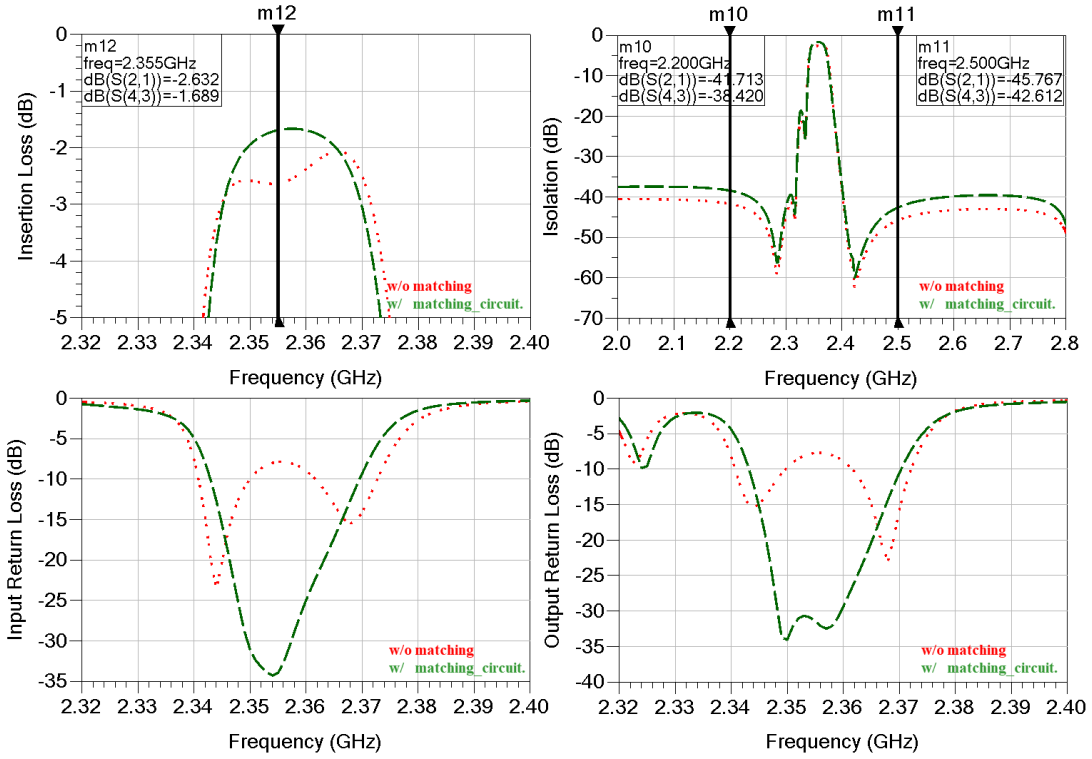
be capacitive, as revealed by the negative imaginary parts of the impedance values. Hence, the impedance mismatch could be simply mitigated by introducing a series inductor at each signal port. The schematic diagrams of designed impedance matching networks for both BAW and SAW filters are illustrated in Figure 4.2, with the calculated inductance.



(a) (b)

Figure 4.2. Schematic diagrams of designed impedance matching networks for (a) a BAW filters, and (b) a SAW filter.

With the designed impedance matching networks, circuit-level simulation results of both filters are presented in Figure 4.3.



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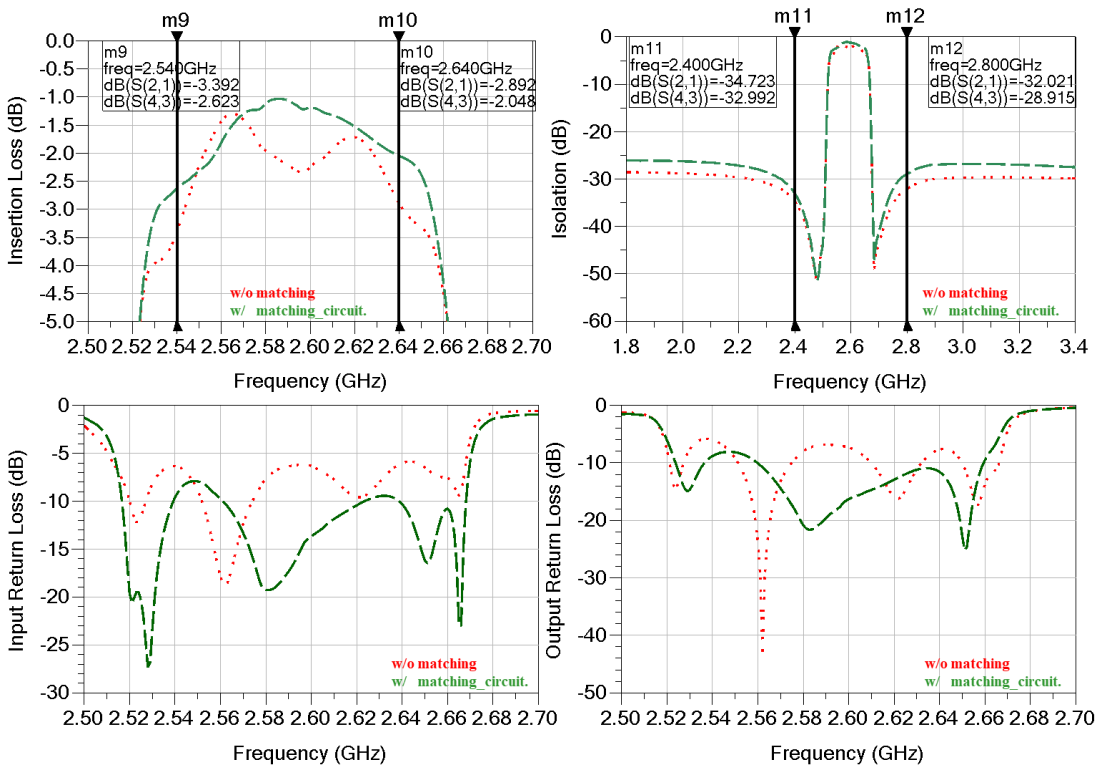


(b)

Figure 4.3. Circuit-level simulation results of (a) BAW filter w/ and w/o impedance matching networks, and (b) SAW filter w/ and w/o impedance matching networks.

Frequency responses of simulated filters' performance were compared to stand-alone filters' transmission characteristics. The impact of impedance matching networks was manifested as improved passband return loss and minimized insertion loss of both SAW and BAW filters.

3D Package Design and Modeling

The RF module modelling and design flow is shown in Figure 4.4.

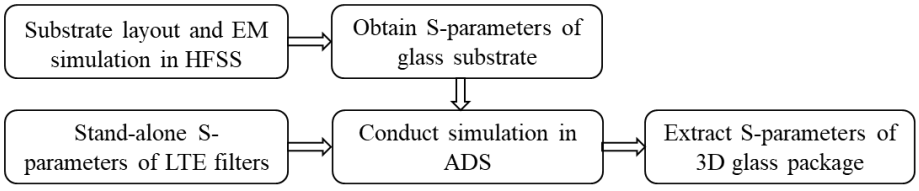
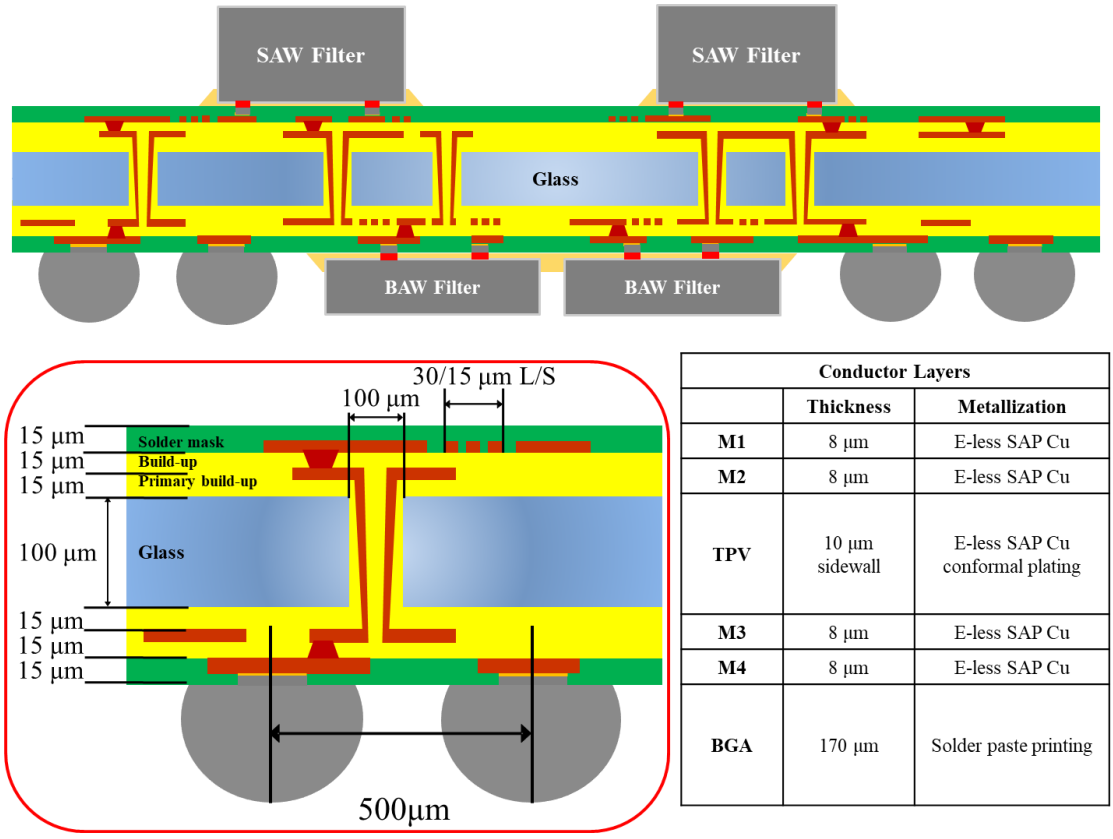


Figure 4.4. Module design and simulation flow.

To create the substrate EM model, a 3D glass package architecture was proposed and is presented in Figure 4.5.



Conductor Layers		
	Thickness	**Metallization**
M1	8 µm	E-less SAP Cu
M2	8 µm	E-less SAP Cu
TPV	10 µm sidewall	E-less SAP Cu conformal plating
M3	8 µm	E-less SAP Cu
M4	8 µm	E-less SAP Cu
BGA	170 µm	Solder paste printing

Figure 4.5. Proposed 3D glass package design and substrate design rules.

The glass substrate consists of 100 µm thick Corning glass as core material and four metal layers of semi-additive patterned copper with electroless seed-layers. GY-11 organic dry films were used as build-up dielectrics because of their low dielectric loss (0.0042 @ 5.8 GHz) and smooth surface. Low dielectric loss is critical for high-performance RF designs. Also, the average roughness of the film after the desmear process is maintained below 30 nm, which enables fine-line patterning with precision and reduces the signal loss at high frequencies due to skin effects. Another notable attribute of this film is the low water absorption, which is essential for substrate reliability.

Two SAW filters were integrated onto the top side of the substrates, while two BAW filters, which are shorter in thickness, were placed on the back side. For compactness of RF modules, the impedance matching networks, which were implemented as inductors in this design, were embedded into substrate build-up layers directly underneath the filters. Since these inductors were directly connected to the solder bumps of the filters' terminals, the shortest interconnection lengths were achieved with minimum loss. The BGAs on the backside of the glass packages were designed at a pitch of 500 μm. The overall 3D package was 3.8 mm × 4.6mm in lateral dimensions and 0.7 mm in thickness, including the 200 μm thick substrates, filters and BGAs.

The glass substrate and design layout were modelled in HFSS and the substrate EM model is captured in Figure 4.6, where BGAs are concealed.

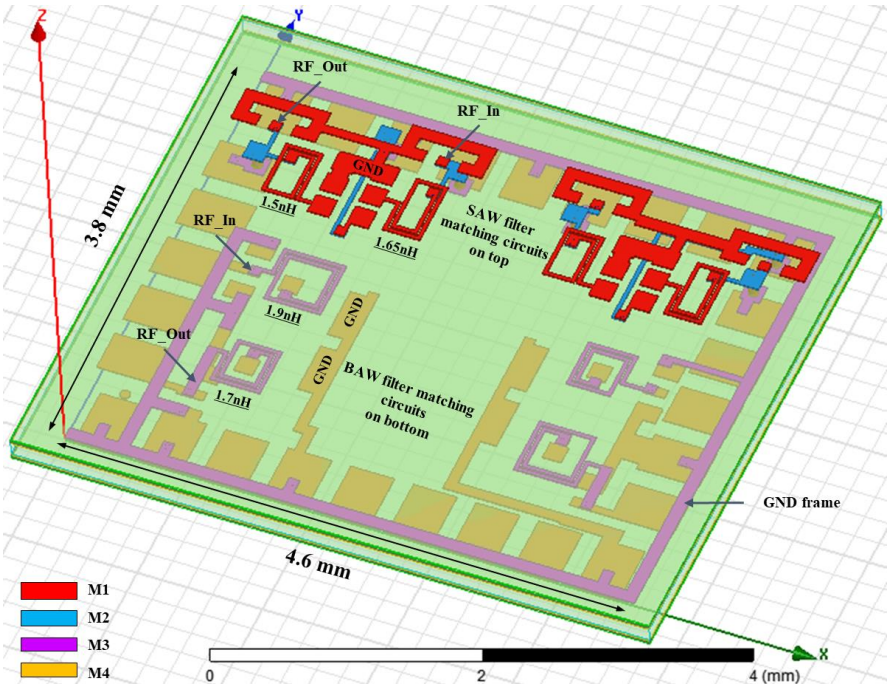


Figure 4.6. EM model of designed 3D glass package substrate.

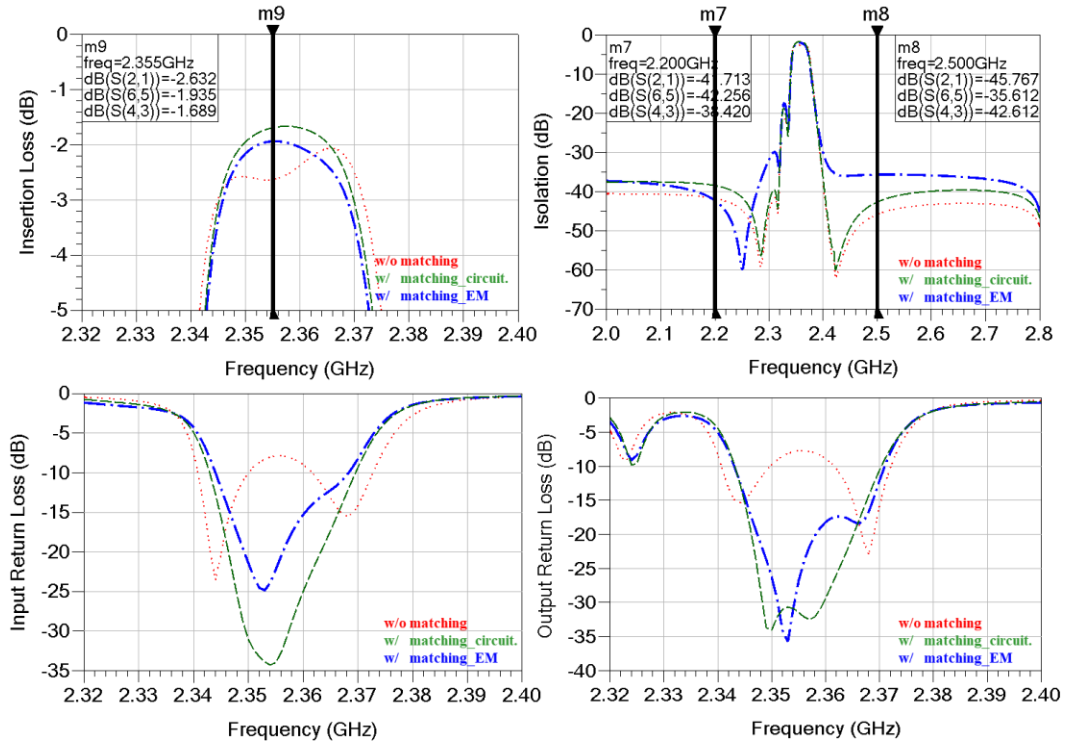
The spiral inductors of 1.5 nH, 1.65 nH, 1.7 nH and 1.9 nH were first designed and modeled in HFSS. Trade-offs between Q factor, SRF, compact size and processability of

thinfilm lamination were made, hence inductors were designed with a minimum linewidth / space of 30 μm / 15 μm and 8 μm thickness with a maximum number of two turns. These compact spiral inductors had inductance densities from 7 nH / mm^2 to 11.5 nH/mm^2 and Q factors between 35 to 40 in LTE bands. They were connected directly to the landing pads of the filter terminals.

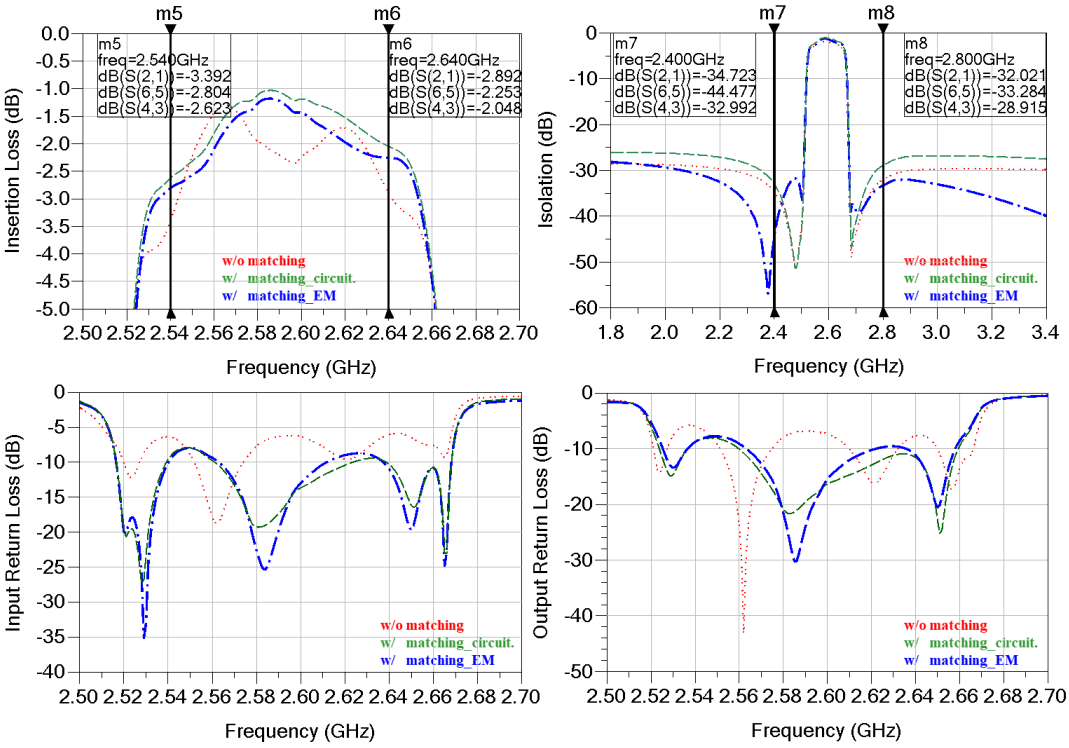
GSG pads were connected to each impedance matching network on the surface metal layers of both top and back sides of the substrate. Hence, the performance of SAW and BAW filters were testable independently at the surfaces of the substrate by probe testing. In addition, TGVs with 100 μm diameter interconnected the topside SAW filters to BGAs, and backside BAW filters were also interconnected to BGAs through M3 and M4 layers, providing board-level testability if the 3D glass package is bonded to a PCB.

With high-density 3D components integration on ultra-thin substrates, the EM radiation could degrade the system performance by generating unwanted cross-talk between components that are in physical proximity. Referring to the SAW filters' matching circuits on top side of the substrates, ground pads of the filters were located in between the two matching network inductors to minimize the electric field coupling. To address the isolation between topside and backside components, superposition of the top and bottom impedance matching circuits was avoided.

Full-wave EM simulation was conducted on the substrate model, and the obtained S-parameters of designed impedance matching networks were imported into ADS and simulated together with the filters. Resultant filter performance metrics were compared to both circuit-level simulation and stand-alone filters' response as reference. These results are shown in Figure 4.7.



(a)



(b)

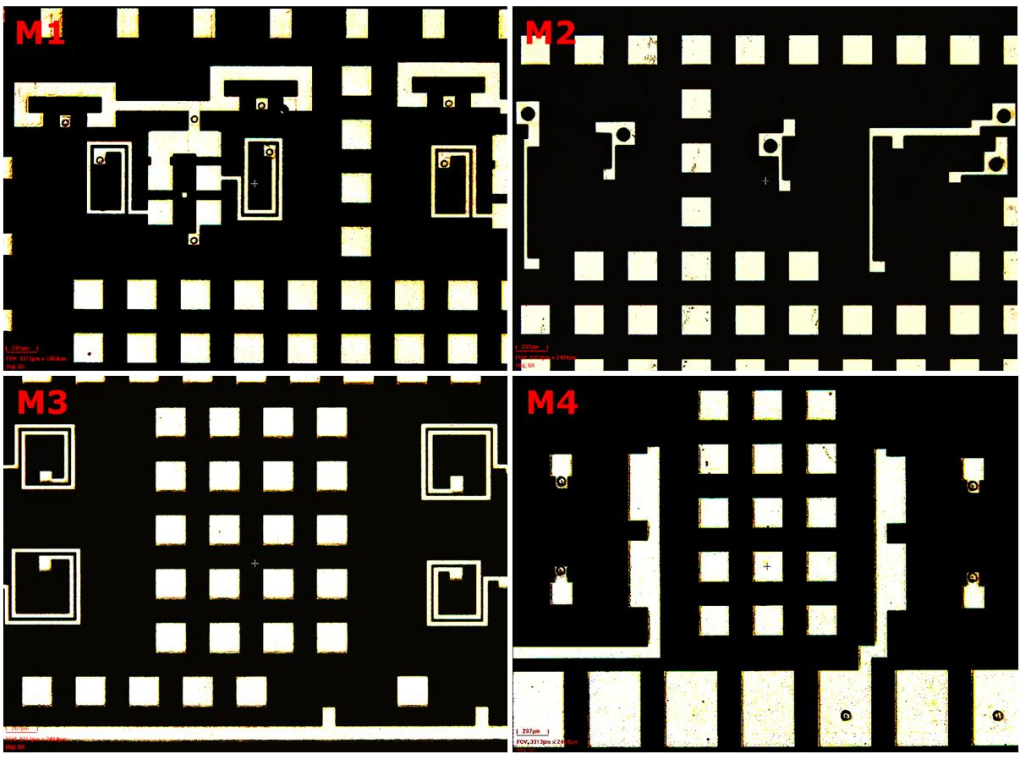
Figure 4.7. EM simulation results of substrate-embedded impedance matching networks for (a) a BAW filter, and (b) a SAW filter.

The discrepancy between circuit-level simulation and EM simulation resulted from non-ideal passive components and inevitable parasitic effects in complex 3D layouts. Given these differences, it could still be concluded that, with the substrate-embedded impedance matching networks in ultra-thin 3D glass packages, the maximum passband insertion loss in SAW and BAW filters was reduced by 0.7 dB and 0.6 dB, respectively.

4.1.2 Fabrication and Assembly of 3D Glass Packages

Substrate Fabrication

As the module substrate stack-up was the same as the previously designed 3D IPD diplexers with organic thinfilms on glass, the same substrate process flow described in Figure 3.16 in Chapter 3 was followed. The fabrication results for impedance matching networks in double-side embedded filters are shown in Figure 4.8.



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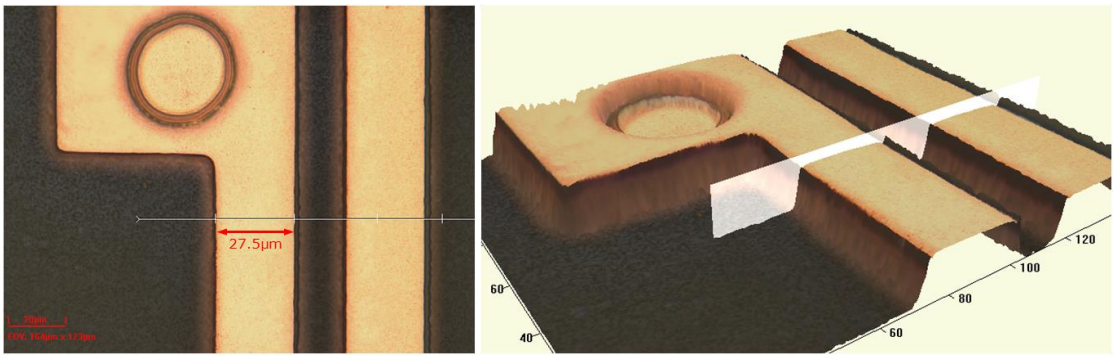


(b)

Figure 4.8. Electroless SAP metallization results of fabricated module substrates: (a) overview of M1-M4 layers, and (b) a spiral inductor imaged by 3D microcopy.

To improve the copper electroplating uniformity and reduce the glass substrate warpage from imbalanced copper structures on both sides, isolated square-shaped dummy patterns were included, filling the open area on each metal layer. During seed-layer removal by isotropic wet etching process, the copper trace suffered sidewall etching to varying degrees. The top surface of copper traces was etched more than the bottom, resulting in a trapezoid shaped cross section. Metrology of the fabricated substrates showed that the copper trace had a smallest width of 27.5 µm on its top, which corresponded to a 2.5 µm reduction compared to the design.

Double-side Assembly

To enable high-volume manufacturability, panel-scale assembly processes were proposed and developed using standard manufacturing infrastructure for laminate substrates. Figure 4.9 below shows the proposed process flow of double-side component flip-chip assembly onto glass substrates and 3D glass packages to PCB bonding.

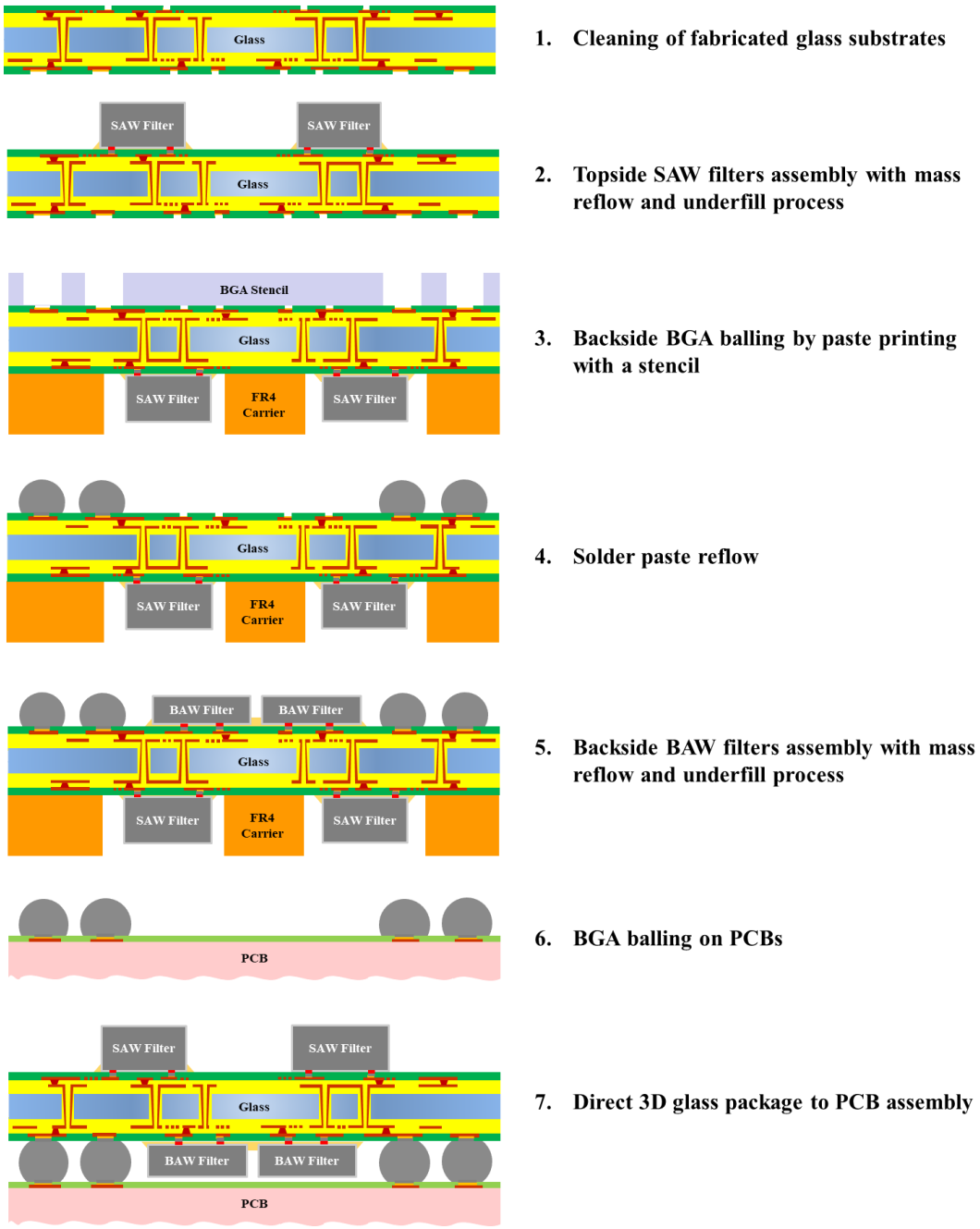
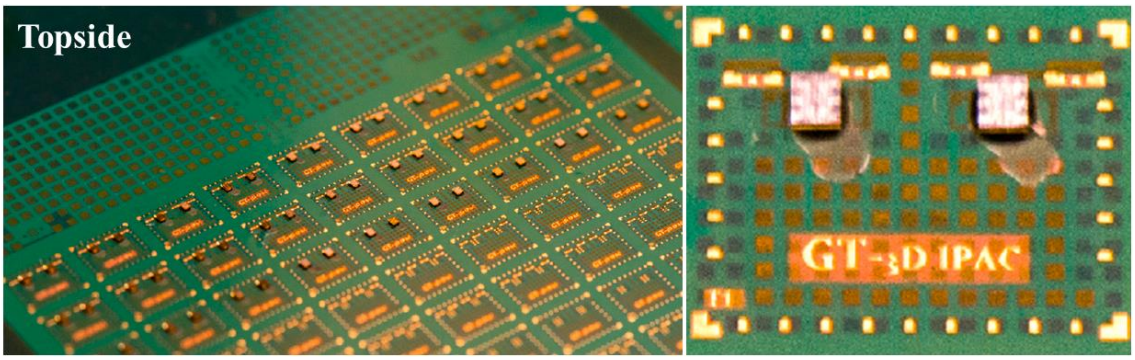


Figure 4.9. Process flow of panel-level double-side component assembly onto glass substrates and 3D glass package to PCB bonding.

SAW filters were first assembled onto the substrates with a flip-chip bonder and mass reflowed at 260°C. The assemblies were then underfilled by manual dispensing, followed by curing at 165°C. The substrates were flipped and placed on a 500 μm thick flat FR4

carrier with drilled cavities to accommodate the SAW filters. BGA balling was performed by solder paste printing through an electroformed nickel stencil. The stencil was designed with a thickness of 5.5 mil (139.7 μm) and opening diameters of 380 μm. It was targeted to achieve a solder ball height of 170 μm for 235 μm diameter BGA opening size in the solder mask. A screen printer was used to print the standard SAC105 solder paste. Solder reflow conditions used ramp-to-spike profiles and set the peak temperature suitably higher than the melting point of solder [51]. A five-zone reflow oven was used for the reflow process and good wetting and uniformity of solder balls were achieved. Following this, the BAW filters were assembled onto the backside of the glass substrates, reflowed and applied with capillary underfill. The FR4 carrier was finally released after the completion of first-level assembly process. The demonstrated 3D glass packages on 6-inch panel are pictured in Figure 4.10.



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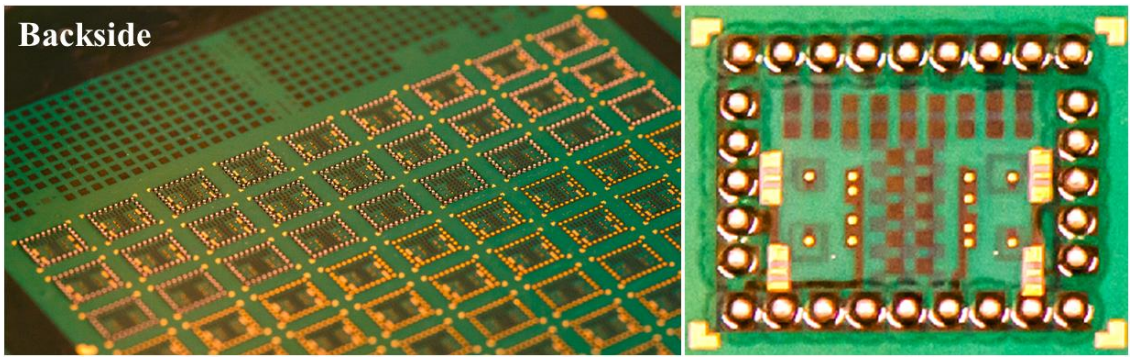

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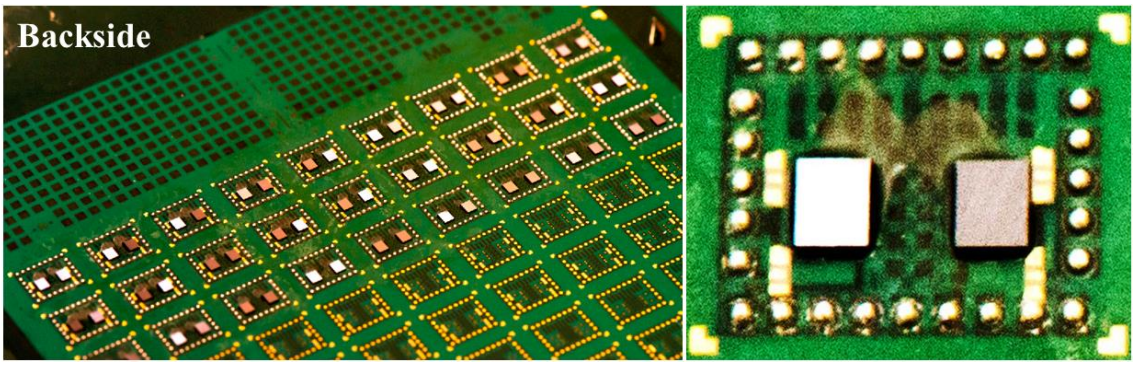


(c)

Figure 4.10. Panel-level process results of double-side assembled 3D glass packages: (a) assembly of SAW filters on the topside of substrates, (b) BGA balling by paste printing, and (c) assembly of BAW filters on the backside of substrates.

The silicon-like low CTE and high modulus attributes of glass prevented significant warpage and retained substrate flatness after each assembly process. Consequently, high yield of 3D double-side assembly was achieved on the thin glass substrates. The paste-printed BGA balls were 164 μm tall as shown in Figure 4.11, smaller than the total thickness of the given BAW filters. To ensure successful assembly of glass packages to PCB without damaging the components, BGA balling was also applied to the BGA landing pads on PCB side to compensate for the shortage in solder height. This increased the complexity of the board-level assembly and could be avoided if thinner components were available.

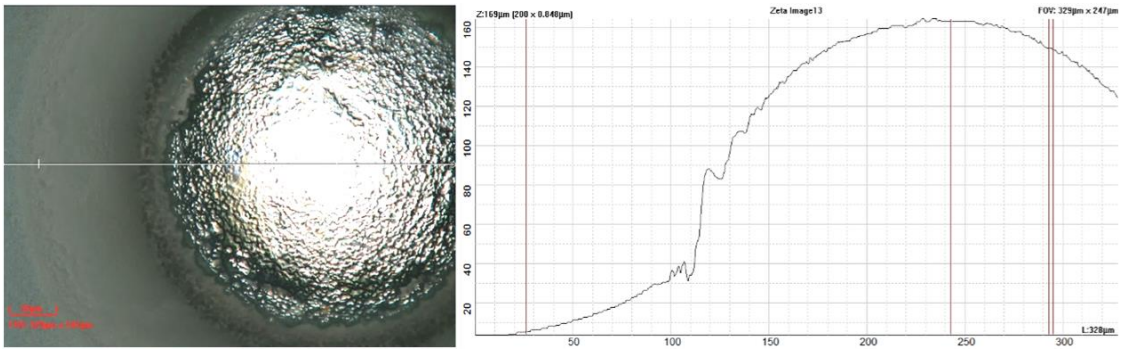
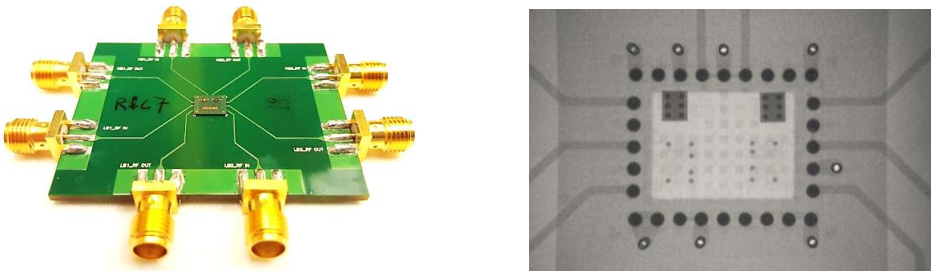


Figure 4.11. Measured profile of a paste-printed BGA ball after reflow.

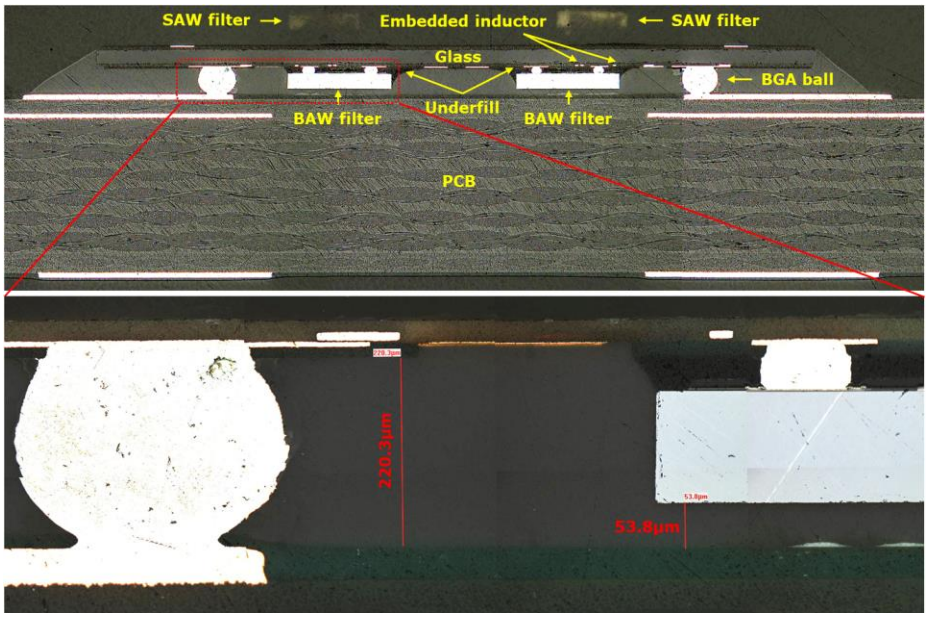
The 3D glass packages were mechanically diced, edge-coated and assembled onto specifically designed PCBs by solder reflow [52]. A photograph of assembled 3D glass package on a PCB, together with an X-ray image are shown in Figure 4.12. The X-ray image indicated good glass package to PCB assembly, with precise alignment and good solder welting.



(a) (b)

Figure 4.12. (a) A photograph and (b) an X-ray image of a 3D glass package assembled on PCB.

Cross-sections were also made to check the yield of both first-level the second-level assembly and the results are presented in Figure 4.13.



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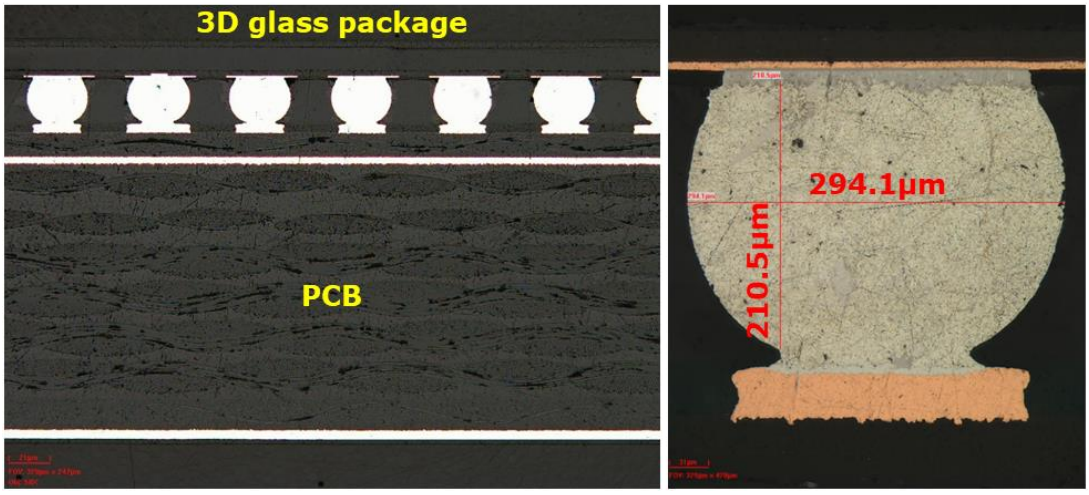


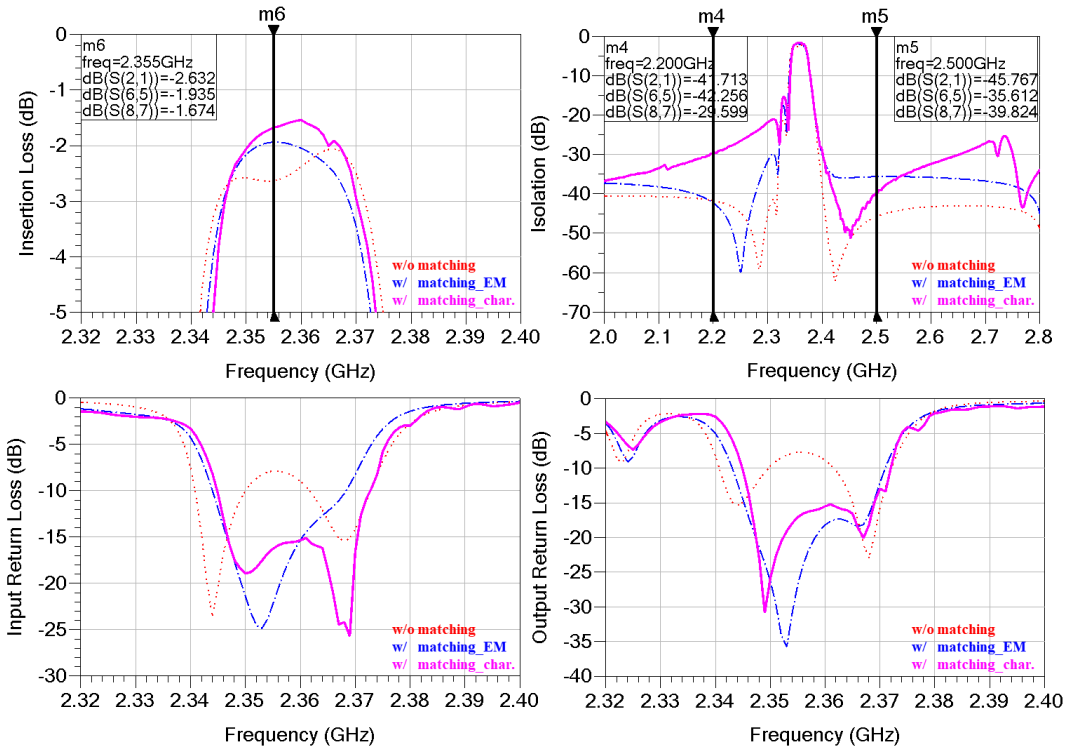
(b)

Figure 4.13. Cross-sectional views of (a) a 3D glass package assembled on a PCB, and (b) reflowed 500 µm pitch BGAs.

Optical inspection of the demonstrated samples indicated successful double-side chip-level assembly of filters onto the glass substrates and board-level assembly of 3D glass packages onto boards. The height of solder balls was 210 µm after reflow, which sufficiently avoided any physical contact between backside of BAW filters and the PCB during assembly. The flatness of the 3D glass packages was also maintained after board-level assembly without significant warpage.

4.1.3 Characterization of 3D LTE Modules

The performance of LTE filters with substrate-embedded impedance matching networks was characterized with a VNA. The measured results of two LTE filters with their corresponding impedance matching networks were compared with EM simulation results and stand-alone filters without impedance matching networks. These results are plotted in Figure 4.14.



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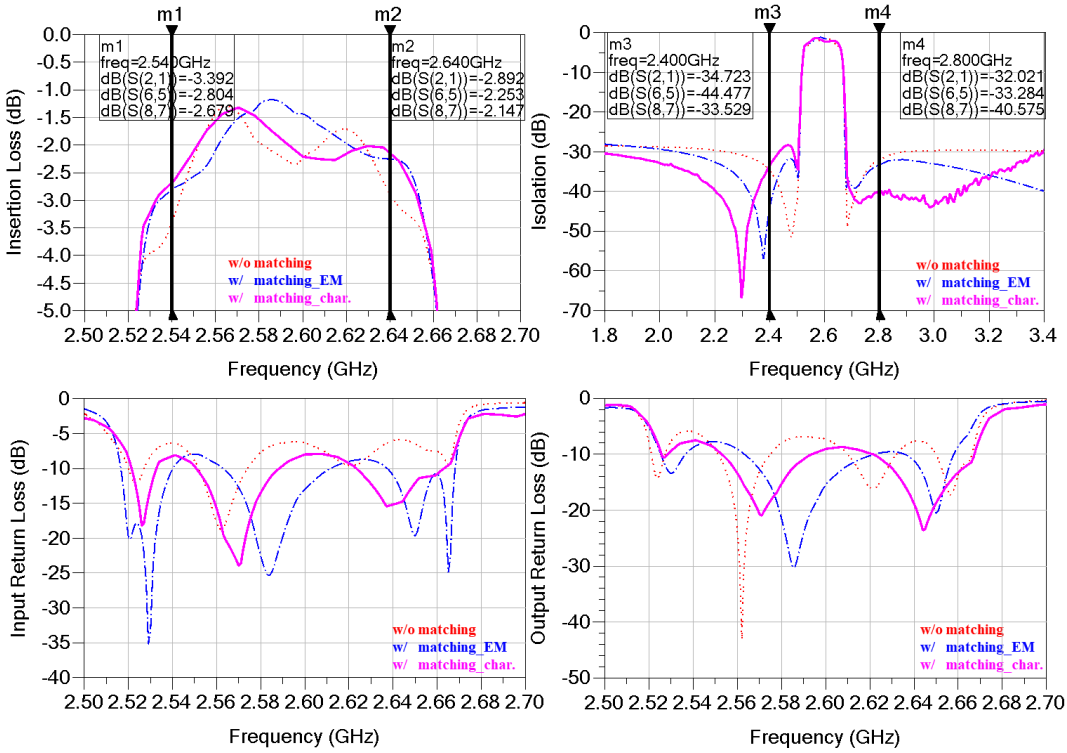


(b)

Figure 4.14. Measured performance of (a) a BAW filter w/ impedance matching network, and (b) a SAW filter w/ impedance matching network.

Passband insertion loss of BAW filters showed good correlation with EM simulation results. As much as 0.96 dB reduction in insertion loss was observed near the center frequency, resulted from the good impedance match at the input and output terminals of filters. However, the isolation to out-of-band signals was degraded compared to the filters' inherent characteristics when the impedance matching networks were not utilized. As for SAW filters, the overall signal transmission efficiency in the passband was improved, particularly at frequencies close to the lower and upper cut-off boundaries.

The discrepancies between simulation and measurement results were due to the process-induced parasitic effects that were not captured in the models. During ultra-thin glass substrate processing, the thickness non-uniformity of thinfilm dielectrics could bring in additional impedance variation and electromagnetic coupling from layer to layer. The variations in metallization process also altered the inductance and quality factor of embedded passives with small feature sizes. Further process optimization was required to improve the predictability of EM models for ultra-thin 3D glass package design.

Another challenge faced by this design was the degradation of filters' selectivity, particularly for BAW filters whose out-of-band signal rejection deteriorated with the presence of unshielded embedded impedance matching networks. The crosstalk between two inductors produced unwanted capacitance coupling as well as mutual inductance, since they were close to each other in the layout. For designing highly-integrated RF FEMs with the proposed 3D glass package approach, electromagnetic compatibility (EMC) failure from proximity between system components is the next critical challenge. To address this, innovative floor planning of signal and ground paths and integration of substrate-embedded EMI shields are required for further performance improvements.

4.1.4 Summary

The very first RF modules in 3D glass packages were successfully designed, fabricated and characterized. Major accomplishments of demonstrated 3D LTE modules are summarized in Table 4.1.

Table 4.1. Accomplishments of demonstrated 3D IPAC LTE modules

Topic	Metrics	Objectives	Accomplishments
3D IPAC Modules	Performance	• IL < 2 dB • RL > 14 dB • Q > 60	• IL = 1.67 dB (BAW filter) • RL = 19.3 dB (BAW filter) • Q < 40
	Miniaturization	• Substrate thickness Z < 100 μm	• Z = 0.2 mm

The primary goal of this work is to prove the feasibility and manufacturability of proposed 3D IPAC RF module concept on glass substrates. To achieve this, low-cost panel-scale processes of 3D glass packages, including ultra-thin substrates fabrication, first- and second-level assembly by solder mass-reflow, and BGA balling by paste-printing were innovatively developed. The demonstrated 3D glass packages have shown reduced volume and improved discrete filters' passband insertion loss with substrate-embedded impedance matching networks.

Further performance improvement of 3D RF modules could come from the integration of high-Q inductors and EMI shields into the glass substrates and further reduction in the substrate thickness with thinner glass.

4.2 High-performance LTE Modules on 50 μm Ultra-thin Glass

Ultra-thin (50 μm) glass substrates can further extend the performance and miniaturization attributes of 3D packaging technologies. However, this brings in additional design challenges that need to be addressed. In the previously demonstrated 100 μm 3D glass modules, when EMI shields were not introduced to prevent crosstalk suppression, the BAW filters' stopband isolation performance was degraded. Hence, EMI shields at component level are required to be designed and integrated into the system. On the other hand, their introduction brings in additional parasitic loss, which should be compensated by enhancing the Q factor of embedded passives, such as inductors. Taking all these concerns into account, the filter impedance matching networks need to be redesigned and demonstrated on 50 μm ultra-thin glass.

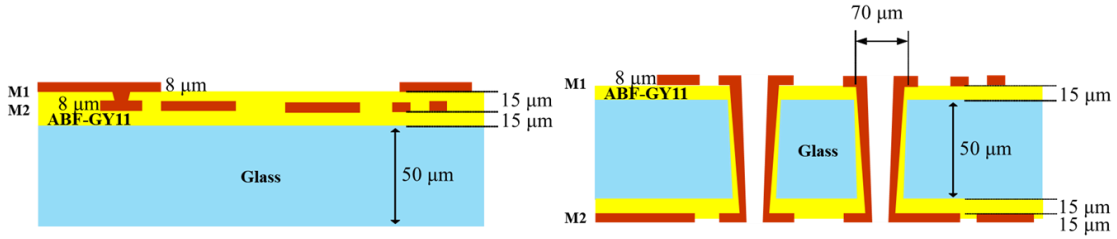
4.2.1 Electrical Design

Design of High-Q Inductors

Inductor Design Topology Selection on 50 μm Ultra-thin Glass

As the substrate becomes thinner, the superiority of 3D lateral solenoid inductors in high Q factors is weakened due to reduced cross-section area of the inductor coils. Therefore, an optimal inductor design topology should be decided. For this purpose, one spiral inductor and one solenoid were designed and simulated, targeting the same inductance of 1.9 nH, and higher than 60 in Q factors at the BAW filter's passband center frequency at 2.35 GHz. To build EM models, two types of two-metal layer substrate stack-up are proposed for each inductor, and are sketched in Figure 4.15. The substrate core material was 50 μm thin Schott AF32 series glass and the build-up layers were 15

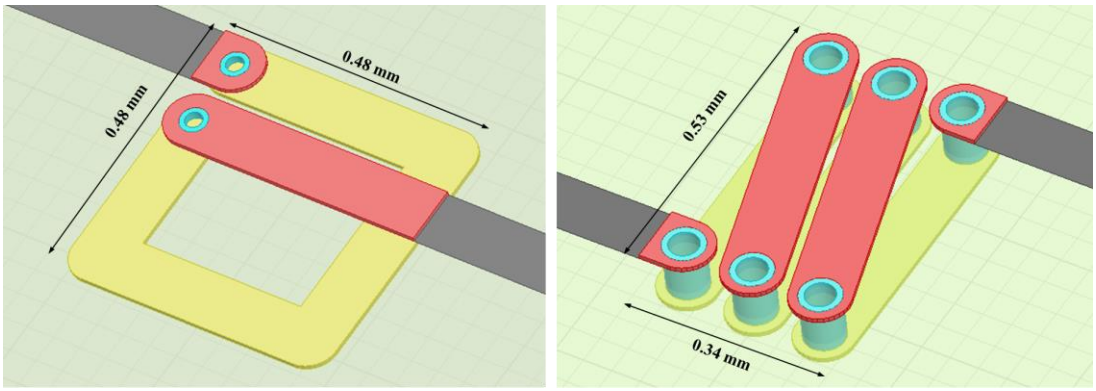
μm thick low-loss ABF GY-11 dry film dielectrics. The TGV diameters in a solenoid inductor design were 70 μm, and could be reduced to as small as 20 μm by laser drilling.



(a) (b)

Figure 4.15. Substrate stack-up for (a) a spiral inductor, and (b) a solenoid inductor.

The linewidth of each inductor physical model was fixed to be 100 μm in both design structures. With all these constraints, the inductors' characteristics were comparable and their design geometries were studied. The EM models of these two inductors in HFSS are presented in Figure 4.16.



(a) (b)

Figure 4.16. EM models of designed (a) spiral inductor, and (b) solenoid inductor.

To maximize the Q factor of a spiral inductor, a square shape single-turn coil was designed with lateral dimensions of 0.48 mm × 0.48 mm. This is also compared with a solenoid inductor with three turns, ending up with lateral dimensions of 0.34 mm × 0.53 mm. The ground reference in both models was placed more than 0.4 mm away from the

inductor to minimize the capacitance coupling. Lumped ports were assigned to each of the inductors' node, allowing the current returning from the ground. With this set up, de-embedded inductor performance metrics were obtained through EM simulations, and the results in inductance and Q factors are presented in Figure 4.17.

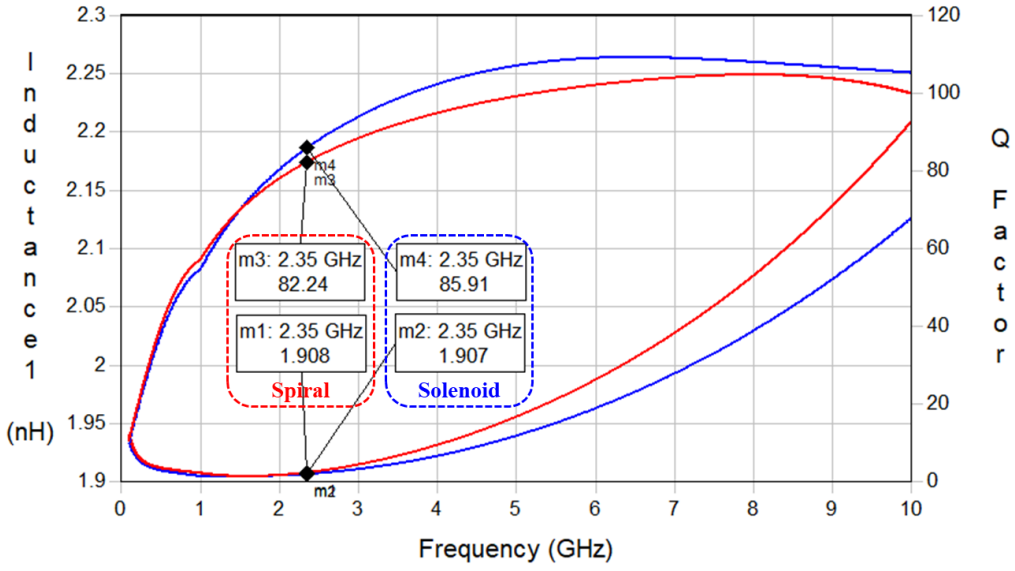


Figure 4.17. EM simulation results of designed (a) spiral inductor, and (b) solenoid inductor.

Both inductors were designed for 1.9 nH at 2.35 GHz, and the Q factor for spiral and solenoid inductor was 82 and 86 respectively. In addition, the SRF of both inductors was more than 10 GHz, showing good inductance stability. The inductance density of the solenoid inductor was calculated as 10.6 nH/mm^2, which was higher than the 8.3 nH/mm^2 of the spiral inductor. By comparing both designed inductor design geometries on 50 μm glass, the performance advances of solenoid inductors were not substantial. However, solenoid inductors are still good candidates to be integrated in a RF module because 1) their inductance density can be improved by reducing the size and pitch of TGVs; 2) they provide more possibilities for EMI shields design; and 3) the conductor distribution was

uniform on both sides of glass, which is critical for warpage control during ultra-thin glass substrates manufacturing. Therefore, solenoid inductors were chosen as the primary high-Q inductor design topology in the current substrate-embedded impedance matching networks design.

Design of Solenoid Inductors on 50 μm Ultra-Thin Glass

As has been discussed in Chapter 3, the Q factor of an inductor highly correlates with its inductance, resistance and operation frequency. The improvement of Q factor could be theoretically achieved by increasing the inductance or reducing the resistance. The enhancement of inductance on a given inductor structure could be accomplished by introducing magnetic materials whose relative permeability is larger than 1. However, the existing magnetic materials only work in the KHz or MHz frequency range, and are not suitable for 4G-LTE applications. On the other hand, the suppression of conductor loss is more flexible and practical.

The skin effect issue manifests as the operation frequency increases, and the resultant skin-depth reduces the effective cross-sectional area of the conductor. At 2 GHz, the skin-depth of copper is smaller than 1.5 μm, indicating that most of the current flows only within the 1.5 μm surface depth. The conductor loss reduction could be implemented by replacing copper with advanced multi-layer conductors or by increasing the cross-sectional area of copper conductors, which include both planar traces and vertical vias. Multilayered conductors showed some promise from published prior works but is not suitable for low-cost and high-throughput manufacturing. An easier practice to reduce the conductor loss at high frequencies is to increase its effective cross-section area by tuning the thickness and linewidth.

Impact of Conductor Thickness on Inductor Q Factor

When the inductors are embedded into thin glass substrates, the conductor thickness is constrained by the thickness of the build-up dielectrics. As the glass becomes thinner, the requirement on the load of build-up layers becomes more stringent. Thinfilm dielectrics are needed to mitigate the stress at the glass to build-up layer interfaces, and therefore the thickness of copper is typically limited to a few microns. In addition, since the conductor thickness is typically much smaller than its lateral dimension as linewidth, the increase of effective cross-section area contributed by increased copper thickness beyond a certain value is very limited.

To quantify the impact of copper thickness variation, the previously designed 1.9 nH solenoid inductor shown in Figure 4.16 (b) was adjusted with copper thickness varying from 2 µm to 16 µm. Resultant inductance and Q factors are plotted in Figure 4.18 below for comparison.

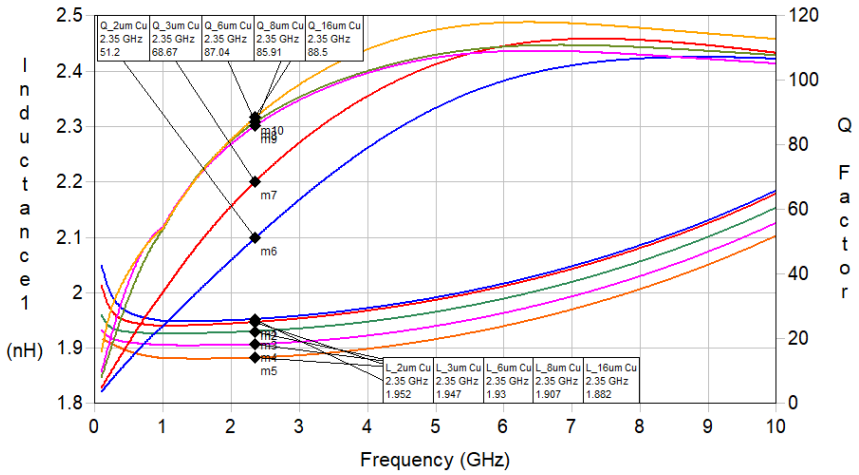


Figure 4.18. Comparison of inductance and Q factors of 1.9 nH solenoid inductors with fixed 100 µm linewidth and varied 2 - 16 µm thick copper.

The increase of copper thickness induced a slight reduction in the inductance. When the copper conductor thickness was smaller than 6 µm, the increase of the copper

thickness showed significant enhancement of inductor Q factors because of apparent augmentation of the effective cross-section area of copper traces. When the thickness of copper was much larger than the skin-depth, the increase of effective cross section area slowed down and the capacitance coupling between two adjacent coil windings dominated. A trade-off analysis between the two counteracting effects, increase in conductance cross-section area and capacitive coupling, indicates that the optimal copper thickness of the designed solenoid inductors was 6 - 8 μm.

Impact of Conductor Linewidth on Inductor Q Factor

The impact of an increase in linewidth on Q factor enhancement was also studied. In contrast to the analysis of copper thickness, the variation of linewidth also altered the inductor's lateral geometry, which also impacts the inductor behavior. To simplify this study, the cross-section of inductor coils (pitch of TGVs in inductor' perpendicular direction), number of turns, via size and minimum spacing between adjacent traces were fixed, while the copper linewidth was doubled from 100 μm to 200 μm, resulting in a dimensional extension in the inductor's longitudinal direction. The results of doubled linewidth were captured in the EM model and are illustrated in Figure 4.19.

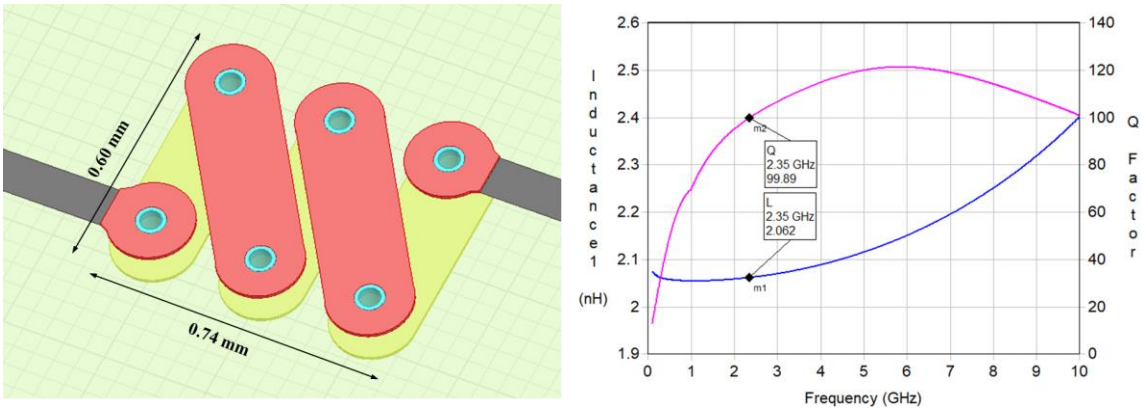
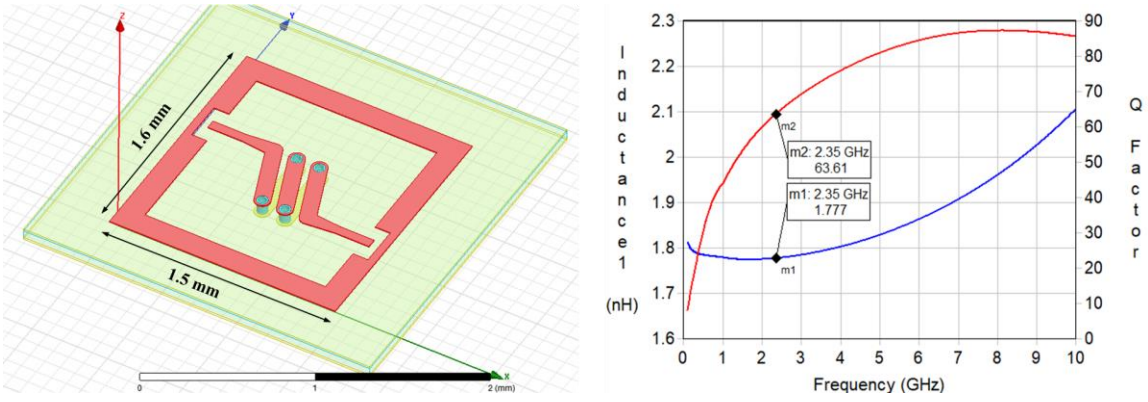


Figure 4.19. Designed solenoid inductor with 200 μm linewidth and 8 μm thick copper.

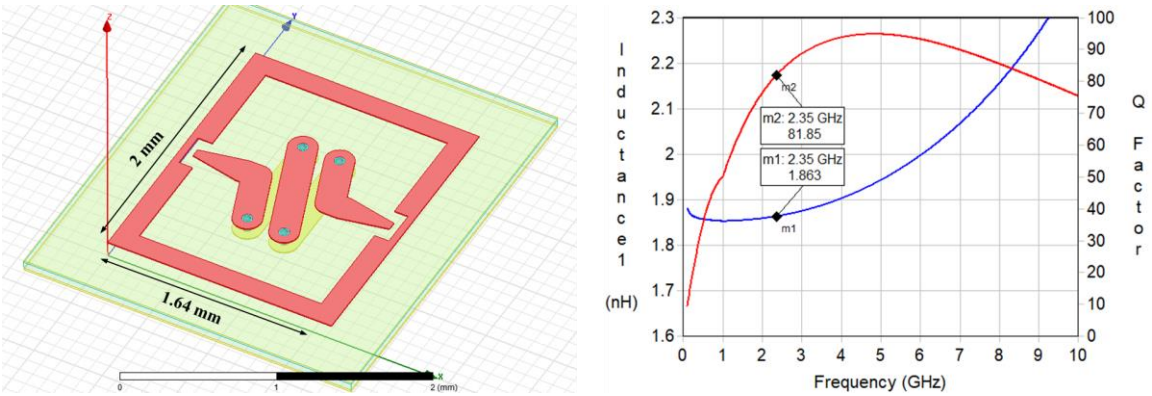
Compared to the reference design where the inductance was 1.9 nH and the Q factor was 86, the broadened linewidth yielded 2 nH inductance and a Q factor as high as 100. Therefore, it is more convenient to mitigate the conductor loss and improve the inductor Q factor by increasing the copper linewidth when the thickness is four times larger than the skin depth. However, this implementation is at the cost of reduced inductance density, hence a trade-off between inductor size and Q factor must be made.

Design of Solenoid Inductors for Measurement

Chapter 3 elaborates that the Q factors of inductors could be extracted from the measured S-parameters of a two-port inductor design. The GSG testing structures were included in the inductor layout so that the frequency response of both inductance and Q factor of the designed inductor could be measured using a VNA. Two types of solenoid inductors with 100 μm and 200 μm linewidth were designed and optimized respectively, using the same substrate-stack-up that was shown in Figure 4.15 (b). Both inductors were designed at 1.7 nH ~ 1.9 nH to be used for SAW filters' impedance matching network. The EM models and simulation results of both designed inductor are presented in Figure 4.20.



(a)



(b)

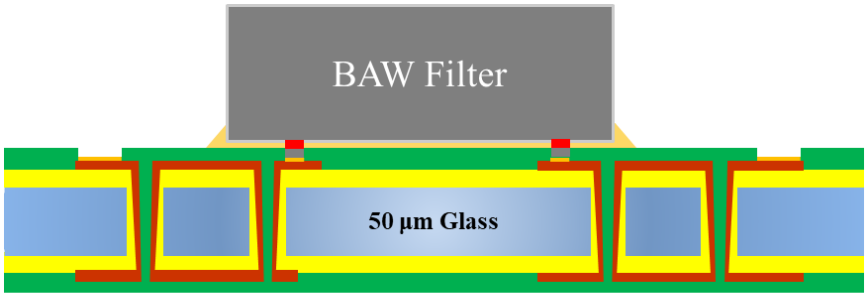
Figure 4.20. EM models and simulation results of solenoid inductors with (a) 100 µm linewidth, and (b) 200 µm linewidth for testing.

Due to the presence the of ground structure and signal feeding lines at each port, inevitable capacitance coupling between the inductor and ground frame, as well as additional parasitic loss affected the inductor performance. Resultant Q factors of both the designed inductors were degraded, showing 64 for the smaller one and 82 for the bigger one.

Although unloaded inductor Q factors can be retrieved by proper de-embedding calibration and measurement techniques, the loaded Q factors have more practical meaning. When these inductors are embedded into 3D module substrates, they suffer losses from impedance discontinuities at interconnections, crosstalk with other passive components and EM coupling to ground or shielding structures. All factors add up and the resultant loaded inductors' Q factors decide the system performance.

Impedance Matching Network Design

The impedance matching network of BAW filter was designed on two-metal layer glass substrates incorporating both high-Q solenoid inductors and EMI shielding structures. The substrate stack-up is captured in Figure 4.21.



Substrate Stack-up				
Layer	**Material**	**Thickness**	**Dk**	**Df**
Solder resist	Hitachi	15 µm	2.7	0.008
Primary build-up layer	ABF GY-11	15 µm	3.2	0.0042
Glass	Schott AF32	50 µm	5.1	0.004
Primary build-up layer	ABF GY-11	15 µm	3.2	0.0042
Solder resist	Hitachi	15 µm	2.7	0.008

Figure 4.21. Substrate stack-up for BAW filters and their impedance matching networks.

The BAW filter impedance matching network was designed with a size of 2.0 mm × 2.8mm, including testing structures and a ground frame. The top view of the substrate layout is illustrated in Figure 4.22.

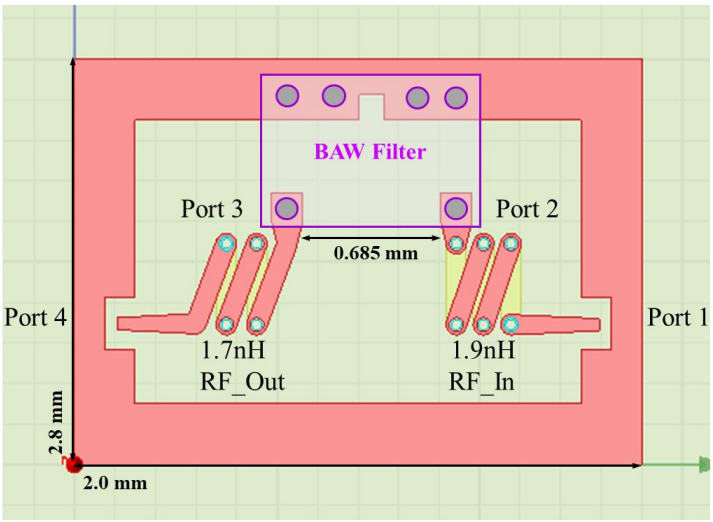


Figure 4.22. Layout of unshielded BAW filter impedance matching network on 50 µm ultra-thin glass.

For miniaturization concerns, small-size inductors were required, hence solenoid inductors were modelled and designed with 70 µm diameter TGVs, 100 µm conductor linewidth and 8 µm conductor thickness on the proposed substrate layout. Individually designed 1.7 nH inductor and 1.9 nH were embedded directly underneath the RF nodes of the BAW. The separation of two inductors was as close as 0.685 mm, with no EMI shielding structure in between.

EM simulation of the substrate model was conducted and its results were compared to the circuit-level simulation results as shown in Figure 4.23.

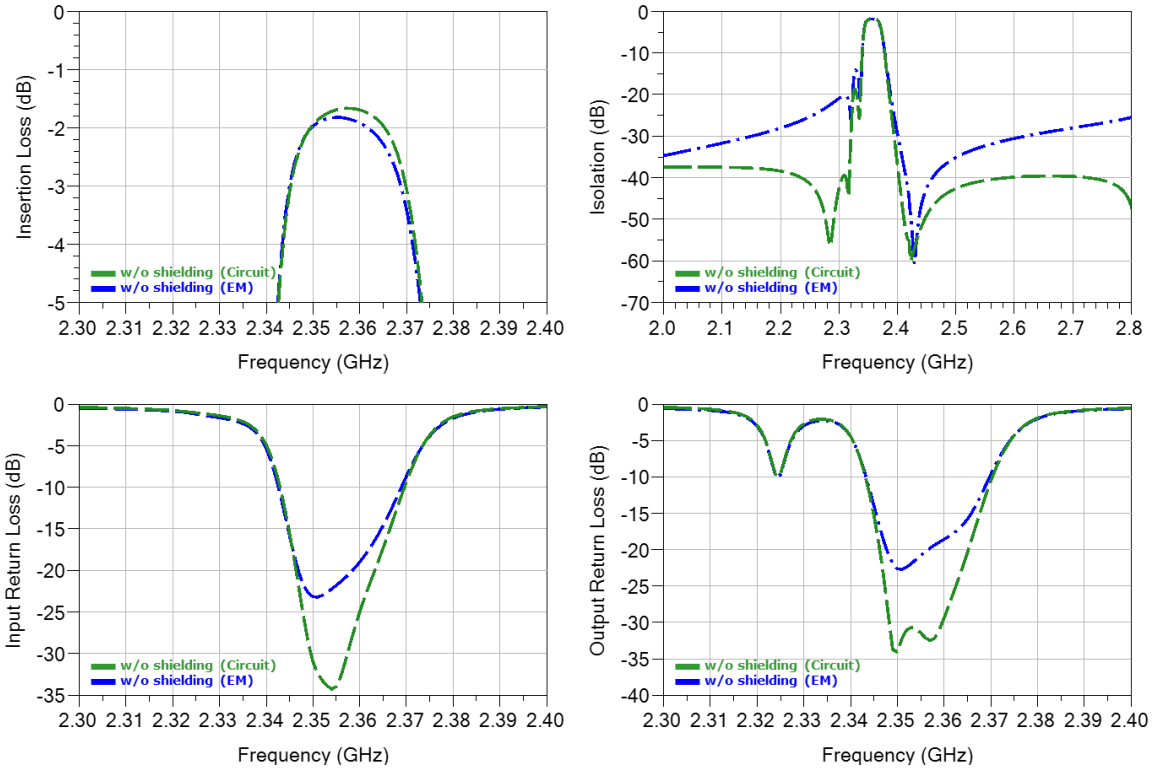


Figure 4.23. EM simulation results of unshielded BAW filter impedance matching network on 50 µm ultra-thin glass in comparison to circuit-level simulation.

An evident, degradation of BAW filter's high isolation attribute was revealed, conveying the message that parasitic effects existed in the EM model. Directly obtained

S-parameter data could be transferred into Y-parameter data, from which the inductance and capacitance could be extracted between any two nodes in the simulated network, as shown in Figure 4.24. These parasitic elements were induced by both electric field and magnetic field coupling, including capacitance between Ports 1 and 3, Ports 2 and 4, and mutual inductance between the two inductors.

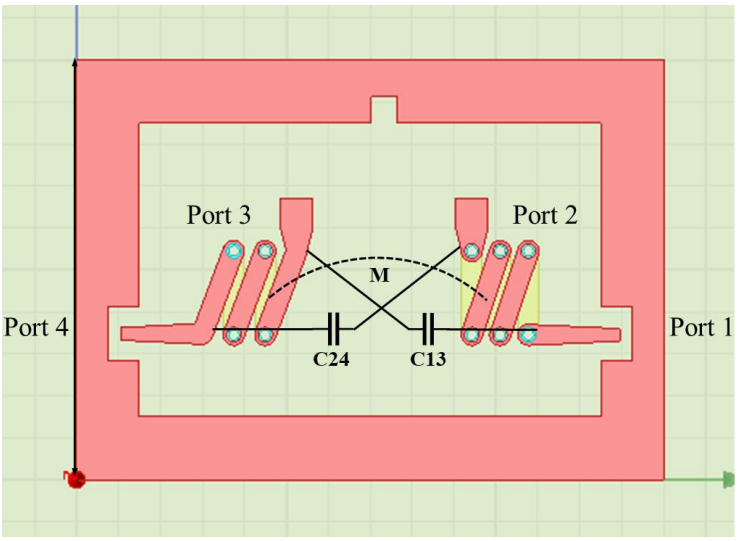
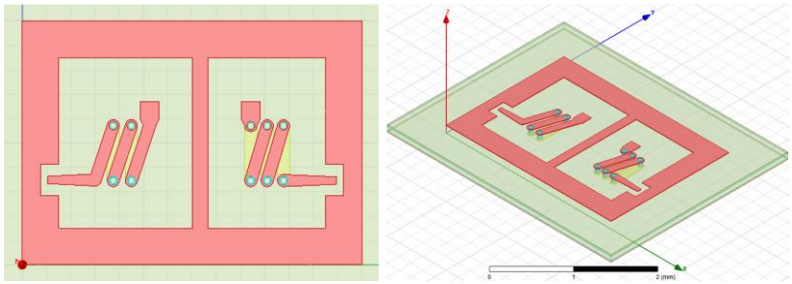
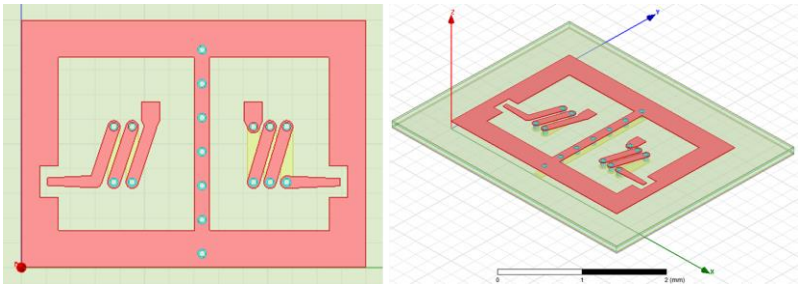


Figure 4.24. EM coupling-induced parasitic effects in unshielded BAW filter impedance matching network.

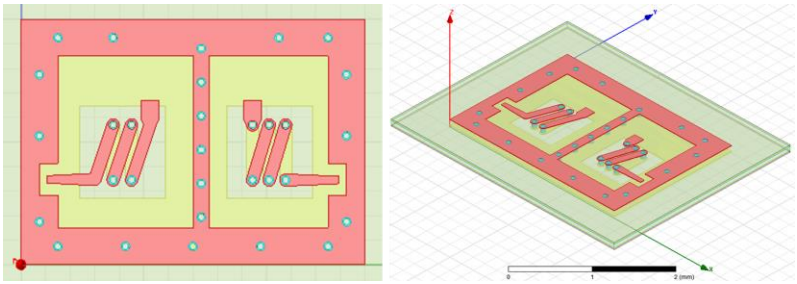
To suppress the crosstalk between two inductors, EMI shielding structures were designed and integrated in three different architectures as shown in Figure 4.25. Since the internal magnetic flux of solenoid inductors was confined to within the substrate, with a direction parallel to the substrate surface, a single-layer planar ground trench shown in Figure 4.25 (a) might not be sufficient to prevent the crosstalk. Therefore, additional two 3D-configuration shielding structures were innovated, where grounded TGVs were used as either EM radiation fence in between two inductors or as a EM radiation cage that encircled each inductor.



(a)



(b)



(c)

Figure 4.25. EM models of BAW filter impedance matching networks on 50 µm ultra-thin glass with EMI shields designed as (a) a single ground trench, (b) a TGV fence, and (c) a TGV cage plus a ground plane.

The EM simulation on three shielding designs were performed in HFSS and S-parameters of four-port networks were obtained. The isolation between Port 2 and 3 on different substrate layouts is plotted in Figure 4.26. The integration of EMI shields showed significant improvement in isolating the two inductors, and more than 50 dB isolation was achieved from the 3D shielding structure when both TGV cage and ground plane were employed.

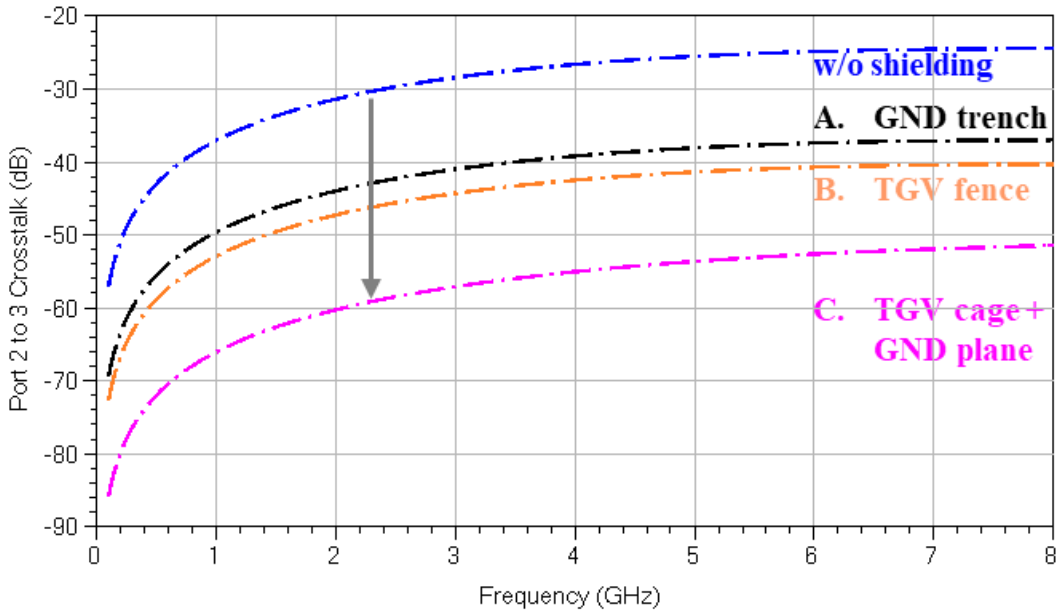


Figure 4.26. Crosstalk between Port 2 to port 3 with different shielding schemes.

These re-designed substrate models were also simulated with the BAW filter to check the filter response. The filter's isolation to out-of-band signals are plotted in Figure 4.25.

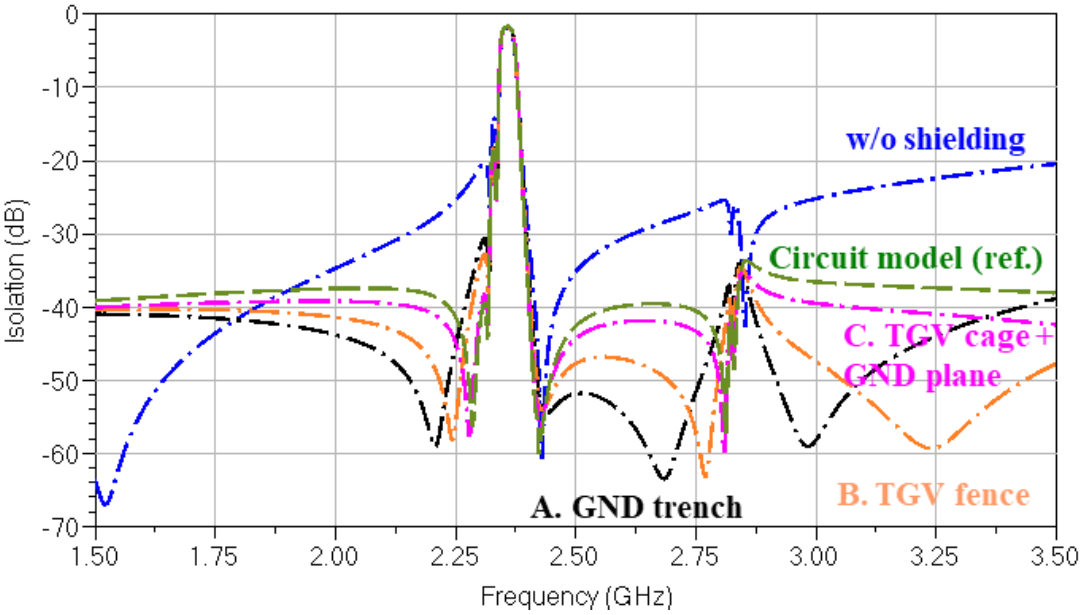
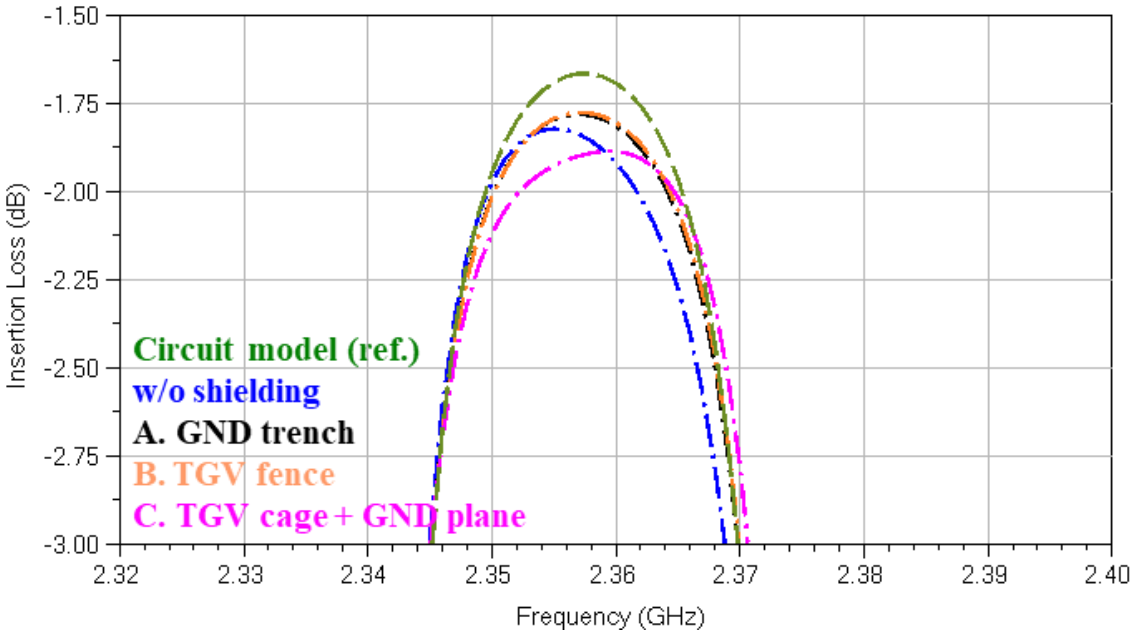


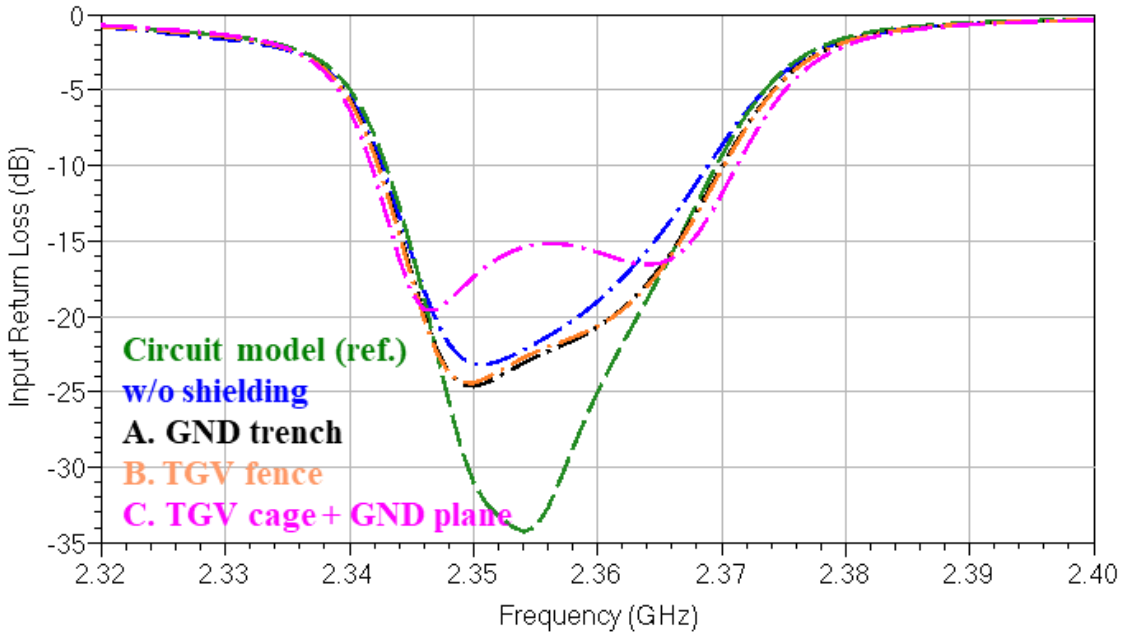
Figure 4.27. Out-of-band signal isolation of BAW filter impedance matching networks.

The degradation of BAW filter's selectivity, as previously observed, was successfully addressed with the presence of component-level EMI shields. With all three types of shield designs, more than 35 dB isolation was achieved to out-of-band signals. Excellent agreement was observed between the ideal circuit model and the impedance matching network design where TGV cage and ground plane were integrated into the shields.

On the other hand, although the crosstalk between two inductors was reduced, parasitic effects between inductors to the EMI shields manifested, predominantly as the capacitance coupling to ground. The resultant inductance and Q factor variation of both inductors altered the filter's response. To study these impacts, the filter's passband insertion loss and return deviation on different impedance matching network designs are presented in Figure 4.28.



(a)



(b)

Figure 4.28. (a) Passband insertion loss, and (b) input port return loss of BAW filter impedance matching networks.

The compressed BAW filter's 3 dB bandwidth was resolved when the inductors are embedded into the substrates and shielded. Both ground trench and TGV fence approach showed an improvement in insertion loss when compared to an unshielded design. The increased return loss in the case of "TGV cage plus ground plane shielding" was due to the tight capacitance coupling between the inductor and ground, which lowered the inductance and Q factors of solenoid inductors. Consequently, the filter suffered higher passband insertion loss. The best passband insertion loss achieved in this case was 1.86 dB.

To study the impact of shielding structures on inductors' performance, the inductance and Q factors of loaded 1.7 nH and 1.9 nH inductors were extracted from these designed impedance matching networks. The inductors' characteristics are summarized in Table 4.2.

Table 4.2. High-Q inductors in designed impedance matching networks

Inductors (@ 2.35 GHz)	1.7 nH		1.9 nH	
	L (nH)	Q	L (nH)	Q
No shielding	1.76	66	1.92	69
GND trench	1.68	61	1.79	64
TGV fence	1.68	64	1.81	68
TGV cage plus GND plane	1.36	52	1.44	54

In both EMI shielding designs with “GND trench” or “TGV fence”, Q factors of more than 60 were observed. Significant degradation of inductance and Q factor on solenoid inductors was observed in the impedance matching network where “TGV cage and GND plane” were used for shielding. This part of loss could be compensated if larger inductors were chosen prior to their integration into the system.

Summary of Electrical Design

Study of high-Q inductor design on 50 μm glass was performed focusing on the design topology optimization. Single-turn planar spiral inductors were compared to 3D solenoid inductors, both of which showed equally good Q factors and SRF. Solenoid inductors were chosen as the building blocks of BAW filter impedance matching networks, since they offered 25% higher inductance density and more options for EMI shield design.

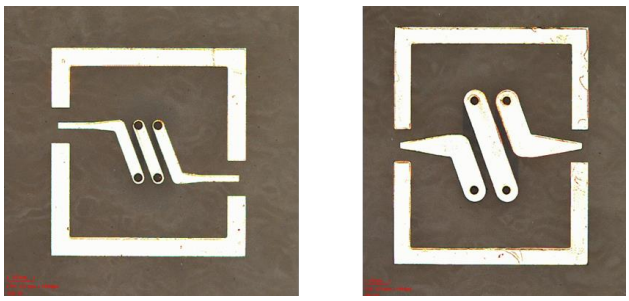
In addition, fundamental limitations for high-Q solenoid inductor design were analyzed and two types of solenoid inductors were designed on 50 μm glass with different sizes. Finally, BAW filter impedance matching networks were designed with integrated small-size solenoid inductors and various substrate-embedded EMI shields, showing improved filter response. The sensitivity of inductors to EMI shields was studied, and their co-design was suggested to maximize the system performance.

4.2.2 Substrate Fabrication and Assembly

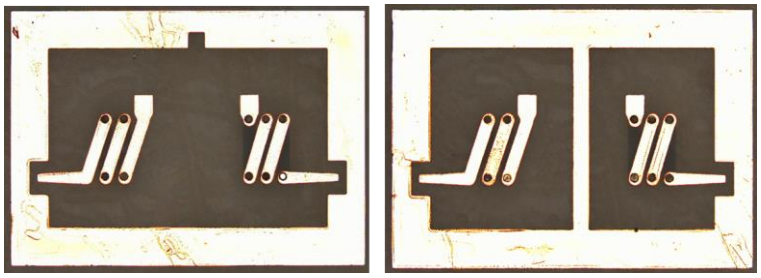
High-Q solenoid inductors and impedance matching works from the 100 µm glass substrates were redesigned and taped-out on 100 mm × 100 mm ultra-thin 50 µm thick glass panels. Special care was given to glass substrate manufacturing process described in Figure 3.16 in Chapter 3, but with only two metal layers. A snapshot of fabricated two-metal layer glass substrate panels before solder-resist lamination is shown in Figure 4.29.

Figure 4.29. Fabricated 100 mm × 100 mm two-metal-layer substrate panel using 50 µm ultra-thin glass.

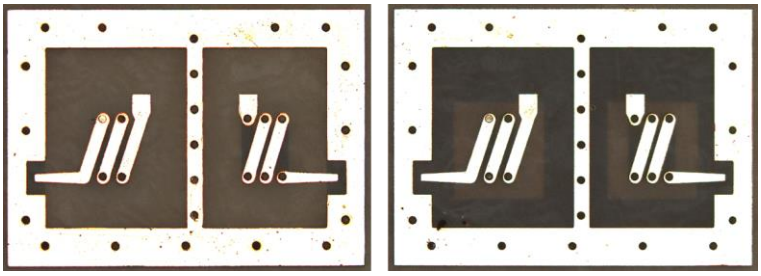
Metallization results of SAP solenoid inductors as well as substrate-embedded impedance matching networks are captured in Figure 4.30.



(a) (b)



(c) (d)



(e) (f)

Figure 4.30. Metallization results of manufactured solenoid inductors with type (a) small size and type (b) higher Q factor; and BAW filter impedance matching networks with (c) no EMI shield, (d) a GND trench, (e) a TGV fence, and (f) a TGV cage plus a GND plane.

The performance of solenoid inductors was characterized first before the solder resist lamination and after surface finish. Examples of substrate-embedded BAW filter impedance matching networks on a finished glass panel are shown in Figure 4.31.

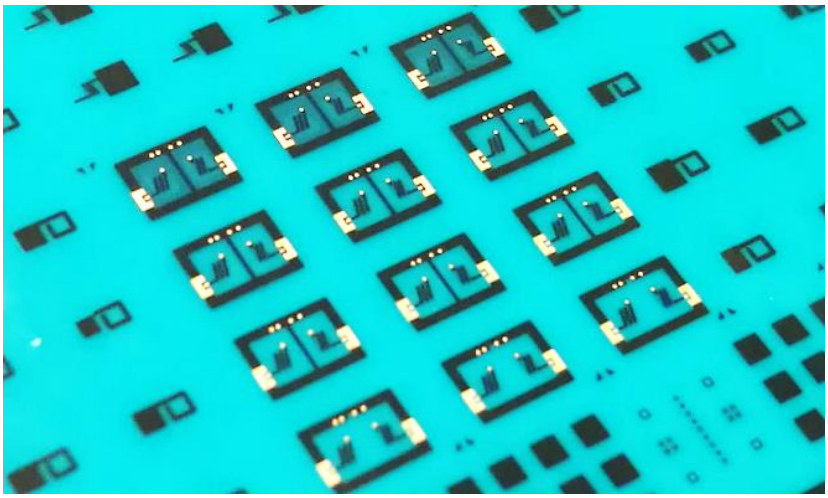


Figure 4.31. BAW filter impedance matching networks on finished glass substrates.

Flip-chip assembly of BAW filters was performed by solder mass reflow on the glass panel and its results are presented in Figure 4.32.

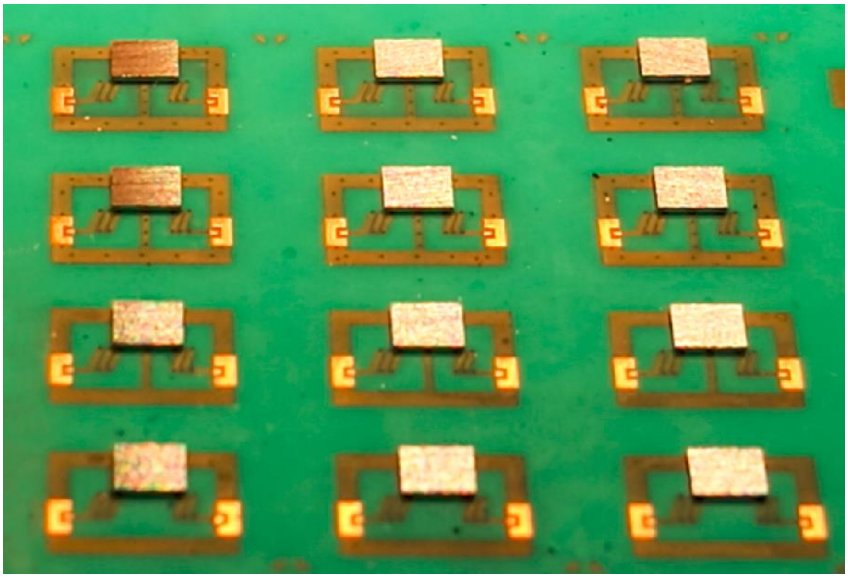


Figure 4.32. Assembled BAW filters on ultra-thin glass substrates.

The rigid attribute of glass maintained the substrate flatness and the small thickness made the substrate flexible. Because of these, high-tolerance substrate manufacturing and high-yield component assembly were obtained.

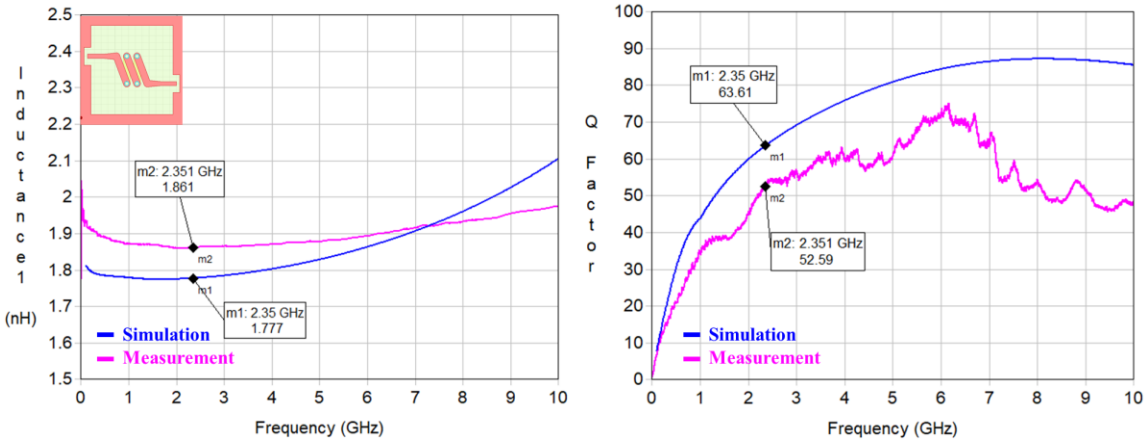
4.2.3 Characterization

A two-port network measurement was set up on a wafer probe station and two GSG probes with 250 μm pitch were connected to a VNA. High-frequency measurement was conducted on both high-Q solenoid inductors as well as on BAW filter impedance matching networks.

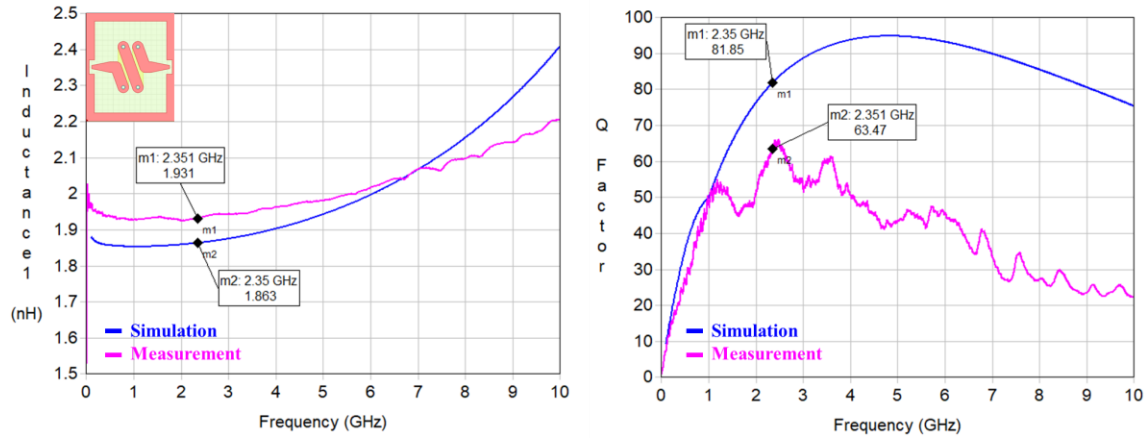
Measurement on High-Q Inductors

Measurement of high Q factors (e.g. Q > 50) on a stand-alone inductor with a VNA has always been a challenging task due to the rigorous requirements on measurement accuracy. The discrepancy between simulations and measurements is more serious with

higher Q factors. With careful calibration, the measured inductance and Q factors of two types of solenoid inductors are plotted in Figure 4.33 together with their EM simulation results for correlation analysis.



(a)



(b)

Figure 4.33. Measured inductance and Q factors of (a) small-size and (b) high-Q solenoid inductors on 50 µm ultra-thin glass.

A good agreement between measured and simulated inductance was observed and less than 5% deviation was achieved up to 8 GHz for both inductors. The Q factor measurement showed reasonably good hardware-to-software correlation under 1 GHz for inductors with Q less than 50, and the deviation increased as the Q factor increased. The

inaccuracy was mainly because of the limited significant digits on measurement data that the VNA could provide [53], as well as the parasitic effects such as ohmic loss induced from the probe contact, that were not completely de-embedded. At 2.35 GHz, measured inductance and Q factor were 1.86 nH and 53 on the small-size solenoid inductor, while on the second type of high-Q solenoid inductor, they were 1.93 nH and 63.

Measurement on BAW Filter Impedance Matching Networks

Four types of designed BAW filter impedance matching networks with and without EMI shields were measured. The measurement results are plotted together with EM simulation results, and are presented in Figure 4.34.

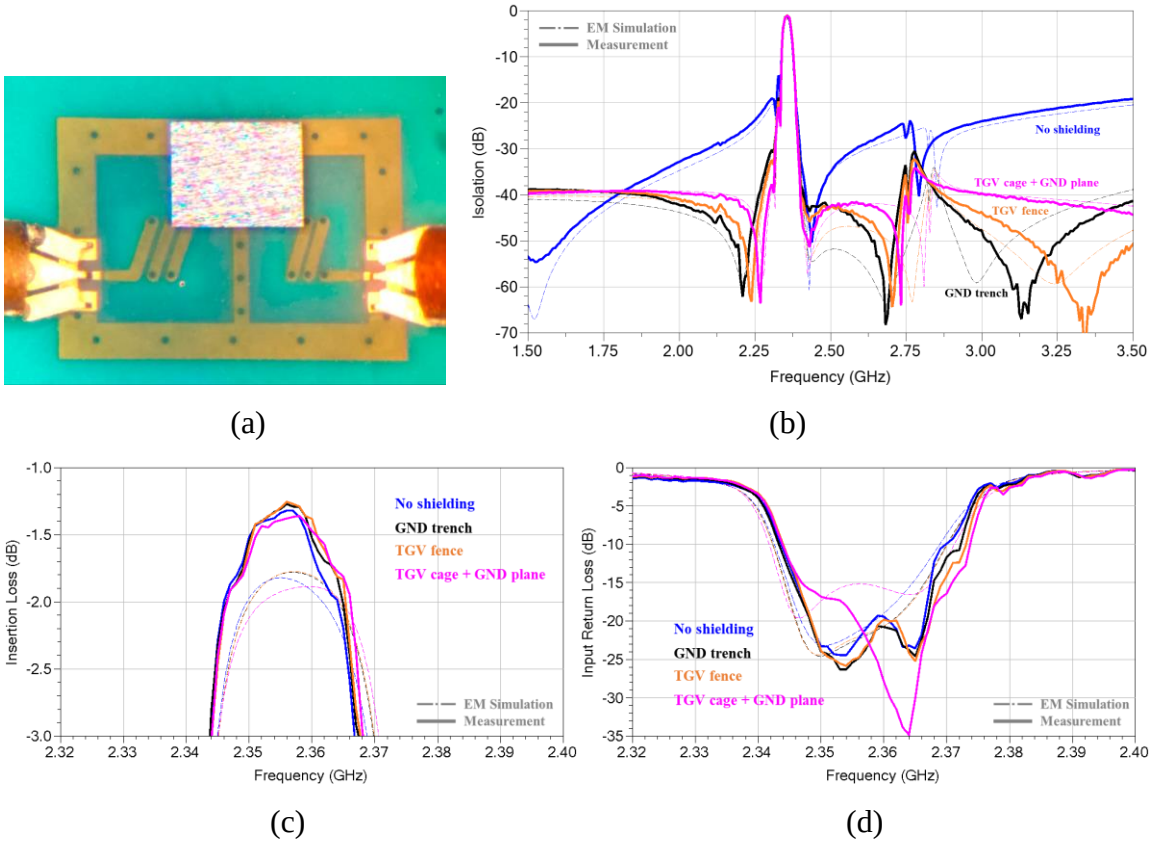


Figure 4.34. (a) A BAW filter impedance matching network under test; and measured filter responses with different EMI shield designs in terms of (b) out-of-band isolation, (c) passband insertion loss, and (d) passband return loss.

The measurement results showed good correlation with EM simulation, and the designed substrate-embedded impedance matching networks with integrated high-Q solenoid inductors and EMI shields showed significant improvement of the BAW filters. With EMI shield integration, the BAW filter held its high isolation attribute to out-of-band signals, and both of passband insertion loss and return loss were significantly improved. A summary of measured BAW filter performance metrics is listed in Table 4.3.

Table 4.3. Measured performance metrics of BAW filters

Design #	EMI Shield	Insertion Loss (dB)	Return Loss (dB)	Isolation (dB)
0	BAW filter alone (Ref.)	> 2.06	7.9 (Min) 7.9 (Cen)	> 34
1	N/A	> 1.32	9.9 (Min) 22.3 (Cen)	> 19
2	GND trench	> 1.27	11.7 (Min) 24.8 (Cen)	> 31
3	TGV fence	> 1.25	12.3 (Min) 24.8 (Cen)	> 32
4	TGV cage plus GND plane	> 1.38	12.2 (Min) 20.5 (Cen)	> 34

In the demonstrated samples, a frequency shift was observed on high-frequency notches and on the LTE band, which was mainly due to the variations in inductor geometries that were induced during the substrate fabrication. As the substrate becomes thinner and thinner, thickness-related deviation are also manifested. More process control in ultra-thin glass-making as well as glass substrate fabrication should be simultaneously carried out.

4.2.4 Summary

For the very first time, ultra-thin 50 μm thick glass was employed for RF module demonstration, where high-performance passives and EMI shields were double-side embedded into the substrates. Major performance metrics of the demonstrated BAW filters with impedance matching networks are summarized in Table 4.4.

Table 4.4. Accomplishments of RF module demonstration on 50 μm ultra-thin glass

Topic	Metrics	Objectives	Accomplishments
3D IPAC Modules	Performance	• IL < 2 dB • RL > 14 dB • Q > 60	• IL = 1.25 dB (Min) • RL - 11.7 dB (Min) - 22.3 dB (Cen) • Q > 60
	Miniaturization	• Substrate thickness Z < 100 μm	• Z = 100 μm

High-Q solenoid inductors with 1.7 nH ~ 1.9 nH inductance were designed on 50 μm thick glass, fabricated and measured, showing Q factors higher than 60 at 2.35 GHz. Small-size high-Q solenoid inductors were embedded into the glass substrates together with three types of EMI shield designs, forming the impedance matching networks of BAW filters. The designed RF modules on 50 μm thick glass were then fabricated, and first-level flip-chip bonding was performed with high assembly-yield. Finally, the electrical characterization results on the filter's responses met all the research objectives.

The proposed 3D RF module integration technology, where high-Q inductors and component-level EMI shields are embedded as double-side passives into the ultra-thin glass substrates, was, thus, demonstrated. Its superiority in small foot-print, ultra-small substrate thickness, and high electrical performance, makes it a promising technology for next-generation RF modules.

CHAPTER 5

RESEARCH SUMMARY, CONTRIBUTIONS AND SUGGESTIONS FOR FUTURE WORK

The objective of this dissertation is to design and demonstrate ultra-thin (100-200 microns) 3D components and modules for ultra-miniaturized, high-performance RF diplexers and front-end modules for advanced 4G -LTE networks. Glass-based double-side or 3D component integration was proposed to achieve superior performance with miniaturization and manufacturability at low cost. Such 3D integration solution with double-side thinfilms and surface-assemble components on glass offers superior electrical performance over conventional 2D packages on laminate or ceramic based substrates because of suppressed interconnection loss from shorter interconnection lengths with through-vias in ultra-thin glass, components with higher Q and volumetric densities. Glass also offers superior manufacturability with process control, and scalable, low-cost and large-area fabrication. Although glass has many benefits such as its excellent electrical and mechanical properties, which benefit substrate loss reduction, manufacturability with good tolerance, and assembly, the thickness reduction in 3D package configuration gives rise to several fundamental challenges, which require major design and process innovations.

In order to design and demonstrate 3D IPD diplexers in ultra-thin glass substrates, fundamental challenges that result in diplexer performance degradation are identified as follows: 1) constrained physical dimensions that limit the design flexibility; and 2) process induced variations that cause the divergence of transmission characteristics. To address these challenges, research tasks are proposed both in electrical design of innovative inductor and capacitor topologies in ultra-thin substrates and their integration

into 3D IPD diplexers, as well as in process development for to achieve geometry control for precision.

Miniaturization of RF modules using 3D glass packages imposes other set of challenges: 1) Q factor degradation of embedded inductors due to lower substrate thickness; 2) EMI issues between system components in proximity; and 3) handling of double-side assembly on sub-100 μm ultra-thin glass. In order to address these challenges, three research tasks were proposed and implemented: 1) high-Q inductor design with integrated EMI shields; 2) ultra-thin glass substrate fabrication with embedded passives; and 3) panel-level assembly process development with low-cost BGA balling and flip-chip bonding.

Details of the electrical modeling, design, fabrication and assembly processes as well as results and analysis for both 3D IPD diplexers and 3D IPAC modules were presented in the previous chapters. The proposed glass substrate-based 3D IPDs and 3D IPAC modules were validated with model-to-hardware correlations. Key research findings associated with each task are summarized in the first section of this chapter. This is then followed by a summary of key contributions of this research and a discussion on future research directions. Finally, a list of publications and awards from this work is provided.

5.1 Research Summary

5.1.1 Design and Demonstration of 3D IPD LTE Diplexers

Electrical Design

Innovative circuit designs that incorporate both component and system-level performance, and manufacturing constraints were developed and incorporated into the circuit-level design phase. Third order elliptic-function filter networks were chosen for both low- and high- frequency bands to achieve high selectivity attributes with a

minimum count of lumped LC elements. Miniaturization of high-Q capacitors is more practical compared to that of inductors. Therefore, the circuits were designed with minimum number of inductors. In addition, when MIM capacitors were employed in practice, their physical dimensions were only a fraction of inductors. Therefore, resonating LC circuits in parallel configuration were avoided to minimize the interconnection loss. By utilizing circuit transformation operations, equivalent series inductance-capacitance networks were obtained. Finally, the Q factors of inductors and capacitors were also captured in the circuit models in order to enhance the simulation accuracy.

Thinfilm Passives

Compared to 2D planar spiral inductors, 3D solenoid inductors that leverage multiple TGVs can achieve higher Q factors. The Q factor of a 3D solenoid inductor designed on 200 μm thick glass can reach 90 around 2 GHz, which is 2-3 times that of a spiral inductor. On the contrary, the inductance density of spiral inductors is 2-3 times higher than that from the solenoid type.

For capacitors, MIM designs with sub-10μm thick polymer-polymer-based dielectrics that were laminated onto the substrates as dry-film build-up layers, as well as nanoscale inorganic thinfilm capacitors with 200-300 nm thick Si_3N_4 dielectrics were considered. Advances in inorganic thinfilm deposition technologies and their high dielectric constant make the capacitance density of MIM capacitors more than 80 times that of organic thinfilm capacitors. These approaches were used to provide guidelines for 3D IPD designs on glass, allowing multiple LC integration options to accommodate different application and cost-structure with high performance and small footprint.

3D IPD Fabrication

Along with superior performance, large-scale manufacturability at low cost, tight process tolerance and high reliability are the key constraints that determine the fabrication approaches. Low-cost fabrication was mainly achieved by designing glass substrate process that are compatible with existing large area substrate manufacturing infrastructure. The key starting point for this is the double-side dry-film lamination of primary build-up layers on TGV-drilled bare glass. Since the ultra-thin glass was coated with thin polymer films, and TGVs were filled with polymer, the damage from brittleness of glass was mitigated. Existing organic substrate manufacturing processes such as TPV formation by laser drilling, electroless SAP for metallization and panel-scale manufacturing can be, thus, easily realized with glass.

A comprehensive study of process-induced electrical performance variations was performed. Both measured and simulated results confirmed that the performance deviation or degradation in thinfilm diplexers, which manifests as a frequency-shift and band-spread, was because of the nonuniform dielectric thickness. A low-cost surface planarization process after the organic thinfilm lamination was proposed and developed. Significant improvement in dielectric thickness uniformity was achieved with this process. Excellent thinfilm thickness uniformity was also realized during the MIM capacitor fabrication by adapting advanced PECVD thinfilm process. By adapting optimized glass substrate process flow, better than 5% fabrication tolerance was achieved for performance-sensitive dimensions such as dielectric thickness uniformity, layer-to-layer mis−registration and linewidth variation on 150 mm × 150 mm panels.

Demonstration of 3D IPD Diplexers

Two types of 3D IPD diplexers were designed and demonstrated on glass based on different LC integration technologies. These two diplexers are compared in Table 5.1.

Table 5.1. Comparison of two types of diplexers

		Ultra-miniaturized Diplexer	**High-performance Diplexer**
Footprint size		2.3 mm × 2.8 mm	2.9 mm× 3.9 mm
Total thickness		0.2 mm	0.28 mm
Performance	Passband IL	< 0.9 dB @ LB 1.3 ~ 2.9 dB @ HB	< 0.4 dB @ LB < 0.7 dB @ HB
	Passband RL	> 15 dB @ LB > 12 dB @ HB	> 16 dB @ LB > 13 dB @ HB
	Isolation	> 26 dB @ LB > 16 dB @ HB	> 23 dB @ LB > 27 dB @ HB
Inductors	Type	2D spiral	3D solenoid
	Q factor (@ 2GHz)	30 ~ 40	80 ~ 90
	Density	20 nH / mm^2	5 nH / mm^2
	Quantity	6	6
Capacitors	Type	Organic thinfilm	MIM with thinfilm Si_3N_4
	Density	3.5 pF/mm^2	250 pF/mm^2
	Quantity	7	8
Process tolerance		< 5%	< 5%
Cost		Low	Low to moderate

Two prototypes of 3D IPD diplexers on ultra-thin glass substrates were successfully modeled, designed and demonstrated in this research. Innovations in both electrical design and ultra-thin glass substrate processing with precision RF circuits were proposed and validated. Ultra-miniaturized high-performance 3D IPDs on ultra-thin glass substrates are thus realized for next-generation high-end RF modules.

5.1.2 Design and Demonstration of 3D IPAC LTE Modules

High-Q Inductors on 50 μm Ultra-thin Glass

Solenoid 3D inductors generally offer higher Q factor than 2D spiral inductors. However, when low-value inductors are desired in ultra-thin glass substrates, both solenoid and spiral inductors seem to be equally viable. Hence, a comprehensive study was performed to compare the performance of high-Q 2D spiral inductors and 3D solenoid inductors on ultra-thin 50 μm glass substrates. For the same design targets of 1.9 nH inductance and Q factor of above 60 at 2.35 GHz, spiral and solenoid inductors were designed and modeled on 50 μm glass, using the same substrate design rules. Both designs resulted in comparable de-embedded Q factors of 82-86 and similar high SRF. Although the stand-alone electrical performance of both design topologies is comparable, the solenoid inductors offer 25% higher inductance density in unit area. Another unique advantage of solenoid inductors is their ability to be shielded from each other when embedded into ultra-thin substrates.

The predominant factor that limits the Q factor of 3D solenoid inductors in 50 μm thick glass is the AC conductor loss induced from the skin effect. EM simulations indicated that the most efficient approach to improve the inductor Q factor was to increase the coil width, which, on the contrary, increases the footprint. Two types of solenoid inductors with different sizes were designed, fabricated and tested. Inductance measurements showed good agreement with simulations. Q factors of more than 60 were obtained.

Component-level EMI Shielding

EMI is a major issue with miniaturized RF systems. In this study, the effect of EMI is clearly observed in the characteristics of BAW filter performance when the impedance matching networks utilized substrate-embedded inductors that are prone to cross-talk

from their neighboring components. The out-of-band signal rejection of the BAW filter is the key performance metric that is affected by EMI. Three types of shielding schemes - planar copper trench, grounded TGV fence and ground-plane structures, were proposed and implemented in high-Q solenoid inductors with integrated impedance matching networks. Their performance metrics were successfully captured by both electrical simulations and experimental characterization. Excellent shielding effectiveness was demonstrated with a combination of TGV fence and properly-designed ground planes.

Double-side Assembly on Ultra-Thin Glass

A unique process for panel-level assembly on both sides of ultra-thin glass substrates was demonstrated. Chip-level assembly was performed by flip-chip bonding and mass reflow. This is followed by BGA balling at 500 μm pitch from low-cost paste printing approaches. The module substrate showed superior flatness and low warpage after double-side assembly.

Dicing of 3D Glass Packages, Assembly and Characterization

A combination of laser ablation and mechanical dicing with a diamond blade solution was employed for the singulation of 3D glass modules. The cross section of the mechanically diced glass surface featured an average roughness of less than 0.16 μm. The dicing-induced defects were mitigated by an edge-coating approach, in which a thin layer of underfill material was dispensed along the dicing edges to encapsulate them. The isolated RF modules were directly assembled onto the PCBs for testing. No degradation in the BAW and SAW filter performance was seen with the 3D IPAC modules, indicating

low parasitics, precision impedance matching and high Q of the matching networks and package interconnects.

5.2 Key Contributions

The key contributions of this research are summarized in the following categories: 1) Electrical design, 2) Fabrication of RF components with less than 5% tolerance, 3) Three-dimensional device and module integration in ultra-thin glass.

Optimization of Electrical Design

Higher-Q (>80 @ 2.35GHz) inductor topologies with 50 μm ultra-thin glass were explored and developed. A TGV-based solenoid inductor design was proposed and demonstrated with optimal density, Q factor and shielding from other components. Resistance from skin-effect was identified as the dominant factor that determined the Q factor of an inductor.

Circuit-level design and optimization methodologies for high-performance diplexers were developed. Various 3D LC networks were investigated on ultra-thin glass substrates, leading to design guidelines for 3D IPDs on glass. Two front-up 3D IPD diplexers were designed and demonstrated on ultra-thin glass, showing equivalent performance but with 3-4X thickness reduction compared to the prior art. Substrate-embedded EMI shields were designed, demonstrated and characterized to suppress the component-level cross talk.

Fabrication of RF Components with 5% Tolerance

A comprehensive study of process-induced electrical performance deviation was conducted. Dielectric thickness was identified as the key process-sensitive design parameter that affects the diplexer tolerance. A low-cost surface planarization approach

was proposed, developed and demonstrated to mitigate the nonuniformity of organic thinfilms, with better than 5% process tolerance control on 6-inch panels.

Three-dimensional Device and Module Integration in Ultra-thin Glass

With the design and process advances, ultra-thin 50 μm thick glass substrates with embedded high-Q passives were demonstrated for the first time. Key process challenges related to handling of thin glass, TGV formation, 3D or double-side component integration were addressed with scalable, stable and manufacturable processes.

Three-dimensional integrated passive and active component (3D IPAC) module with thinfilm passives and double-side assembled components was also modeled and designed. A complete process flow for module fabrication and double-side assembly on ultra-thin 100 μm thick glass was proposed and developed, and the very first 3D glass-based packages for RF FEMs were demonstrated.

5.3 Suggestions for Future Work

This dissertation explored, developed and validated the concepts of 3D IPDs and 3D IPAC modules or packages with ultra-thin glass for 4G-LTE applications. Good electrical performance and system miniaturization are achieved with design innovations in system unit blocks, process development of unique 3D structures, substrate fabrication and assembly. Prototype test vehicles were successfully demonstrated with superior electrical performance. Suggestions for future research directions are provided below.

EMI Shielding

In addition to the innovations in topologies for miniaturized RF components, another critical enabler for system miniaturization is the EMI shielding of those components. With component-level shielding, the EM field emission of a signal component is confined so that it would not affect other victims and also has immunity to external

interference. These self-shielded components could stay close to each other, thus minimizing the system size and interconnect losses. In addition, in the proposed 3D architectures, since both sides of substrates have integrated components, their coupling effect has a destructive interference on system performance. This effect becomes further aggravated when the substrate thickness is reduced. Without proper shielding, the vertical superposition of double-side components is impractical. Therefore, the benefits of 3D packages cannot be realized. Three avenues are suggested for advances in EMI shielding: engineering frequency-selective surfaces such as artificial magnetic conductors (AMCs); trench and via-cage structures for isolation without degrading the component performance; multilayered or nanocomposite shield materials with superior attributes over monolithic materials and their integration into 3D RF modules.

Extension to 5G Application

The 3D glass packaging technology developed in this dissertation is extensible to 5G applications for higher data rates and smaller form factor that next-generation communication modules require. It is foreseen that the early phase of 5G networks will extend the advanced carrier aggregation technology in current 4G-LTE systems, while the carrier frequencies will be simultaneously increased to 7 GHz. In this regard, both the high-frequency electrical design of passives and 5G modules, and development of much denser integration technology needs to be studied. The 3D architectures demonstrated in this dissertation should be further optimized and implemented to meet the needs for 5G applications.

5.4 Publications and Awards

The research outcomes from this dissertation and other related research activities of the PhD candidate has resulted in the following journal and conference papers, and awards.

Peer-reviewed Journals

1. **Z. Wu,** J. Min, V. Smet, M. R. Pulugurtha, V. Sundaram, R. R. Tummala, "Ultra-miniaturized 3D IPAC Packages with 100 μm Thick Glass Substrates for RF Front-end Modules", *Journal of Electronic Packaging,* 2017, Vol. 13, No. 3, pp. 041001.
2. **Z. Wu**, J. Min, M. R. Pulugurtha, V. Sundaram, R. R. Tummala, "Ultra-miniaturized 3D IPD Diplexers on 100 μm Thick Glass Substrates for LTE Applications", submitted to *IEEE Transactions on Component, Packaging, and Manufacturing Technology*.
3. **Z. Wu**, M. R. Pulugurtha, V. Sundaram, M. Letz, C. Hoffman, R. R. Tummala, "Embedded High-Q Inductors and EMI Shields on Ultra-thin 50 μm Thick Glass for RF Front-end Modules", to be submitted to *Journal of Microelectronics and Electronic Packaging.*
4. B. Sawyer, Y. Suzuki, **Z. Wu**, V. Sundaram, K. Panayappan, R. R. Tummala, "Design and Demonstration of Fine-Pitch and High-Speed Redistribution Layers for Panel-Based Glass Interposers at 40-μm Bump Pitch", *Journal of Microelectronics and Electronic Packaging,* 2016, Vol. 13, No. 3, pp. 128-135.
5. S. Sitaraman, V. Sukumaran, M. R. Pulugurtha, **Z. Wu**, Y. Suzuki, Y. Kim, V. Sundaram, J. Kim, R. R. Tummala, "Miniaturized Band-Pass filters as Ultra-thin 3D IPDs and Embedded Thinfilms in 3D Glass Modules", *IEEE Transactions on Component, Packaging, and Manufacturing Technology,* 2017, Vol. 7, No. 9, pp. 1410 - 1418.
6. M. S. Kim, M. R. Pulugurtha, V. Sundaram, **Z. Wu**, M. Ali R. R. Tummala, "Ultra-thin High-Q 2D and 3D RF Inductors in Glass Packages", submitted to *IEEE Transactions on Component, Packaging, and Manufacturing Technology*.

Conference Proceedings

1. **Z. Wu**, J. Min, M. S. Kim, M. R. Pulugurtha, V. Sundaram, R. R. Tummala, "Design and Demonstration of Ultra-thin Glass 3D IPD Diplexers", in *2016 Proceedings 66th ECTC*, pp. 2348-2352, Las Vegas, NV, 2016.
2. **Z. Wu**, C. Nair, Y. Suzuki, F. Liu, V. Smet, D. Foxman, H. Mishima, F. Ryuta, V. Sundaram, R. R. Tummala, "Modeling, Design and Fabrication of Ultra-thin and Low CTE Organic Interposers at 40μm I/O Pitch", in *2015 Proceedings 65th ECTC*, pp. 301-307, San Diego, CA, 2015.
3. W. Su, **Z Wu**, Y. Fang, R. Bahr, M. R. Pulugurtha, R. Tummala, M. Tentzeris, "3D Printed Wearable Flexible SIW and Microfluidics Sensors for Internet of Things and Smart Health Applications", in *IEEE MTT-S International Microwave Symposium*, 2017.
4. J. Min, **Z. Wu**, M. R. Pulugurtha, V. Smet, V. Sundaram, A. Ravindran, C. Hoffmann, R. Tummala, "Modeling, Design, Fabrication and Demonstration of RF Front-End Module with Ultra-thin Glass Substrates for LTE Applications", in *2016 Proceedings 66th ECTC*, pp. 1297-1302, Las Vegas, NV, 2016.
5. S. J. Kim, **Z. Wu**, M. Kobayashi, F. Liu, V. Smet, M. R. Pulugurtha, V. Sundaram, R. R. Tummala et al, "Design and Demonstration of Paper-Thin and Low-Warpage Single and 3D Organic Packages with Chip-Last Embedding Technology for Smart Mobile Applications", in *2014 Proceedings 64th ECTC*, pp. 1384-1388, Orlando, FL, 2014.
6. B. Sawyer, Y. Suzuki, **Z. Wu**, V. Sundaram, K. Panayappan, R. R. Tummala, "Design and demonstration of 40 micron bump pitch multi-layer RDL on panel-based glass interposers", in *International Symposium on Microelectronics*, pp. 379-385, 2016.

7. M. S. Kim, M. R. Pulugurtha, **Z. Wu**, V. Sundaram, R. R. Tummala, "Innovative Electrical Thermal Co-design of Ultra-high Q TPV-based 3D Inductors in Glass Packages", in *2016 Proceedings 66th ECTC*, pp. 2384-2388, Las Vegas, NV, 2016.
8. T. Sun, M. R. Pulugurtha, J. Min, **Z. Wu**, H. Sharma, T. Takahashi, K. Takemura, H. Yun, F. Carobolante, R. R. Tummala, "Magnetic materials and design trade-offs for high inductance density, high-Q and low-cost power and EMI filter inductors", in *2016 Proceedings 66th ECTC*, pp. 1297-1302, Las Vegas, NV, 2016.

Awards

1. CPMT ECTC Student Travel Award in 2015
2. GT-PRC Outstanding GRA Award, (June, 2016)
3. GT-PRC Outstanding GRA Award, (October, 2016)

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