HIGH EFFICIENCY SWITCHING CMOS POWER AMPLIFIERS FOR WIRELESS COMMUNICATIONS

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By

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HIGH EFFICIENCY SWITCHING CMOS POWER AMPLIFIERS FOR WIRELESS COMMUNICATIONS

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SUMMARY

High-efficiency performance is one of the most important requirements of power amplifiers (PAs) for wireless applications. However, the design of highly efficient CMOS PAs for watt-level applications is a challenging task. This dissertation focuses on the development of the design method for highly efficient CMOS PAs to overcome the fundamental difficulties presented by CMOS technology.

In this dissertation, the design method and analysis for a high-power and high-efficiency class-E CMOS PA with a fully integrated transformer have been presented. This work is the first effort to set up a comprehensive design methodology for a fully integrated class-E CMOS PA including effects of an integrated transformer, which is very crucial for watt-level power applications. In addition, to improve efficiency of cascode class-E CMOS PAs, a charging acceleration technique is developed. The method accelerates a charging speed to turn off the common-gate device in the off-state, thus reducing the power loss. To demonstrate the proposed cascode class-E PA, a prototype CMOS PA was implemented in a 0.18-μm CMOS process. Measurements show an improvement of approximately 6% in the power added efficiency. The proposed cascode class-E PA structure is suitable for the design of high-efficiency class-E PAs while it reduces the voltage stress across the device.

CHAPTER 1

INTRODUCTION

1.1. Background

Wireless applications have grown quickly to become significant markets due to the advancements in wireless devices. Such applications include global systems for mobile communications (GSM), general packet radio service (GPRS), wideband code division multiple access (WCDMA), wireless local area network (WLAN), enhanced data rates for GSM evolution (EDGE), worldwide interoperability for microwave access (WiMAX), automotive radar, and the like. Figure 1 shows the wireless communication trends with generation progress. As the generation moves on, many standards have been introduced and data rate is increased.

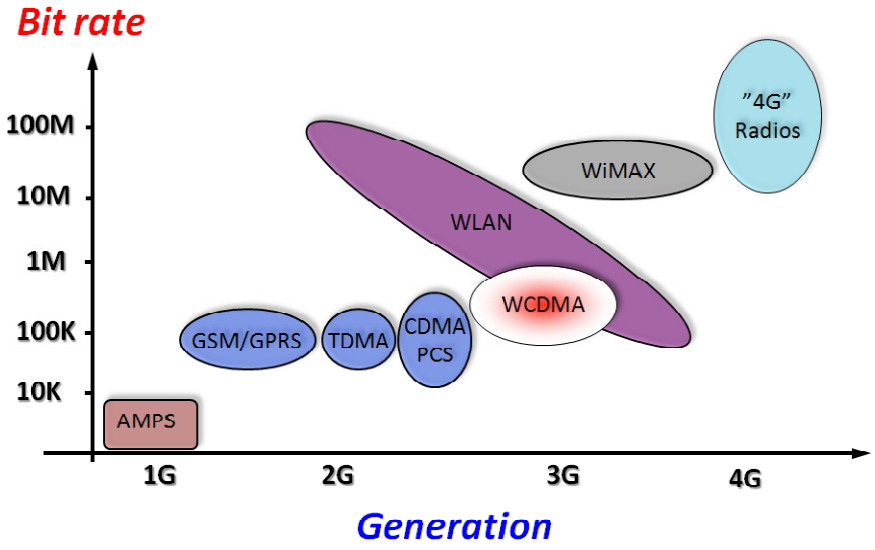


Figure 1. Evolution of wireless communications.

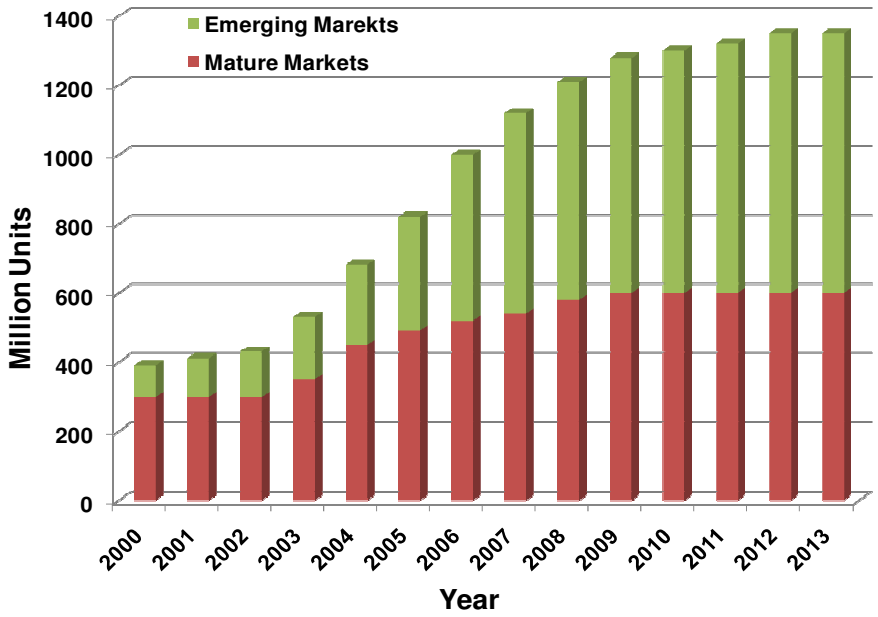


Figure 2. Output power requirements of various standards.

Mobile terminal is a huge market in wireless communications. Figure 2 describes a mobile handset shipment in each year. Even though the market is expected to get saturated around 2013, it will reach around 1.3 billion units due to emerging markets [1].

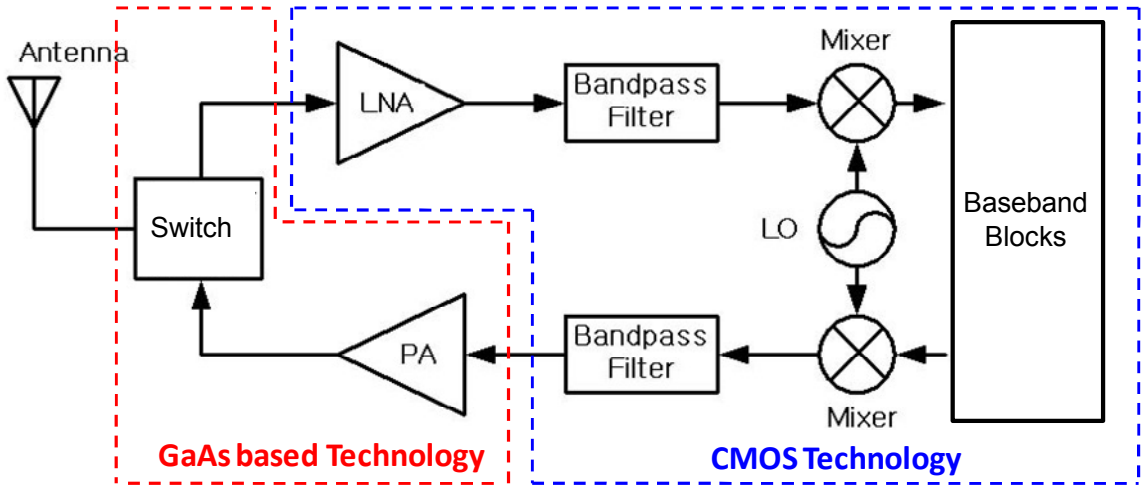


Figure 3. Fundamental functional building blocks for wireless communications.

Fundamental functional building blocks for wireless communications are shown in Figure 3. The advance in low-cost complementary metal-oxide-semiconductor (CMOS) technology has made it a natural choice for radio frequency (RF) transceivers in wireless applications. Its progress has enabled the integration of baseband and other functional blocks. CMOS technology will be the most feasible solution for full integration on a single die, reducing package form factors and their costs. In addition, CMOS technology provides good thermal characteristics and a low-cost advantage owing to its matured process technology as well as a high level of integration. However, still CMOS power amplifiers (PAs) design is a challenging task for full integration. Although some efforts for full integration have been reported, they are only for PAs with low output power [2]-[5]. Also, the performance of CMOS PAs is not good enough for some applications. Furthermore, when PAs are integrated with other functional blocks, isolation needs to be improved. Therefore, compound semiconductor-based PAs prevail in the wireless market due to technological difficulties.

In PAs, the performance issues output power, efficiency, linearity, gain, and reliability. In constant envelope systems, such as GPRS and GSM, the demand of high-efficiency performance has been a priority to extend battery lifetime. For highly efficient operation, nonlinear switching PAs are attractive due to their high DC-to-RF conversion efficiency. High efficiency improves the operation time and reliability of RF transceivers.

On the other hand, in envelope-varying systems, such as WCDMA, WLAN, EDGE, and WiMAX, PAs need to operate linearly to modulate the amplitudes of the signals. The linear PAs amplify the input signals linearly, but they have the drawback of low efficiency, resulting in reduced battery lifetime. To meet the linearity and efficiency

requirements of the systems simultaneously, switching PAs can be utilized with linearization techniques. Envelope elimination and restoration (EER) technique and outphasing power amplification are two major linearization techniques to create amplitude modulated signals using nonlinear switching PAs [6], [7]. The EER system changes a supply voltage of a nonlinear PA according to the amplitude of the signal since the envelope of the RF output signal is proportional to the supply voltage and the efficiency performance is independent of the supply voltage. The outphasing power amplification, also called linear amplification using nonlinear components (LINC), combines the outputs of two switching PAs [8], [9]. The summed output can generate a modulated signal by changing the phase difference between these two input signals.

Although the demands for the design of high efficiency switching PAs have rapidly increased during the last decade, their implementations using CMOS technology are greatly challenging tasks for wireless applications because of low breakdown voltage [10] and lossy substrate compared to III-V technology [11]. This dissertation consists of two contributions for fully integrated highly efficient watt-level switching CMOS PAs. First, the analysis and design of high power class-E CMOS PAs will be discussed, and the measurement results will be demonstrated. Second, the charging acceleration technique for highly efficient class-E CMOS cascode PAs will be proposed.

1.2. Organization

This dissertation consists of five chapters:

Chapter 1 is the introduction of wireless market trend, and the requirement of switching CMOS PAs for wireless communications, and the motivation of this dissertation.

Chapter 2 reviews typical classes of PAs and linearization techniques for switching PAs. The chapter focuses on the highly efficient operation of switching CMOS PAs.

Chapter 3 discusses technical difficulties and prior arts to overcome these problems. Two main problems, low breakdown of CMOS devices and low quality factor of passive structure using CMOS process are presented.

Chapter 4 presents the analysis of design of high power class-E CMOS PAs integrated with on-chip transformer. A prototype PA design based on the presented analysis is described and verified by measurement results. It is shown that the design procedure optimizes the impedance looking into the transformer for high power and high efficiency.

In Chapter 5, the transition power loss of cascode class-E topology using the suggested simplified model is introduced. Then a charging acceleration technique is presented to minimize this power loss without adding lumped element. The implementation results of prototype PAs are presented. The proposed BS-cascode class-E PA structure embedding a charging acceleration technique shows performances improvement while it reduces the voltage stress across the device.

Chapter 6 concludes the whole dissertation.

CHAPTER 2

RF POWER AMPLIFIERS

2.1. Introduction

The PAs are categorized to several classes of the operation based on the voltage and current waveforms at the drain node. The operation classes can be divided into two main types. Conventional transconductance PAs represent to class-A, B, AB, and C PAs. In these types of PAs, the device operates as a voltage-controlled current source. Conventional switching PAs refer to class-D, E, and F. In the operation of the switching PAs, the device is assumed to operate as either an open switch or a closed switch with a low resistance.

2.2. Transconductance Power Amplifiers

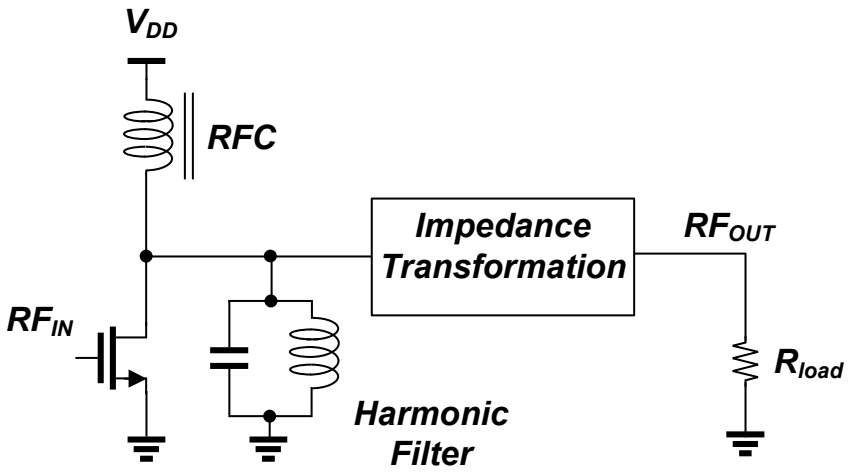


Figure 4. Schematic of a transconductance PA.

Figure 4 shows a typical transconductnace PA. The RF choke is assumed to allow only a DC current. The output load conducts only AC current through DC-coupling capacitor. The harmonic filter provides very high impedance at the fundamental frequency and very low impedance at the harmonic frequencies. Therefore, the drain voltage waveform of the device will be sinusoidal regardless of the current waveform driven by the device. The impedance transformation network provides the necessary impedance to the device output.

2.2.1. Class-A Power Amplifiers

Class-A PAs are highly linear PAs. The DC supply voltage is biased at the mid-point of maximum allowable voltage. Also, PA DC current is constructed using the exact mid-point of the linear range as the bias point. If the driving RF signal is perfectly sinusoidal, then the output voltage and current will also be sinusoidal without any harmonic contents. Figure 5 shows the typical voltage and current waveforms and load-line. The current waveform has no distortion and clipping. The device conducts the current all the time and has a conduction angle, α, of 2π. In load-line analysis, the device is assumed as an ideal voltage-controlled current source, and any output parasitics of the device are considered to be part of the external output network including an impedance transformer and harmonic filter. Therefore, the output capacitance of the device will be incorporated into the output network, which means the load value is purely real. For the simplicity of the analysis, it is assumed that the knee voltage, V_{knee}, is negligible. In optimally matched condition, the RF fundamental output power is given by:

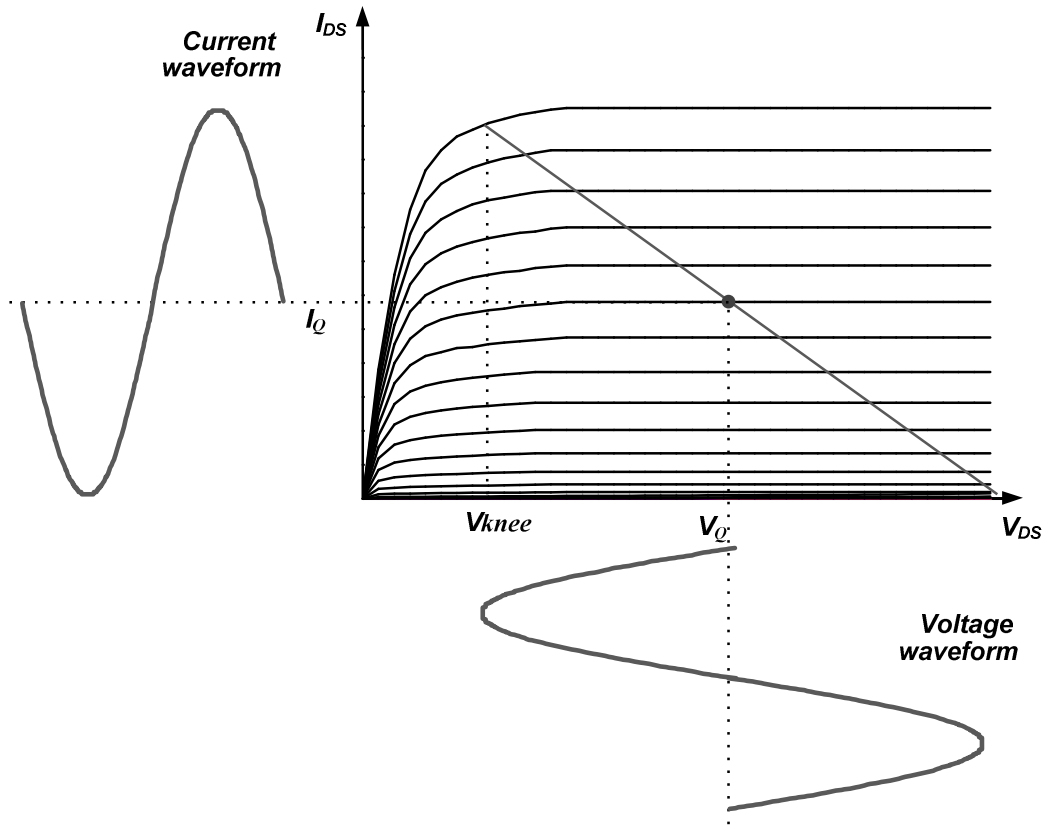


Figure 5. Voltage and current waveforms and load-line of a class-A PA.

$$P_{OPT} = \frac{1}{2} V_{DC} I_{DC}. \tag{2.1}$$

Therefore, class-A PAs can achieve a maximum efficiency of 50%. The dissipated power of the time cycle can be defined as

$$P_{Loss} = \frac{1}{2\pi} \int i_{DS}(\omega t) v_{DS}(\omega t) d(\omega t). \tag{2.2}$$

The minimum power loss of class-A through a conductive channel PA is 50%. Because the DC current is biased at the mid-point of maximum current peak, large quiescent flows, resulting in low efficiency. Due to low efficiency performance, simple class-A PAs are not widely used for typical wireless applications.

2.2.2. Class-AB, B, C Power Amplifiers

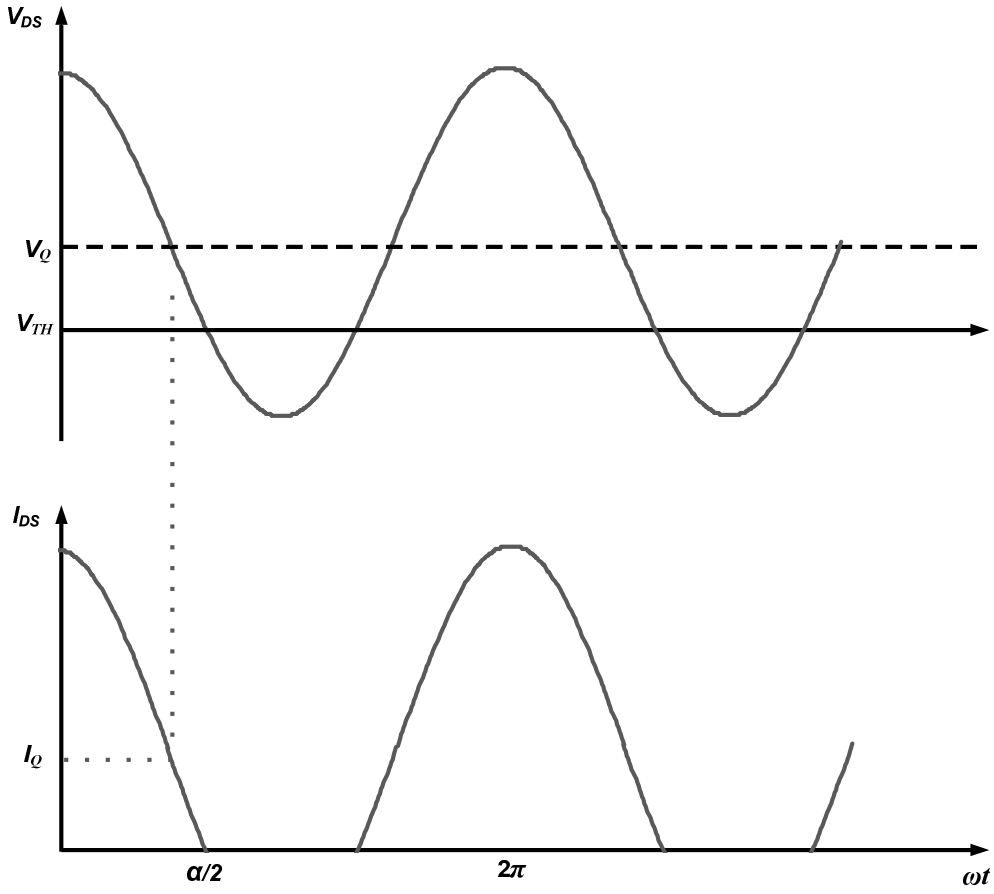


Figure 6. Voltage and current waveforms with reduced conduction angle.

As shown in equation (2.2), to minimize the power loss due to the overlapping of current and voltage waveforms, at least one of the waveforms should be non-sinusoidal. If the gate is biased to a quiescent point, I_Q, toward cut-off region, the clipping occurs due to the limited α, as shown in Figure 6. The entire angle of conduction is represented by α. These distortion of the current waveform generates harmonic, resulting in poor linearity. On the other hand, because the current is zero at the part of the cycle, no power dissipation through the conductive channel exists, as shown in equation (2.2).

The current waveform can be expressed as [8]:

$$i_D(\theta) = I_Q + \left(I_{Max} - I_Q\right)\cos\theta, \qquad -\frac{\alpha}{2} < \theta < \frac{\alpha}{2}$$

$$= 0, \qquad -\pi < \theta < \frac{\alpha}{2} \text{ and } -\frac{\alpha}{2} < \theta < \pi. \tag{2.3}$$

where $\cos(\alpha/2) = -I_Q/\left(I_{Max} - I_Q\right)$, so equation (2.3) can be simplified as

$$i_D(\theta) = \frac{I_{Max}}{1 - \cos\left(\frac{\alpha}{2}\right)}\left(\cos\theta - \cos\left(\frac{\alpha}{2}\right)\right). \tag{2.4}$$

Equivalent DC current can be given by

$$I_{DC} = \frac{1}{2\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{Max}}{1 - \cos\left(\frac{\alpha}{2}\right)}\left(\cos\theta - \cos\left(\frac{\alpha}{2}\right)\right) d\theta$$

$$= \frac{I_{Max}}{2\pi}\frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)}{1 - \cos\left(\frac{\alpha}{2}\right)}. \tag{2.5}$$

The equivalent DC current will be reduced as α is decreased. The magnitude of the fundamental current , I_1, can be obtained as

$$I_1 = \frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{Max}\cos\theta}{1 - \cos\left(\frac{\alpha}{2}\right)}\left(\cos\theta - \cos\left(\frac{\alpha}{2}\right)\right) d\theta$$

$$= \frac{I_{Max}}{2\pi}\frac{\alpha - \sin\alpha}{1 - \cos\left(\frac{\alpha}{2}\right)}. \tag{2.6}$$

The device in the operation of class-AB PA conducts more than 50% of the cycle ($\pi < \alpha < 2\pi$). If it conducts 50% of the cycle ($\alpha = \pi$), it is denoted class-B PA, and if it conducts less than 50% of the cycle ($\alpha < \pi$), it is class-C PA.

The fundamental output power at the output load can be given by

$$P_1 = \frac{V_{DD}}{\sqrt{2}}\frac{I_1}{\sqrt{2}} = \frac{V_{DD}I_{Max}}{4\pi}\frac{\alpha - \sin\alpha}{1 - \cos\left(\frac{\alpha}{2}\right)}. \tag{2.7}$$

The DC power consumption can be expressed by

$$P_{DC} = V_{DD}I_{DC} = \frac{V_{DD}I_{Max}}{2\pi}\frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)}{1 - \cos\left(\frac{\alpha}{2}\right)}. \tag{2.8}$$

The efficiency of the output load is defined by

$$\eta = \frac{P_1}{P_{DC}} = \frac{\alpha - \sin\alpha}{4\sin\left(\frac{\alpha}{2}\right) - 2\alpha\cos\left(\frac{\alpha}{2}\right)}. \tag{2.9}$$

The maximum efficiency of class-B operation is 78.5%. In case of class-AB operation, the maximum efficiency is between 50% and 78.5%. For the class-C condition, the efficiency can achieve 100% with α=0 because the overlap between voltage and current is reduced as implied in (2.2). Although the efficiency is increasing as the conduction angle is reduced to low values, this is accompanied by output power reduction because I_1 approaches zero. The output power is also zero with α=0.

2.3. Switching Power Amplifiers

In ideal switching operation, the switch is either completely turn-on (short circuit) or completely turn-off (open circuit). In addition, the transition between two states should occur instantly. Figure 7 shows a generalized schematic of a switching PA. The load network of a switching PA minimizes the power loss by always keeping one of either the voltage or the current zero. Theoretically, class-D, E, and F PAs have 100% DC-to-RF conversion efficiency. At no time ideally current and voltage coexist, which means no energy is wasted as heat in device. Only the current exists in the on-state, while only the

voltage exists in the off-state. In ideal switching conditions, DC energy converts into the fundamental output power without transferring into harmonic powers through the load network of the switching PA.

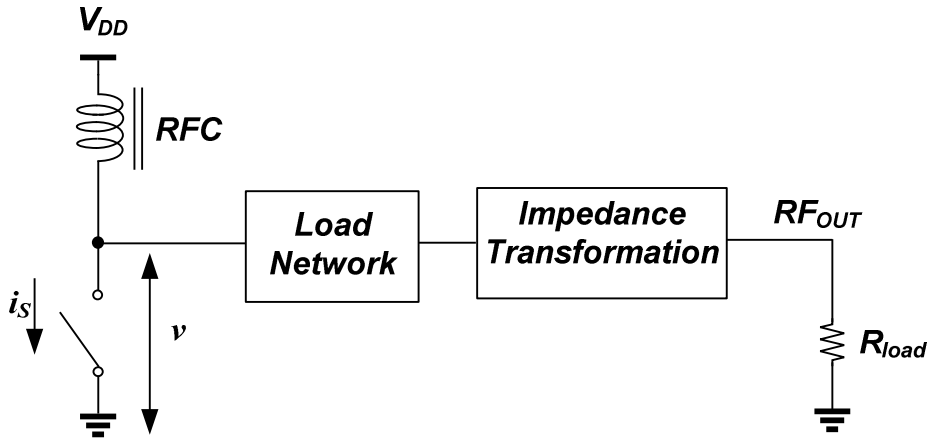


Figure 7. Schematic of a switching PA.

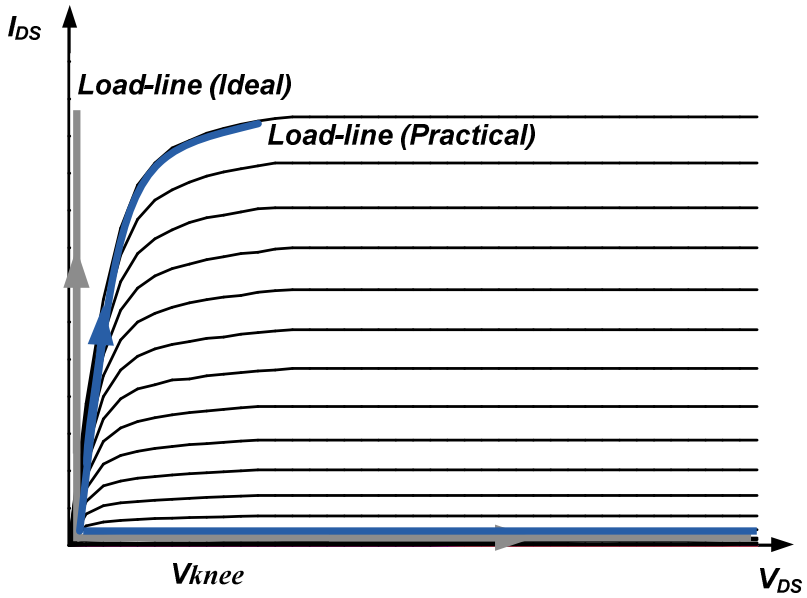


Figure 8. Load-line of a switching PA.

To obtain this condition, device is assumed to operate either in the triode region (low resistance) or the cut-off region (open circuit) by driving a sufficiently large signal. In practical realizations, it is not possible to voltage keep zero in the on-state. In the triode region, small voltage exists due to r_{ON} resistance, resulting in the power loss in the on-stage. Figure 8 shows the load-line in the switching PA. Another power loss in the device is due to the finite transition from between on-stage to off-state and vice versa.

2.3.1. Class-D Power Amplifiers

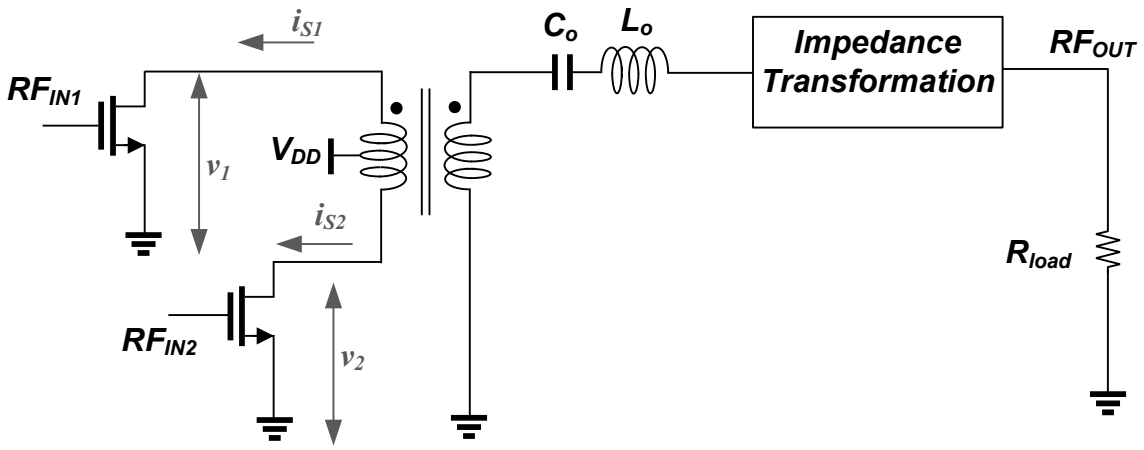


Figure 9. Schematic of a voltage-mode class-D PA.

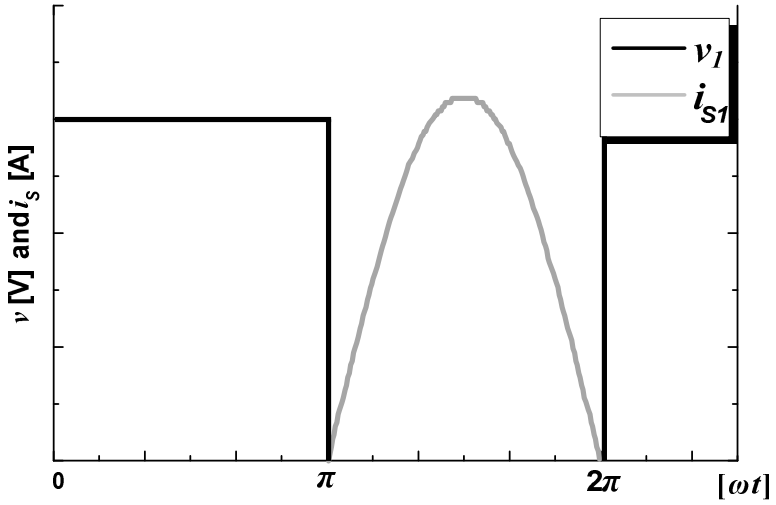


Figure 10. Waveforms of a voltage-mode class-D PA.

A class-D PA uses a pair of devices driven in a push-pull mode and an output load network to tune the fundamental frequency. The devices operate as a two-pole switch that defines either a square voltage of rectangular current waveforms.

Figure 9 shows a schematic of voltage-mode class-D PA. In this configuration, two devices are alternately switched on and off. The load network contain resonator to remove the harmonic contents of the waveforms, resulting in a sinusoidal output. The voltage waveform is a square wave, while the current waveform is a sinusoidal wave as shown Figure 10. If switch "A" conducts a positive half-sinusoidal, switch "B" conducts a negative half-sinusoidal, which combined together to form a full sinusoidal at the output load.

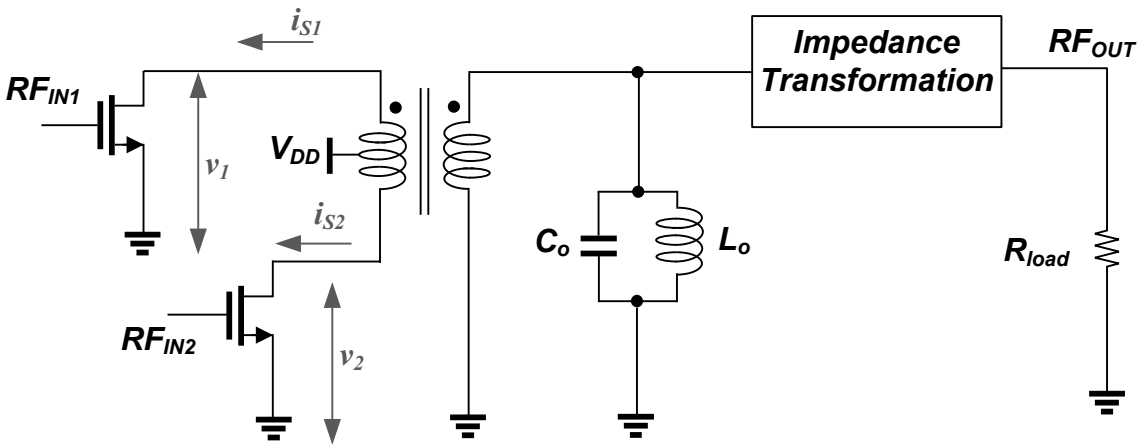


Figure 11. Schematic of a current-mode class-D PA.

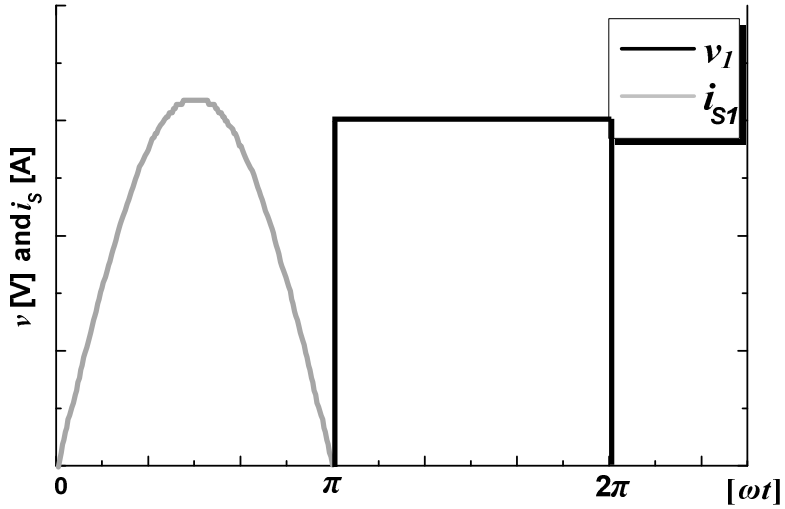


Figure 12. Waveforms of a current-mode class-D PA.

Figure 11 shows a schematic of current-mode class-D PA, which is the dual of voltage-mode class-D PA because the voltage and current waveforms are interchanged. The voltage waveform is a sinusoidal wave, while the current waveform is a square wave, as shown Figure 12. This topology is sometimes called a class-D^{-1} PA. The

fundamentally tuned resonator is connected in a parallel, instead of a series tuned resonator in the voltage-mode class-D PA.

Due to non-overlapping between the voltage and current waveforms at any time of the cycle, class-D PA achieves 100% efficiency. Regarding the switching device, device parasitic capacitances should be concerned in RF applications. In practical class-D PAs, because of a discharge of large device output parasitic capacitance, voltage and current can be coexisted, and then it generates device loss. Since large devices are required to generate high output power, this problem is significant in watt-level applications. In addition, the susceptance due to this capacitance increases with frequency, the class-D PA is rarely used above VHF band.

2.3.2. Class-E Power Amplifiers

The class-E power amplifier was introduced by Sokals in 1975 and has been used widespread applications due to its high efficiency characteristic and design simplicity. Although the class-E PA topology is possible to operate push-pull configuration, it generally has a single-ended configuration. Figure 13 shows a circuit schematic of a typical class-E PA. The RF choke is assumed to allow only a constant DC current with infinite impedance. C_O and L_O are designed to form a series resonator, and its loaded quality factor is high enough that the output load current is purely a sinusoidal wave. *C* and *jX* are designed based on two class-E switching conditions [12]-[14].

1) voltage across the switch returns to zero at the end of the off state (i.e., $v(\omega t) = 0$).
2) the first derivative of the voltage across the switch is zero at the end of the off stage (i.e., $dv(\omega t)/d(\omega t) = 0$).

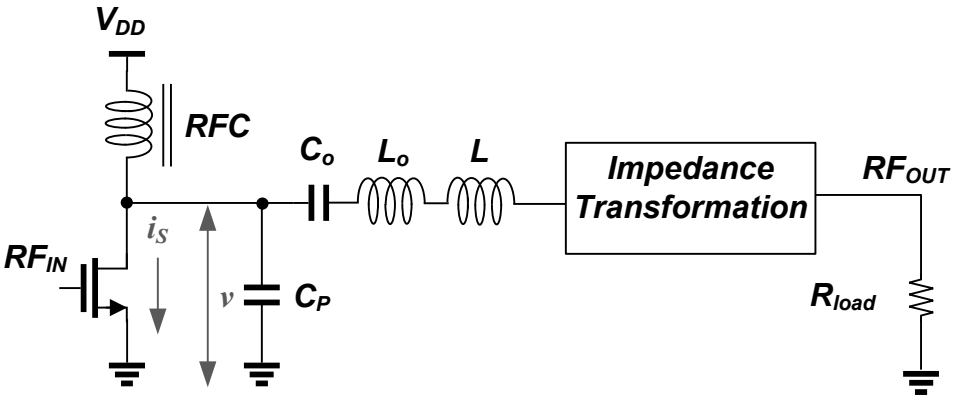


Figure 13. Schematic of a class-E PA.

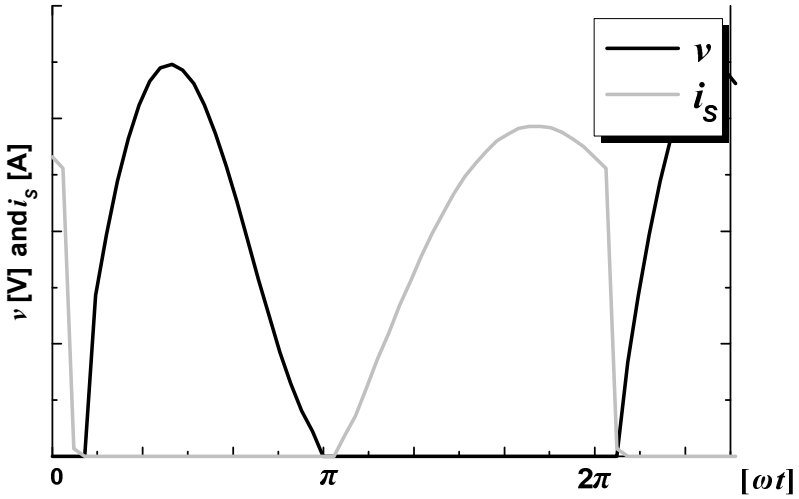


Figure 14. Waveforms of a class-E PA.

The current of the switching network is assumed sinusoidal and is given by

$$i_{load}(\omega t) = I_{load} \sin(\omega t + \varphi). \tag{2.10}$$

where I_{load} is the current amplitude and φ is the initial phase shift.

When the switch is on during $0 \leq \omega t < \pi$ in 50% duty cycle, the capacitor current $i_C(\omega t)$ through the capacitance and the voltage across the switch are equal to zero, i.e.

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d(\omega t)} = 0. \tag{2.11}$$

Because $i_S(0) = 0$, the initial value for I_O can be found using (2.10)

$$I_O = i_S(0) - i_{load}(0) = -I_{load}\sin\varphi. \tag{2.12}$$

The current $i_S(\omega t) = I_O + i_{load}(\omega t)$ flowing through the switch can be written as

$$i_S(\omega t) = I_{load}\,(\sin(\omega t + \varphi) - \sin\varphi). \tag{2.13}$$

When the switch is off during $\pi \leq \omega t < 2\pi$, the switch current $i_S(\omega t)$ is 0, and the capacitor current, $i_C(\omega t) = I_O + i_{load}(\omega t)$, can be rewritten as

The capacitor voltage can be given by

$$v(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_C(\omega t)\, d(\omega t)$$

$$= \frac{I_{load}}{\omega C}[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi]. \tag{2.14}$$

Voltage and current waveforms are shown in Figure 14. Appling the first optimum switching conditions, φ can be determined as

$$\varphi = \tan^{-1}\left(\frac{-2}{\pi}\right) = -32.482^{\circ}. \tag{2.15}$$

In addition, for optimum design conditions, the following design parameters can be determined as [12]-[14]

$$R_{load} = 0.5768\frac{{V_{DD}}^2}{P_{T_{IN}}}, \tag{2.16}$$

$$L = 1.1525\frac{R_{load}}{\omega}, \tag{2.17}$$

$$C = \frac{0.1836}{\omega R_{load}}. \tag{2.18}$$

Main advantage of the class-E PA is that the output parasitic capacitance is absorbed into the required the parallel capacitance for class-E switching conditions. In addition, its implementation is simple and has a compact form factor. Thus class-E PAs are widely used for RF applications.

2.3.3. Class-F Power Amplifiers

Class-F and Class-F^{-1} topology utilize harmonic terminations to shape voltage and current waveforms. The class-E PA employs load network in time domain, while the load network in class-F PA is utilized in frequency domain.

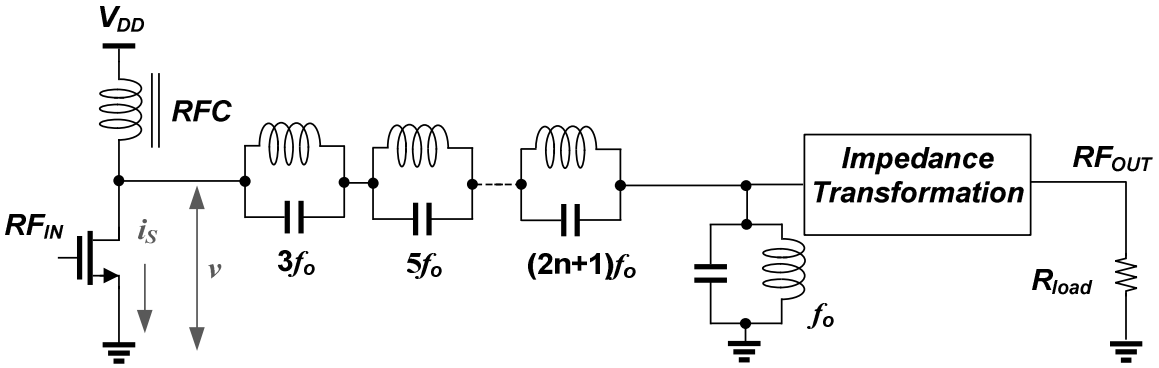


Figure 15. Schematic of a class-F PA.

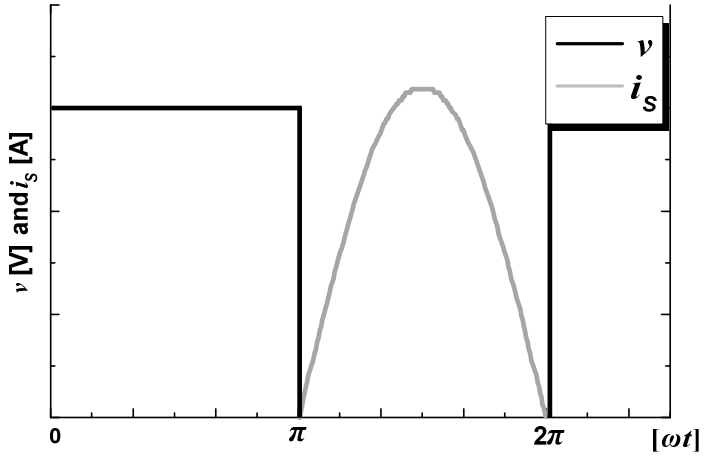


Figure 16. Waveforms of a class-F PA.

Ideal class-F PA is constructed with an infinite number of series odd harmonic terminations and a parallel resonator of the fundamental frequency, as shown in Figure 15. The voltage waveform is a square waveform, and current waveform is a half-sinusoidal waveform, as shown in Figure16. As a result, the current and voltage waveforms do not overlap simultaneously. At the output load, a purely sinusoidal current flows.

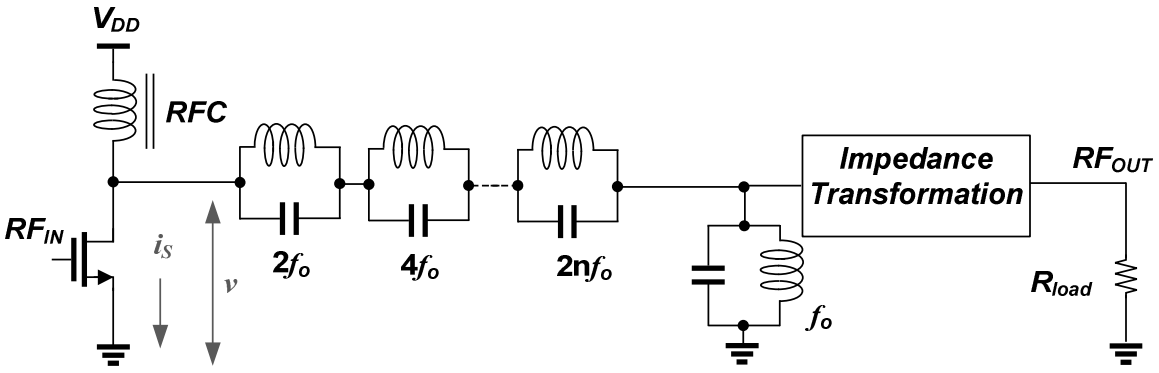


Figure 17. Schematic of a class-F^{-1} PA.

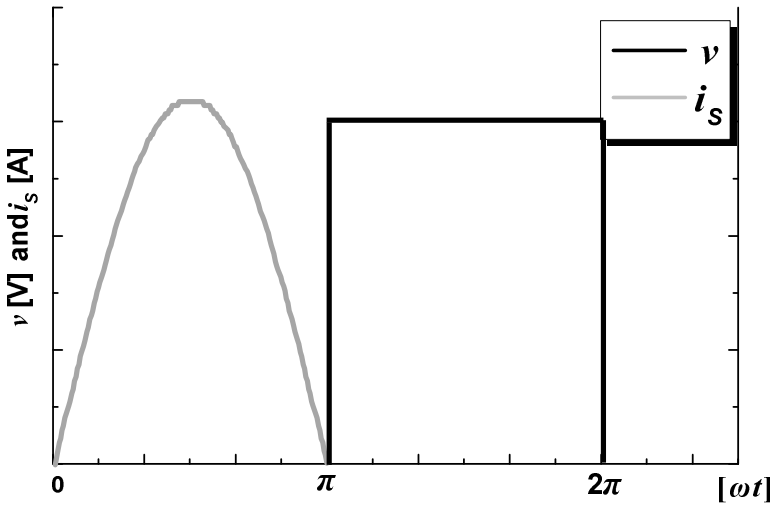


Figure 18. Waveforms of a class- F^{-1} PA.

Like that in the class-D^{-1} PA, the class-F^{-1} PA is the dual of class-F PA because the voltage and current waveforms are interchanged, as shown in figure 18. The voltage waveform is a sinusoidal wave, while the current waveform is a square wave. Ideal class-F^{-1} PA is constructed with an infinite number of series even harmonic terminations and a parallel resonator of the fundamental frequency, as shown in Figure 17. The voltage waveform is a half-sinusoidal waveform, and current waveform is a square waveform. However, these harmonic circuitries are complicated and bulky. In practice, the class-F PAs are usually implemented using only up to third harmonic termination by scarifying a little bit of the efficiency performance.

2.4. Linearization Techniques for Switching Power Amplifiers

Linearity of a PA represents the ability to restore the signal throughout the PA. The amplitude and phase of the input signal should be reconstructed at the output load without any distortions. In general, the performance of linearity is conflict with the performance of efficiency. Switching PAs have poor performance of linearity. In switching PA, since they are assumed to operate with a large signal input, the amplitude of the output signal is not a function of the input signal and is constant with varying the amplitude of the input signal.

Switching PAs can be directly applied to the system employing constant-envelope signals like GSM and GPRS. For the system using envelope-varying signals such as CDMA, EDGE, WLAN, the switching PAs can be employed with linearization techniques. Two major techniques are polar modulation and outphasing power amplification. Because CMOS linear PA has a poor efficiency performance, recently,

many efforts related to these techniques have been going on. Thus, high efficiency switching PAs can be widely used for various systems.

2.4.1. Outphasing Power Amplifiers

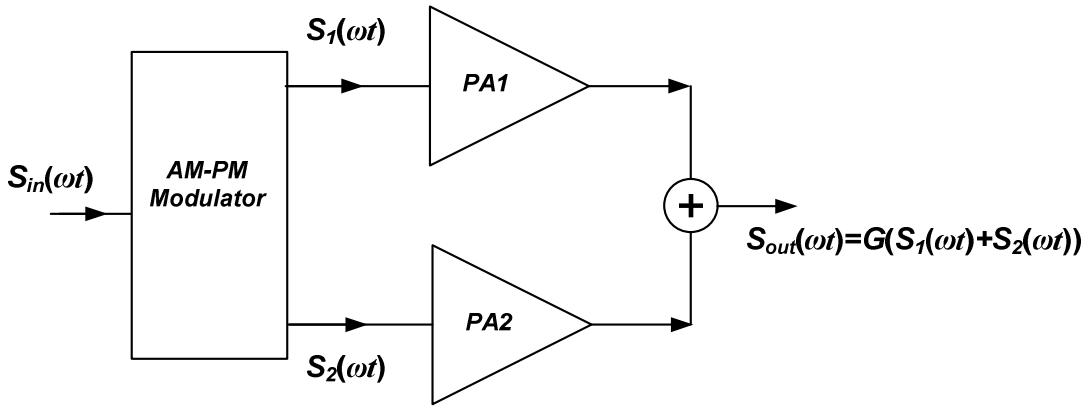


Figure 19. Block diagram of an outphasing PA.

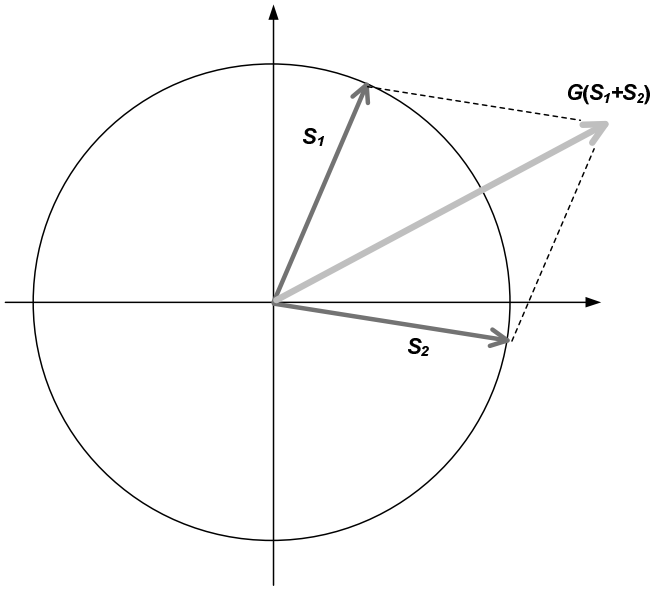


Figure 20. Vector decomposition diagram of an outphasing PA.

The technique of the outphasing PA dates back to the 1930s, and this idea is firstly developed by Henri Chireix. Since two nonlinear PAs are employed to amplify two input signals with different phase, it is sometime called LINC. Figure 19 describes the signal decomposition of an outphasing PA. The input signal, $S_{in}(\omega t)$, is the amplitude and phase modulated signal and expressed by

$$S_{in}(\omega t) = \mathrm{A}(\omega t)\cos(\omega t) \tag{2.19}$$

where $\mathrm{A} = \omega t + \varphi$. The AM-PM modulator converts the amplitude modulated signal into two phase-modulated signals, $S_1(\omega t)$, and $S_2(\omega t)$, given by [8]

$$S_1(\omega t) = \cos[\omega t + \cos^{-1}(A(\omega t))]\,,$$
$$S_2(\omega t) = \cos[\omega t - \cos^{-1}(A(\omega t))]. \tag{2.20}$$

Two switching PAs can be used to amplify each signal with high efficiency. If the gain of each PA is G, the output signal after the power combiner can be written by

$$S_{out}(\omega t) = G[S_1(\omega t) + S_2(\omega t)]$$
$$= 2G\mathrm{A}\cos(\omega t) \tag{2.21}$$

Figure 20 shows a vector diagram of the signal decomposition and reconstruction of the outphasing PA. The key elements of this architecture are the phase modulator and power combiner. The phase and amplitude information generated from the phase modulator should be reconstituted through the power combiner without any distortion.

2.4.2. Envelope Elimination and Restoration (EER)

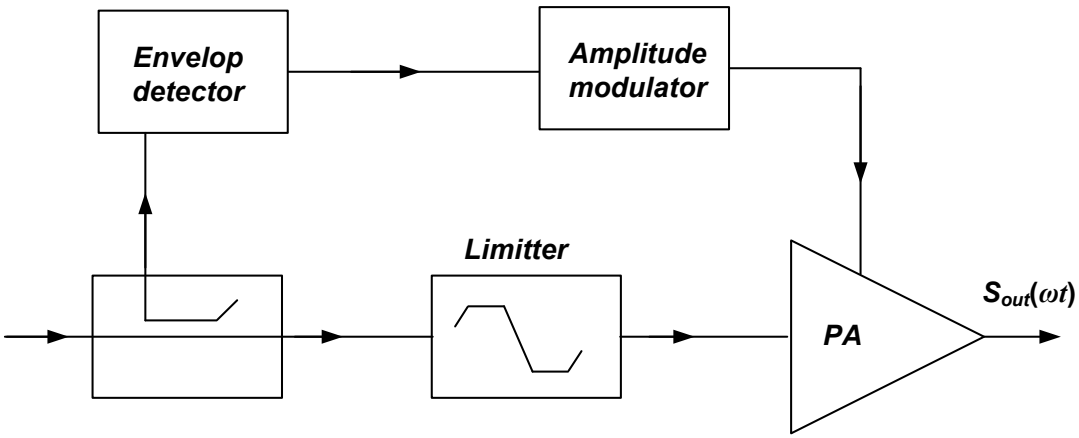


Figure 21. Block diagram of envelope elimination and restoration (EER) system.

The EER technique was originally proposed by Kahn [15] as a more efficient class-AB PA. In this system, the input signal is passed through a limiter eliminating the possibility of AM-PM distortion. Figure 21 shows a block diagram of EER system. The envelope amplitude of the input signal feeds through the other path. If the switching PA is employed, the amplitude of the signal will be controlled by an amplitude modulator. The amplitude modulation is applied to the constant-envelope PA using the amplitude modulator.

CHAPTER 3
CHALLENGES OF CMOS RF POWER AMPLIFIERS

3.1 Introduction

A highly efficient PA is desirable because major power consumption in the front-end comes from the PA. Theoretically, class-D, E, and F switching PAs have 100% efficiency. However, a class-D PA is not suitable at RF because the output capacitance of the transistors causes a significant power loss [16]. Since this power loss can be a critical problem in the high-frequency range, class-D PAs are widely used only for audio frequencies. A class-F PA requires several lumped elements to perform harmonic termination, resulting in complicated circuitry and large size for the integration. A class-E PA has a strong switching operation while it incorporates an output capacitance of a transistor as a part of switching operation. Also, its implementation is simple and has a compact form factor compared to the class-F topology. Thus class-E PAs are widely used for RF applications since they provide high efficiency and circuit simplicity [17]-[20].

Figure 22 shows the circuit schematic of a typical class-E PA with an output network. C_O and L_O are designed to form a series resonator, and C and jX are designed based on the two class-E switching conditions. The RF choke (RFC) is assumed to allow only a constant DC current with infinite impedance at the fundamental frequency and any harmonics. In reality, however, it is difficult to realize an on-chip RF choke because its quality factor is generally poor, which decreases efficiency. Also, an inductor having large inductance requires large area. Metal width should be increased to reduce DC resistance. Therefore, for RF-choke integration it requires large die area, resulting in

increased cost. Hence, a class-E PA using a finite DC-feed inductance should be employed for on-chip design.

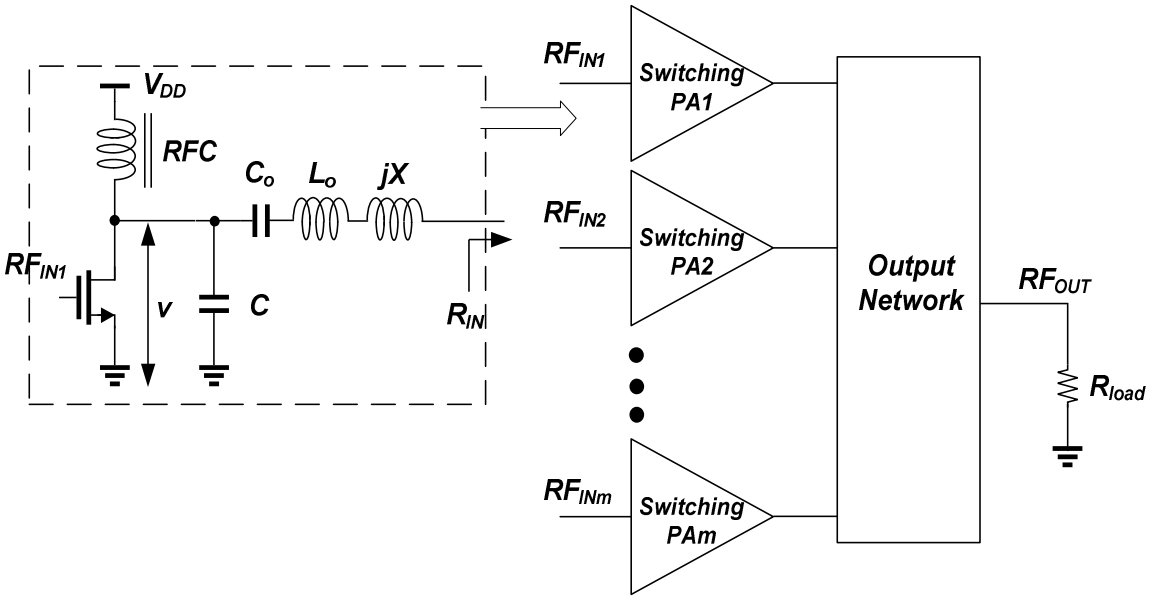


Figure 22. Schematic of a class-E PA with an output network.

As shown in Figure 22, several class-E PAs should be combined for watt-level output power. The output network in Figure 22 provides the necessary impedance transformation from optimum impedance, R_{IN}, to R_{load} for class-E operation. Because a voltage swing is limited due to low breakdown voltage in the CMOS process, a large amount of AC current is required to attain watt-level output power. As a result, a required load resistance should be impractically too small to enable a transistor to provide a large amount of current for watt-level output power. Also, the efficiency of the output network is generally quite poor when the impedance transformation ratio is large. Therefore, several class-E PAs should be effectively combined to reduce the burden of the impedance transformation ratio. Therefore, the output network provides the necessary

impedance transformation as well as power combining.

3.2 Low Breakdown Voltage in CMOS Technology

3.2.1 Low Breakdown Voltage

One of main concerns in a CMOS PA design is low breakdown voltage of CMOS device. Breakdown voltages of CMOS devices are relatively small compared to GaAs device. High-voltage stress across the device can cause reliability problems, such as gate-oxide breakdown, hot carrier degradation, punchthrough, and junction breakdown [10], [21]. Gate-oxide breakdown is caused by high voltage drop across the gate oxide, resulting in an irreversible gate-to-channel short. According to decreasing the gate-oxide thickness in each process generation, gate-oxide breakdown voltage also decreases. The hot carrier effect occurs with sufficient horizontal or vertical electric field. It increases the gate current due to hot carriers such as injected electrons or holes into the oxide. Punchthrough depends on two depletion regions around source and drain touching, resulting in the current flow without any significant gate bias. Junction breakdown is related to drain-substrate *pn*-junction breakdown. With exceeding reverse voltage in the *pn*-junction, the drain current increases abruptly.

In common practice, regarding CMOS PA design, the maximum voltage drop across device's two nodes should be less than twice nominal supply voltage to assure reasonable device and circuit's life-time [22]. On the other hand, along with the progress in CMOS technology, its supply voltage is also scaled down and then its breakdown voltage is also reduced. However, since output power is proportional to the square of the supply voltage, high supply voltage is desirable for high output power. For watt-level output power at

low supply voltage, the necessary load impedance will be quite small, and the impedance transformation will be large. A high supply voltage can reduce the necessary impedance transformation ratio. Also, the battery voltage of mobile terminals is fixed and does not scale down. A cell voltage of the current Lithium-ion (Li-ion) batteries is 3.6 V. Therefore, PAs are often under the increasing voltage stress.

3.2.2 Cascode Topology in CMOS Power Amplifiers

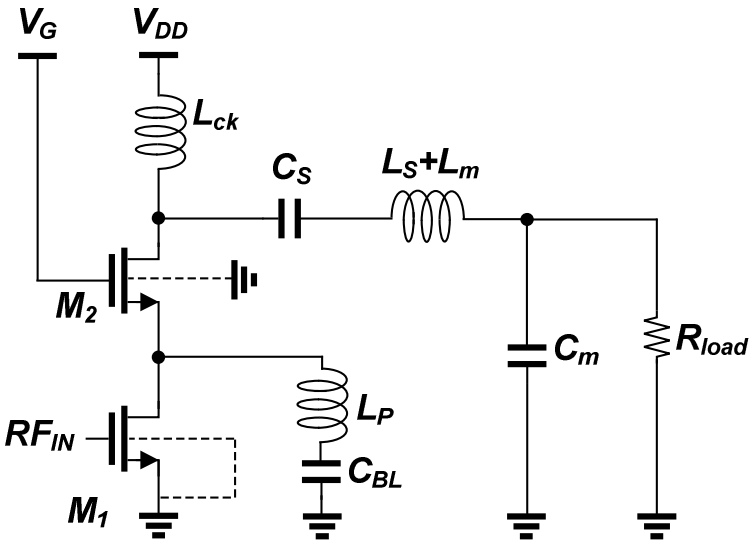


Figure 23. Inductor tuning technique in cascode class-E PA.

As mentioned before, the maximum AC voltage drop across the devices at any node should be below twice the nominal supply voltage. However, in a conventional common-source class-E PA, the drain and gate voltages are out of phase and the voltage difference between two terminals will be large. In the class-E operation especially, the peak drain voltage can be as large as 3.56 times the DC supply value, resulting in severe stress

between two terminals. The device staking is a way to reduce the voltage stress of each device without decreasing supply voltage. Large drain voltage can be divided by all stacked devices. Cascode topology is one example of a device stacking [18], [23], [24]. However, there are additional power losses as a property of a cascode configuration in a class-E PA. In this configuration, two devices should be turned-on or turned-off simultaneously to minimize power loss. However, in practical implementation, two devices cannot be turned-on or turned-off simultaneously. It decreases the efficiency performance. A tuning inductor technique has been proposed to reduce the leakage current of the common-gate device, as shown in Figure 23 [23].

3.3 Low Quality Factor of Passive Structures in CMOS Technology

3.3.1 Low Quality Factor

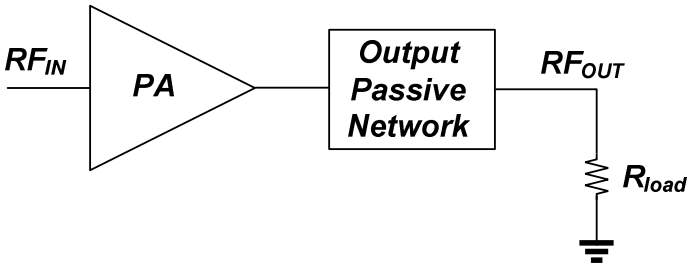


Figure 24. Output passive network of PA.

Another main concern is related to low quality factor of passive structure in CMOS technology. Output passive network is a necessary block to deliver the power from the

PA to output load, as shown in Figure 24. This structure is implemented using metallization layers in a standard CMOS technology. It should have good quality factor to deliver the power efficiently. However, a good passive design using CMOS technology is challenging due to the poor characteristics.

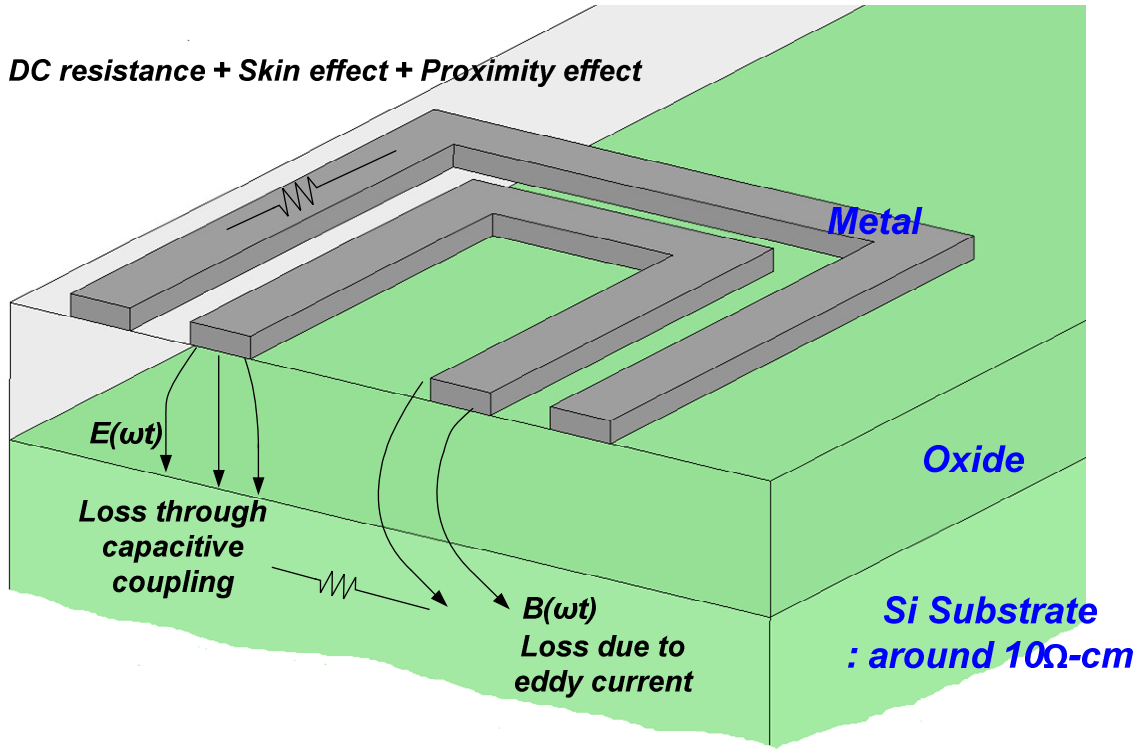


Figure 25. Loss mechanisms in a CMOS Technology.

Figure 25 describes a typical passive structure layout in CMOS technologies including all loss resistors. At low frequencies, DC resistance is a dominant loss. Because current flow generates ohmic losses, the quality factor of a passive structure is governed by the conductivity of metal layers. However, a commercial CMOS 0.18-μm process uses Al metallization instead of Cu metallization, resulting in increased resistivity of the metal tracks due to low conductivity. Generally, DC resistance in CMOS process is higher than that of compound semiconductor process. At high frequencies, because Si-substrate has

low resistivity, substrate loss though magnetic and electric coupling will deteriorate the quality factor of passive structure. The quality factor is mainly affected by the eddy current effect induced in Si substrate. The substrate in the Si technology is one of the great sources of loss due to its low substrate resistivity, typically between 2 and 10Ω/□ [11].

Therefore, due to innate drawbacks of CMOS devices compared to III-V devices, it is extremely challenging to design a highly efficient output passive structure operating at RF frequencies. In addition, the quality factor of an inductor in CMOS will be lower in a single-ended operation compared to that in differential operation [25]. Since the output load is generally a single-ended configuration in the PA design, this effect should be considered for the design of the output passive network. In practical CMOS implementation, substrate parasitic capacitances and resistances should be considered. Figure 26 describes the physical model of an inductor including substrate parasitics. C_{OX} represents the oxide capacitance between the transformer and the substrate. The silicon substrate capacitance and resistance are modeled by C_{si} and R_{si}, respectively. The series branch of C_{OX}, R_{si}, and C_{si} is substituted by R_p and C_p in Figure 26(b) [26].

$$R_P = \frac{1}{\omega^2 {C_{ox}}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{{C_{ox}}^2}, \tag{3.1}$$

$$C_P = C_{ox} \frac{1 + \omega^2 (C_{ox} + C_{si}) C_{si} {R_{si}}^2}{1 + \omega^2 (C_{ox} + C_{si})^2 {R_{si}}^2}. \tag{3.2}$$

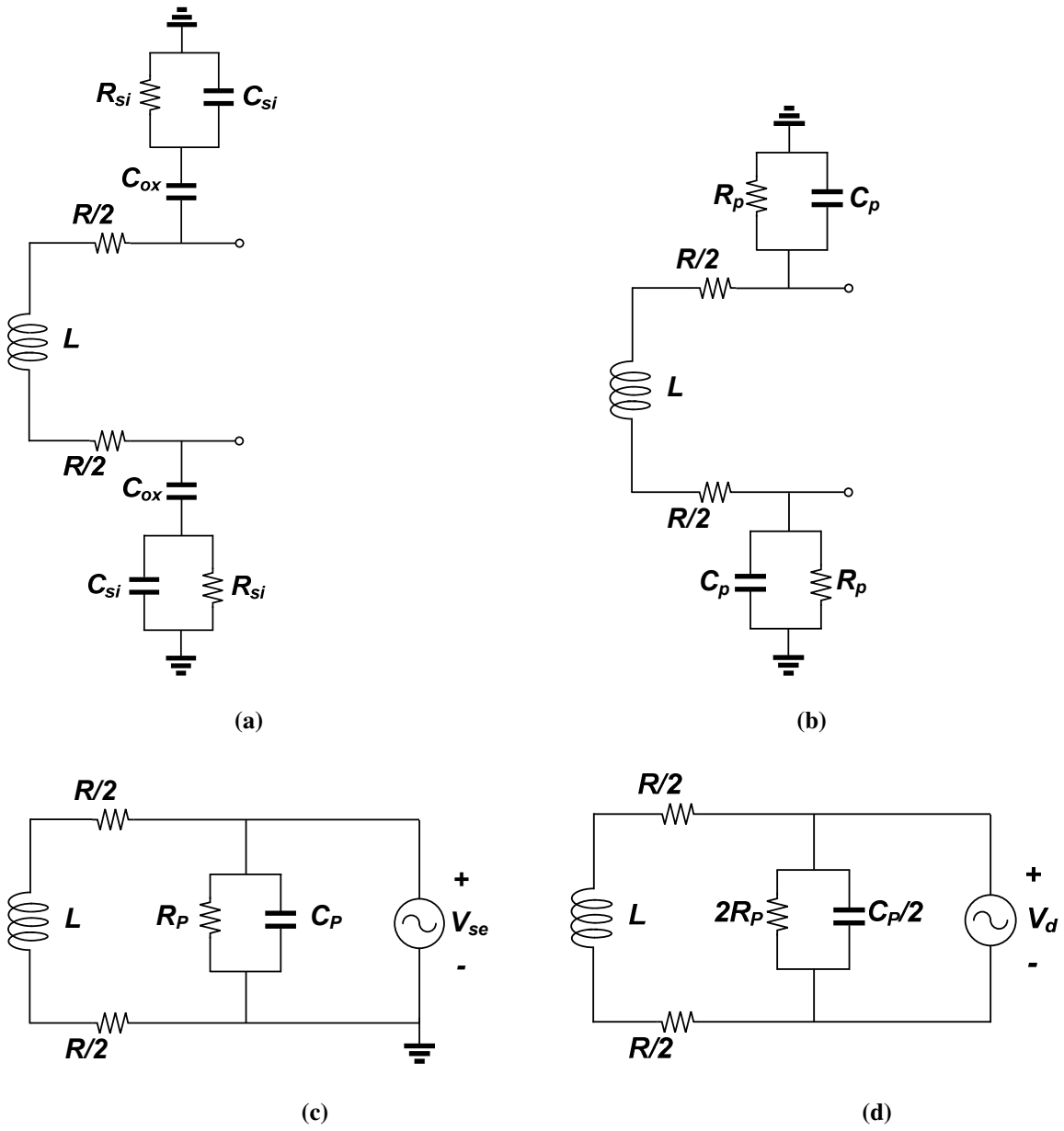
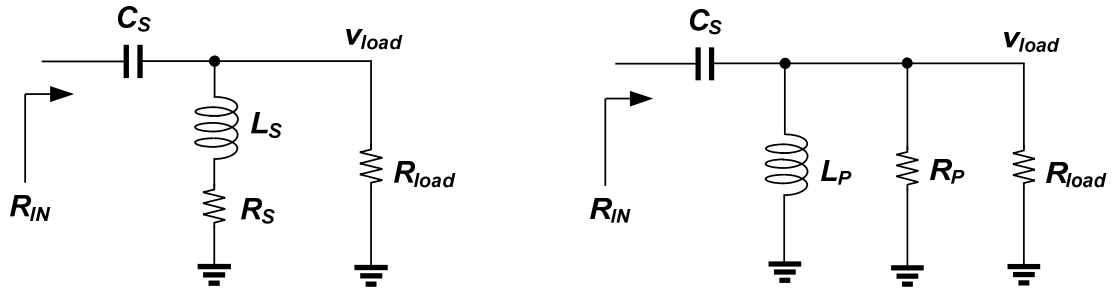


Figure 26. Equivalent transformer model including substrate parasitics. (a) Equivalent transformer model with the combined impedance C_{ox}, C_{si}, and R_{si} (b) substituted by R_P and C_P. (c) Single-ended model. (d) Differential model.

For the single-ended case, one of the ports in the secondary winding is grounded, and the equivalent circuit is shown in Figure 26(c). The impedance of the substrate parasitic is

the parallel combination of R_P, and C_P. For the differential case, the signal exists between two ports in the secondary winding, and the equivalent circuit is shown Figure 26(d). The impedance of the substrate parasitic is twice that of the single-ended case (parallel combination of $2R_P$, and $C_P/2$). Because the impedance due to these parasitic in the differential case is higher than that in the single-ended case, the quality factor of the differential case is higher than that of the single-ended [25]. Thus, the passive efficiency of the inductor when taking a single-ended output is lower than that of the inductor when taking a differential output.

3.3.2 Output Passive Structure in CMOS Technology



(a) **(b)**

Figure 27 (a) Resonant *LC* impedance-transformation network with loss (b) Equivalent parallel network with loss.

Losses of impedance transformation networks are normally functions of the impedance transformation ratio. The higher the impedance transformation ratio is, the higher the loss of the impedance transformation network is. The impedance-transformation ratio r is the ratio of the load impedance, R_{load}, to the transformed

impedance, R_{IN},(R_{load}/R_{IN}). r increases with increasing turn ratio of the transformer (r=n^2 in an ideal transformer). The loss of the transformer is proportional to the turn ratio. As shown in the above figures, *LC* resonant matching is one of the most straightforward means of impedance transformation. Series *RL* network of Figure 27(a) can be replaced by a purely parallel *RL* network of Figure 27(b). We can obtain the unloaded quality factor, Q_{ind} of an inductor

$$Q_{ind} = \frac{R_P}{\omega L_P} = \frac{\omega L_S}{R_S} \tag{3.3}$$

where $R_P = R_S(Q^2 + 1) \cong R_S Q^2$ and $L_P = L_S\big((Q^2 + 1)/Q^2\big) \cong L_S$.

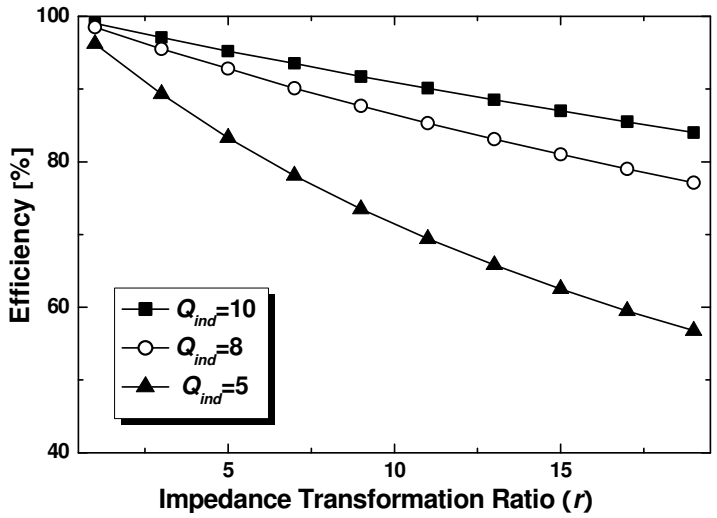


Figure 28. Efficiency versus *r* and inductor *Q* for *L-C* impedance-transformation network.

The impedance-transformation ratio r is the ratio of the load impedance, R_{load}, to the transformed impedance (R_{load}/R_{IN}). The efficiency of impedance transformation network η with r variation can be calculated [27]

$$\eta = \frac{P_{out}}{P_{in}} = \frac{|V_{load}|^2/(2R_{load})}{|V_{load}|^2/(2(R_{load} \| R_P))}$$

$$\cong \frac{1}{1 + \frac{r}{Q_{ind}{}^2}}. \quad (3.4)$$

As shown in the above figure 28, a large impedance transformation results in a large power loss at given *Q* value. Therefore, power combining is a way to reduce the burden of the necessary impedance transformation to get a watt-level output power without increasing n too much. The transformer has the advantage over *LC* output network since it can provide the impedance transformation and power combining simultaneously, resulting in reducing circuit complexity and die area.

Most of the initial works have used external output passive structures such as off-chip components or external baluns to achieve higher quality factor and to improve passive losses [17]-[19], [28]. For an on-chip implementation, the output passive structure can be implemented by transformer [29]-[32] or inductor-capacitor (*LC*) matching network [20]. The transmission line can be another option. However, its implementation using silicon substrate is very lossy. Recently, the distributed active transformer (DAT)-based transformer was successfully demonstrated for a fully integrated watt–level PA [29], [32]. Figure 29 shows an electrical diagram of a class E/F circuit power amplifier using the DAT. The DAT is an extended structure of a transformer-based balun to increase voltage swing at the secondary winding. In the ideal case, the output voltage swing in a differential structure is twice that of a single-ended structure. Adding *N* differential structures in series using multi-primary windings, the output voltage swing at the secondary winding is boosted to 2*N* times the voltage. Class-E/F PA is combined with the DAT to achieve high-efficiency performance. The class-E/F PAs operate the active

device as a switch, and their tuning networks incorporate the output capacitance into the load network as in class-E PAs, but allow improved waveforms by tuning some of the harmonics as in inverse class-F [16]. This structure is required the relatively large passive structures. In addition, circular structure may cause an instability issue due to possible coupling of the input signal feeding line with the transformer [33].

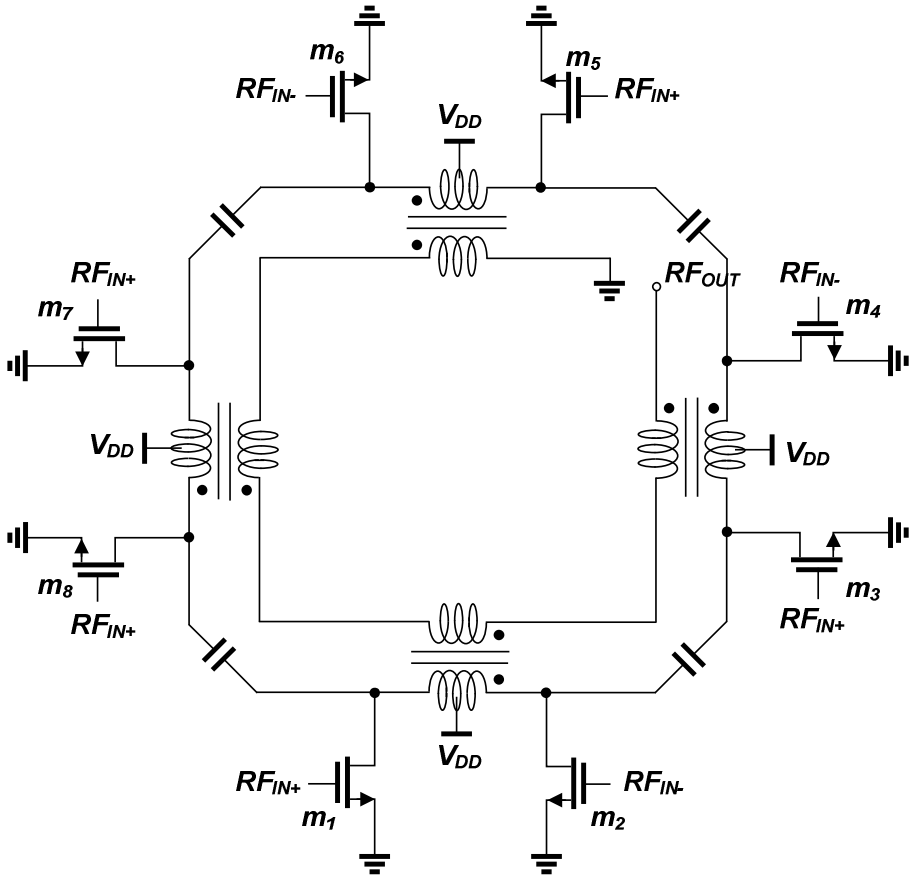


Figure 29. DAT with a switching PA.

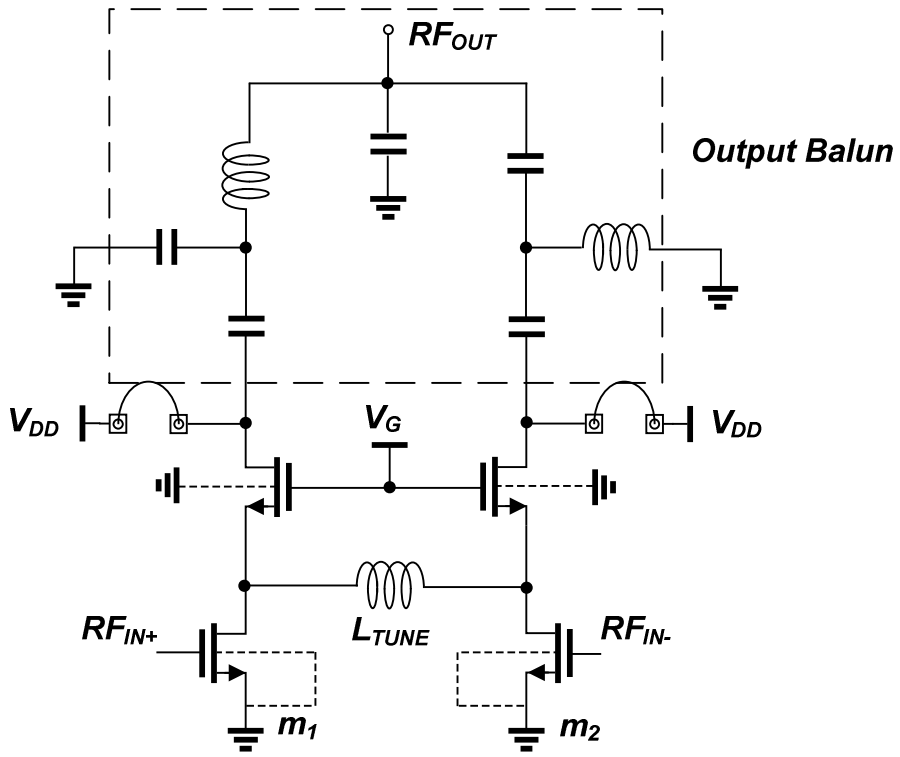


Figure 30. *LC*-Balun with a switching PA

An integrated *LC-CL* lumped balun has been combined to perform signal recombination and impedance matching simultaneously, and also embedding the class-E PA output network in Figure 30 [20]. To minimize power losses due to low *Q* of an on-chip inductor for full integration, an *LC-CL* network is adopted, allowing a minimum number of inductors.

CHAPTER 4

ANALYSIS AND DESIGN OF FULLY INTEGRATED HIGH POWER CLASS-E CMOS POWER AMPLIFIERS

4.1 Introduction

A magnetically coupled transformer is an attractive solution for the output network because it can provide the impedance transformation and power combining simultaneously for watt-level output power. Therefore, a class-E PA using a finite DC-feed inductance combined with the magnetically coupled transformer is a good solution for on-chip integration. Recently, several papers have been published for class-E or class-E/F PAs using a finite DC-feed inductance integrated with transformers [29]-[32]. When a transformer is combined with a class-E PA, the impedance looking into the transformer can be a part of a class-E load network, thereby minimizing the number of elements and maximizing efficiency. In this condition, the operation and power loss of a class-E PA using a finite DC-feed inductance are a function of the transformer's design parameters. Several studies have addressed the power losses in a class-E PA including an output network [34]-[36], but only for a class-E PA using an RF choke. Also, no analogous approach has yet been reported for the operation and power loss of a class-E PA combined with a transformer as a function of the transformer's design parameters. A precise class-E PA characterization and analysis associated with the transformer are required to achieve high-efficiency and high-power performance.

In this chapter, analysis of the operation and power loss of a class-E PA using a finite

DC-feed inductance combined with a transformer is presented in terms of transformer parameters.

4.2 Analysis of Fully Integrated Class-E CMOS Power Amplifier

4.2.1 Operation of Parallel-Circuit Class-E Power Amplifier with Transformer

Many papers have reported different analyses of a class-E PA using a finite DC-feed inductance [37]-[42]. Among these analyses, the concept of a parallel-circuit class-E PA was introduced by Grebennikov [42], [43].

It is a subclass of class-E PAs using a finite DC-feed inductance, as shown in Figure 31(a). It has no additional reactive element connected in series to the L_OC_O filter tuned to the fundamental frequency. Thus, the number of elements can be reduced. Also, among the family of class-E load networks, a parallel-circuit class-E load network offers the largest value of R, which reduces the impedance transformation ratio to match a 50-Ω load. Another advantage of this topology is that the maximum operating frequency for an optimum parallel-circuit class-E PA is 1.4 times higher than that for the optimum class-E PA using an RF choke [14].

Figure 31(b) shows a parallel-circuit class-E PA combined with a *1:n* transformer. It consists of a finite parallel inductance, L, a parallel capacitance, C, a series capacitance, C_O, resonating with L_O at the fundamental frequency, and the *1:n* transformer for impedance transformation. The transformer can be modeled with the equivalent series resistance, R_{T1} and R_{T2}, and the equivalent net inductance, L_{T1} and L_{T2}, for the primary and secondary windings. M is the mutual inductance between the primary and secondary windings, n is the turn ratio, and k is the coupling factor.

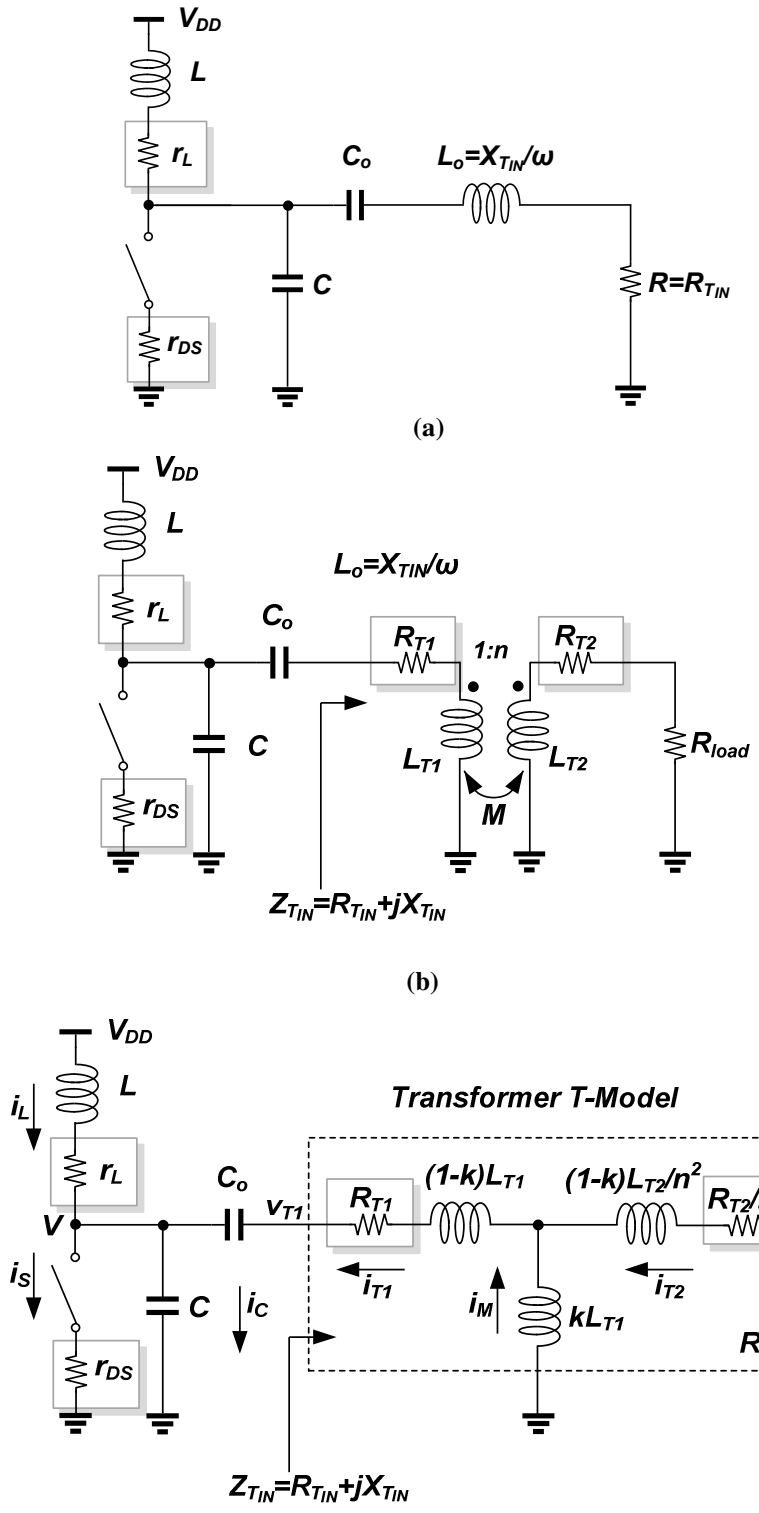


Figure 31. (a) Parallel-circuit class-E PA. (b) Schematic of a parallel-circuit class-E PA with a transformer. (c) Equivalent class-E network with a transformer equivalent T-model.

The strength of the magnetic coupling between the primary and secondary windings is indicated by k as $k = M/\sqrt{L_{T1}L_{T2}}$. The impedance looking into the transformer, $Z_{T_{IN}}$, is the ratio of the voltage phasor to the current phasor at the input of the transformer. $R_{T_{IN}}$ is the resistance, and X_{TIN} is the reactance of the impedance looking into the transformer. For the optimum parallel-circuit class-E load network, $R_{T_{IN}}$ and X_{TIN} should be R and ωL_O, respectively, as shown in Figure 31(a). The output capacitance of the device can be incorporated into C. The equivalent series resistance of the parallel inductor, r_L, and on resistance of the transistor, r_{DS}, are added to analyze the loss mechanism. The four loss resistances, r_{DS}, r_L, R_{T1}, and R_{T2}, are highlighted in Figure 31(b). Generally, the Q factor of capacitors is much higher than that of inductors at operation frequency bands of typical wireless applications, so the loss resulting from capacitors is neglected.

Figure 31(c) shows the parallel-circuit class-E PA with transformer equivalent T-model. To determine power loss at each loss resistance, the currents flowing through loss resistances, $i_L(\omega t)$, $i_S(\omega t)$, $i_{T1}(\omega t)$, and $i_{T2}(\omega t)$, should be obtained. The current can be calculated following the procedure in [42]. It is assumed that the ideal operation of the class-E PA is not affected by the loss resistances. Thus, all waveforms remain like those of ideal class-E PAs. The current of the switching network is assumed sinusoidal and is given by

$$i_{T1}(\omega t) = I_T \sin(\omega t + \varphi). \tag{4.1}$$

where I_T is the current amplitude and φ is the initial phase shift.

When the switch is on during $0 \leq \omega t < \pi$, the capacitor current $i_C(\omega t)$ through the capacitance and the voltage across the switch are equal to zero, i.e.

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d(\omega t)} = 0 \tag{4.2}$$

$$v(\omega t) = V_{DD} - v_{L\_ON}(\omega t) = 0 \tag{4.3}$$

The inductor voltage across the DC-feed inductance, $v_{L\_ON}(\omega t)$, is expressed

$$v_{L\_ON}(\omega t) = \omega L \frac{di_L(\omega t)}{d(\omega t)} \tag{4.4}$$

From (4.3)and (4.4), $i_{L\_ON}(\omega t) = \int_0^{\omega t} \frac{v_{L\_ON}(\omega t)}{\omega L} d(\omega t)$

$$= \frac{V_{DD}}{\omega L} \int_0^{\omega t} d(\omega t) = \frac{V_{DD}}{\omega L} \omega t + i_L(0). \tag{4.5}$$

Because $i_S(0) = 0$, the initial value for $i_L(\omega t)$ at $\omega t = 0$ can be found using (4.1)

$$i_L(0) = i_S(0) - i_{T1}(0) = -I_T sin\varphi \tag{4.6}$$

Using (4.5) and (4.6) the inductor current, $i_{L\_ON}(\omega t)$, is expressed as

$$i_{L\_ON}(\omega t) = \frac{V_{DD}}{\omega L} \omega t - I_T sin\varphi. \tag{4.7}$$

The current $i_S(\omega t) = i_{L\_ON}(\omega t) + i_{T1}(\omega t)$ flowing through the switch can be written as

$$i_S(\omega t) = \frac{V_{DD}}{\omega L} \omega t + I_T[\sin(\omega t + \varphi) - \sin\varphi]. \tag{4.8}$$

When the switch is off during $\pi \leq \omega t < 2\pi$, the switch current $i_S(\omega t)$ is 0, and the capacitor current, $i_C(\omega t) = i_{L\_OFF}(\omega t) + i_{T1}(\omega t)$, can be rewritten as

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d(\omega t)}$$

$$= \frac{1}{\omega L} \int_{\pi}^{\omega t} [V_{DD} - v(\omega t)] d(\omega t) + i_{L\_OFF}(\pi) + I_T \sin(\omega t + \varphi). \tag{4.9}$$

Solving this linear second-order differential equation, the capacitor voltage can be given by

$$v(\omega t) = V_{DD}[C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + 1 - \frac{q^2 p}{1-q^2}\cos(\omega t + \varphi)] \quad (4.10)$$

where $q = (1/\omega t)\sqrt{LC}$, $p = \omega L_{T1}/V_{DD}$, and the coefficients C_1 and C_2 are determined from the initial off-state conditions ($v(\pi) = 0$ and $i(\pi) = V_{DD}\pi/\omega L - I_T \sin\varphi$). The current $i_{L\_OFF}(\omega t) = i_C(\omega t) - i_{T1}(\omega t)$ flowing through the finite DC-feed inductance can be expressed as

$$i_{L\_OFF}(\omega t) = \omega C V_{DD}[-qC_1 \sin(q\omega t) + qC_2 \cos(q\omega t) + \frac{q^2 p}{1-q^2}\sin(\omega t + \varphi)] - I_T \sin(\omega t + \varphi). \quad (4.11)$$

To define the unknown parameters q, p, and φ, two switching conditions and the DC Fourier component equation, $V_{DD} = (1/2\pi)\int_0^{2\pi} v(\omega t)d(\omega t)$, are applied. For optimum design conditions, the following design parameters can be determined as [42]

$$R_{T_{IN}} = 1.365\frac{{V_{DD}}^2}{P_{T_{IN}}}, \quad (4.12)$$

$$L = 0.732\frac{R_{T_{IN}}}{\omega}, \quad (4.13)$$

$$C = \frac{0.685}{\omega R_{T_{IN}}}. \quad (4.14)$$

The current on the primary winding is $i_{T1}(\omega t)$. The current on the secondary winding, $i_{T2}(\omega t)/n$, can be calculated using the transformer equivalent T-model in Figure 31(c). Assuming $L_{T1} \cong L_{T2}/n^2$, the phasor form of $i_{T2}(\omega t)$ will be given by

$$I_{T2} = \frac{j\omega k L_{T1}}{\frac{j\omega(1-k)L_{T2}}{n^2} + \frac{R_{T2}}{n^2} + \frac{R_{load}}{n^2} + j\omega k L_{T1}} I_{T1}$$

$$= \frac{j\omega n^2 k L_{T1}}{j\omega n^2 L_{T1} + R_{T2} + R_{load}} I_{T1}. \quad (4.15)$$

Using phasor notation, the input impedance of the transformer, Z_{TIN}, is given by

$$Z_{T_{IN}} \equiv \frac{V_{T1}}{I_{T1}} \equiv R_{T_{IN}} + jX_{T_{IN}}$$

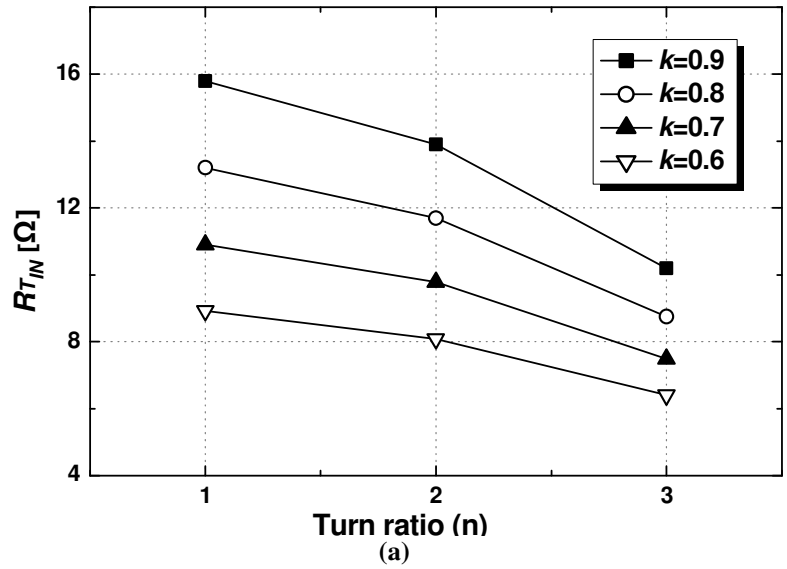
$$= R_{T1} + j\omega(1-k) + \frac{j\omega k L_{T1}[j\omega(1-k)L_{T2} + R_{T2} + R_{load}]}{j\omega n^2 L_{T1} + R_{T2} + R_{load}}. \quad (4.16)$$

R_{TIN} is the real part and X_{TIN} is the imaginary part of the input impedance Z_{TIN} can be derived as

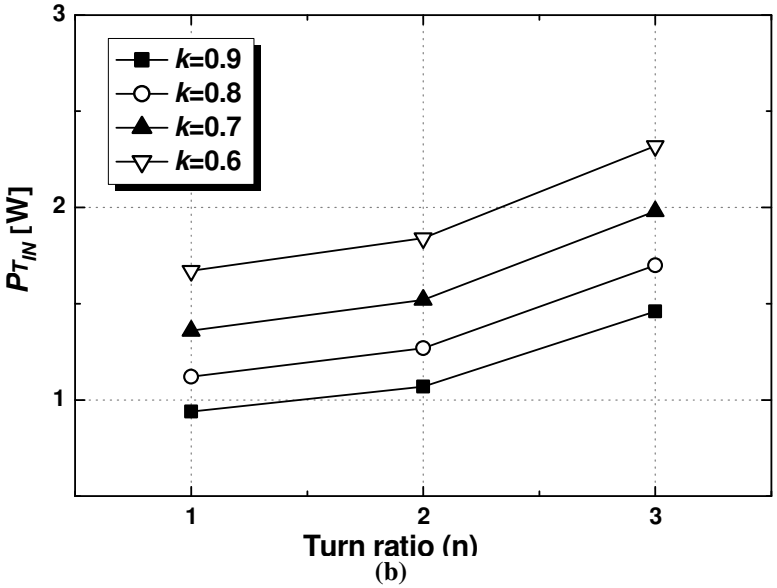
$$R_{T_{IN}} = R_{T1} + \frac{\omega^2 n^2 k^2 {L_{T1}}^2 (R_{T2} + R_{load})}{(R_{T2} + R_{load})^2 + (\omega n^2 L_{T1})^2}, \quad (4.17)$$

$$X_{T_{IN}} = \frac{\omega L_{T1}(R_{T2} + R_{load})^2 + \omega^3 n^4 (1-k^2) {L_{T1}}^3}{(R_{T2} + R_{load})^2 + (\omega n^2 L_{T1})^2}. \quad (4.18)$$

Since the transformer is a part of the class-E switching network, R_{TIN} and X_{TIN} should satisfy the class-E switching conditions in (4.12)-(4.14). For high-power operation, the resistance looking into the transformer should be small in (4.17). Figure 32(a) shows the plots of R_{TIN} versus a turn ratio, n, with different k values using (4.12). All given values for R_{T1}, R_{T2}, and L_{T1} have been determined as practical values from electromagnetic simulations. Figure 32(b) shows the power capability of the class-E PA derived from (4.12), versus n according to k variations when V_{DD} is 3.3 V. The generated power, P_{TIN}, is increased as n increases. Also, low k also increases the power capability of a class-E PA network because it decreases R_{TIN}.



(a)



(b)

Figure 32. (a) Resistance looking into the transformer, R_{TIN}, versus n for k variations. (b) Power transferred to the transformer input, $P_{T_{IN}}$, versus n for k variations (assuming Q_{T1}=Q_{T2}=10, L_{T1}=3 nH, R_{load}=50 Ω, V_{DD}=3.3 V, and frequency=1.8 GHz).

4.2.2 Power Loss of Parallel-Circuit Class-E Power Amplifier with Transformer

The power loss at each loss resistance can be calculated using the above determined current equations, (4.1), (4.7), (4.8), and (4.11), with loss resistances, r_{DS}, r_L, R_{T1}, and R_{T2}.

The power loss due to the on resistance of the switch can be expressed as

$$P_{r_{DS}} = \frac{1}{2\pi}\int_0^{2\pi} {i_s}^2(\omega t) r_{DS} d(\omega t)$$

$$= \frac{r_{DS}}{2\pi}\int_0^{\pi} \left\{\frac{V_{DD}}{\omega L}\omega t + I_T[\sin(\omega t + \varphi) - \sin\varphi]\right\}^2 d(\omega t)$$

$$\cong 3.138\frac{r_{DS}}{R_{T_{IN}}} P_{T_{IN.}} \tag{4.19}$$

where $P_{T_{IN}} = (1/2){I_T}^2 R_{T_{IN}}$. While the power loss due to the on resistance of the switch in a class-E topology using an RF choke is expressed as [34]

$$P_{r_{DS\_RFC}} \cong 1.365\frac{r_{DS}}{R_{T_{IN}}} P_{T_{IN}}. \tag{4.20}$$

The switch current $i_S(\omega t)$ at on state is the sum of $i_{TI}(\omega t)$ and $i_{L\_ON}(\omega t)$. The current $i_{L\_ON}(\omega t)$ flowing through the finite DC-feed inductance, L, in a parallel-circuit class-E PA consists of AC current as well as DC current, while the current $i_{L\_ON}(\omega t)$ in a class-E PA using an RF choke has only DC current. Hence, power loss in a parallel-circuit class-E PA is larger than that of a class-E PA using an RF choke if $R_{T_{IN}}$ is the same in both cases.

The power loss due to parasitic resistance of a finite DC-feed inductance is given by

$$P_{r_L} = \frac{1}{2\pi}\int_0^{2\pi} {i_L}^2(\omega t) r_L d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} {i_{L\_ON}}^2(\omega t) r_L d(\omega t) + \int_{\pi}^{2\pi} {i_{L\_OFF}}^2(\omega t) r_L d(\omega t)\right]$$

$$\cong 3.365\frac{r_L}{R_{T_{IN}}} P_{T_{IN}}. \tag{4.21}$$

The power loss due to the equivalent series resistance of the transformer primary winding, R_{TI}, can be obtained as

$$P_{R_{T1}} = \frac{1}{2\pi}\int_0^{2\pi} {i_{T1}}^2(\omega t)R_{T1}d(\omega t)$$

$$= \frac{R_{T1}}{2\pi}\int_0^{2\pi} [I_T \sin(\omega t + \varphi)]^2 d(\omega t)$$

$$= \frac{R_{T1}}{R_{T_{IN}}} P_{T_{IN}}. \tag{4.22}$$

The power loss due to the equivalent series resistance of the secondary winding, R_{T2}, is given by

$$P_{R_{T2}} = \frac{1}{2\pi}\int_0^{2\pi} {i_{T2}}^2(\omega t)(R_{T2}/n^2)d(\omega t)$$

$$= \frac{1}{2}\frac{(\omega n^2 k L_{T1})^2}{(R_{T2} + R_{load})^2 + (\omega n^2 L_{T1})^2}|I_{T1}|^2(R_{T2}/n^2)$$

$$= \frac{(\omega n^2 k L_{T1})^2}{(R_{T2} + R_{load})^2 + (\omega n^2 L_{T1})^2}\frac{(R_{T2}/n^2)}{R_{T_{IN}}} P_{T_{IN}}. \tag{4.23}$$

To compare each power loss with the power delivered to the load, P_{load}, P_{load} can be calculated using $i_{T2}(\omega t)$ and can be given by

$$P_{load} = \frac{1}{2\pi}\int_0^{2\pi} {i_{T1}}^2(\omega t)(R_{laod}/n^2)d(\omega t)$$

$$= \frac{(\omega n^2 k L_{T1})^2}{(R_{T2} + R_{load})^2 + (\omega n^2 L_{T1})^2}\frac{(R_{laod}/n^2)}{R_{T_{IN}}} P_{T_{IN}}. \tag{4.24}$$

The power losses due to each loss resistance, normalized to P_{load}, are shown in Figure 33 using (4.19), (4.21)-(4.24). Because the current through the primary winding is n times larger than that through the secondary winding in an ideal 1:n transformer, the power loss due to R_{T1} compared to that due to R_{T2} is larger if the resistances are the same values. Also,

the power losses due to r_{DS} and r_L are much larger than those due to R_{T1} and R_{T2} since DC and harmonic contents are included in $i_L(\omega t)$ and $i_S(\omega t)$, as shown in Figure 33.

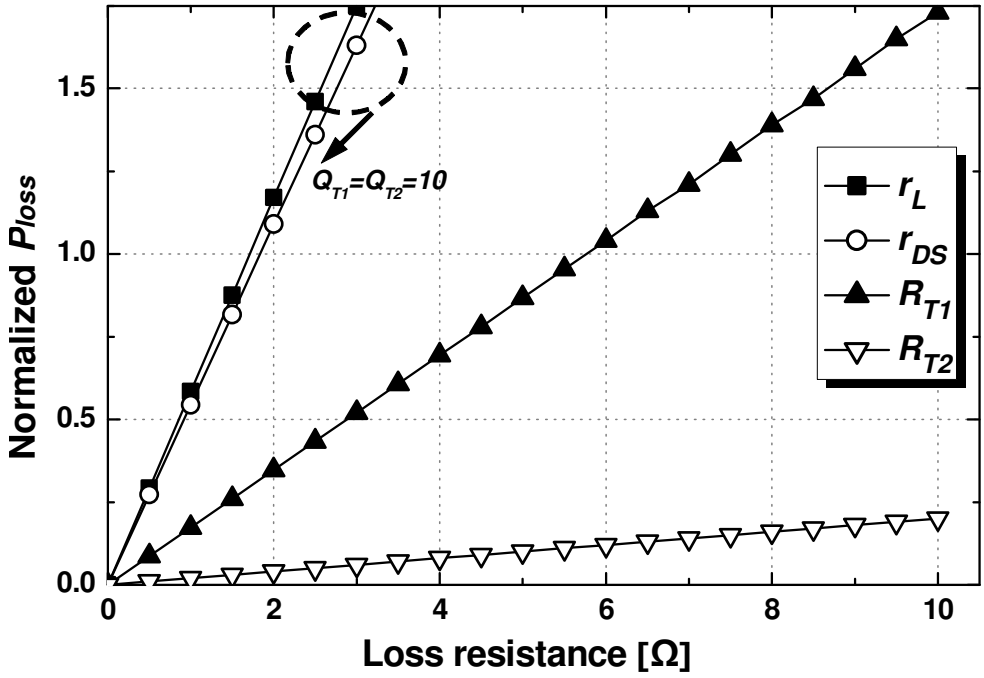
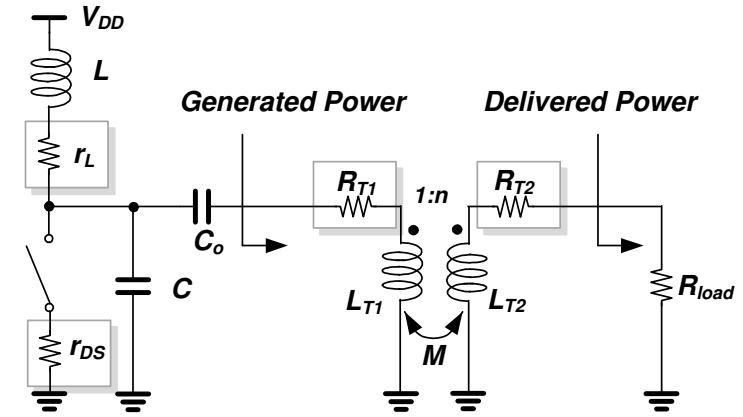


Figure 33. Power losses of a parallel-circuit class-E PA with a transformer normalized to P_{load} (assuming L_{T1}=3 nH, R_{load}=50 Ω, n=2, k=0.75, and frequency=1.8 GHz).

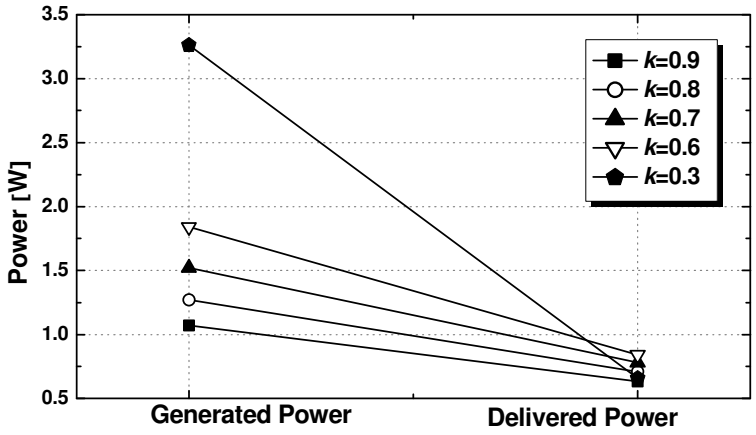
4.2.3 CMOS Implementaion of Parallel-Circuit Class-E Power Amplifier with Transformer

To design a high-efficiency PA, it is necessary to reduce the loss resistance. Using a high-Q wire bonding inductor is a way to minimize its loss due to r_L. The power loss due to r_{DS} can be minimized by increasing the device size.

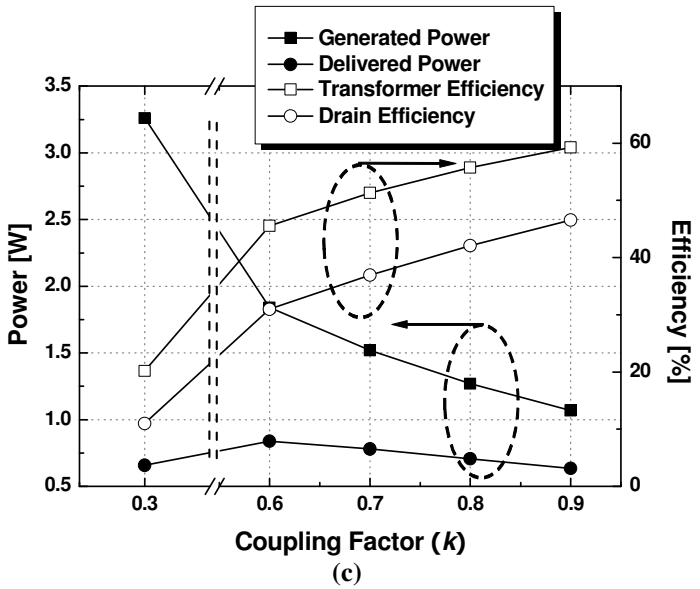
Figure 34 shows the relation between the power transferred to the transformer input and the power transferred to the load. The bonding wire inductance is chosen to be around 1 nH, considering a practical implementation. Assuming the Q of the bond-wire,



(a)



(b)



(c)

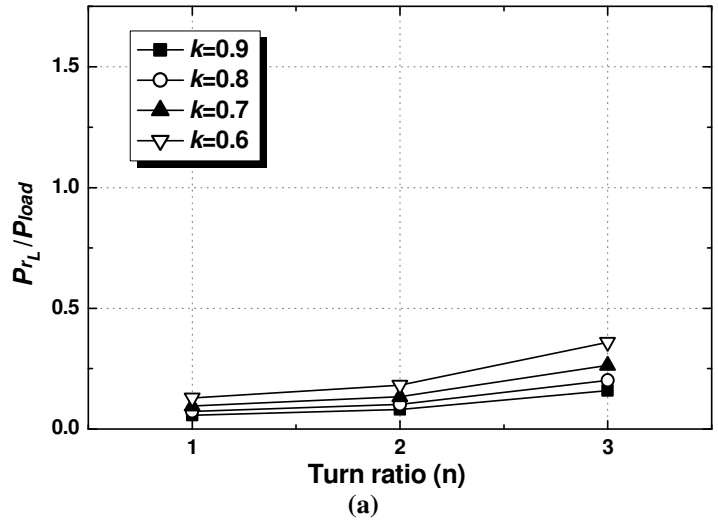
Figure 34. (a) Schematic of a parallel-circuit class-E PA with a transformer. (b) Power level diagram corresponding to (a). (c) Power and efficiency for k variation (assuming Q_{T1}=Q_{T2}=10, L_{T1}=3 nH, R_{load}=50 Ω, n=2, r_L=0.2 Ω, r_{DS}=1.0 Ω, and frequency=1.8 GHz).

Q_{bond}, is around 50 [10], $r_L=(j\omega L)/Q_{bond} \cong 0.2\ \Omega$ at 1.8 GHz. The on resistance, r_{DS}, of 1 Ω, is determined from Agilent ADS™ simulations. Because the switching efficiency is inversely proportional to the on-resistance, r_{DS}, the device size should be large enough to reduce r_{DS}. However, increasing device size also increases the parasitic capacitance. Large input capacitance decreases the input driving capability of the PA. Although the gate capacitance can be tuned out by the resonant network, a large device still requires more driving power, resulting in degradation of the overall efficiency. Therefore, device size should not be excessively increased in order to compensate for driving loss since the accompanying large input capacitance would only exacerbate the problem [44]. All given transformer parameters for Q_{T1}, Q_{T2}, and L_{T1} have been determined as practical values from electromagnetic simulations. Low k reduces the amount of transformed impedance as implied in (4.17), thus increasing the generated power of a class-E PA network. The generated power is delivered to the output load through the transformer in Figure 34(a). The transformer efficiency can be expressed as the ratio of the power delivered to the load to the generated power as shown below.

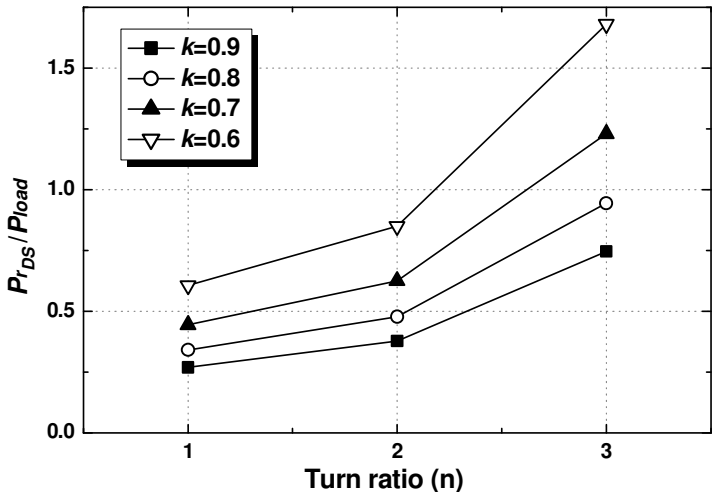
$$\text{Transformer efficiency} = \frac{P_{load}}{P_{T_{IN}}} = \frac{P_{load}}{P_{R_{T1}} + P_{R_{T2}} + P_{load}}. \tag{4.25}$$

Assuming the total power—including the delivered power to the output load and all power losses—is equal to DC power, drain efficiency can be given by

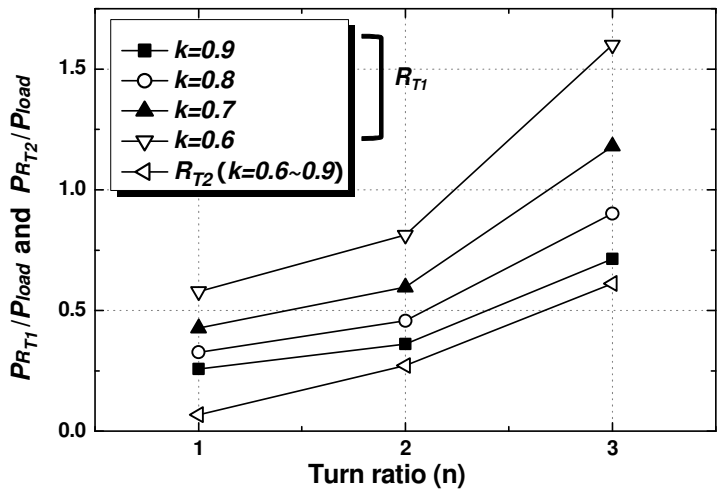
$$\text{Drain efficiency} = \frac{P_{load}}{P_{DC}} \cong \frac{P_{load}}{P_{r_{DS}} + P_{r_L} + P_{R_{T1}} + P_{R_{T2}} + P_{load}}. \tag{4.26}$$



(a)



(b)



(c)

Figure 35. Power losses due to r_L, r_{DS}, R_{T1}, and R_{T2} normalized to P_{load} (assuming Q_{T1}=Q_{T2}=10, L_{T1}=3 nH, R_{load}=50 Ω, and frequency=1.8 GHz) (a) r_L=0.2 Ω, (b) r_{DS}=1.0 Ω.

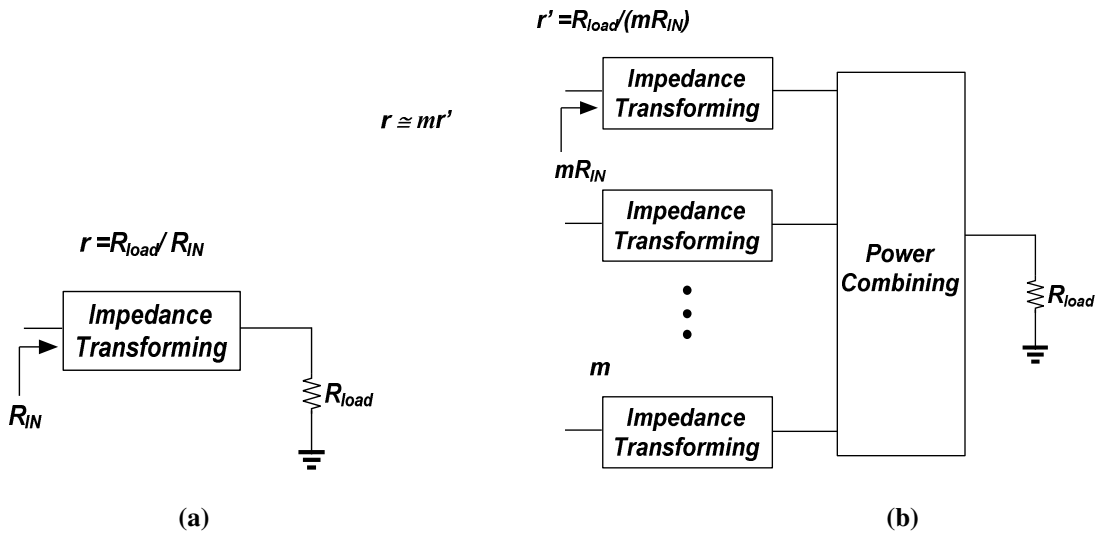


Figure 36. (a) Output impedance transformation network. (b) Output impedance transformation networks with power combining network.

The power loss of the transformer can be minimized using k close to unity. Since $i_{T2}(\omega t)$ is a fraction of $i_{T1}(\omega t)$, k should be large to minimize the magnetizing current, $i_M(\omega t)$. Thus, the decreased power due to the power loss of the transformer can be small, as shown in Figure 34(b). Figure 34(c) shows the relation between the power and efficiency versus k. Both of the efficiency performances are degraded when k is decreased. On the other hand, with decreasing k, the generated output power increases, and the delivered output power to the load can be also increased to some extent. However, for very low k, the generated power cannot be fed to the output load, and most of the generated power will be consumed in the equivalent series resistance of the primary winding. Since the coupling factor, k, is mainly determined by the geometry of windings and permeability of the core materials, the design range of this parameter is very narrow in a practical CMOS implementation. Considering a realizable k value, the output power and efficiency can be estimated, and the other design parameters can be optimized accordingly.

Figure 35 shows the power loss due to the each loss resistor, normalized to output power, versus n with different k values using (4.19), (4.21)-(4.24). The impedance-transformation ratio, r, is the ratio of the load impedance, R_{load}, to the transformed impedance, $R_{T_{IN}}$, $(r = R_{load}/R_{T_{IN}})$. r increases with increasing turn ratio of the transformer ($r=n^2$ in an ideal transformer), resulting in increased the loss of the transformer. For a watt-level output power, large n is generally required to reduce $R_{T_{IN}}$, as shown in (4.17). However, this increases the power losses normalized to output power, as shown in Figure 35. It indicates that a large impedance transformation results in a large power loss. Generally, the higher the impedance transformation ratio, the higher the loss of the impedance transformation network [22], [45]. Also, since the losses due to r_L and r_{DS} are proportional to the current squared, these losses are increased by increasing current due to the increase of the impedance transformation ratio, as shown in Figure 35. Power combining is a way to reduce the burden of the necessary impedance transformation to get a watt-level output power with relatively low r. If m amplifiers are combined, the impedance transformation ratio for each individual power amplifier, r', is reduced by m times, as shown in Figure 36, resulting in reducing power loss. Power combining can be implemented by transformer or inductor-capacitor (LC) matching network for an on-chip implementation. However, a transformer has an advantage over an LC output network since it can provide the impedance transformation and power combining simultaneously in a compact form, resulting in reduced circuit complexity and die area. Series combining transformers [29], [32], [33] and parallel combining transformers [31], [46], [47] can be applied to obtain watt-level output power using low n.

However, combining losses owing to phase mismatch and degradation of passive efficiency should be considered.

4.2.4 Power Loss at Maximum Transformer Efficiency

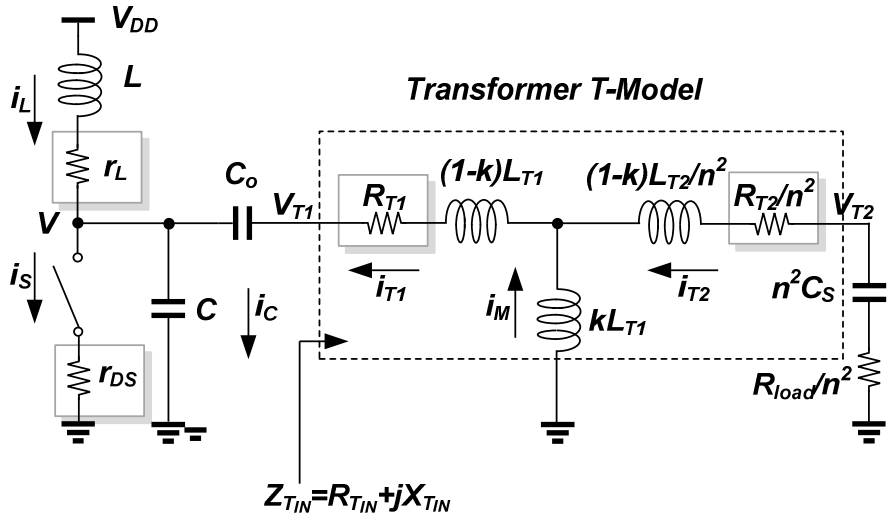


Figure 37. Schematic of a parallel-circuit class-E PA with a transformer equivalent T-model including an output tuning capacitance.

To maximize the efficiency of the transformer, the following conditions are required [27]. A capacitor C_S shown in Figure 37 is required to resonate with L_{T2}

$$\omega L_{T2} = \frac{1}{\omega C_S}. \tag{4.27}$$

To minimize the transformer's loss, tuning capacitors on both primary and secondary side of the transformer are required [27]. The output capacitor on the secondary side of the transformer tunes out some of the transformer's inductance to minimize the transformer's loss. Also, the input capacitor on the primary side of the transformer adjusts the reactive

part of the transformer input impedance to provide the required load impedance for the chosen class of the amplifier [27].

The optimum primary inductance can be obtained by differentiating η_T by L_{T1}. The primary inductance can be obtained as

$$\omega L_{T1} = \frac{R_{load}}{n^2\sqrt{\frac{1}{{Q_{T2}}^2} + \frac{Q_{T1}}{Q_{T2}}k^2}} \tag{4.28}$$

where $Q_{T1} = \omega L_{T1}/R_{T1}$ and $Q_{T2} = \omega L_{T2}/R_{T2}$.

In the above two conditions, the maximum transformer efficiency can be expressed using (19)-(26):

$$\eta_{T\_max} = \frac{1}{1 + 2\sqrt{\left(1 + \frac{1}{Q_{T1}Q_{T2}k^2}\right)\frac{1}{Q_{T1}Q_{T2}k^2}} + \frac{2}{Q_{T1}Q_{T2}k^2}}. \tag{4.29}$$

Using the above particular minimum transformer loss conditions, each power loss, normalized to P_{load}, can be specified as a function of Q_{T1}, Q_{T2} and k:

$$\frac{P_{r_{DS}}}{P_{load}} = 3.138\frac{r_{DS}}{R_{load}}n^2\frac{\left(1 + \sqrt{1 + Q_{T1}Q_{T2}k^2}\right)^2}{k^2{Q_{T2}}^2}, \tag{4.30}$$

$$\frac{P_{r_L}}{P_{load}} = 3.365\frac{r_L}{R_{load}}n^2\frac{\left(1 + \sqrt{1 + Q_{T1}Q_{T2}k^2}\right)^2}{k^2{Q_{T2}}^2}, \tag{4.31}$$

$$\frac{P_{R_{T1}}}{P_{load}} = \frac{1}{k^2Q_TQ_{T2}}\frac{\left(1 + \sqrt{1 + Q_{T1}Q_{T2}k^2}\right)^2}{\sqrt{1 + Q_{T1}Q_{T2}k^2}}, \tag{4.32}$$

$$\frac{P_{R_{T2}}}{P_{load}} = \frac{1}{\sqrt{1 + Q_{T1}Q_{T2}k^2}}. \tag{4.33}$$

4.2.5 Push-Pull Transformer Combined with Class-E Power Amplifier

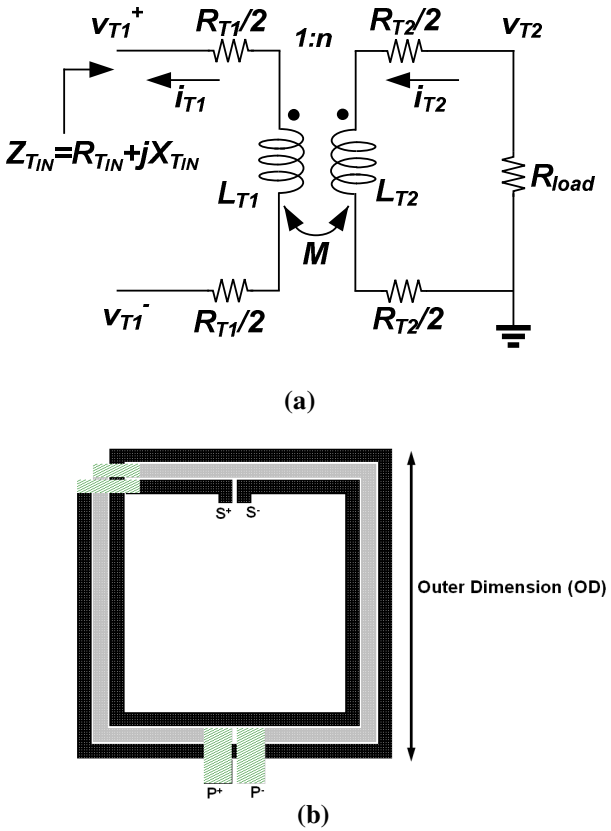
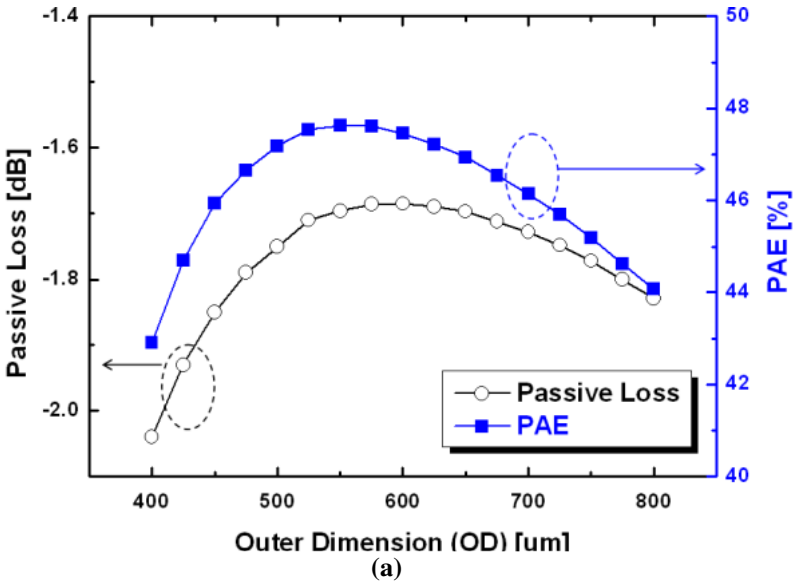


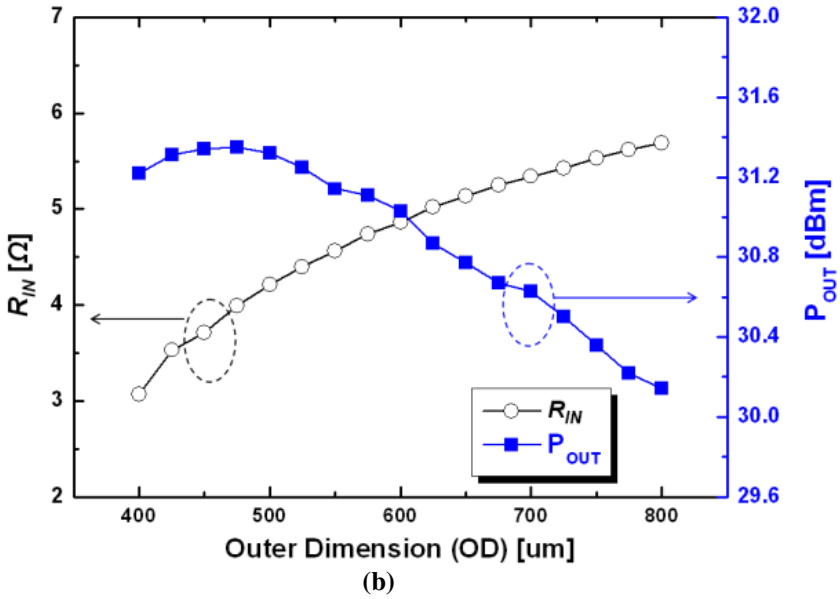
Figure 38. **(a) Physical layout of push-pull 1:2 transformer. (b) Physical layout of push-pull 1:2 transformer.**

From the above proposed analysis of 1:*n* transformer, the transformer can be further optimized for the extended design. The push-pull transformer enables combining the two PAs, as shown in Figure 38(a). Also, in the ideal case, it has its own 1:2 impedance transformation ratio, improving the power capability. Furthermore, the push-pull topology neutralizes the bond-wire inductance and suppresses the second harmonic.

Figure 38(b) shows an exemplary layout of the push-pull 1:2 transformers in a lateral structure. To gain insight, the momentum and harmonic balance simulation using an Agilent ADS^{TM} were performed.



(a)



(b)

Figure 39. Simulation results of push-pull class-E PA with 1:2 transformer. (a) Passive loss and PAE versus outer dimension (OD) of transformer. (b) R_{IN} and P_{OUT} versus OD of transformer.

A passive efficiency and PAE of the designed PA with the push-pull 1:2 transformer are presented in Figure 39(a), and R_{TIN} and output power of the designed PA with the 1:2

transformer are shown in Figure 39(b) as the outer dimension (OD) of transformer increases. As the OD of the transformer increases, the series resistance increases, resulting in a larger series loss. Also, the decreasing transformer's OD increases the magnetizing current not participating in coupling, resulting in the decrease of k. Therefore, an optimum size exists to minimize the passive loss [27]. The performance of passive efficiency is directly related to the PAE performance, as shown in Figure 39(a).

In Figure 39(b), the resistance looking into the transformer, R_{TIN}, is decreased with the decrease of the transformer's OD. Coupling factor, k, and series resistance, R_{T1} and R_{T2}, are reduced with the decrease of the transformer's OD. Low k and low series resistance decrease R_{TIN} as can be seen in Figure 39(b). As shown in Figure 39(b), the output power, P_{OUT}, of the PA is inversely proportional to R_{TIN}. The P_{OUT} can be increased with the decrease of the transformer size. However, below a certain size, the passive loss becomes dominant, and there is no more power enhancement from low R_{TIN}. The maximum point of P_{OUT} is different from the maximum point of PAE. The output power can be increased further, while scarifying PAE. Therefore, according to the design specification, the transformer should be carefully optimized. Since the metal width and the spacing between primary and secondary windings will be the other design parameters affecting passive efficiency and R_{TIN}, these parameters should be carefully chosen in the design procedure.

4.2.6 *Multi-Primary Push-Pull Transformer Combined with Class-E Power Amplifier*

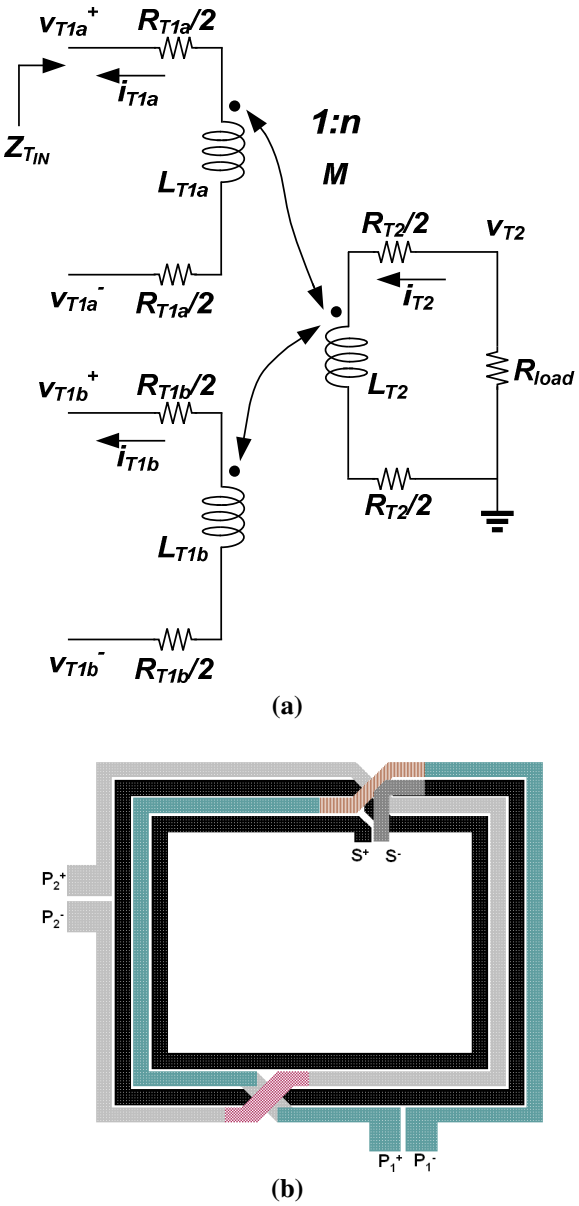


Figure 40. (a) Schematic of 2×1:2 step-up transformer. (b) Physical layout of 2×1:2 step-up transformer.

For further increase of output power, more unit PAs should be combined effectively.

Power combining is a way to reduce the burden of the necessary impedance transformation to get a watt-level output power without increasing n too much. Series combining and parallel combining can be applied to obtain watt-level output power using low n. However, combining losses owing to phase mismatch and degradation of passive efficiency should be considered.

Figure 40 shows an exemplary layout of parallel combining (2×1:2 transformer), which consists of two 1-turn primary windings and one 2-turn secondary winding. In a 2×1:2 transformer, multi-primary windings are used for power combining. The size of the transformer can be significantly reduced by incorporating the multi-turn structure. Also, since the transformer is separable from other components in this structure, an instability issue can be minimized.

4.3 Design of Parallel-Circuit Class-E Power Amplifier with Transformer

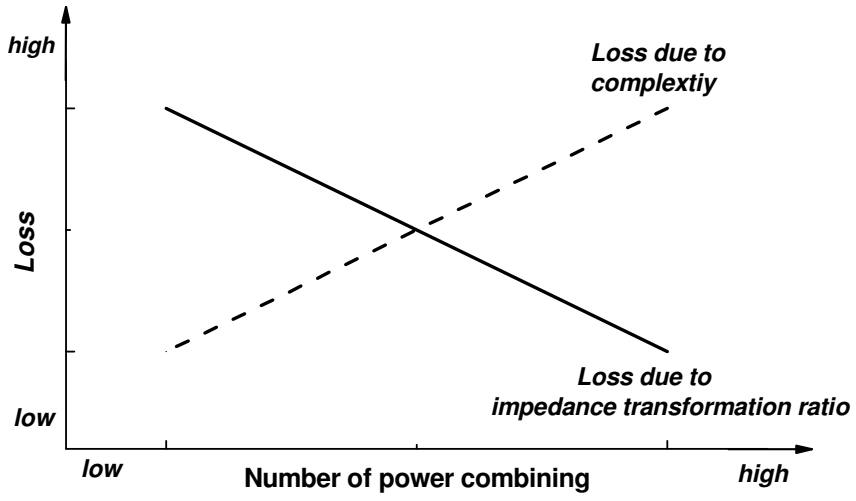


Figure 41. Loss of the output network versus number of power combining.

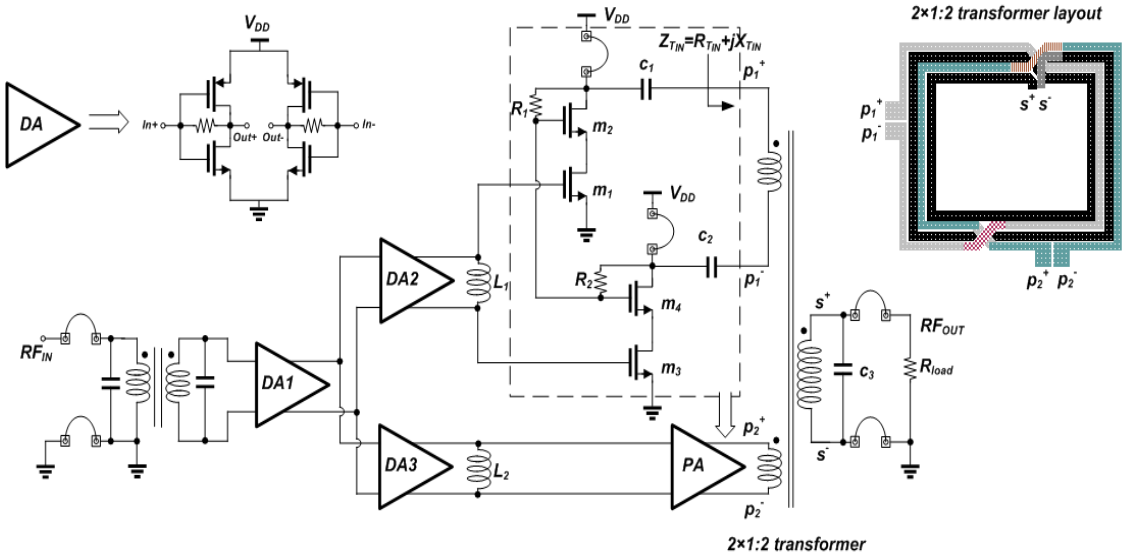
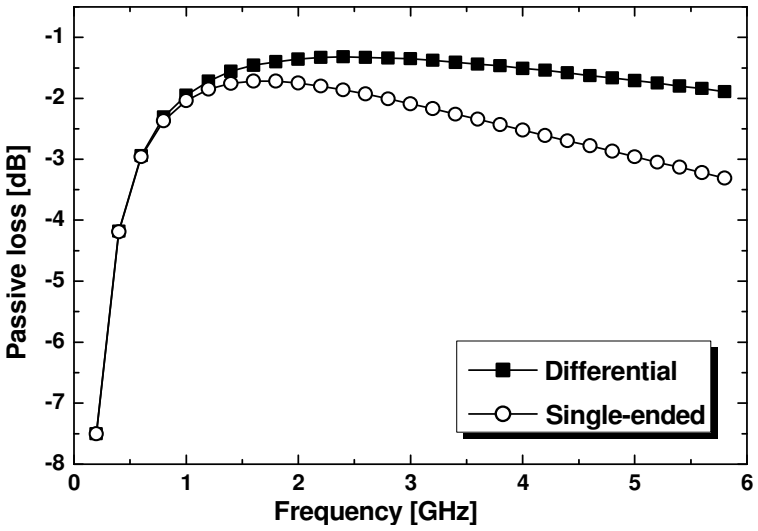


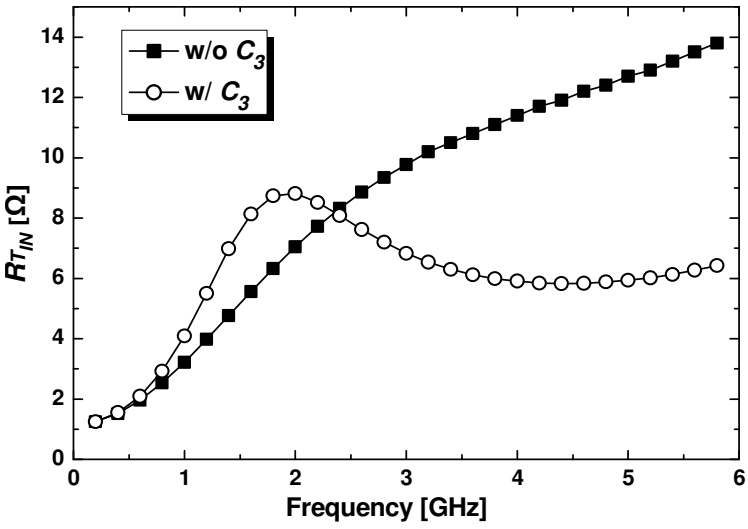
Figure 42. Schematic of the two push-pull parallel-circuit class-E PA with a 2×1:2 transformer.

The power loss can be reduced when multiple amplifiers are combined, since each individual power amplifier has a lower impedance transformation ratio. However, combining loss owing to phase mismatch and loss of combining structure should be considered for optimization. First of all, turn ratio should be small to minimize the power losses. In this design, two-turn secondary winding was selected to provide the necessary impedance transformation ratio to achieve 2-watt output power. By adding primary winding, the power loss can be reduced due to relatively low impedance transformation ratio for individual power amplifier. However, adding additional primary windings decreases the quality factor and coupling factor of the transformer in a lateral transformer structure. Also, the amplitude and phase errors can cause destructive overlap of the current at the secondary winding, resulting in failure to achieve the best performance. Finally, two primary windings and a two-turn secondary winding (2×1:2 transformer)

were chosen to minimize the power loss and achieve high output power at the same time, as shown in Figure 41.



(a)



(b)

Figure 43. Simulated passive loss of 2×1:2 step-up transformer (b) Effective resistance, R_{TIN}, looking into transformer at each input port.

A fully integrated PA was implemented in a commercial 0.18-μm CMOS technology. The proposed circuit is shown in Figure 42, consisting of two-stage drive amplifiers and a power stage amplifier with a fully integrated transformer. To minimize the power loss due to r_L, bonding inductors were used for a finite DC-feed inductance. A 2×1:2 step-up transformer is employed for achieving a target 2-W output power without decreasing R_{TIN} too much. Using a 2.34-μm top metal layer, the lateral transformer is composed of one-turn double-lateral primary windings and one two-turn secondary winding for power combining and impedance transformation. To attain high output power, the performance of the transformer was carefully optimized. Primary and secondary windings consist of interweaved 30-μm-wide lines with 5-μm line spacing, which were optimized using 2.5-D Agilent ADS Momentum and 3-D Ansoft HFSS. To consider the layout effects of interconnections between series capacitors, C_1 and C_2, and the transformer, EM simulations were heavily performed. The size of the transformer is 0.8 mm × 0.7 mm, as shown in Figure 42. It was significantly reduced by incorporating the multi-turn on-chip structure. Coupling between the transformer and other components of the PA is minimized by the use of physical separation. R_{TIN} shown in Figure 42 is the resistance of the impedance looking into the transformer at each input port.

Figure 43(a) shows the passive loss of the transformer versus frequency. At 1.8 GHz, insertion loss of the transformer is 1.75 dB (66.8%) when driving the input differently and taking out a single-ended output. It is 1.4 dB (72.4%) when taking differential output. Figure 43(b) shows the frequency sweep of R_{TIN} with and without the shunt capacitor, C_3. The shunt-output load network can be converted into an equivalent series network, as shown in Figure 37 [48]. $R_{T_{IN}}$ is 8.75 Ω at 1.8 GHz with C_3. Since C_3 is resonated with

some of the transformer's inductance, $R_{T_{IN}}$ is increased when it is connected at the output to minimize the transformer loss.

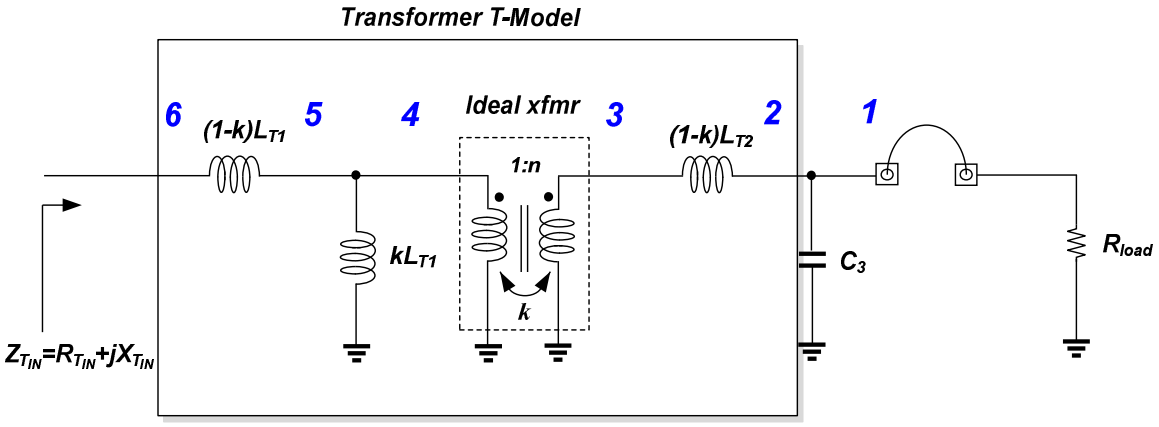


Figure 44. The transformer with output tuning capacitors and bond-wires.

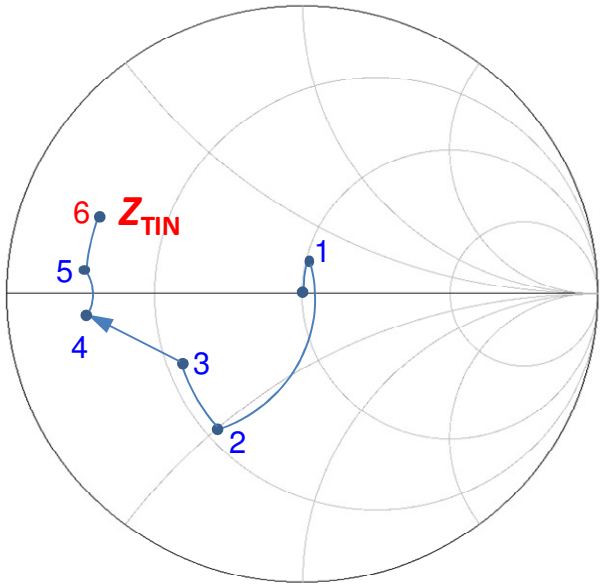


Figure 45. Equivalent impedance transformation.

To resonate with the effective inductance looking into the transformer, series capacitors, C_1 and C_2, are placed in the class-E PA. With considering bond-wire inductors and tuning capacitors, R_{TIN} will be affected. Figure 44 shows an equivalent schematic of the transformer with output tuning capacitor and bond-wires. The impedance transformation including these elements can be explained by the use of Smith chart, as shown in Figure 45.

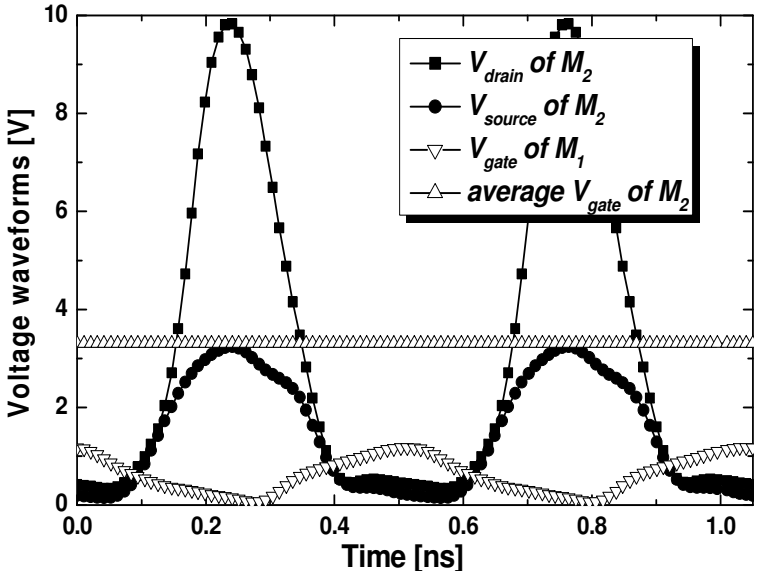


Figure 46. Simulated voltage waveforms of power devices.

The power stage amplifier employs a cascode topology to reduce the voltage drop across a single device to avoid breakdown incidence. The devices in the common-source stage, m_1 and m_3, and common-gate stage, m_2 and m_4, have a gate length of 0.18-μm and 0.35-μm, respectively. To minimize the power loss due to r_{DS}, the large devices are chosen, so that the shunt capacitance, C, in Figure 31(c) is entirely implemented by the output capacitance of the device. To tune out the input capacitances of the devices, shunt

inductors, L_1 and L_2, were used in the inter-stage between the power stage and the driver stage. The input on-chip balun is used for a differential operation. Figure 46 shows the simulated voltage waveforms of m_1 and m_2. The maximum voltage stress across a single device is kept below twice the nominal supply voltage. To minimize voltage stress between gate and drain of the common-gate device, the common-gate device is fed through a 3.3 supply voltage.

4.4 Measurement Results

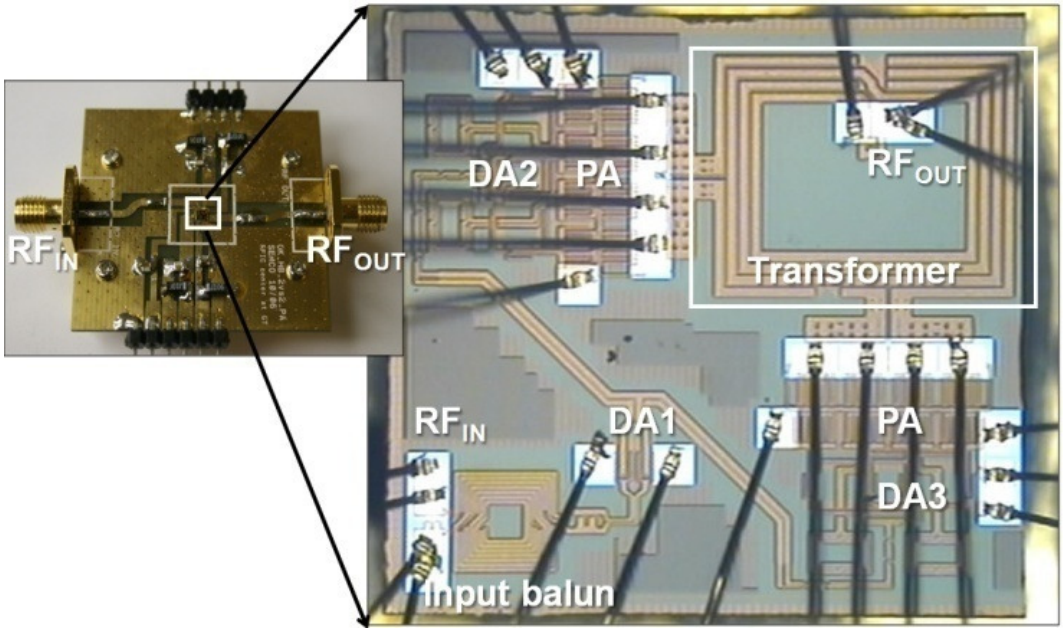


Figure 47. Photograph of the PA (Chip size: 1.8 mm × 1.65 mm).

Figure 47 shows the microphotograph of the PA fabricated in 1P6M 0.18-μm CMOS technology of which area is 1.8 mm × 1.65 mm including the pads for the chip-on-board test. The bare die was attached on the ground heat sink of printed circuit board (PCB). The ground pads were wire-bonded to the heat sink and the input and output pads were

wire-bonded to a 50-Ω micro-strip line on PCB. The voltage drop of the bias cable and the loss of connector, and PCB loss were calibrated out in the measurement procedure.

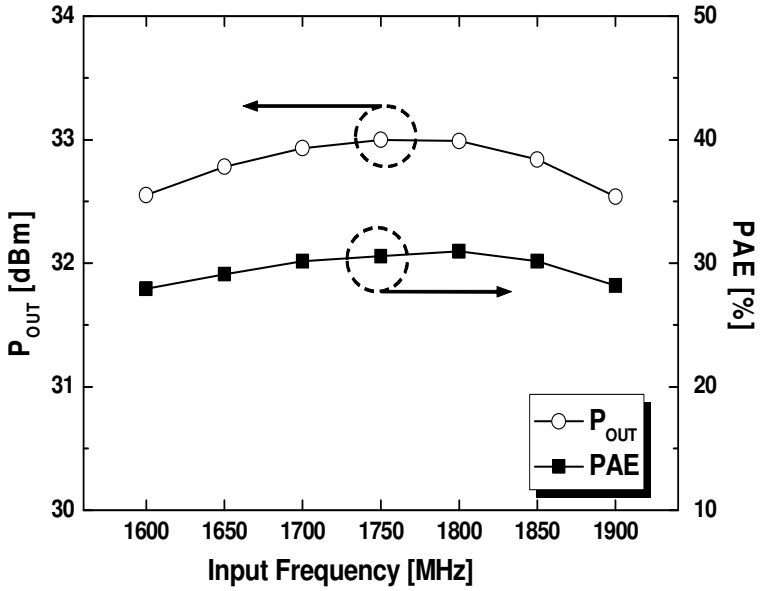


Figure 48.Measured P_{OUT} and PAE versus frequency.

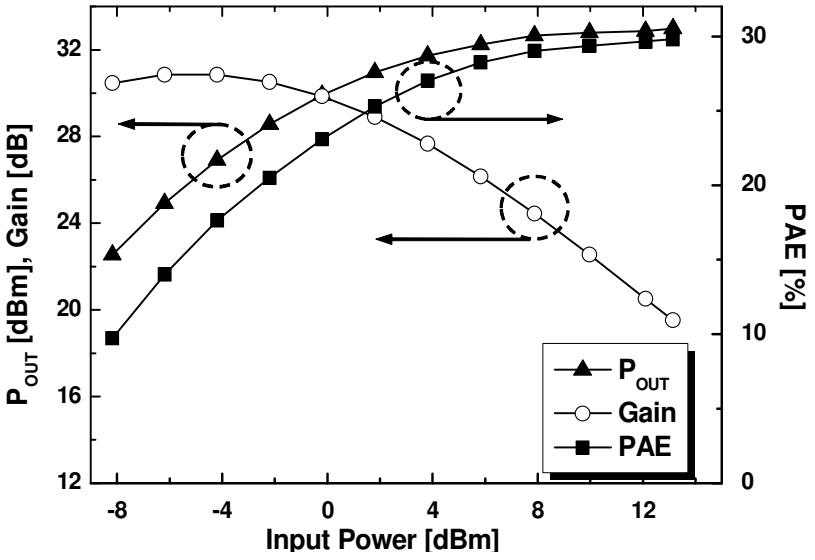


Figure 49. Measured P_{OUT}, gain and PAE versus input power.

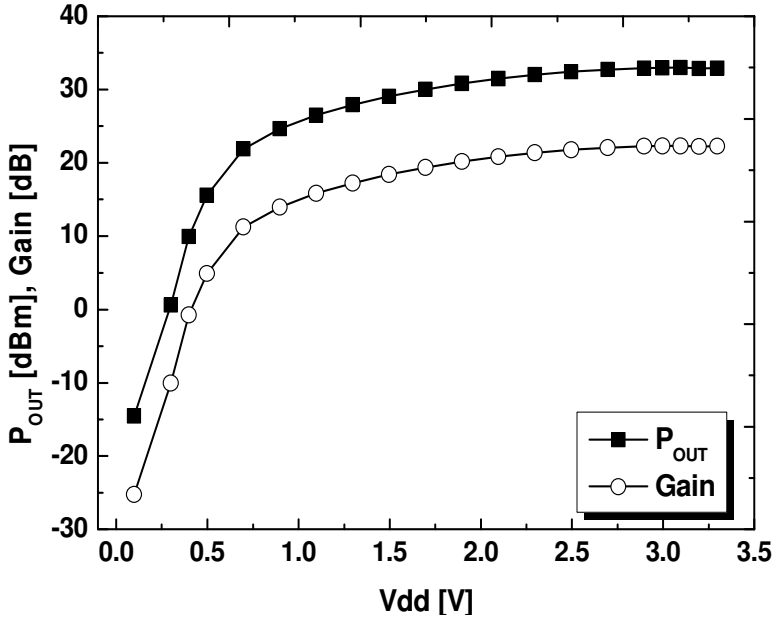


Figure 50. Measured P_{OUT} and gain versus supply voltage at 1.8 GHz.

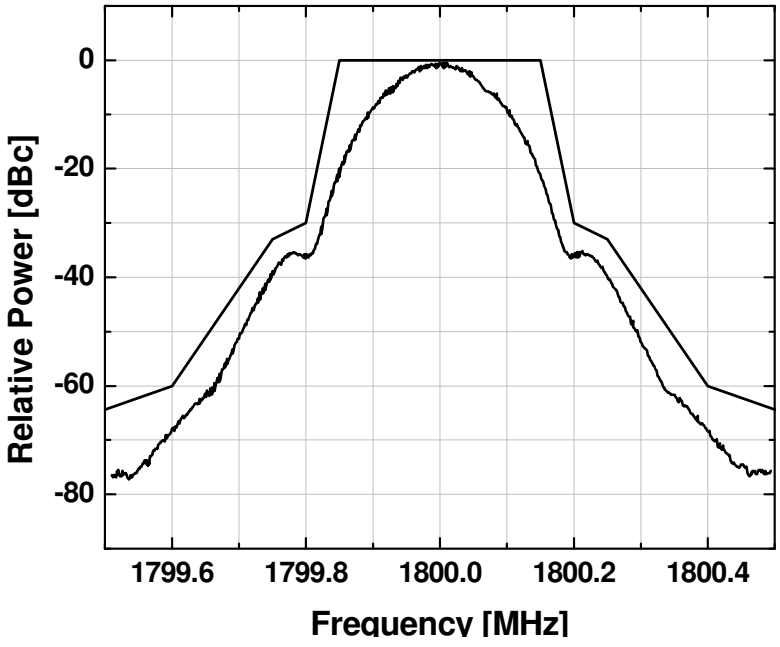


Figure 51. Amplified GMSK modulated signal and the GSM spectrum emission mask at 1.8 GHz.

Figure 48 shows the output power and PAE, as a function of frequency. With a 3.3-V supply, the PA achieves 31% PAE and 33 dBm (2 W) output power (P_{OUT}) in a single-ended 50-ohm input and output condition at 1.8 GHz. The performance of the measured P_{OUT} and PAE was fairly constant over the frequency range of 300 MHz. It covers the GSM high band specification. In this design, the lateral transformer was implemented using metallization layers in a standard 0.18-μm CMOS technology. This technology provides the aluminum top metal layer of 2.34-μm thickness. Because current flow generates ohmic losses, the quality factor of passive structure is mainly governed by the conductivity and thickness of metal layer. Generally, advanced technologies (0.13-μm and 90 nm technologies) compared to 0.18-μm CMOS technology provide Cu top metal layer. The conductivity of Cu (5.813×10^7 S/m) is much higher than that of Al (3.816×10^7 S/m). Thickness of Cu top metal layer in advance technologies is higher than 2.34-μm. Therefore, passive efficiency performance will be improved if this metallization layers are used. If these technologies are applied to the current design, the efficiency performance of power amplifier will be improved. Figure 49 shows the measured P_{OUT}, the power gain and PAE as a function of the input power at 1.8 GHz. The compressed power gain was around 19.5 dB at the peak power. The measured output power and gain of the PA are shown as a function of the supply voltage in Figure 50. A greater than 40 dB of dynamic range was observed with an adjustment of the power supply voltage from 0.2 to 3.3 V. To verify its potential wireless communication application, the fabricated PA was tested with a Gaussian minimum shift keying (GMSK) modulated input signal. The product of the Gaussian filter bandwidth and the symbol duration (BT) was chosen to be 0.3. Figure 51 shows the measured spectrum with the GSM mask in dBc with 33 dBm

of output power. The output spectrum of the PA was confined in the GSM spectral emission mask over the whole output power range. Therefore, the proposed CMOS PA is a good candidate for GSM applications.

4.5 Conclusion

A design methodology for watt-level, fully integrated CMOS power amplifiers is presented. It is based on the analysis of the operation and power loss mechanism of class-E PAs, which includes the effects of a finite DC-feed inductance and an impedance matching transformer. Using the proposed approach, a class-E PA with a 2×1:2 step-up on-chip transformer was implemented in a 0.18-μm CMOS technology. With a 3.3 V supply, the fully integrated PA achieves an output power of 2 W and a power-added efficiency (PAE) of 31% at 1.8 GHz.

CHAPTER 5

CHARGING ACCELERATION TECHNIQUE FOR HIGHLY EFFICIENT CASCODE CLASS-E CMOS POWER AMPLIFIERS

5.1 Introduction

The objective of this research work is to analyze and develop design techniques to implement highly efficient fully integrated switching CMOS PAs for wireless communications, which incorporate a cascode structure.

Recently, the demand for CMOS PAs for fully integrated CMOS transceivers has increased. Though there are several successful demonstrations for watt-level PAs, the design of a fully integrated CMOS PA with high efficiency and high output power is still a very challenging task. A highly efficient PA is desirable because major power consumption in the front-end comes from the PA so that a switching-mode PA is attractive due to its high DC-to-RF conversion efficiency. Theoretically, class-D, E, and F switching mode PAs have 100% efficiency. At no time current and voltage coexist. This implies no energy is wasted as heat in devices. Regarding switching devices, device parasitic capacitances should be concerned in radio frequency (RF) applications. These device parasitic capacitances should be incorporated or tuned out in switching operation. A class-D PAs are not suitable at RF and widely used only for audio frequencies because the output capacitance of the transistors causes a significant power loss at the high-frequency range [16]. A class-F PA requires several lumped elements to perform

harmonic terminations, resulting in a complicated circuitry and large size for the integration. A class-E PA has a strong switching operation while it incorporates an output capacitance as a part of the switching operation. In this case, the power loss from the output capacitance is minimized because the output capacitance of the transistor can be a part of the switching network. In addition, its implementation is simple, and thus the form factor of the class-E PA is more compact than they are in the class-F PA.

In PAs, because output power is proportional to the square of the supply voltage, the high supply voltage is desirable for high output power. Also, the battery voltage of mobile terminal is fixed and does not scale down. Therefore, PAs are often under the increasing voltage stress, especially in the class-E operation. This voltage stress between two terminals will be severe to CMOS devices. High voltage stress across the device can cause reliability problems, such as gate-oxide breakdown, hot carrier degradation, punchthrough, and junction breakdown. This reliability issues should be main concern in PA design because breakdown voltages of CMOS devices are relatively small compared to those of GaAs devices. In common practice, regarding CMOS PA design, the maximum voltage drop across the device at any node should be below twice the nominal supply voltage [22]. However, along with the progress in CMOS technology, its supply voltage is also scaled down and then its breakdown voltage is also reduced. The device stacking in a series is a good way to divide voltage stress across each device without decreasing supply voltage. Cascode topology is one example of device stacking. To the best of the author's knowledge, the body of the common-gate device is commonly grounded (BG-cascode) for the design of the CMOS cascode class-E PA. In this configuration, two devices should be turned on or turned off at the same time to minimize

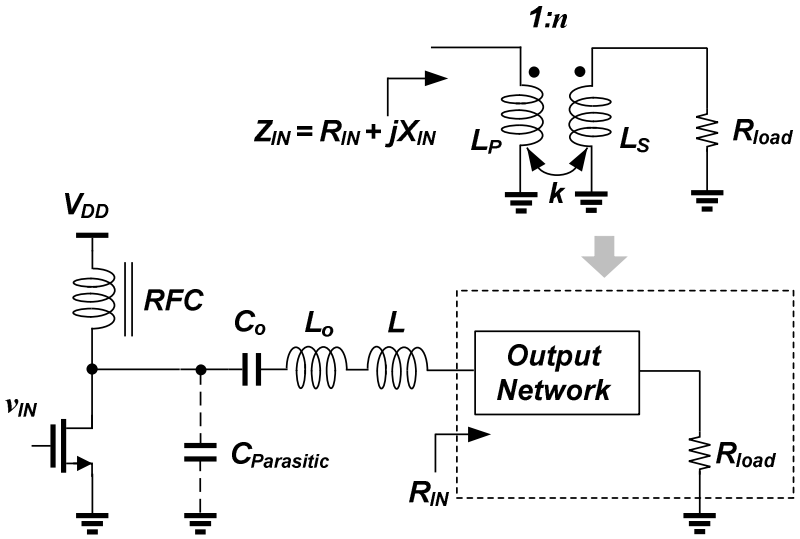
power loss. However, in practical implementation, the common-gate device cannot be instantly switched from the triode region to the cut-off region. Although this effect is significant in loss, it has not been well-studied except a recent work about the analysis of reliability and efficiency in [23]. The application of the tuning inductor technique was proposed to minimize the power loss in the common-gate device [23]. However, the additional inductor requires a large die area and its performance depends on the quality factor, Q. In addition, this technique may degrade the bandwidth performance due to a resonant characteristic.

In this work, to turn off common-gate device instantly after common-source device is turned off, a charging acceleration technique (CAT) is suggested. Simulations and measurements on a prototype CMOS cascode class-E PA are used to demonstrate its effectiveness. In addition, a BS-cascode topology for cascode configuration is suggested, where a body of common-gate is tied to the source of the common-gate device. The BS-cascode class-E PA embeds CAT using a parasitic capacitance and improves the efficiency.

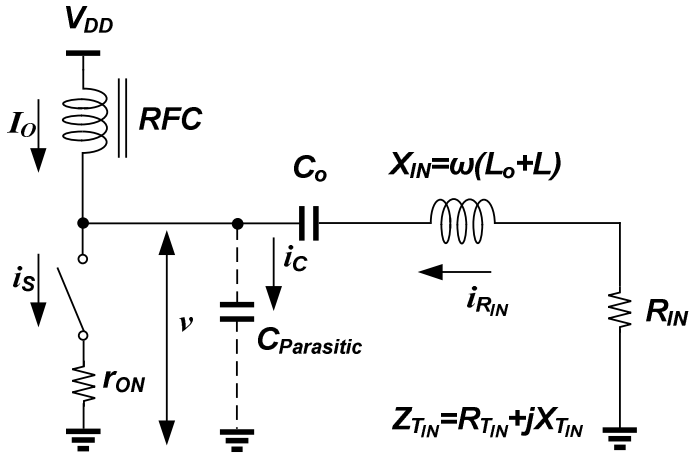
This chapter is organized as follow: Section 5.2 address the device power loss of CMOS cascode class-E PA using a proposed simplified model. Section 5.3 introduces a scheme to minimize this device power loss, and hence improve overall amplifier efficiency. Section 5.4 and 5.5 presents practical design and measurement results, respectively. Finally, section 5.6 draws conclusions.

5.2 Power Loss of Cascode Class-E CMOS Power Amplifier

5.2.1 Power Loss of Common-Source Class-E CMOS Power Amplifier



(a)



(b)

Figure 52. (a) Schematic of a class-E PA with an output network. (b) Schematic of an equivalent class-E PA network.

Figure 52(a) shows the circuit schematic of a typical class-E PA with an output network. C_O and L_O are designed to form a series resonator, and the device output capacitance, $C_{parasitic}$, and jX are designed based on two class-E switching conditions [12]- [14].

1) voltage across the switch returns to zero at the end of the off-state (i.e., $v(\omega t) = 0$).
2) the first derivative of the voltage across the switch is zero at the end of the off stage (i.e., $dv(\omega t)/d(\omega t) = 0$).

The output network in Figure 52(a) provides the necessary impedance transformation from optimum impedance, R_{IN}, to R_{load} for class-E operation. The output network can be implemented by a transformer for an on-chip implementation, as shown in Figure 52(a). The transformer can be modeled with the equivalent net inductances, L_P and L_S, for the primary and secondary windings. n is the turn ratio, and k is the coupling factor. When the transformer is a part of a class-E network, L_O and jX can be eliminated by a reflective inductance from the transformer, resulting in a more simplified circuit as shown Figure 52(b) [49].

For optimum class-E design conditions, the following design parameters can be determined as [12]-[14].

$$R_{IN} = 0.5768 \frac{{V_{DD}}^2}{P_{IN}}, \tag{5.1}$$

$$L = 1.1525 \frac{R_{IN}}{\omega}, \tag{5.2}$$

$$C = \frac{0.1836}{\omega R_{IN}}. \tag{5.3}$$

Because the device is driven by a large signal in a switching operation, the device operates in either the triode region or cut-off region during most of the period. Thus, the core device can be modeled as a switch with an equivalent on-resistance, r_{ON}. When the device operates in the cut-off region, it acts as an open switch. When the device operates in the triode region, it acts as a closed switch with series r_{ON}. If $V_{DS} \ll 2(V_{GS} - V_{TH})$, r_{ON} in the triode region is given by [50]

$$r_{ON}(\omega t) = \frac{1}{\mu_n C_{OX} \frac{W}{L}(v_{GS}(\omega t) - V_{TH})} \tag{5.4}$$

where L is the gate length, W is the gate width, C_{OX} is the gate oxide capacitance per unit area, μ_n is the electron mobility, and V_{TH} is the threshold voltage.

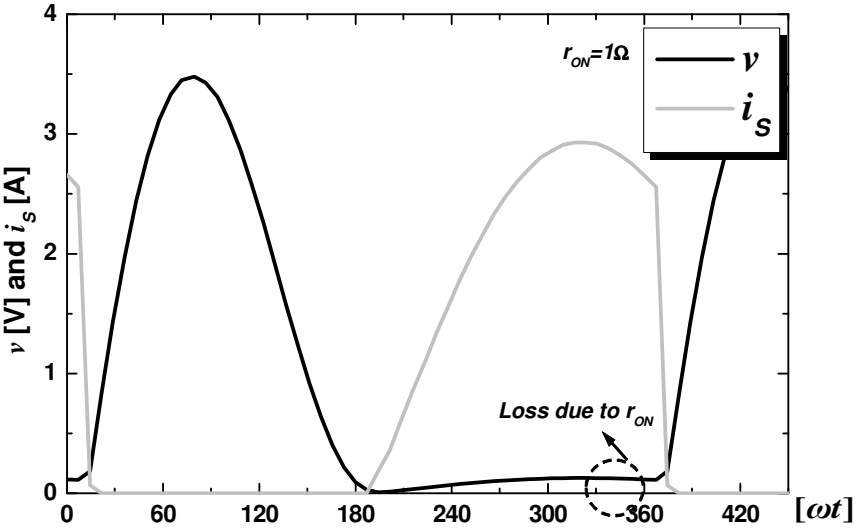


Figure 53. Normalized voltage and current waveforms of a common-source class-E PA.

This conductive resistance in device generates the power loss. Because input matching network is designed generally to form a resonator to tune out input gate capacitance of power device, the waveform of input signal, v_{GS}, is sinusoidal not a square. Therefore, r_{ON} will be varied as a function of v_{GS} in (5.4). However, it is difficult to calculate the power loss with varying r_{ON} so that typically constant value is assumed for an analytical solution [34], [36], [49], [51]. Figure 53 shows the simulated voltage and current waveforms for a constant r_{ON}. Voltage and current are simultaneously positive in the on-state due to r_{ON}, which causes power loss in device. This power loss can be minimized by increasing the device size, W, in (5.4). Generally, to minimize power loss due to r_{ON}, the device size needs to be increased until the device parasitic capacitance, $C_{parasitic}$, seen from the drain of M_2 can be replaced the required parallel capacitance for the class-E switching condition. However, device size should not be excessively increased in order to compensate for driving loss since the accompanying large input capacitance would only exacerbate the problem [44], [52].

In addition, power losses can be caused by lossy passive element. Using a high-Q passive is a way to minimize its loss due to r_L. This power loss in device can be minimized by increasing the device size.

5.2.2 Simplified Model and Power Loss of Cascode Class-E CMOS

For a watt-level output power, a large impedance ratio is generally required to reduce R_{IN} in (1.1) at the given V_{DD}. However, a large impedance transformation results in a large power loss. Generally, the higher the impedance transformation ratio, the higher the loss of the impedance transformation network [22], [45]. Increasing V_{DD} is a way to reduce the burden of the necessary impedance transformation to get watt-level output power without increasing impedance transformation ratio. In addition, the battery voltage of mobile terminal is fixed and does not scale down. PAs in mobile terminal were mostly built using 3.6V lithium ion batteries. However, this high supply voltage increases the stress causing reliability problem across the device. Using a cascode topology is a way to sustain a high supply voltage using sub-micron standard CMOS device.

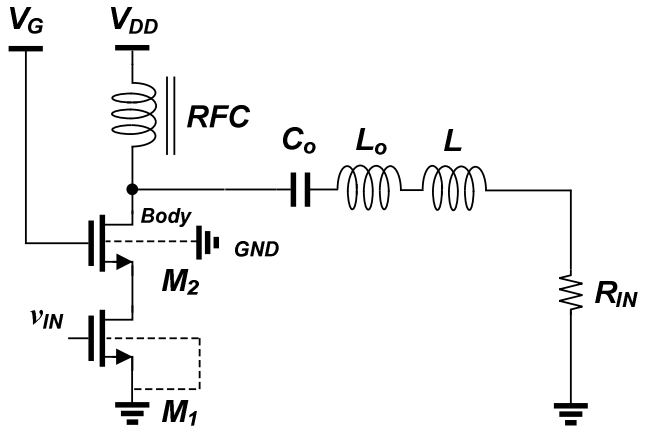


Figure 54. Conventional cascode class-E PA (BG-cascode class-E PA).

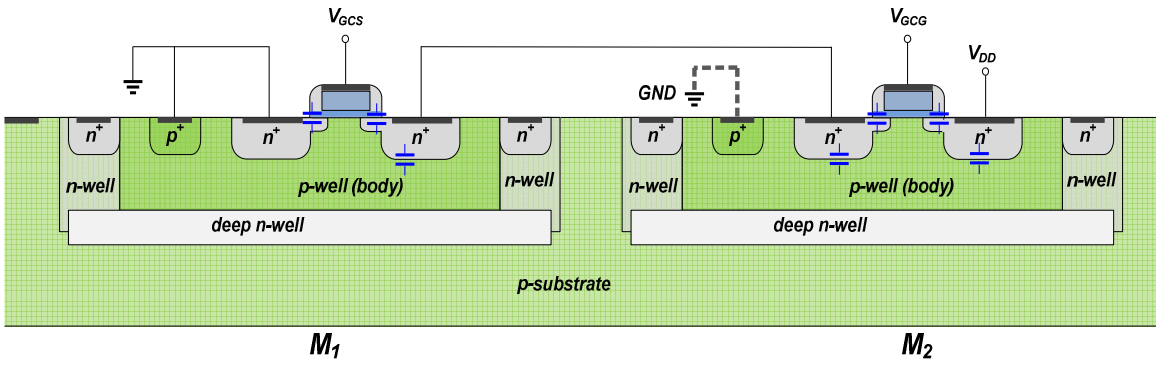
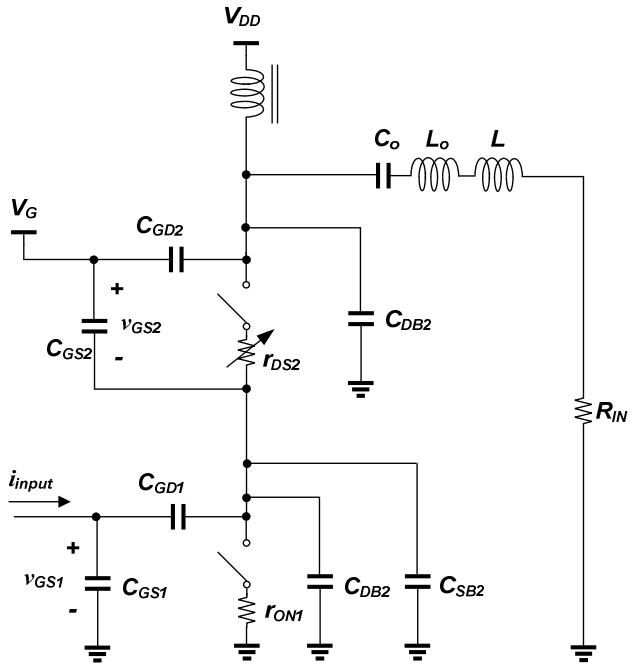


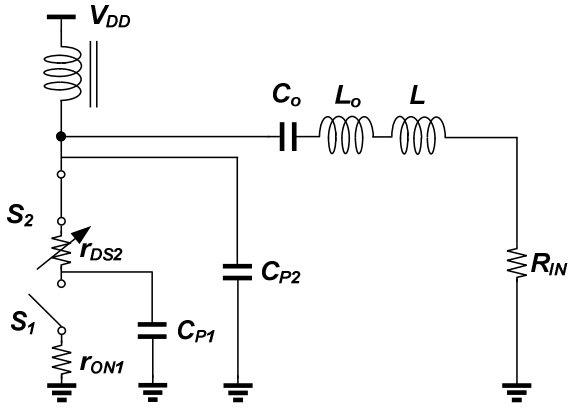
Figure 55. Capacitance composition in deep N-well process in BG-cascode structure.

However, in addition to power loss due to r_{ON}, a property of CMOS cascode class-E PA generates another loss in device. Because two devices cannot be turned on or turned off at the same time, voltage and current coexist, causing power loss in the device. Figure 54 shows cascode class-E PA using the conventional cascode structure. Body of common-gate device is commonly connected to ground (BG-cascode) for the design of the cascode PA. Traditionally, before foundries support deep N-well process, the body of common-gate device is connected to ground. Figure 55 shows the parasitic capacitance composition of a BG-cascode structure in a typical deep N-well technology. In class-E PA design, these device parasitic capacitances should be incorporated or tuned out in switching operation. Figure 56(a) shows the equivalent circuit model for the BG-cascode structure with the relevant parasitic capacitance composition. For the core model of the devices, the common-source device can be replaced as a switch with a constant low r_{ON} like a common-source class-E PA. However, the common-gate device should be modeled as a switch with a variable drain-source resistance, r_{DS}, whose value is varied with each node voltage in the time period, as shown in Figure 56(a). Because the common-gate

device cannot be switched from the triode region to cut-off region, the transient time of the common-gate device cannot be neglected. In this case, the device can operate in the sub-threshold region during the large part of the cycle and its equivalent resistance will vary from low r_{ON} to very high impedance before turning off.



(a)



(b)

Figure 56. (a) Complete equivalent BG cascode class-E PA circuit model. (b) Simplified BG-cascode class-E PA model.

Junction capacitances, such as the common-source device drain-body capacitance, C_{DB1}, the common-gate device drain-body capacitance, C_{DB2} and the source-body capacitance, C_{SB2}, dominate in the cut-off region of the device and have the voltage dependence. The common-source device gate-source capacitance, C_{GS1}, and the gate-drain capacitance, C_{GD1} and the common-gate device gate-source capacitance, C_{GS2}, and the gate-drain capacitance, C_{GD2}, depend on the operation region of the device. To simplify the analysis, C_{GD} capacitance can be separated into input referred capacitance, C_{GD}'', and output referred capacitance, C_{GD}' [53]. In addition, C_{GD}'' and C_{GS1} can be tuned out using an additional tuning inductor to minimize the driving loss. When several capacitors can be combined together, finally simple BG-cascode PA model can be obtained, as shown in Figure 56(b). The on-resistance of M_1, r_{ON1}, and variable drain-source resistance of M_2, r_{DS2}, are connected in series. The output capacitance of M_2, C_{P2}, is the sum of C_{DB2} and C_{GD2}. If an additional lumped capacitor is not added, C_{P2} should meet the conditions (5.3). The output capacitance of M_1, C_{P1}, is the sum of C_{DB1}, C_{GS2}, C_{SB2}, and C_{GD}'. This total capacitance is directly related to the transition loss of the cascode class-E operation.

In ideal class-E operation, only two states exist in the period of time, on and off state. The current flows through two series conductive channels in the on-state and flows through C_{P2} in the off-state. Thus, these two current generate a sinusoidal current at the output. However, due to cascode property, two devices cannot be turned off simultaneously, which generates a significant power loss.

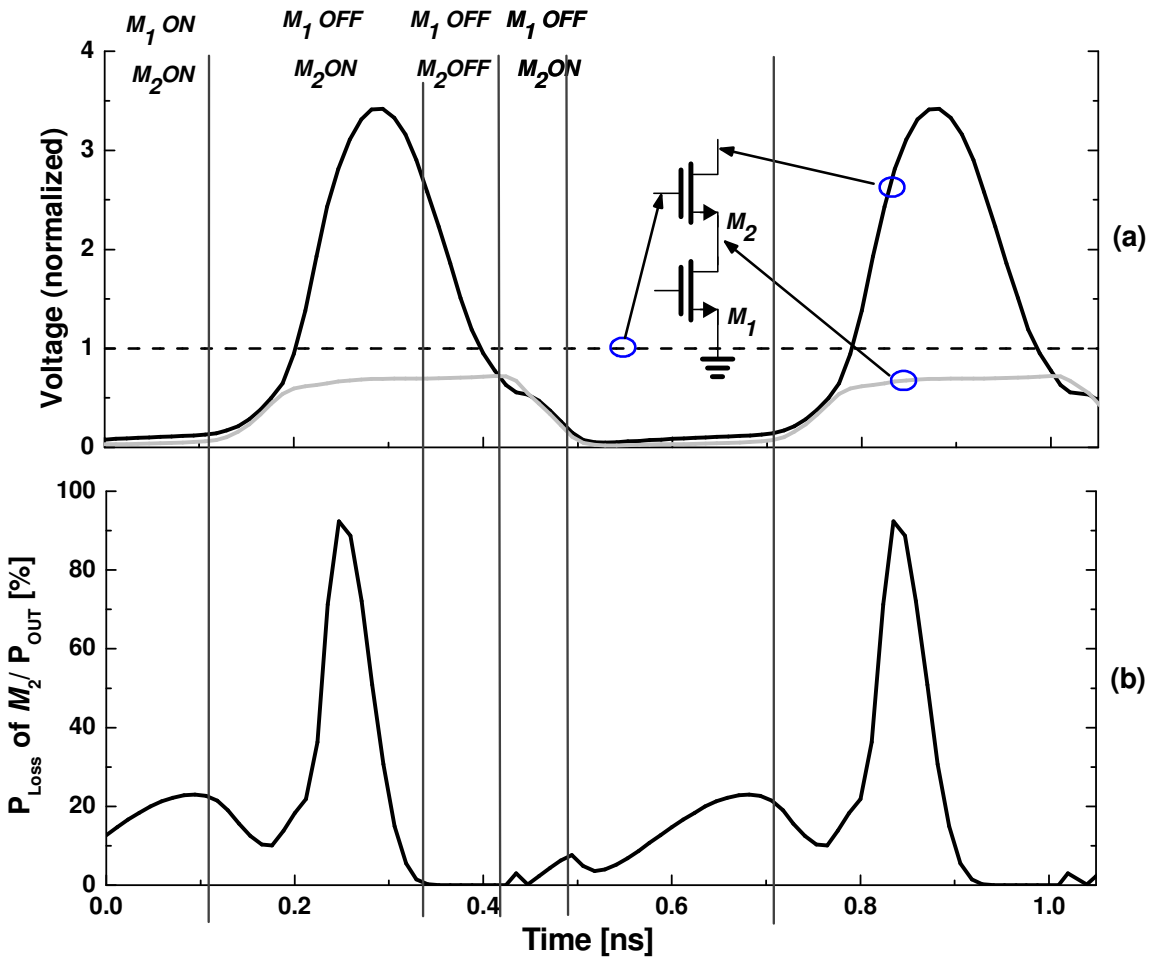
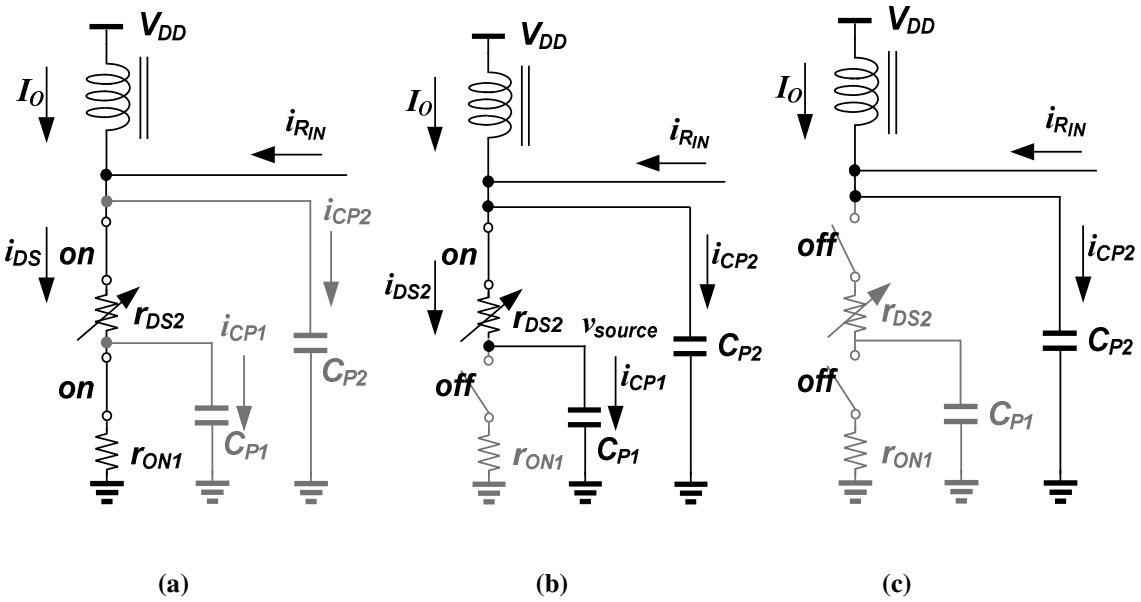


Figure 57. (a) Voltage waveforms of BG-cascode class-E PA. (b) Normalized power loss in M_2.

Figure 57(a) shows the simulated waveforms of conventional BG cascode class-E PA using TSMC 0.18-μm process. The cascode structure has a stacked configuration of 0.18-μm for common-source device and 0.35-μm for common-gate device. Figure 57(b) shows instantaneous power loss in M_2 using ADS harmonic balance simulation. Instantaneous power loss can be defined as

$$P_{Loss} = i_{DS}(\omega t)v_{DS}(\omega t) = {i_{DS}}^2(\omega t)r_{DS}(\omega t) \tag{5.5}$$

The power loss in the transition state is much larger than that of on-state, as shown in Figure 57(b) and has been identified in [23]. $v_{DS}(\omega t)$ is the voltage difference between the drain and the source and $i_{DS}(\omega t)$ is the current through the conductive channel.



(a) **(b)** **(c)**

Figure 58. (a) Equivalent circuit model for on-state (b) Equivalent circuit model for transition state (c) Equivalent circuit model for off-state.

The loss mechanism in the cascode device can be explained using this suggested simplified model. Main cause of device loss is due to flowing currents, $i_{DS}(\omega t)$, through two conductive channels. Thus, the dissipated power can be defined as

$$P_{Loss} = \frac{1}{2\pi}\int i_{DS}(\omega t)v_{DS}\,(\omega t)d(\omega t) = \frac{1}{2\pi}\int {i_{DS}}^2(\omega t)r_{DS}\,(\omega t)d(\omega t) \tag{5.6}$$

The voltage difference between drain and source is v_{DS}, and i_{DS} is a flowing current through conductive channel. We distinguish four cases and consider the power loss in each case:

1. The operations of common-source and common-gate devices are both in the triode region, as shown in Figure 58(a). In this case, two devices are both in on-state and the current flows through two switches. The power losses due to each r_{DS} resistance of the device can be expressed as

$$P_{Loss} \approx \frac{1}{2\pi}\int {i_{DS1}}^2(\omega t) r_{ON1}(\omega t) d(\omega t) + \frac{1}{2\pi}\int {i_{DS2}}^2(\omega t) r_{ON2}(\omega t) d(\omega t)$$

$$= \frac{1}{2\pi}\int {i_{DS}}^2(\omega t)[r_{ON1}(\omega t) + r_{ON2}(\omega t)] d(\omega t) \quad (5.7)$$

where $i_{DS}(\omega t) \cong i_{DS1}(\omega t) \cong i_{DS2}(\omega t)$ and $i_{CP1}(\omega t) \cong i_{CP2}(\omega t) \cong 0$

Drain-source resistance is the on-resistance of the device in this case. This power loss is relevant to the dominant device power loss in a common-source class-E PA.

2. M_1 operates in the cutoff region while M_2 is in the on-state. With negative angle of large signal input, M_1 is completely turned off but M_2 is still on. Figure 58(b) shows the equivalent circuit model in this transition state. In this time period, the DC currents, I_O and output load current, i_{RIN}, flow into two paths, r_{DS2}-to-C_{P1} path and C_{p2} path, based on the magnitude ratio between $r_{DS2}+1/\omega C_{P1}$ and $1/\omega C_{P2}$. Therefore, drain and source voltage of M_2 goes up due to C_{P1} and C_{P2} charging. Right after M_1 is turned off, equivalent drain-source resistance, r_{DS2}, of M_2 is small in this time period, voltage difference between gate and drain is small, as shown in Figure 57(a).

The source voltage of M_2 rises due to C_{P1} charging and can be express as

$$V_{Source\ of\ M_2}(\omega t) = \frac{1}{C_{P1}} \int i_{CP1}(\omega t) d(\omega t) \tag{5.8}$$

With increasing source voltage of M_2, r_{DS2} will be much larger than the magnitude of $1/\ \omega C_{P2}$ and the small amount of currents will flow into r_{DS2}-to-C_{P1} path. Then C_{P1} is slowly charging. While drain voltage of M_2 goes up sharply because relatively large amount of these current flows into C_{P2} capacitor. Thus, this slow C_{P1} charging increases device power loss. Even though this conductive channel current is small, power loss can be large due to the large voltage drop between drain and source of M_2. Current flow through r_{DS2} causes power loss until M_2 is turned off. Its loss can be described as

$$P_{Loss} \approx \frac{1}{2\pi} \int i_{DS2}(\omega t) v_{DS2}(\omega t) d(\omega t) = \frac{1}{2\pi} \int {i_{DS2}}^2(\omega t) r_{DS2}(\omega t) d(\omega t) \tag{5.9}$$

where $i_{DS2}(\omega t) \cong i_{CP1}(\omega t)$ and $i_{DS1}(\omega t) \cong 0$.

To turn off M_2, the source voltage of M_2 is larger than V_G- V_{TH2}. V_G is the gate voltage of M_2 and V_{TH2} is the threshold voltage of M_2.

3. Both M_1 and M_2 operate in cutoff region. In this case, no power dissipation through conductive channels exists, as shown in Figure 58(c).

4. Before two devices operate in the triode region, M_1 operates in the cutoff region and M_2 is on-state. The mechanism of power loss is similar with case 2. However, its loss is much smaller than that of case 2 because voltage difference between drain and source in M_2 is relatively small.

5.3 Charging Acceleration Technique

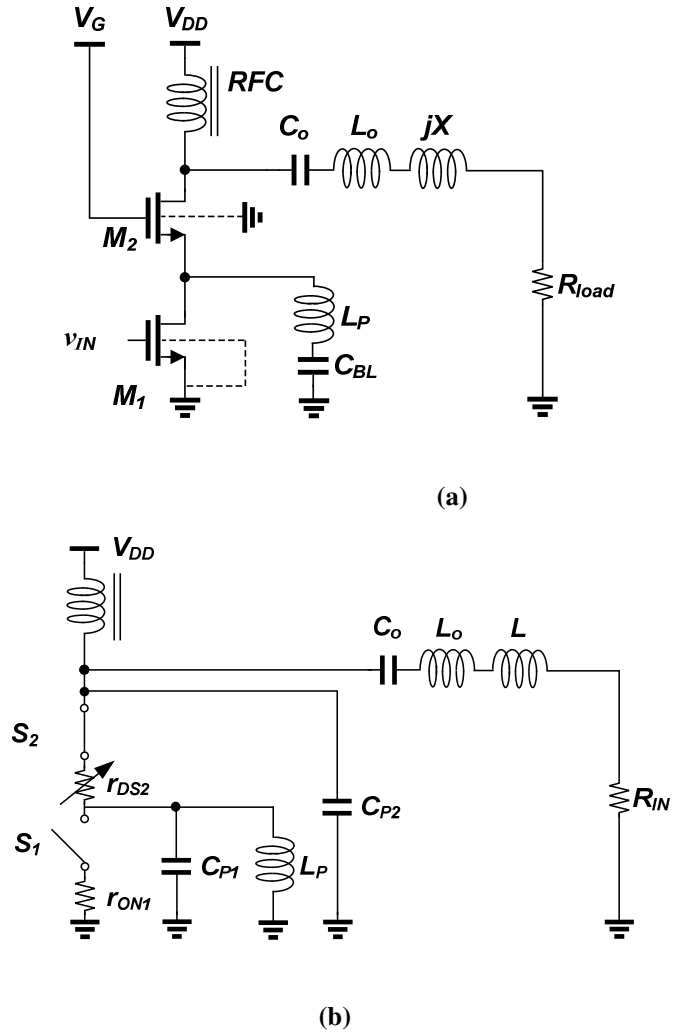


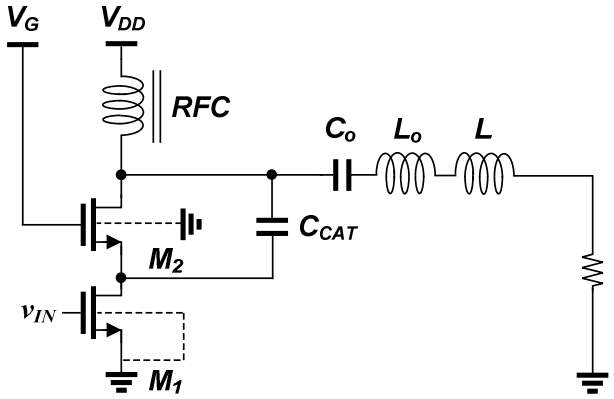
Figure 59. (a) Schematic of BG cascode class-E PA with tuning inductor. (b) Equivalent circuit model of BG cascode class-E PA with tuning inductor.

To minimize resistive conduction current generating power loss of M_2 in the transition state, a voltage difference between gate and source, V_{GS2}, should be less than threshold voltage V_{HT2} right after M_1 is turned off. Decreasing gate voltage in M_2 also helps to turn off M_2. However, this decreasing gate voltage increases voltage stress between gate and drain of M_2. Because the drain voltage of M_2 reaches around 3.56 V_{DD}

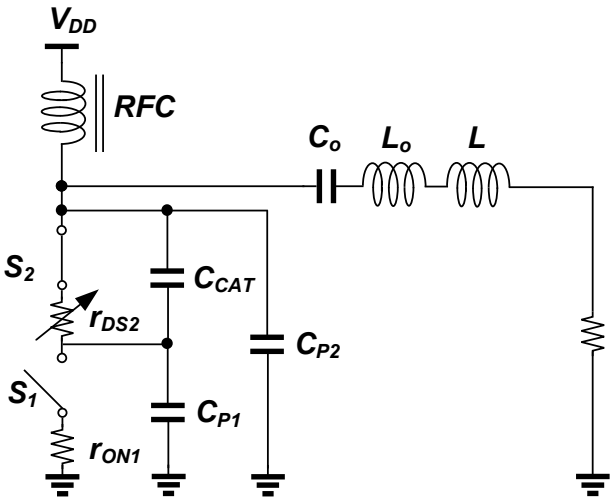
in off stage, it is desirable that the drain of M_2 needs to connect the highest DC voltage to minimize voltage stress between gate and drain of M_2. Because the gate voltage of M_2 is fixed at the DC voltage, the source voltage of M_2 needs to rise immediately to turn off M_2 after M_1 is turned off. One way to increase source voltage of M_2 is to reduce the parasitic charging capacitor. In prior art, inductor tuning technique was proposed to minimize C_{P2} [23]. A tuning inductor is connected to the source of M_2 in parallel to resonate out the parasitic capacitance, C_{P1}, as shown in Figure 59. Blocking capacitor, C_{BL}, is located between the tuning inductor and ground. Because the amount of capacitor is tuned out, the source voltage of M_2 rises abruptly after M_1 is turned off. However, the additional tuning inductor requires a large die area. In addition, due to low Q of on-chip inductor, it can generate additional loss. Furthermore, Q of LC resonator can affect the performance of bandwidth.

Source voltage of M_2 can be increased by an alternative way. Adding additional capacitor between drain and source of M_2, as shown in Figure 60(a) increases the source voltage of M_2 by accelerating C_p charging. Right after M_1 is turned off with large signal input, M_2 is in linear region and its drain-source resistance is small. With increasing source voltage, r_{DS2} will be high. In this region, additional current path in Figure 60(b) helps to increase C_{P1} charging speed. Generally, the Q factor of capacitors is much higher than that of inductors at operation frequency bands of typical wireless applications, so the loss resulting from capacitors is negligible. In addition, since this additional capacitance can be the part of necessary output capacitance satisfying class-E switching condition, it does not affect class-E operation. In this case, the total output capacitance

(C_{P2}+(C_{P1}//C_{DB2})) at the drain of common-gate device should meet equation (3) if an additional lumped capacitor is not added at the drain of M_2 in Figure 60(b).



(a)



(b)

Figure 60. (a) Schematic of BG cascode class-E PA with charging acceleration capacitor. (b) Equivalent circuit model of BG cascode class-E PA with charging acceleration capacitor.

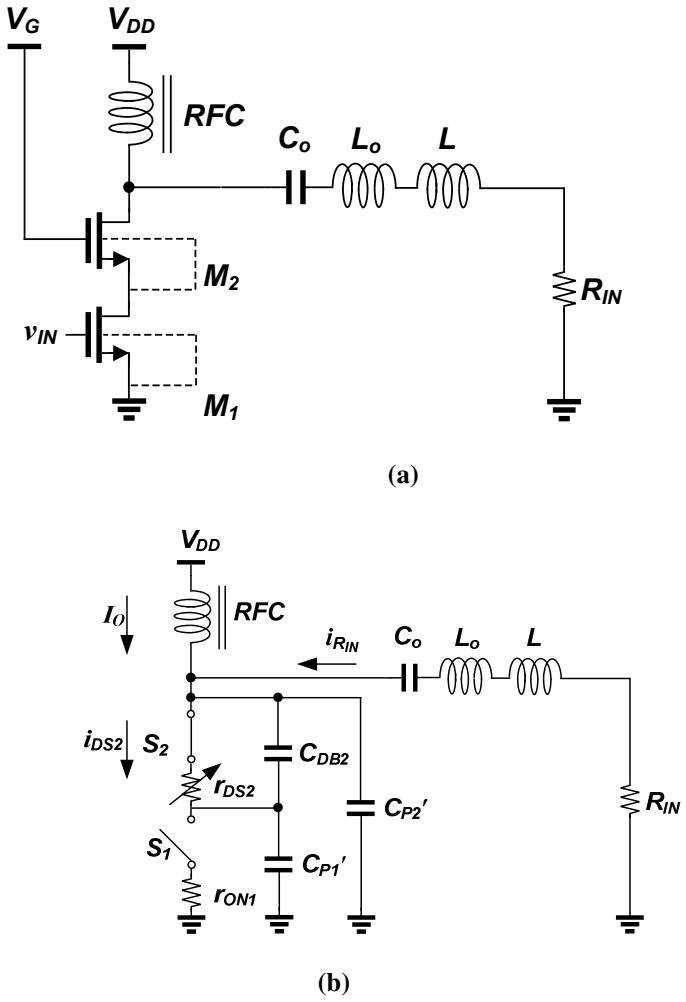


Figure 61. (a) Schematic of BS cascode class-E PA. (b) Equivalent circuit model of BS cascode class-E PA.

If the body of M_2 is tied to its source, as shown in Figure 61, this structure has its own capacitor connection property between the drain and source without an additional lumped element. The conductive channel current through M_2 can be minimized, when the body-source-tied cascode structure (BS-cascode) is incorporated for the design of a switching CMOS PA. Figure 62 shows the capacitance composition of BS-cascdoe structure in a deep N-well technology. Because the body and source are tied together, it gives a series connection between drain and source of M_2. Figure 61(b) shows its equivalent circuit

model based on parasitic capacitance composition. The on-resistance of M_1, r_{DS1} and drain-source resistance of M_2, r_{DS2}, are connected in series as like the BG-cascode. C_{P2} is the common-gate device gate-drain capacitance, C_{GD2}. The output capacitance of M_1, C_{P1}, is the sum of the drain-to-substrate capacitance of M_1, C_{DB1}, the gate-to-source capacitance of M_2, C_{GS2}, and the capacitance between the body of M_2 and well connection. Source-to-substrate capacitance, C_{SB2}, does not exist since the source of M_2 is tied with the body of M_2. Drain-to-substrate capacitance of M_2, C_{DB2} and the output capacitance of M_1 is connected in series.

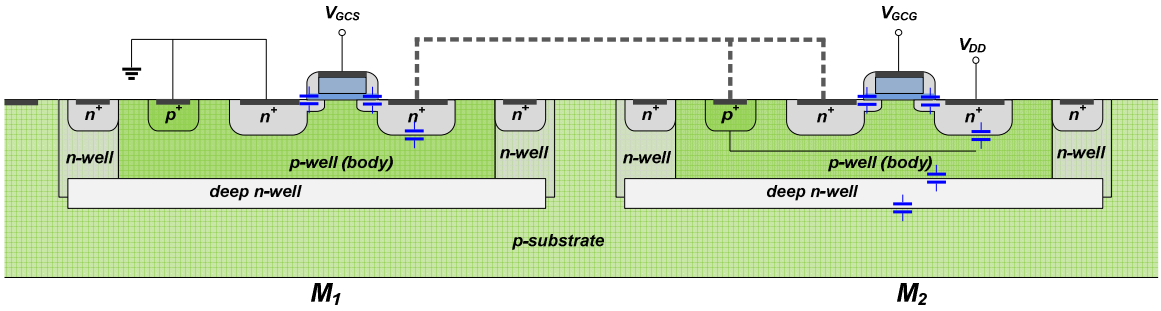


Figure 62. Capacitance composition in deep N-well process in BS-cascode structure.

Figure 63 shows the simulated voltage waveforms at the drain and source of M_2 and the V_{GS} of M_2 for both the BG-cascode and the BS-cascode. Each of the cascode structures has a stacked configuration of 0.18-μm for common-source device and 0.35-μm for common-gate device.

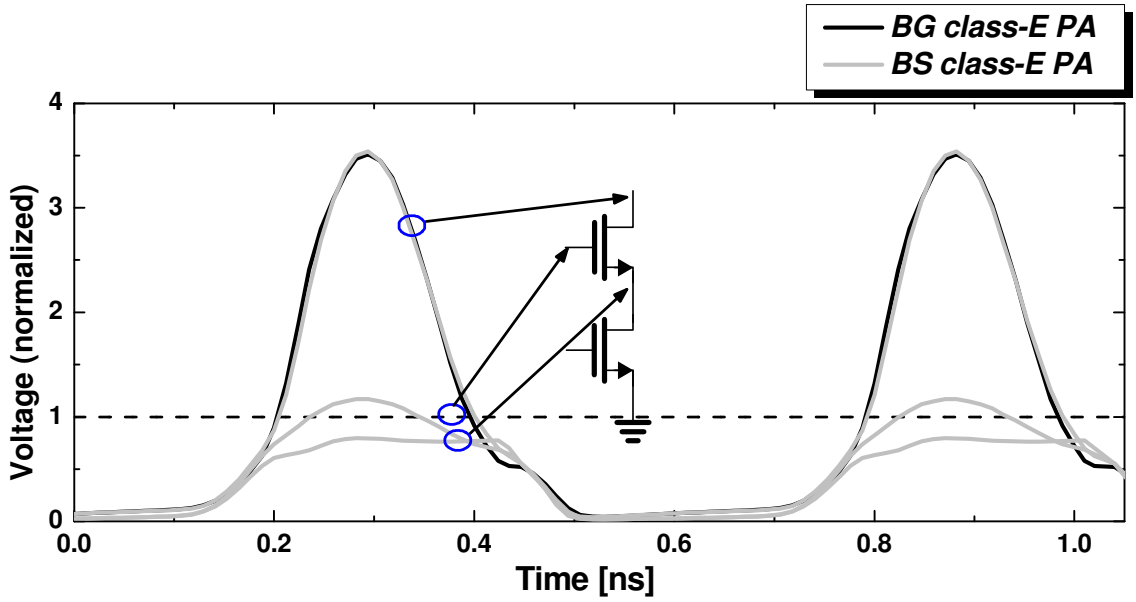


Figure 63. Voltage waveforms of BG-cascode class-E PA and BS-cascode class-E PA.

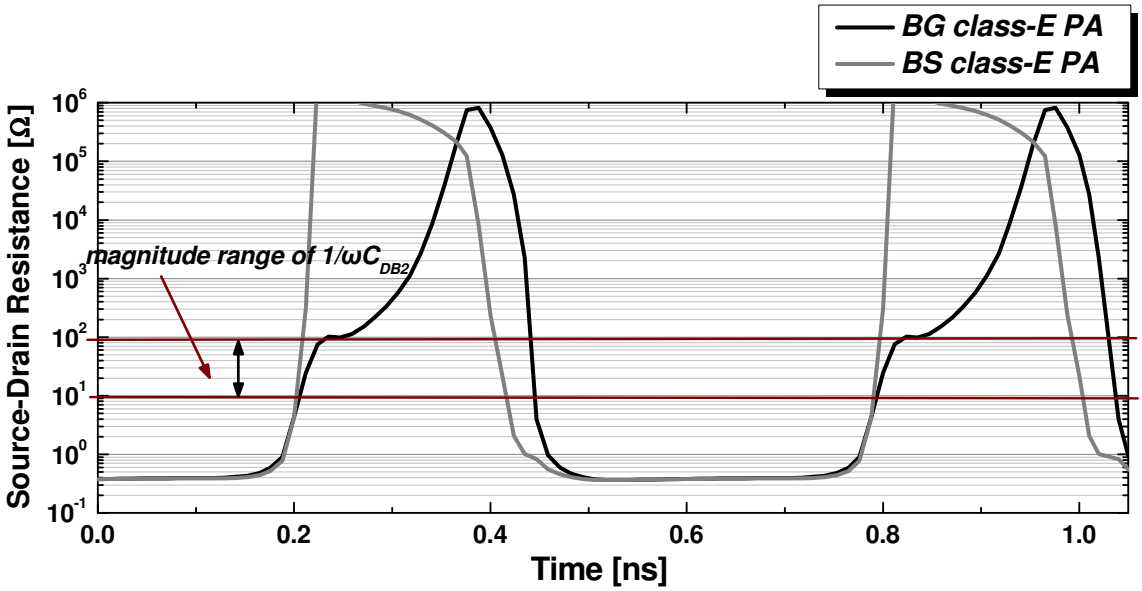


Figure 64. Equivalent source-drain resistance in M_2 (f =1.75 GHz).

Figure 64 shows the simulated drain-source resistance of M_2 for the period of time. When M_1 is turned off, M_2 still operates in the triode region. In this region, r_{DS2} is expressed as the on resistance of the device, r_{ON2}. The magnitude of r_{ON2} will be much smaller than that of $1/\omega C_{DB2}$ at operation frequency bands of typical wireless applications because C_{DB2} is typically about few pico-farad (pF) range for few millimeter device width, as shown in Figure 64. Therefore, I_O and i_{RIN} flow into two paths, r_{DS2}-to-C_{P1} path and C_{p2} path like BG-cascode class-E PA. The output capacitance of M_1, C_{P1} starts charging and the source voltage of M_2 rises due to the current through r_{DS2}-to-C_{P1} path. With increasing the source voltage of M_2, the magnitude of r_{DS2} will be comparable to that of $1/\omega C_{DB}$. Then, the currents start to flow through C_{DB2} and this additional current path accelerates C_{P1} charging as the magnitude of r_{DS2} increases. This raises the source voltage of M_2 and then increases the magnitude of r_{DS2}, which further enhances the current through C_{DB}. This process of charging acceleration causes further increase of the source voltage in M_2, resulting turn off M_2. The source voltage of M_2 in the BS-cascode goes up more than V_{G}-V_{TH2} unlike BG-cascode class-E PA because C_{DB2} and output capacitance of M_2 , C_{GS2}+C_{DB1}, are connected in series and the AC current flows though the series capacitors, as shown in Figure 61.

Therefore, in the off-state of M_1, V_{GS} of M_2 in the BS-cascode is much smaller than that in the BG-cascode so that the conductive channel current of the BS-cascode is much smaller than that in BG-cascode; thus, the power loss is minimized without adding an additional inductor. Figure 65 shows the instantaneous power losses normalized to output power for BG cascode class-E PA, BG-cascode class-E PA with a tuning inductor, BG-cascode class-E PA with a charging acceleration capacitor, and BS cascode embedding

charging acceleration technique. Using charging acceleration technique the power loss in the transition state is significantly reduced without adding a bulky lumped inductor. In addition, because this current flow charges the shunt capacitor in the class-E power amplifier without flowing through a resistive path, it does not cause power loss.

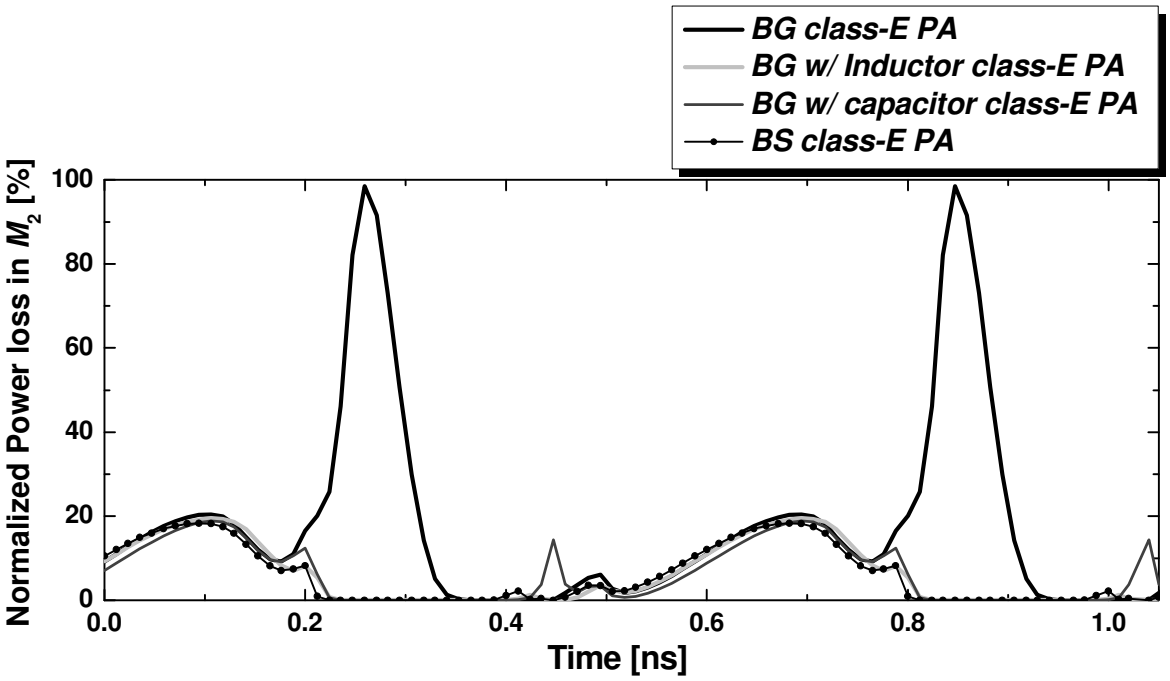


Figure 65. Power loss of cascode class-E PAs.

5.4 Design

To demonstrate the advantage of the class-E PA using BS-cascode embedding charging acceleration technique over BG-cascode topology, two types of 1.75-GHz CMOS Class-E PAs were designed. Because the two PAs share the same layout excepting the body connection of common-gate device, the geometry dependent parameters are the same for the two PAs. It consists of two driver stages and a power stage, as shown in Figure 66. An input on-chip balun is employed for differential

operation of the first driver stage. No DC gate bias of common-source is applied, since the output of class-D amplifier is connected to the input of the power stage. Input capacitance of power device is tuned out by parallel inductor, L_d. For the cascode configuration of the PA, the devices in the common-source stage, m_1 and m_3, and common-gate stage, m_2 and m_4, have a gate length of 0.18-µm and 0.35-µm, respectively. The widths of each common-gate device and common-source device are 4096 μm and 3072 μm, respectively. To minimize voltage stress between gate and drain of the common-gate device, the gate is tied to the drain with the 3.3 V supply voltage. The maximum voltage stress across the single device is kept below twice that of the nominal supply voltage for reliable circuit operation.

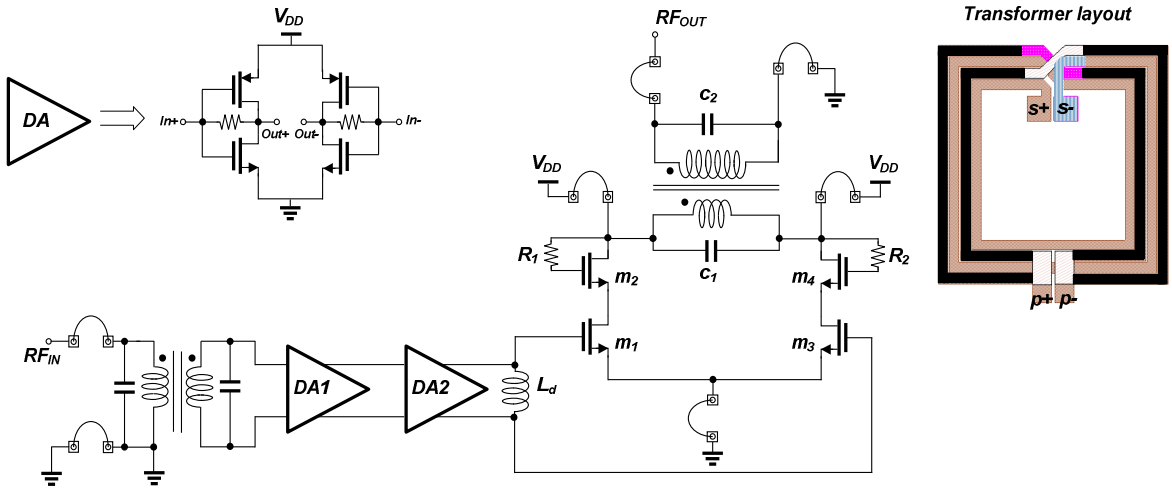


Figure 66. Schematic of the CMOS cascode class-E PA with 1:2 transformer.

For power stage design, a differential topology is adopted to desensitize the effect of bonding wire inductance and combine powers from two power devices. A parallel resonant circuit class-E PA is employed to reduce number of elements instead of using series network. This topology requires one resonant circuit while a series resonant circuit requires two resonant circuits. Therefore, this structure can reduce the size and number of the elements, resulting in a more simplified circuit.

To transform the low impedance of the switching network to a 50-ohm load and combine powers from two power devices, a transformer with a two-segment primary and two-turn secondary was designed. A 0.18-µm CMOS technology with Al process is adopted for this work. Compared to Cu process, the careful concern should be considered to make a high efficient output network because the relatively lower quality factor of passive component with Al-metal. A multi-turn secondary transforms the impedance while a multi-segment primary increases the magnetic coupling [33], therefore minimizing passive loss. An Agilent ADS^{TM} simulator was used for total PA simulation. At 1.8 GHz, the insertion loss of the transformer is 70% when driving the input differentially and taking a single-ended output. It is 75% when taking differential output. Tuning capacitors of the transformer, C_1 and C_2, are optimized to satisfy class-E switching condition and minimize the passive loss of the transformer for each PA.

5.5 Measurement Results

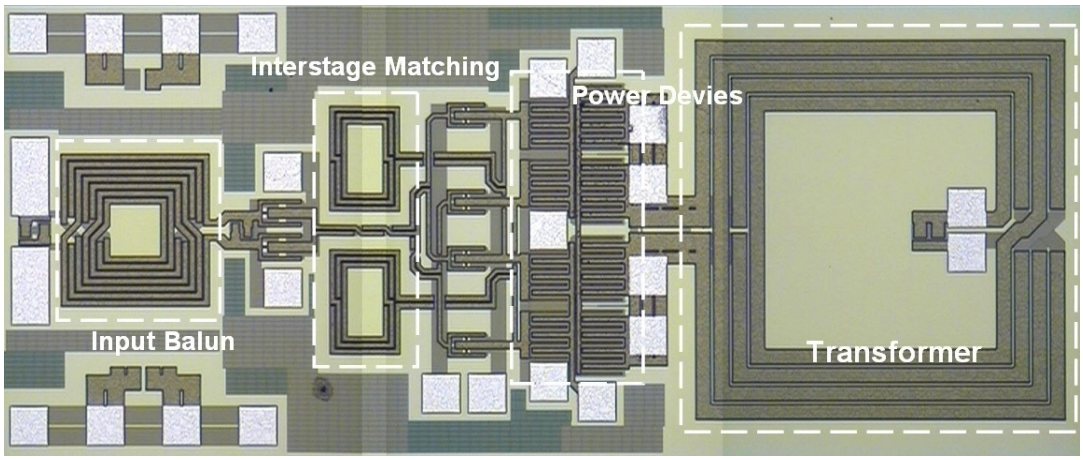
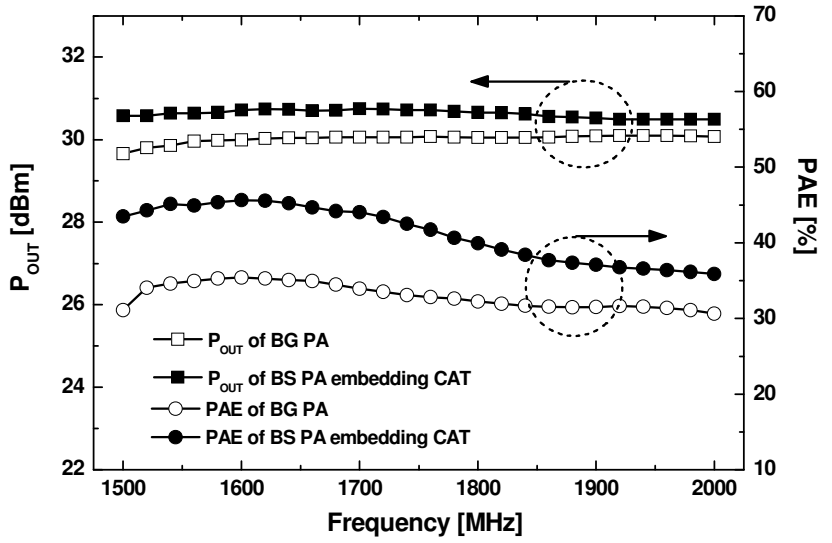


Figure 67. Microphotographs of the PA (Chip size: 2.15mm × 0.8 mm).

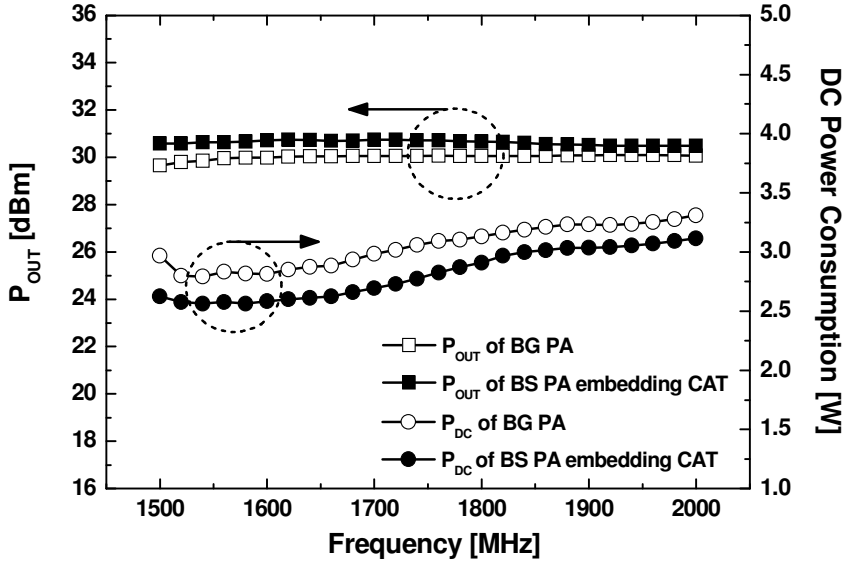
Figure 67 shows the microphotograph of the fully integrated PA fabricated in 1P6M 0.18-μm CMOS technology. The die area is 2.15 mm × 0.8 mm, including pads. The bare die was mounted on the ground heat sink of a printed circuit board (PCB). The input and output pads were wire-bonded to a single 50-Ω micro-strip line. All the pads, including input and output, were wire-bonded on the PCB. The cable and PCB loss have been carefully de-embedded, but pad losses are included in the measurement results.

We measured the performance of each PA as a function of the frequency for an input power of 1.5 dBm. Maximum efficiency is achieved at 1.6-GHz frequency for both cases as shown in Figure 68(a). This is likely that an underestimation of parasitic capacitances, in the layout of routing line and transformer winding. The maximum output power obtained from the BS-cascode class-E PA embedding CAT is 30.7 dBm with a PAE of 45.6% and a gain of 29 dB. The output power, P_{OUT}, and PAE of the BS-cascode class-E PA are improved about 0.5 dB and 7%, respectively, across the broad band level. As shown in Figure 68(b), although DC power consumption of the BS-cascode class-E PA is smaller than that of the BG-cascode class-E PA, P_{OUT} of the BS-cascode class-E PA is

higher than that of the BG-cascode class-E PA. This result indicates that a significant power loss reduction in the common-gate device results in high DC-to-RF conversion efficiency.



(a)



(b)

Figure 68 (a) Measured output power and PAE as a function of the operation frequency. (b) Measured output power and DC power consumption as a function of the operation frequency.

Figure 69 shows the measured P_{OUT} and PAE versus input power at 1.6 GHz. Comparing the two PAs, the BS-cascode class-E PA shows higher P_{OUT} and PAE with increasing input power. Figure 70 shows the performance of P_{OUT} and PAE with supply voltage sweep. Output power increases proportional to the square of V_{DD}. More than 40 dB of dynamic range was achieved with an adjustment of the power supply from 0.5 to 3.3 V. To verify its potential in wireless communication application, the fabricated BS-cascode class-E PA was tested by applying a Gaussian minimum shift keying (GMSK) modulated signal with BT=0.3. Figure 71 shows the measured spectrum at the maximum output power with the GSM mask. The output spectrum of the PA was confined in the GSM spectral emission mask over the whole output power range.

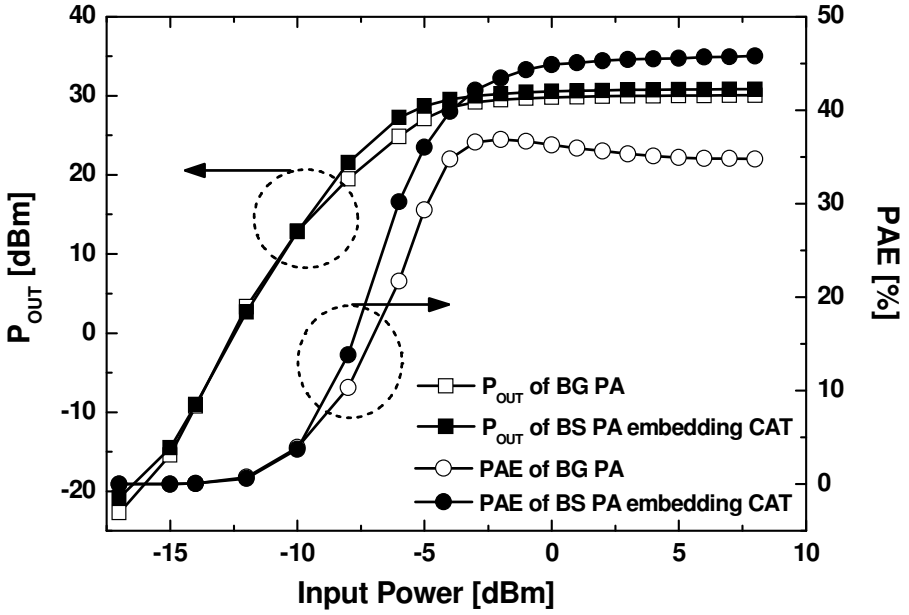


Figure 69. Measured output power and PAE versus input power.

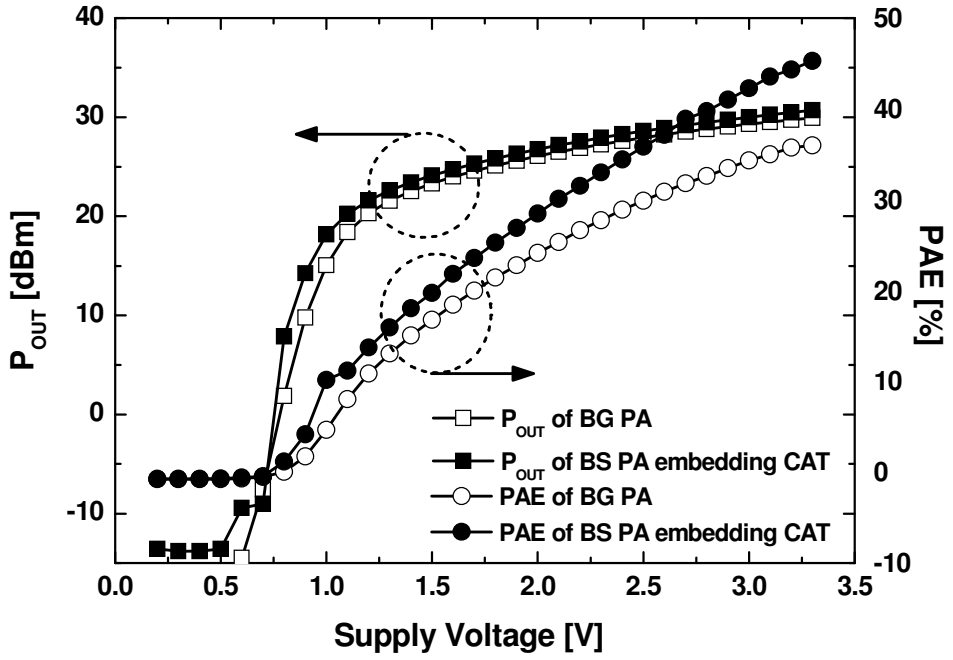


Figure 70. Measured output power and PAE as a function of the supply voltage.

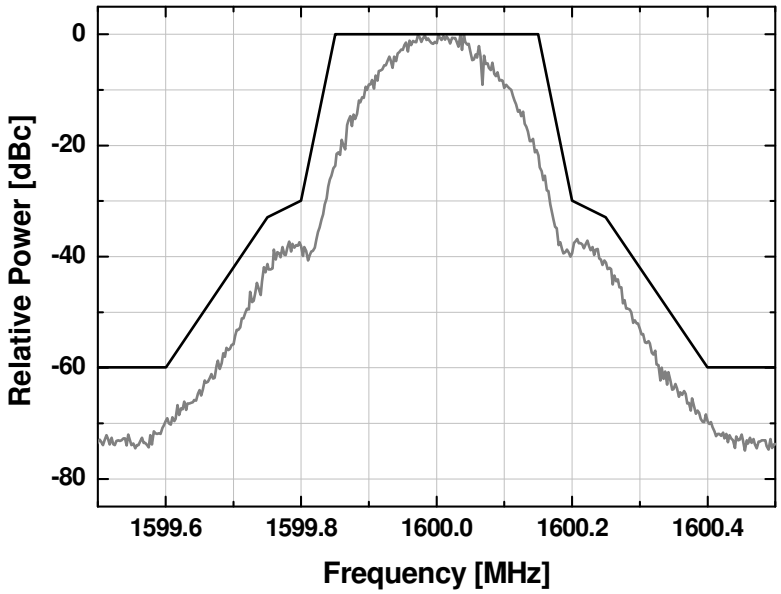


Figure 71. Amplified GMSK modulated signal and the GSM spectrum emission mask of the BS-cascode class-E PA at 1.6 GHz (BT=0.3).

5.6 Conclusion

In this work, the efficiency effect of the equivalent variable resistance of a common-gate device in a power stage using the simple equivalent model has been investigated. It is shown that adding a proper value capacitance between the drain and the source of the common-gate device (CAT) improves the efficiency due to minimization of the power loss in the common-gate device. To demonstrate the CAT, two prototype CMOS PAs were implemented with a 0.18-μm CMOS process including input and output matching networks. The BS-cascode class-E PA embedding CAT shows an improvement of approximately 0.5 dB in output power and 7% in PAE. The BS-cascode class-E PA structure is suitable for the design of high-efficiency class-E PAs while it reduces the voltage stress across the device.

CHAPTER 6
CONCLUSIONS

High efficiency is the most important requirement of PAs for wireless application. However, the design of highly efficient CMOS PA for watt-level application is challenging task. This dissertation consists of two main contributions. First, the design methodology of high power class-E PA including output passive structure is introduced. Second, the charging acceleration technique is presented for highly efficient cascode CMOS PAs.

For watt-level applications, class-E PA with an integrated transformer is most feasible solution. In this dissertation, design method and analysis for a high-power class-E CMOS PA with a fully integrated transformer have been presented. The design procedure optimizes the impedance looking into the transformer for high power and high efficiency. A detailed analysis shows that power losses due to the conduction loss as well as the resistance looking into the transformer, R_{TIN}, are strongly affected by the design parameters of the transformer, such as n, k, R_1, R_2, L_1, and L_2. Based on the analytic results, a compact CMOS class-E PA with multi-primary windings and a multi-turn secondary transformer has been successfully demonstrated for high-power and high-efficiency operation. Experimental data demonstrates an output power of 33 dBm and a PAE of higher than 30% with a 3.3-V power supply at 1.8 GHz operation. The proposed structure is a good candidate for a fully integrated watt-level CMOS PA with a compact

form factor. This work is the first effort to set up a comprehensive design methodology for a fully integrated class-E CMOS PA including the effects of an integrated transformer, which is very crucial for watt-level power applications.

Although, cascode configuration increases power loss, it is the most common topology to sustain high supply voltage. In this dissertation, to improve efficiency of CMOS cascode class-E power amplifiers (PAs), charging acceleration technique (CAT) is developed. The method involves placing a capacitor between the drain and source of a common-gate device. It helps to accelerate charging speed to turn off the common-gate device in the off-state, thus reducing the power loss. A 1.75-GHz CMOS PA was implemented in a 0.18-µm CMOS process, to demonstrate the proposed cascode class-E PA. With a 3.3-V power supply, the fully integrated CMOS PA achieves 30.5 dBm maximum output power and 45% power-added efficiency (PAE) with a dynamic range of 40 dB at 1.75 GHz. Measurements show an improvement of approximately 6% in PAE. The proposed BS-cascode class-E PA structure is suitable for the design of high-efficiency class-E PAs while it reduces the voltage stress across the device.

PUBLICATIONS

[1] **O. Lee**, K. H. An, H. Kim, K. S. Yang, D.-H. Lee, J. H. Han, C.-H. Lee, H. Kim, and J. Laskar, "Analysis and Design of Fully Integrated High Power Parallel-Circuit Class-E CMOS Power Amplifiers," accepted to *IEEE Trans. Circuits Syst. I.*

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